Spring 2012

Module-level power converters for parallel connected photovoltaic arrays

Zachary Scott Johnson

Follow this and additional works at: https://scholarsmine.mst.edu/masters_theses

Part of the Electrical and Computer Engineering Commons

Department:

Recommended Citation

MODULE-LEVEL POWER CONVERTERS FOR PARALLEL CONNECTED

PHOTOVOLTAIC ARRAYS

by

ZACHARY SCOTT JOHNSON

A THESIS

Presented to the Faculty of the Graduate School of the

MISSOURI UNIVERSITY OF SCIENCE AND TECHNOLOGY

In Partial Fulfillment of the Requirements for the Degree

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

2012

Approved by

Jonathan W. Kimball, Advisor
Mariesa L. Crow
Maciej Zawodniok

ABSTRACT

A new solar technology with the capability to increase array-level power production is introduced by using simple integrated power converters that connect directly to photovoltaic (PV) panels is investigated. The power converters proposed here are full-bridge DC-DC converters with high voltage gain that operate with an open-loop control scheme. The outputs of these converters could then be directly connected to a grid-tie converter eliminating the need to connect panels in series to achieve the appropriate voltage. With a high-efficiency converter, the total system efficiency would increase even though one panel in the array may be compromised. The simulation results show that a highly-efficient converter is possible. To assist in experimentation, an auxilary circuit using a microcontroller was implemented to supply power and gate signals to the gate driver of the power converters. The design and construction of a transformer for use with the full-bridge converter is discussed. A novel transformer topology is utilized to increase converter efficiency. The converters were tested both in a laboratory environment and outdoors for solar data collection. Transient response, source regulation and load regulation analysis was performed. The maximum power points of the array were investigated for different insolation levels. Even when insolation differs substantially, the panel output power levels are within their individual maximum power levels when the total output is maximized even without independent power trackers. Analysis of both field data and random insolation indicate that the new approach does increase power generation and therefore system efficiency.

ACKNOWLEDGMENTS

I would like to thank my advisor Dr. Jonathan Kimball for the opportunity to conduct this research. I appreciate all of his contributions and his patience in helping me through my Master's program. Without his patience and wisdom, completion of the project would not have been attainable.

I would also like to acknowledge the members of my committee, Dr. Mariesa Crow and Dr. Maciej Zawodniok for their interest in my research topic.

I would especially like to thank all my friends and family, particularly Lydia Tucker, Jonathan Homan, and James Summitt. They are my motivation for completing this degree and without their support I would not have reached this level of academic achievement. To all of my friends and family, I dedicate this thesis.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

NOMENCLATURE

Symbol	Description
PV	Photovoltaic
MPPT	Maximum Power Point Tracking
PWM	Pulse-Width Modulation
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
PCB	Printed Circuit Board
LDO	Low Drop Voltage Regulator
WDT	Watchdog Timer
V_{in}	Input Voltage
V_{out}	Output Voltage
I_o	Output Current
P_o	Output Power
f_{sw}	Switching Frequency
η	Efficiency
α	Regulation
B_{ac}	Operating Flux Density
K_u	Window Utilization
K_g	Core Geometry
P_t	Apparent Power
K_e	Electrical Conditions
K_f	Waveform Coefficient
W_{tcu}	Copper Weight
W_{tfe}	Core Weight
MLT	Mean Length Turn
MPL	Magnetic Path Length
A_c	Cross-Sectional Area
W_a	Window Area
A_p	Area Product
A_t	Surface Area

N_p	Primary Turns
J	Current Density
I_{in}	Input Current
$A_{wp(B)}$	Primary Bare Wire Area
R_p	Primary Resistance
P_p	Primary Copper Loss
N_s	Secondary Turns
$A_{ws(B)}$	Secondary Bare Wire Area
R_s	Secondary Resistance
P_s	Secondary Copper Loss
P_{cu}	Total Copper Loss
W/kg	Watts Per Kilogram
P_{fe}	Core Loss
P_{Σ}	Total Power Loss
ε	Skin Depth
SR	Source Regulation

1. INTRODUCTION

1.1. PROBLEM

The number of installation locations with unshaded southern exposure over an area large enough for a conventional photovoltaic (PV) array is limited. If the array's performance under parital shading could be increased, the number of suitable installation sites would increase significantly.

A typical solar panel generates up to 200 W at about 26 V. A typical inverter is rated for at least 250 V on its input terminals. Conventionally, PV panels are connected in series strings that achieve the desired system voltage, and then these strings are connected in parallel to achieve the desired system power rating. Unfortunately, if one panel is compromised (due to shading, obstructions, damage, etc.) the output power of its whole string is significantly reduced. Since PV system designers and installers are aware of the detrimental effects of shading, they design for as minimal shading as possible.

With the proposed approach, panels can be connected in parallel instead. Then any single compromised panel will only affect that particular panel, rather than the whole array. This will cause the average system output power to increase. While shading should still be avoided or minimized, moderate shading can be tolerated, so more installation sites can be considered.

In the proposed array topology, each individual PV panel has an integrated dc-dc converter which increases the input voltage by a fixed gain. The output of the converter could then be directly connected to a grid-tie inverter that performs maximum power point tracking (MPPT). Good source and load regulation are needed so that individual

panels operate near the same voltage, regardless of system voltage and individual panel power production.

In particular, the converters proposed are full-bridge converters, which are buck-derived isolated converters. The transformers have a ten times gain in order to allow the output voltage to be connected to a grid-tie inverter. A microcontroller, supplied by the PV panel, will be used in order to perform the gate switching for the converter with an open-loop control scheme using pulse-width modulation (PWM).

1.2. LITERATURE REVIEW

A model of a PV panel has been developed using datasheet values [1]. The model uses the single-diode, five-parameters model which takes into account the series and shunt resistance of the panel. With a proper model, simulation could easily be achieved and expected values of current and voltage could be predicted. Simulation and analysis of individual PV cells or modules has been performed [2]. This could also be adjusted to include the converter power stage and extended to comprise added control or other functions. Partial shading simulation of a PV panel is possible as well [3].

The impact of shading on array performance has been investigated [4-6]. There have been efficiency improvements in a series-connected PV array using individual power converters for each panel with partial shading [7]. This allows the maximum power from each panel to be delivered to the string with the use of module-level MPPT. However, the advantage is not as significant as a parallel-connected array. The effects of shading when comparing a series string to a parallel array at varying levels of insolation

corresponding to field data were analyzed and the parallel configurations yielded better performance [8].

There have been studies in different types of converters to use in photovoltaic applications. There has been extensive research of non-isolated converters used in photovoltaic applications [9]. Non-isolated converters could be designed in such a way that high-efficiency is possible regardless of the wide input range from a PV panel or a wide load range [10]. By analyzing the behaviors of the semiconductors, a converter could be optimized in order to achieve high efficiency. With improved semiconductor technologies, new boost converters are being developed for PV applications [11]. Multifunctional converters that integrate energy storage devices for use with PV generation system have been examined [12, 13].

The full-bridge converter can be designed in various ways. The typical conversion process in power electronics usually requires the use of magnetic components (such as inductors and transformers) that are frequently the heaviest and bulkiest item in the converter. These have a significant effect upon the overall performance, efficiency, size, and cost of the converter. Some studies have investigated the design and analysis of zero-voltage switched (ZVS), PWM converters [14-16]. This leads to a reduction in switching losses at higher frequencies. With higher frequency operation, the size and cost of the magnetic components, the inductors and transformers, in the circuit will be reduced. There has also been some investigation of zero-current switching (ZCS) to further reduce switching losses [17-20]. For higher power levels, high efficiency can be achieved with soft switching [21, 22]. From a lower power-scale prototype, a higher power converter could be designed. The converter could be designed for a flat efficiency

curve over a wide load range[23]. A current-fed full-bridge converter comparable in power level and efficiency has also been developed [24].

1.3. CONTRIBUTIONS OF THE THESIS

The main contributions of this thesis are:

- development and experimentation of an auxiliary circuit to supply gate drivers with power from a step-down circuit and gate signals from a microcontroller,

- development and implementation of a Labview interface to control devices and take measurements,

- development of the full-bridge buck-derived, isolated converter with novel parallel input, series-output transformer topology,

- presenting the simulation results to verify the design is sufficient,

- acquiring hardware bench-testing results, and

- obtaining outdoor solar-testing results.

1.4. THESIS ORGANIZATION

This thesis is organized into four sections. Section 1 provides a general introduction with a problem statement, literature review and contributions of the thesis. Section 2 describes the methodology used for the research, which covers the hardware and software design of a microcontroller circuit used for control, the development of a Labview interface to set an electronic load and measure input and output currents and voltages, and a discussion of the use of pyranometers and thermocouples. Section 3

presents the full-bridge converter used for experimentation, which explains the design and simulation of the full-bridge converter, the design and construction of the transformers used in the converter, and the experimental results from bench testing. Section 4 explains the setup and experimentation of the full-bridge converters with solar panels. Section 5 concludes the thesis and describes future work.

Following the solar testing conclusions, Appendix A contains the schematics and board layouts for the printed circuit boards used for collecting the experimental data. Appendix B includes the microcontroller code written to produce the pulse-width modulation gate signals. Appendix C illustrates the block diagram for the Labview interface and the human-machine interface screen used to capture data. Appendix D includes the data tables for solar testing at different isolation levels as well as the figures of the I-V and P-V curves for each isolation level, similar to Section 4 but more extensive.

2. METHODOLOGY

In this section the methods used to assist the project will be detailed. These include the methods to develop a microcontroller, a Labview program for data acquisition, and the use of a pyranometer and thermocouple.

2.1. MICROCONTROLLER

2.1.1. Hardware Design. The full-bridge converter is used in conjunction with another circuit which provides the voltage and the gate signals for the gate drivers. The schematic of this circuit is in Appendix A along with the printed circuit board (PCB) layout. This circuit has two step-down circuits, one to power the gate driver and the other to power the microcontroller. A buck converter, a TL2575-ADJIKTTR from Texas Instruments, with a variable gain is used in order to obtain the desired voltage for the gate drivers. The recommended circuit can be seen in Figure 2.1 [25].

The output voltage is determined by resistors R_1 and R_2 according to

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right)V_{ref} \tag{1}$$

where $V_{ref} = 1.23$ V. Resistors R_1 and R_2 were chosen to be 1kΩ and 6.8kΩ respectively to get an output voltage of 9.594 V. Capacitors C_1 and C_2 were recommended to be 100 μF and 330 μF, respectively. These are EEE-FP1V101AP and EEE-FP1C331AP, respectively, aluminum electrolytic capacitors from Panasonic. The diode D_1 was chosen to be a surface mount schottky diode, SSA34-E3/61T from Vishay. The inductor L_1 was recommended to be 330 μH. The inductor chosen is a MSS1260-334KLB from Coilcraft.
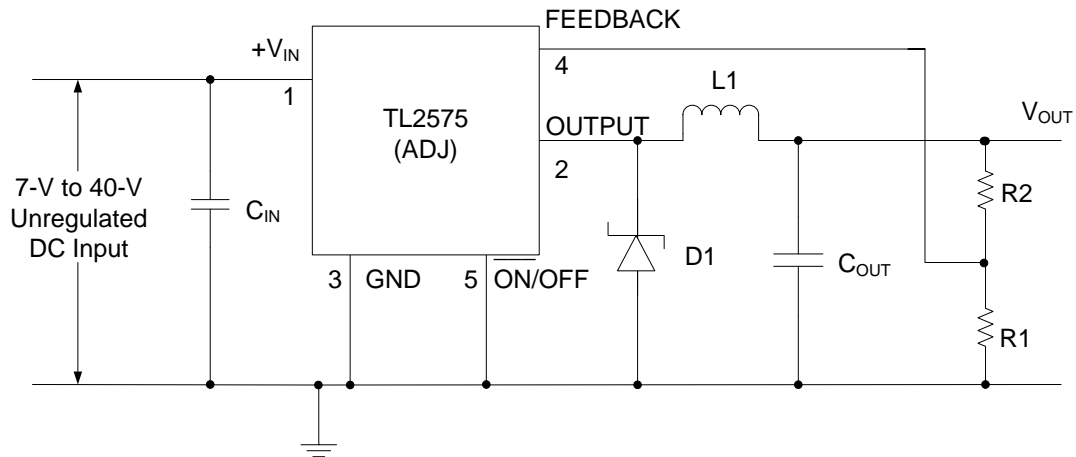
Figure 2.1. Recommended Circuit for Buck Converter

This voltage is then connected to a LD1117S33CTR low drop voltage regulator (LDO), from STMicroelectronics, in order to get a fixed 3.3 V to power the microcontroller, a MSP430F1222IDW from Texas Instruments. The recommended circuit can be seen in Figure 2.2 [26].

The input capacitor and output capacitors to the LDO are ceramic capacitors of 0.1 μF and 10 μF respectively. The output is connected to V_{cc} of Figure 2.3 [27], which shows the circuit design for in-circuit programming. Resistor R1 has a value of 47kΩ. Capacitors C1, C2 and C3 are ceramic capacitors with values of 2.2 nF, 10 μF and 0.1 μF respectively. The microcontroller was programmed with a debugging/programming interface, a MSP-FET430UIF from Texas Instruments. This is a USB to JTAG interface.
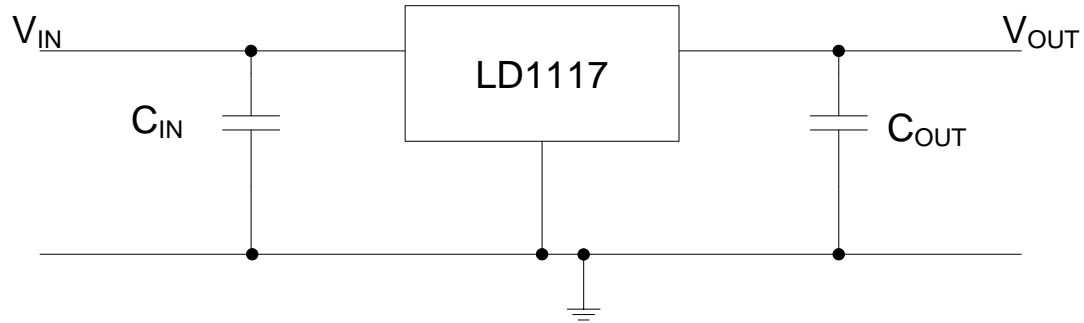
Figure 2.2. Recommended Circuit for LDO

For programming when the power to the microcontroller is supplied by the board, connect J1. For programming when the power of the microcontroller is supplied by the programming adapter, connect J2.

The outputs of the microcontroller are two signals connected to TA1 and TA2 which are used for the gate signals. Additionally, there are connections for alternative uses of the circuit. There is a connection to use a crystal oscillator on pins XIN and XOUT of the microcontroller. These would be used if the microcontroller internal oscillator is not sufficiently accurate. There are connections for the use of two push buttons on input pins P3.0 and P3.1 of the microcontroller. Two analog to digital converter (ADC) inputs are connected to pins P2.0 and P2.1 of the microcontroller that could be used for closed-loop control. A USART or UART mode can be used with pins UTXD0, which transmits data, and URXD0, which receives data. These additional connections can be seen in the PCB schematic shown in Appendix A. The present work did not use these extra features.
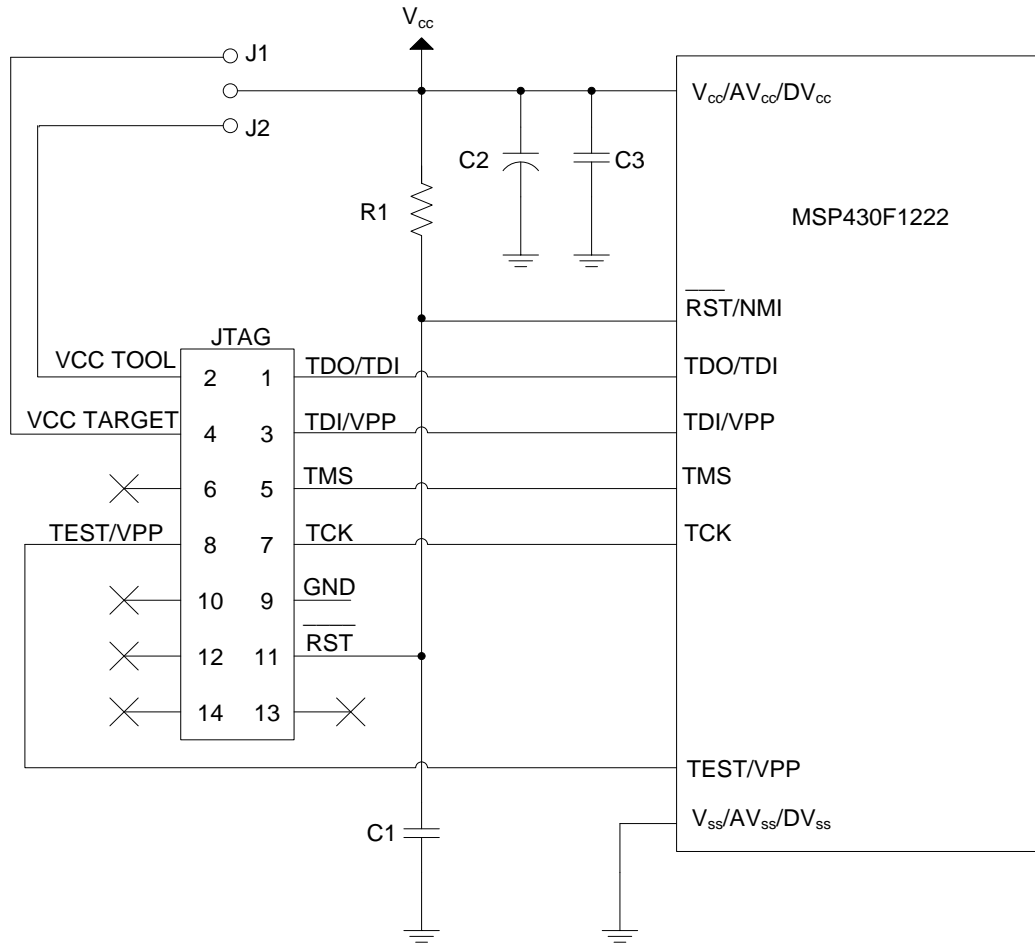
Figure 2.3. Circuit Design for In-Circuit Programming

2.1.2. Software Design. The microcontroller program was designed such that it will produce two gate signals with the same duty cycle and switching frequency but with a phase shift of 180 degrees. The desired switching frequency is 100 kHz. The program turns off unnecessary peripherals and the CPU enters a low power mode after the program is loaded in order to minimize power consumption.

The program first turns off the watchdog timer. The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software

problem occurs or if the selected time interval expires. Since there is no need for a system reset or interrupt routine, the watchdog timer is disabled.

Next the program will set two different registers, the DCOCTL and BCSCTL, in order to adjust the internal clock frequency. The DCOCTL register sets the DCO value to 7 and the BCSCTL register sets the RSEL value to 7. From the datasheet[28], the maximum value of the internal clock frequency is 5.4 MHz.

The program then sets the pins P1.2 and P1.3 to be PWM output pins using Timer A in up/down mode. The P1DIR register sets the pins as output pins and P1SEL designates the use of Timer A. The value of TACCR0 defines half of the PWM period and the values of TACCR1 and TACCR2 the PWM duty cycles. Using the system clock of 5.4MHz as Timer A clock, the value of TACCR0 can be determined with

$$TACCR0 = \frac{f_{CLK}}{2 \times f_{SW}} - 1 \qquad (2)$$

For a desired switching frequency of 100 kHz and the maximum clock frequency of 5.4 MHz, the value of TACCR0 is 26. However through experimentation the value of switching frequency was measured as 93.3 kHz. The lower than expected value is attributed the tolerance in clock frequency but based on the switching frequency, the estimated clock frequency is 5.038 MHz

In order to achieve the phase shift necessary, TACCR1 is set to toggle/set mode and TACCR2 is set to toggle/reset mode, using the TACCTL1 and TACCTL2 registers respectively. The value of TACCR1 was set to 15 and the value of TACCR2 was set to 11. This gives each signal an effective duty cycle of 42%. An example of the operation of the PWM signals can be seen in Figure 2.4[29].
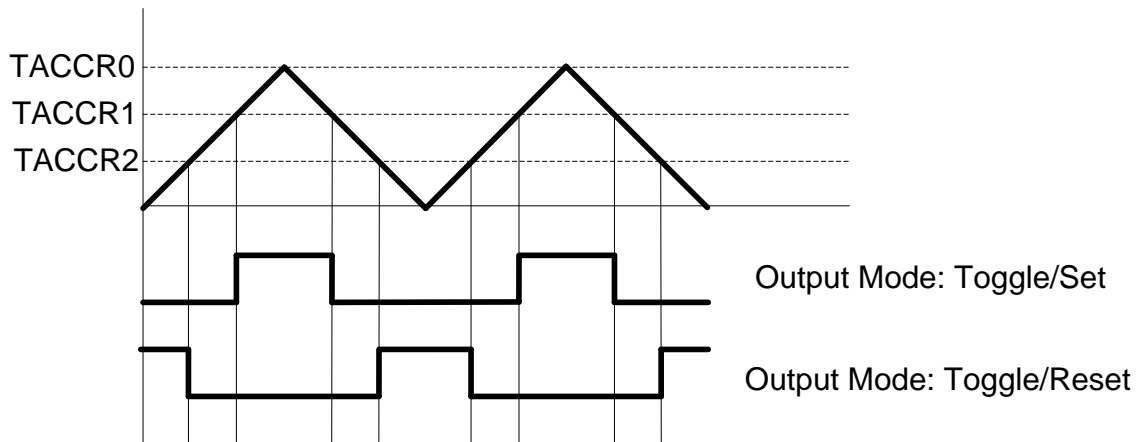
Figure 2.4. PWM Output Signals

The last thing done in the program is to set the microcontroller into low-power mode. In this mode, the central processing unit and the master clock are disabled. The entire microcontroller program can be seen in Appendix B.

2.2. LABVIEW

The Labview interface was developed using Labview 10.1 in order to measure the input voltages, input currents, output voltages and output currents of the converters for specific load points. The block diagram can be seen in Appendix C. The electronic load, an Agilient N3300A, uses two modules in order to be within voltage ratings. Each module can handle 240 V and 30 A. One module is used as a voltage source to handle large voltages while the other module is used as a current or resistive load. There are three main parts to the visual interface. These include an initialization routine, the main routine and a shutdown routine.

For the initialization routine, the mulitimeters (Fluke 8845A) and the electronic load are configured. The multimeters are set to their specific function, whether that be

measuring dc voltage or dc current, and individual ranges were also set. The multimeters connected to the inputs of the converters were set with a 10 A range for the input current and a 100 V range for the input voltage. The multimeters connected to the outputs of the converters were set with a 3 A range for the output current and a 1000 V range for the output voltage. The first module on the electronic load is set to a current load with a 1 A range and a value of 1 mA. The range is set in order to receive a better degree of precision on the value of the current. The particular ranges are 48, 480, or 4800 ohms. The second module is set to a voltage load with a value of 100 V. This is in order to protect the first module in case the output voltage of the converter is greater than 240 V. This circuit is shown in Section 4.

The main routine takes the values of the maximum current and the step size that the user inputs into the visual interface to run a for-loop. This determines the amount of times the for-loop runs. The commanded current is determined by the step size and that value is sent to a text builder. The text is a program command to the electronic load. After a short time delay, the multimeters will measure the input voltages and input currents for each converter. There are some time delays inserted in this process to avoid software crashes. The electronic load will measure the output voltage and output current for the paralleled output of the converters. The output voltage data is sent to a voltage selector to determine a safe value of voltage for the voltage mode module of the electronic load. It is also used for determining the proper resistive load when the electronic load switches from a current load to a resistive load. When the commanded current is greater than 0.4 A, the program commands change the electronic load from a current load to a resistive load. Resistance is determined according to

$$R = \frac{V[k-1] - V_{OFFSET}}{I[k]} \tag{3}$$

where *I[k]* is the commanded current value, *V[k-1]* is the measured output voltage from the previous measurement, and V_{OFFSET} is the voltage offset on Channel 3. The range for the resistive load is also set in order to increase precision for the resistance commanded.

The values of the input and output voltages and currents are sent to various plotting blocks and a block that records the data into an excel spreadsheet. This is for verification by the end-user to see if the data is correct and sufficient based on what is expected.

The shutdown routine starts by setting the voltage module of the electronic load to 100 V. The electronic load is also set back to a current load. The routine then runs through a for-loop designed to ramp down the current on the load from the maximum current to 500 mA and then dropping down by 100 mA increments to 100 mA. There is a time delay between steps in order to limit software crashes.

2.3. PYRANOMETER/THERMOCOUPLES

A Li-Cor pyranometer is used in order to measure the solar radiation flux density (in watts per meter square) on the solar panel surface. The pyranometer was connected to a Fluke 115 hand-held digital multimeter in order to measure the DC voltage signal produced. The conversion from the DC voltage to solar radiation flux density is given by the manufacturer as $1mV = 100 \frac{W}{m^2}$.

A thermocouple is a device consisting of two different conductors that produce a voltage proportional to a temperature difference between either end of the pair of

conductors. A K-type thermocouple, from Newport, was attached to the bottom of the solar panel and the signal was measured on a Metex M-3850D digital multimeter to measure the temperature in Fahrenheit or Celsius.

2.4. SUMMARY

The devices and programs described here were used to supplement the design and experimental process. The microcontroller circuit was developed to supply the gate drivers with power and gate signals. The Labview program was created to control the multimeters and electronic load in order to make changes to the equipment and take measurements at a higher rate than by hand. The thermocouples and pyranometers were utilized to determine the temperature on the individual PV panel and the insolation levels being received.

3. FULL-BRIDGE CONVERTER

3.1. DESIGN

The converters proposed are full-bridge converters, which are buck-derived isolated converters. This can be seen in Figure 3.1. The converter used a high-reliability, high-ripple-current capacitor on the input terminals (C1); four MOSFETs arranged in an H-bridge; two transformers connected in an input-parallel, output-series topology; a full-bridge rectifier composed of ultrafast diodes; and an output filter composed of an inductor (L1) and a capacitor (C2). The converters have been built with the circuit parameters shown in Table 3.1. The interface between the controller and the MOSFETs used dielectric-isolated gate drivers. The designed operating frequency was chosen to be 93 kHz to minimize transformer size.
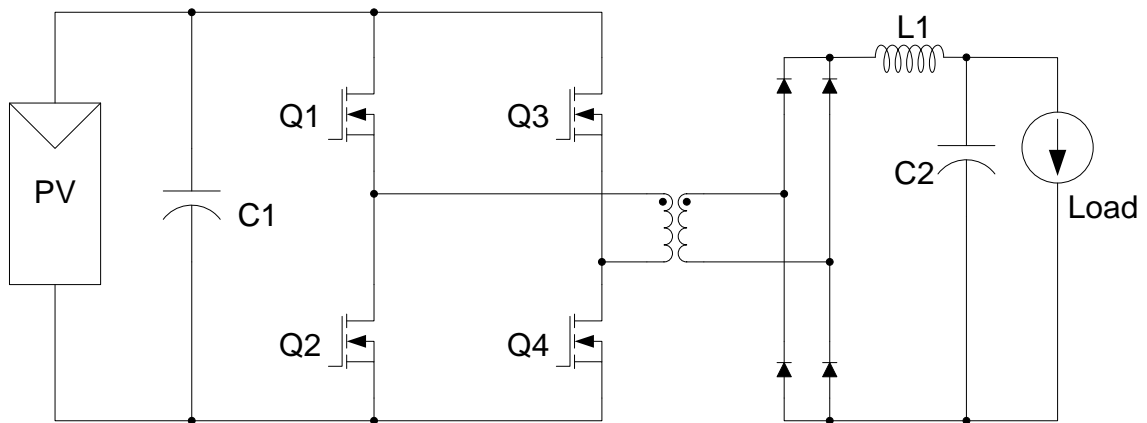

Figure 3.1. Full-Bridge Converter Topology

To limit the effect of the primary winding losses on the transformer, two transformers were connected in parallel on the primary and in series on the secondary, as

may be seen in Figure 3.2. With the series connection, the secondary currents were

forced to be equal, so the primary currents were equal by necessity. The MOSFETs are

controlled with a microcontroller, set to generate PWM waveforms with an effective duty

ratio (after rectification on the secondary) of 84%, as described in Section 2.1.

Table 3.1. Converter Circuit Parameters

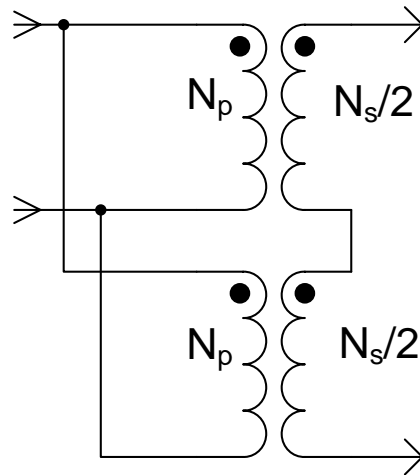| Parameter	Value	Parameter	Value
Input Capacitance (C1)	68 μF	MOSFET	TPCA8048-H
Output Capacitance (C2)	100 μF	Rectifier Diode	PDU540
Output Inductance (L1)	470 μH	Switching Frequency (f_{sw})	93.3 kHz

Figure 3.2. Input-parallel-output-series transformer connections

Toshiba TCPA8048 MOSFETs were chosen for the bridge because of their

exceptionally low on-state resistance and reasonable gate charge and output capacitance.

These are packaged in an enhanced (for low thermal resistance and low on-state

resistance) version of an SO-8, a surface-mount package measuring 6 mm $\times$ 5 mm.

The gate drivers used in the first revision of the board were International Rectifier IR2110 dual drivers. In the second revision, these were replaced with IR2101 drivers, which are smaller and less expensive but with otherwise similar specifications. The IR driver chips have one channel that is referred to the input common and one channel that is floating, suitable for driving the high-side MOSFET in one leg of the full-bridge.

The output rectifier bridge used ES3J diodes in the first revision and PDU540 diodes in the second revision. Both types are ultrafast (with reverse recovery times of 35 ns) with suitable voltage ratings. The PDU540 was chosen because of a lower on-state conduction loss.

The PCB schematics and board layouts of the complete converter circuit with auxilary circuit can be seen in Appendix A.

3.2. TRANSFORMER DESIGN AND CONSTRUCTION

For the initial design of the transformers using the K_g core geometry approach (from McLyman [30]), the design specifications can be seen in Table 3.2.

Table 3.2 Transformer Design Specifications

Input Voltage, V_{in}	26.6V
Output Voltage, V_{out}	266V
Output Current, I_o	0.7519A
Output Power, P_o	200W
Switching Frequency, f_{sw}	100kHz
Efficiency, η	97%
Regulation, α	2%
Operating Flux Density, B_{ac}	0.1T
Window Utilization, K_u	0.4

The regulation and power-handling ability of a core is related to the core geometry. In order to calculate the appropriate core geometry, K_g, the regulation, the apparent power (P_t), and the electrical conditions (K_e) need to be determined. The regulation is determined from the specifications in Table 3.2. The transformer apparent power, P_t, is determined using

$$P_t = P_O\left(\frac{1}{\eta} + 1\right) \tag{4}$$

where the output power and the expected efficiency can be seen in Table 3.2. The calculated value of the apparent power is 406.19 W. K_e is determined by the magnetic and electric operation condtions, which are related by

$$K_e = 0.145\left(K_f\right)^2\left(f_{sw}\right)^2\left(B_{ac}\right)^2\left(10^{-4}\right) \tag{5}$$

where the waveform coefficient, K_f, has a value of 4 due to a square wave gate signal. The electric conditions equaled 23200. The core geometry, K_g, is calculated using

$$K_g = \frac{P_t}{2K_e\alpha} \tag{6}$$

The core geometry equaled 0.004377 cm^5 where the constant α has a value of 2 and not its percentage value of 0.02.

The next step is to select an appropriate core that meets or exceeds this minimum required core geometry, K_g. Also in the selection of the core is to find one with the proper core material. For this design, an ETD-29 ferrite core was chosen with a core material of 3C90. The ETD-29 core geometry value is 0.0517 cm^5 which is higher than the calculated value. This means the ETD-29 core is suitable for the transformer design. Although a smaller core could have been chosen, the ETD-29 core was chosen for ease of

transformer construction . The design specifications for the ETD-29 can be seen in Table 3.3.

Table 3.3. Design Data for ETD-29 Ferrite Core

Copper Weight (W_{tcu})	32.1 grams
Core Weight (W_{tfe})	28 grams
Mean Length Turn (MLT)	6.4 cm
Magnetic Path Length (MPL)	7.2 cm
W_a/A_c	1.865
Cross-Sectional Area (A_c)	0.761 cm^2
Window Area (W_a)	1.419 cm^2
Area Product (A_p)	1.08 cm^4
Core Geometry (K_g)	0.0517 cm^5
Surface Area (A_t)	42.5 cm^2
AL	1000 mh/1K

Next, the parameters of the primary winding are determined. These are the number of turns on the primary, current density, calculated input current, primary bare wire area, the resistance of the primary winding, and the power loss on the primary winding. The number of primary turns, N_p, can be expressed using Faraday's Law

$$N_p = \frac{V_{in}\left(10^4\right)}{K_f B_{ac} f_{sw} A_c} \qquad (7)$$

The number of primary turns was calculated to be 8.7385 turns and was rounded down to 8 turns. The current density, J, was calculated using

$$J = \frac{P_t\left(10^4\right)}{K_f K_u B_{ac} f_{sw} A_p} \qquad (8)$$

The current density was calculated to be 235.06 A/cm^2. The input current, I_{in}, was evaluated to verify what is expected using

$$I_{in} = \frac{P_o}{V_{in}\eta} \tag{9}$$

The calculated input current was 7.751337 A, which is within the expected range of input current. The primary bare wire area, $A_{wp(B)}$, was calculated using

$$A_{wp(B)} = \frac{I_{in}}{J} \tag{10}$$

The calculated primary bare wire area was 0.032975 cm^2. The appropriate wire size was selected from [30] to be 12 AWG. 12 AWG has a bare wire area of 0.03308 cm^2 and is larger than the calculated value, making it suitable for use. The primary resistance, R_p, was calculated using

$$R_p = MLT\left(N_p\right)\left(\frac{\mu\Omega}{cm}\right)\left(10^{-6}\right) \tag{11}$$

where $\left(\frac{\mu\Omega}{cm}\right)$ was given as 52.1. The primary resistance was 2.668mΩ. The primary copper loss, P_p, was predicted using

$$P_p = I_p^2 R_p \tag{12}$$

The primary copper loss was predicted to be 0.1603 W.

Next, the parameters of the secondary winding are determined. These are the number of turns on the secondary, secondary bare wire area, the resistance of the secondary winding, and the power loss on the secondary winding. The number of secondary turns, N_s, was calculated using

$$N_s = \frac{N_p V_s}{V_{in}}\left(1 + \frac{\alpha}{100}\right) \tag{13}$$

The number of secondary turns was calcultated to be 81.6 turns and was rounded down to 80 for a ten times gain on the transformer. The secondary bare wire area, $A_{ws(B)}$, was calculated using

$$A_{ws(B)} = \frac{I_o}{J} \tag{14}$$

The calculated secondary bare wire area was 0.003199 cm^2. The appropriate wire size was selected from [30] to be 22 AWG. 22 AWG has a bare wire area of 0.003243 cm^2 and is larger than the calculated value, making it suitable for use. The secondary winding resistance, R_s, was calculated using

$$R_s = MLT\left(N_s\right)\left(\frac{\mu\Omega}{cm}\right)\left(10^{-6}\right) \tag{15}$$

where $\left(\frac{\mu\Omega}{cm}\right)$ was given as 531.4. The calculated secondary resistance was 0.27208Ω.

The secondary copper loss, P_s, was predicted using

$$P_s = I_o^2 R_s \tag{16}$$

The secondary copper loss was predicted to be 0.15382 W.

The last step is to calculate the total system parameters. These include the total primary and secondary copper loss, the transformer regulation, the core loss, the total loss and the calculated window utilization. The total primary and secondary copper loss, P_{cu}, was calculated using

$$P_{cu} = P_p + P_s \tag{17}$$

The total primary and secondary copper loss was calculated to be 0.31412 W. The transformer regulation, α, was calculated using

$$\alpha = \frac{P_{cu}}{P_o}(100) \tag{18}$$

The calculted transformer regulation was 0.15706 %. In order to determine the core loss,

a watts per kilogram value must be determined. The watts per kilogram, W/kg, was

calculated using

$$\frac{W}{kg} = k\left(f_{sw}\right)^m \left(B_{ac}\right)^n \tag{19}$$

where k equals 0.001983, m equals 1.36 and n equals 2.86 based on material properties of

the chosen core [30]. The calculated core loss power density was was 17.2712 W/kg.

The core loss, P_{fe}, was calculated using

$$P_{fe} = \left(\frac{W}{kg}\right)\left(W_{rfe}\right)\left(10^{-3}\right) \tag{20}$$

The calculated core loss was 0.48359 W. The total loss, P_{Σ}, was calculated using

$$P_{\Sigma} = P_{cu} + P_{fe} \tag{21}$$

The total power loss of the transformer was calculated to be 0.7977 W. The total

calculated window utilization, K_u, was determined using

$$K_u = \frac{N_p A_{wp(B)} + N_s A_{ws(B)}}{W_a} \tag{22}$$

The total calculated window utilization was 0.366. This value is the percentage of the

window area that is being utilized by bare wire cross-sectional area (which is 36.6%). An

example diagram of the transformer windings can be seen in Figure 3.3.
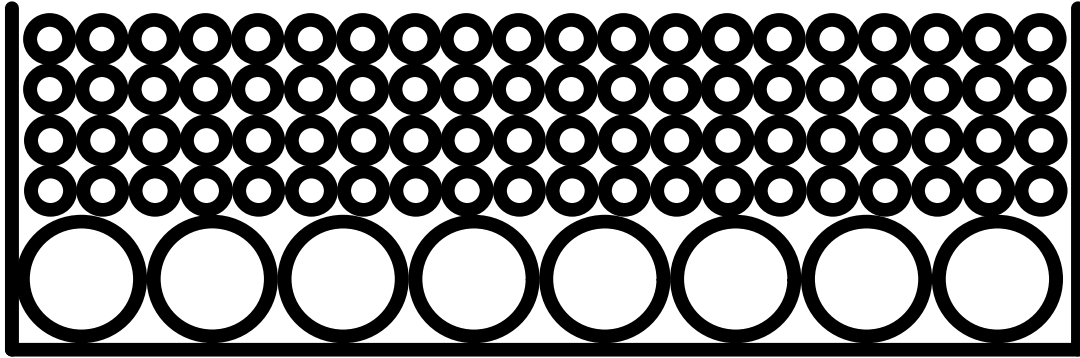
Figure 3.3. Transformer Winding Diagram

From the initial transformer design, early attempts used larger ETD cores (ETD34, ETD44, ETD49 and ETD54) with a foil winding for the primary and round-wire winding for the secondary for ease of construction. At 93 kHz, the skin depth in copper (ε), calculated using

$$\varepsilon = \frac{6.62}{\sqrt{f_{sw}}} \tag{23}$$

 is 0.02171 cm. This value needs to be doubled to determine the proper wire size. The wire diameter would need to be 0.04342, which is approximately the diameter of 26 AWG wire. To minimize skin and proximity effect, a wire size with a radius equal to the skin depth is desired. However, to achieve the proper current density, the equivalent of 12 AWG is needed on the primary, 22 AWG on the secondary. To approximate 12 AWG, copper foil of a width similar to the bobbin width and 813 μm thickness was used. The copper foil was wrapped in insulating tape. For the secondary, 22 AWG wire was used as a reasonable compromise.

Unfortunately, manufacturing a transformer with low-resistance termination connections using the foil was unattainable. Therefore, a different approach was used.

The largest component of power loss was the copper loss on the primary winding. Thus to decrease the power loss in the primary winding, two transformers with parallel primaries were designed. This would decrease the magnitude of primary current by a factor of two and the overall resistance of the parallel-input would decrease by a factor of two. To ensure current sharing, their secondaries were connected in series, as shown in Figure 3.2. With the series connection, the secondary currents were forced to be equal, so the primary currents were equal by necessity. With the reduced primary current, 15 AWG equivalent was needed, so the transformers were constructed with 2×18 AWG in parallel on the primary. Again 22 AWG was used on the secondary. Since power handling decreased, the size of the core could be decreased to an ETD29. This approach was much easier to construct, and therefore achieved better results despite the theoretical advantage of foil windings.

3.3. SIMULATION

In order to assist in part selection and feasibility, a simulation was developed using Simulink and PLECs. The simulation was helpful in determining if the ratings of the components chosen were sufficient. In a simulated environment, the currents on surface mount components (MOSFETs, rectifier diodes, inductors, etc.) could be measured whereas on the physical board this was not possible. Figure 3.4 shows the simulaiton model built in PLECs.
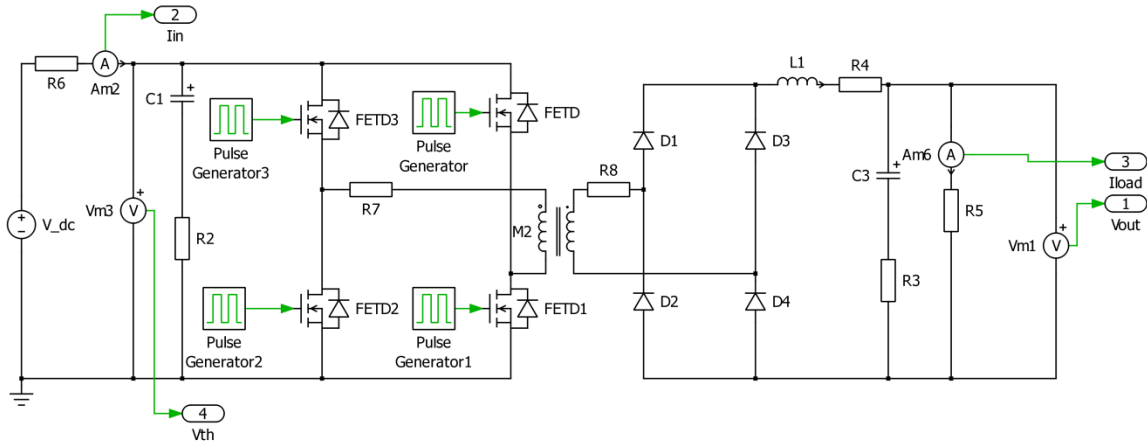
Figure 3.4. Simulation Model of Full-Bridge Converter

Along with this model an m-file was used to input component values into the

simulation model. In this way, the converter parameters could easily and convieniently

be changed. The initial constructed transformers were connected to a Hewlett Packard

4284A Precision LCR Meter in order to measure the inductance of each of the windings.

This was done by connecting the LCR meter to the respective winding and leaving the

other winding in an open-circuit. For leakage values, the LCR would be connected to the

appropriate winding and the other winding would be shorted. The resistance vaues

values received from the LCR were either exceptionally high or negative values. Thus

the calculated winding resistance values were used because of error in measurement of

the resistance with the LCR meter. The values of the components (given in Table 3.1),

the expected value of the on-state resistance, the measured values of the transformer were

put into a ideal transformer model (coupled inductors) and the calculated winding

resistance values were were put into the m-file.

The values of on-state resistance, transformer winding inductances, and calculated

transformer values can be seen in Table 3.4.

Table 3.4. Simulation Model Values

Parameter	Value	Parameter	Value
Input Capacitor Resistance	28 mΩ	Output Capacitor Resistance	0.86 Ω
Output Inductor Resistance	707 mΩ	MOSFET Resistance	4.3 mΩ
Primary Inductance (L_P)	122 µH	Secondary Inductance (L_S)	12.94 mH
Calc. Primary Resistance	2.67 mΩ	Calc. Secondary Resistance	272 mΩ

From the values for the transformer inductances, the mutual inductance can be

approximated using

$$M = L_P \left(\frac{N_S}{N_P} \right) \tag{24}$$

This value would need to be included in the coupled inductor matrix as

$$\begin{bmatrix} L_P & M \\ M & L_S \end{bmatrix} \tag{25}$$

With the values in MATLAB, the simulation was ran and a high efficiency (greater than

95%) was verified along with expected voltages and currents of the converter. The

simulated results of the power and efficiency can be seen in Figure 3.5.

From the results we can see where the value of input power (approximately 203

W) is about what is expected (205 W). The output power ripple is within a reasonable

amount of tolerance with less than 1 W of ripple. The simulated efficiency is nearly

98%.
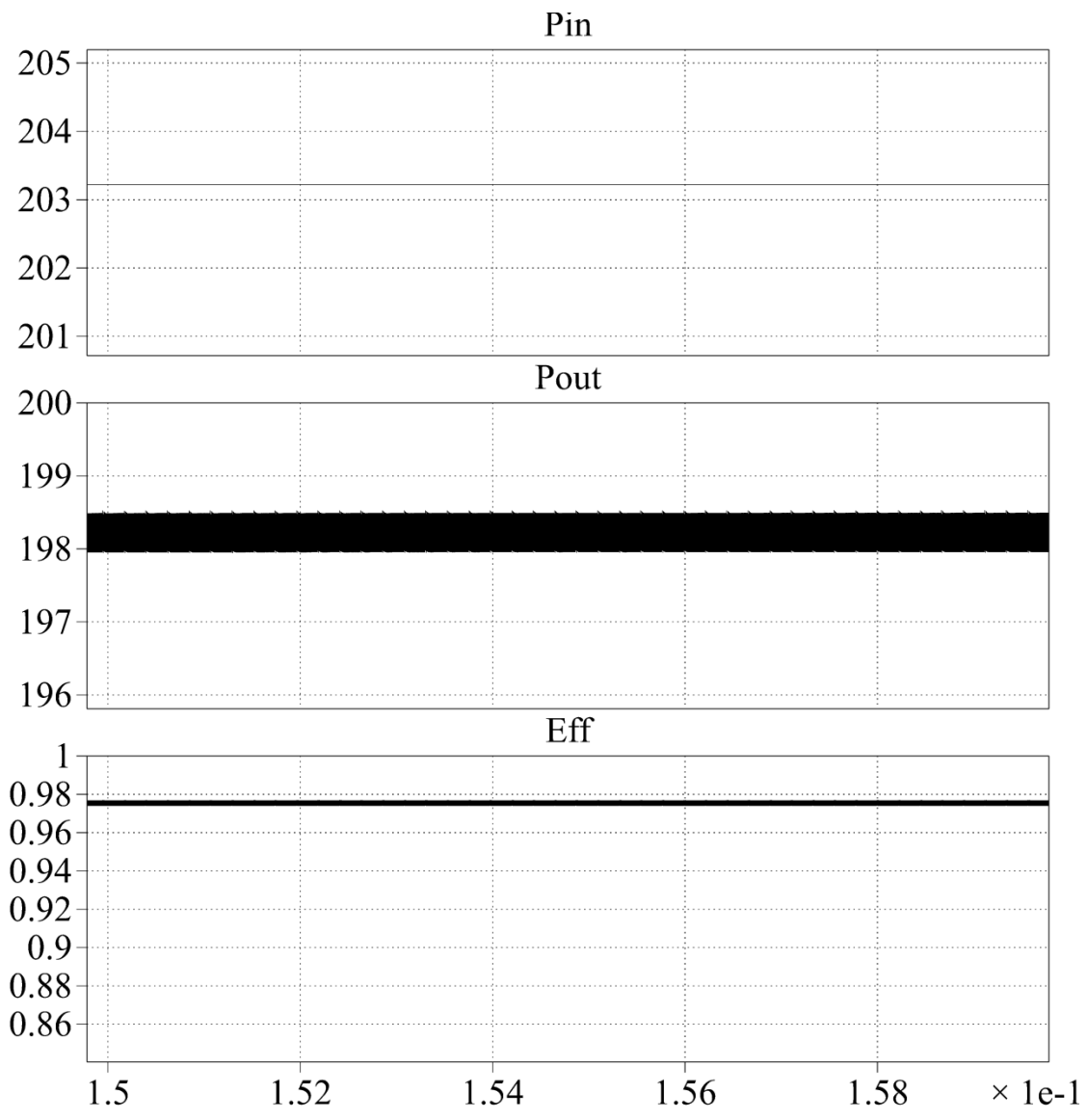
Figure 3.5. Simulation Results

3.4. EXPERIMENTAL RESULTS

There were multiple experiments ran in order to measure the capabilities of the converters. There was a transient response experiment to ensure that the converter could respond to a change in the input within a reasonable amount of time. Source and load

regulation were measured as well. The current and voltage on the input and output was measured in order to produce relevant graphs to what is expected for outdoor testing.

Figure 3.6 shows the transient response to a step in current load from 100 mA to 150mA. The input voltage is shown on Channel 1 with 10 V per division and the output voltage is shown on Channel 2 with 5 V per division and a voltage offset.
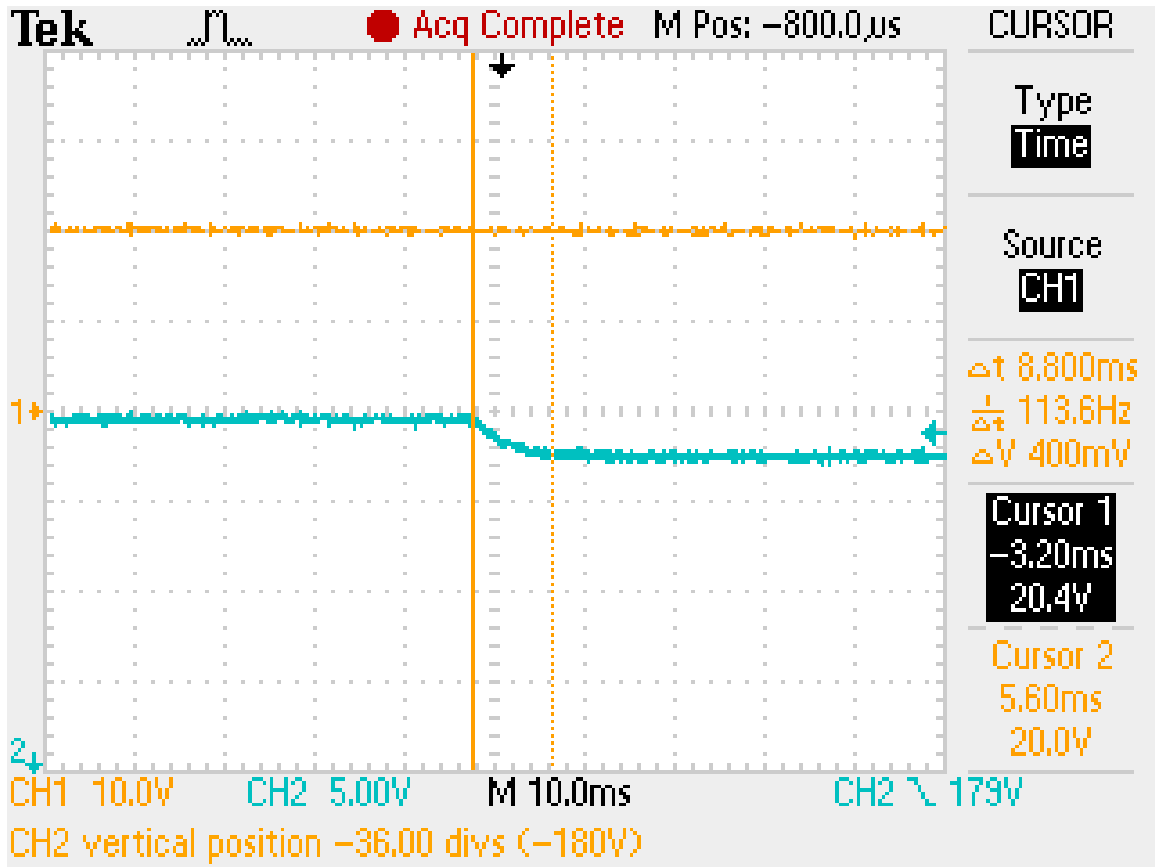
Figure 3.6. Transient Response

Figure 3.7 shows the source regulation (*SR*), defined as

$$SR = \frac{\left.\frac{V_{out}}{V_{in}}\right|_{V_{in}=25} - \left.\frac{V_{out}}{V_{in}}\right|_{V_{in}=20}}{\left.\frac{V_{out}}{V_{in}}\right|_{V_{in}=25}} \tag{26}$$

The objective of the source regulation experiment is for the gain of the converter, output voltage (V_{out}) divided by input voltage (V_{in}), to remain constant regardless of input voltage. This is essentially a gain error. The mean source regulation for output currents above 100 mA (where the converter entered continuous conduction mode) was approximately 2%.

Figure 3.8 shows the load regulation for two different values of input voltage. For very low load currents, the converter enters discontinuous conduction mode and the output voltage floats up. Measuring from the point where the converter enters continuous conduction mode (an output current of 100mA) to full load, the load regulation was 7.71%.

The current versus voltage (I-V) waveforms for the two converters can be seen in Figure 3.9 and Figure 3.10. Figure 3.9 shows the input current versus input voltage waveforms and Figure 3.10 shows the output current versus output voltage waveforms. This shows how well the two converters perform in relation to eachother. Ideally the waveforms would be identical and the converters would behave similarly. The difference in transformer construction is at fault for the small differences seen.
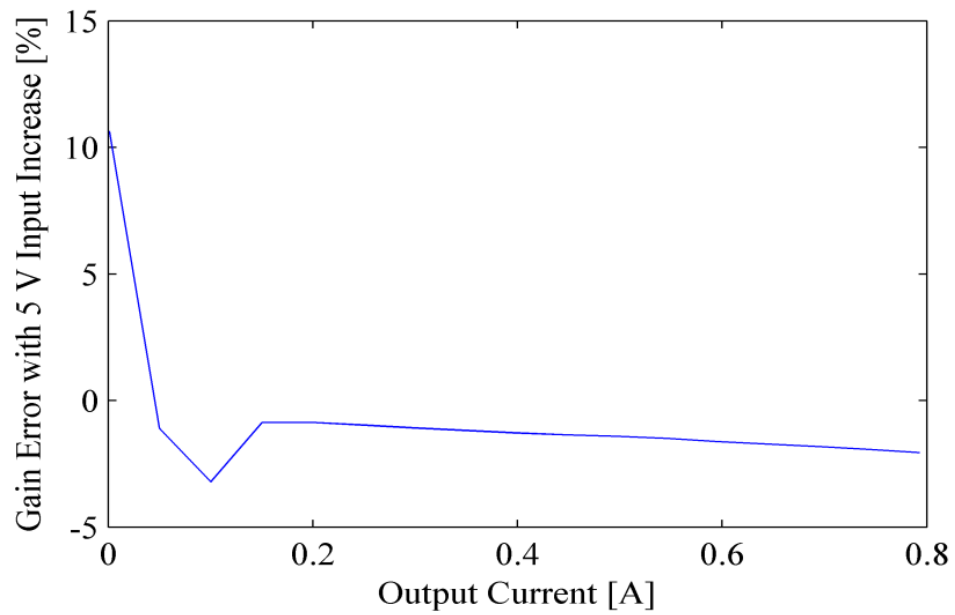
Figure 3.7. Source Regulation
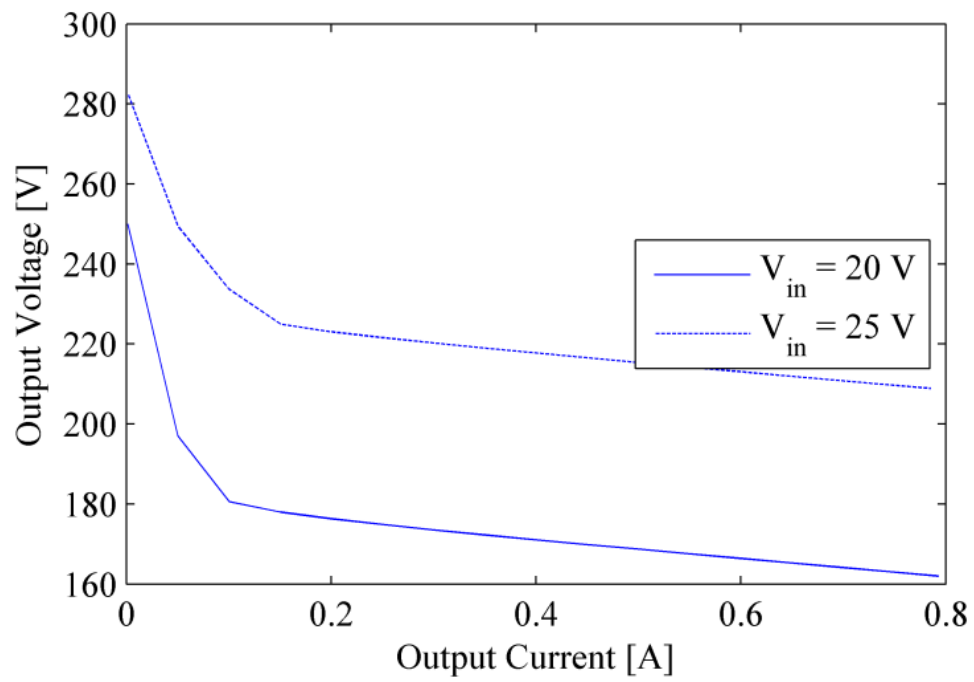
Figure 3.8. Load Regulation
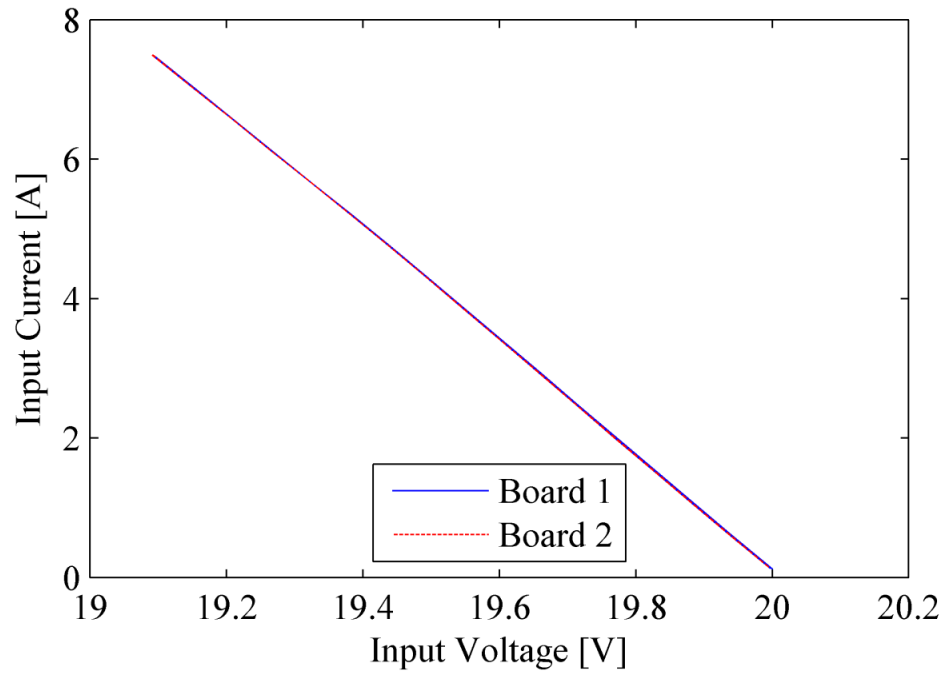
Figure 3.9. Input I-V Waveforms
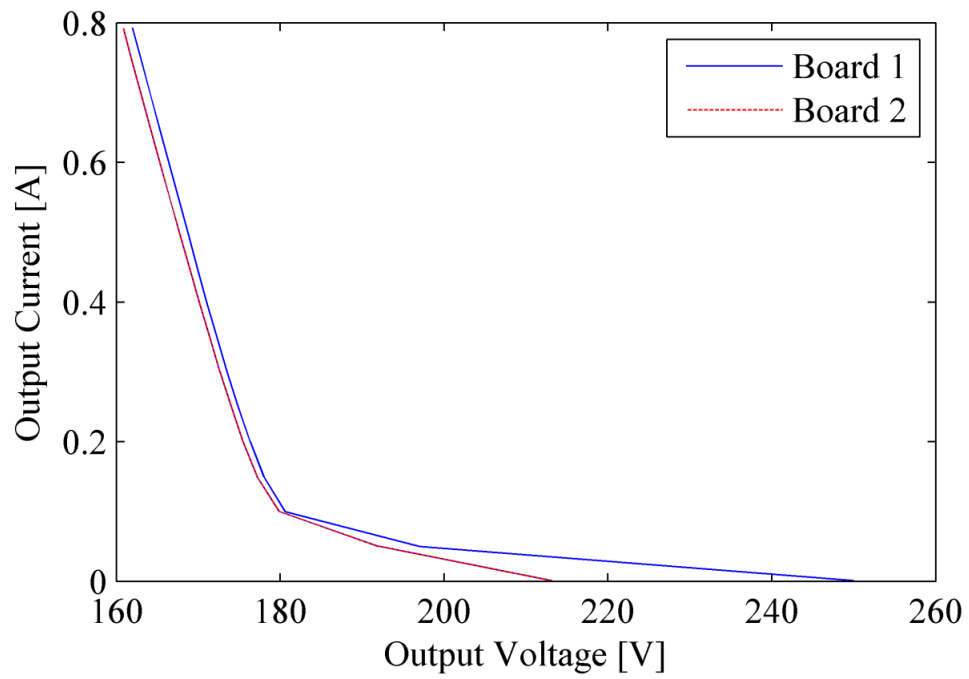
Figure 3.10. Output I-V Waveforms

The power versus voltage (P-V) waveforms for the two converters can be seen in

Figure 3.11 and Figure 3.12. Figure 3.11 shows the input power versus input voltage

waveforms and Figure 3.12 shows the output power versus output voltage waveforms.

As in the I-V waveforms, this shows how well the two converters perform in relation to

eachother. Ideally, the waveforms would be identical and the converters would behave

similarly. The difference in transformer construction is at fault for the small differences
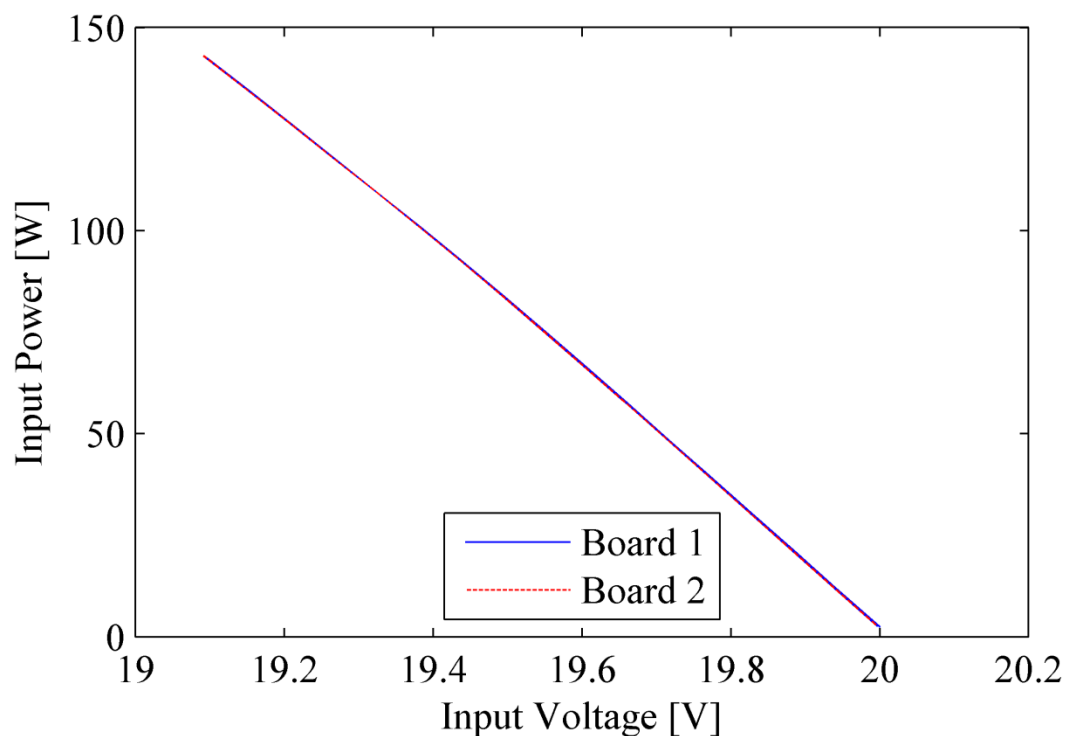
seen.

Figure 3.11. Input P-V Waveforms

The efficiency versus output current can be seen in Figure 3.13. The peak efficiency for

Board 1 was 90.98% at approximately 450mA output current. The peak efficiency for

Board 2 was 90.16% at approximately 450mA output current. This was almost entirely

due to construction of the transformer. With a better manufacturing process, a highly

efficient transformer could be constructed and high efficiency converters could be

achieved.
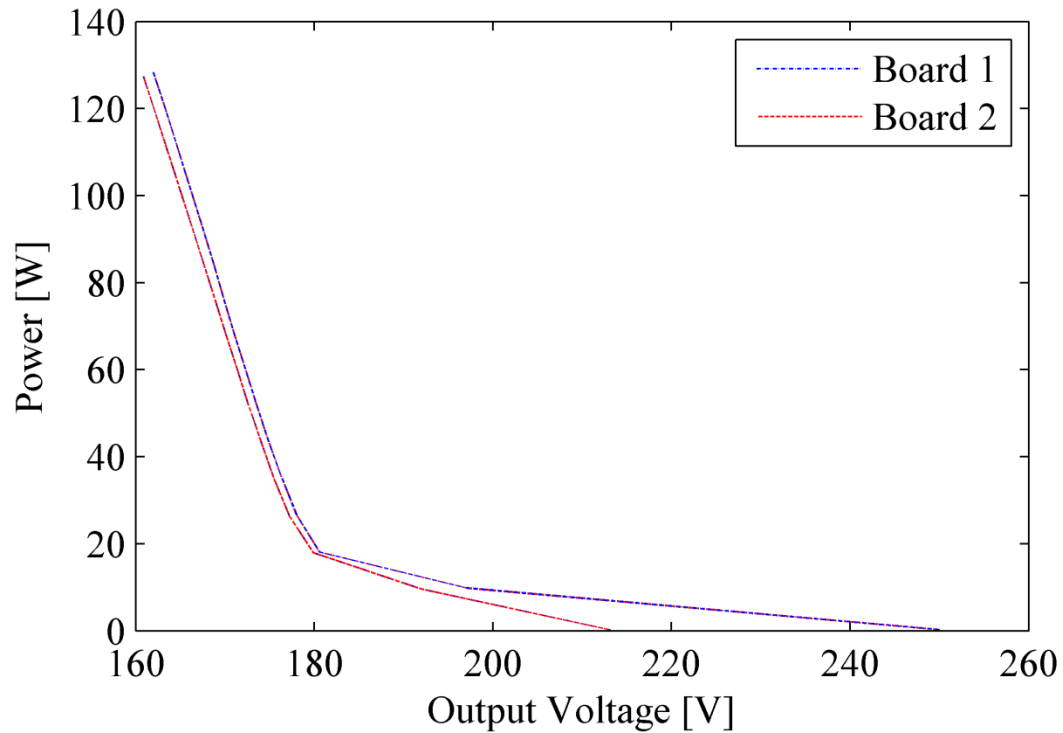
Figure 3.12. Output P-V Waveforms

The efficiency graphs are nearly identical which is expected from the I-V and P-V

waveforms. The very low efficiency at the beginning can be attributed to a constant

control current of 1mA for the commanded output current. This was a safety constraint

of Labview to give a low control value for measurement.
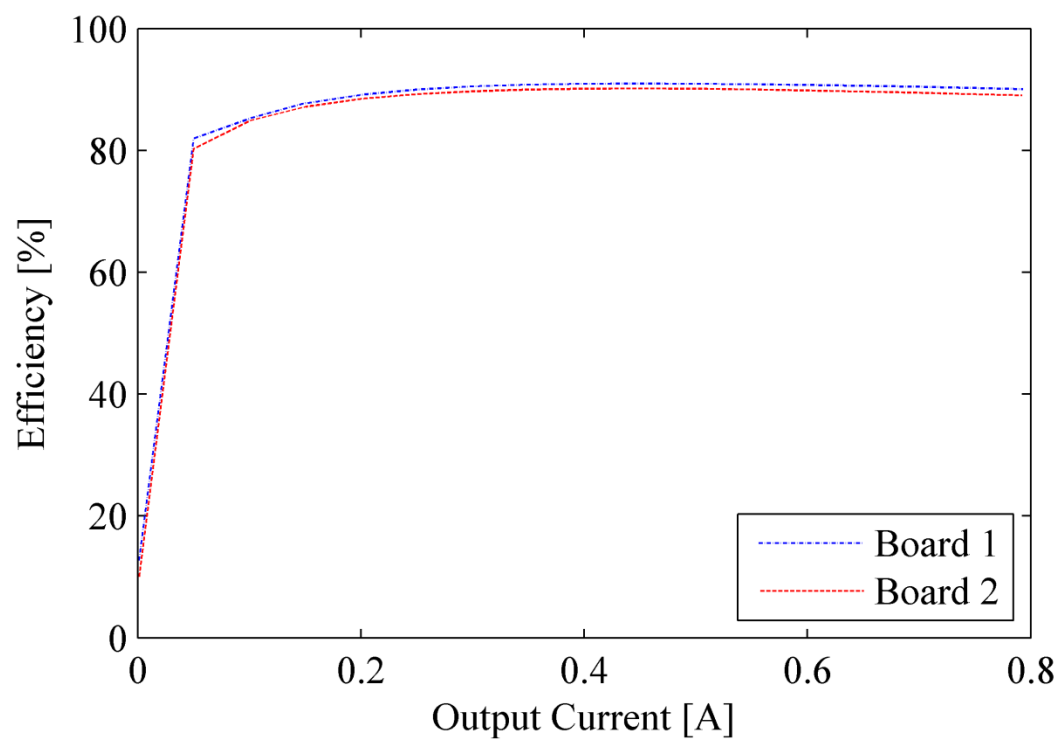
Figure 3.13. Efficiency Waveforms

4. SOLAR TESTING

4.1. SETUP

  Experimental data was obtained through outdoor solar testing of the full-bridge

converters with parallel connected photovoltaic array as shown in Figure 4.1. Shown in

the electronic load block is the different modules used as described in Section 2.2. Each

solar panel is connected to a full-bridge converter. For the tests described in this chapter,

Kyocera KD215GX-LPU multicrystalline panels were used. The experimental setup for

outdoor solar testing is shown in Figure 4.2. For our experiments, Board 1 was

connected to Panel 1 and Board 2 was connected to Panel 2. The bench results of Board

1 and Board 2 can be seen in Section 3.4.
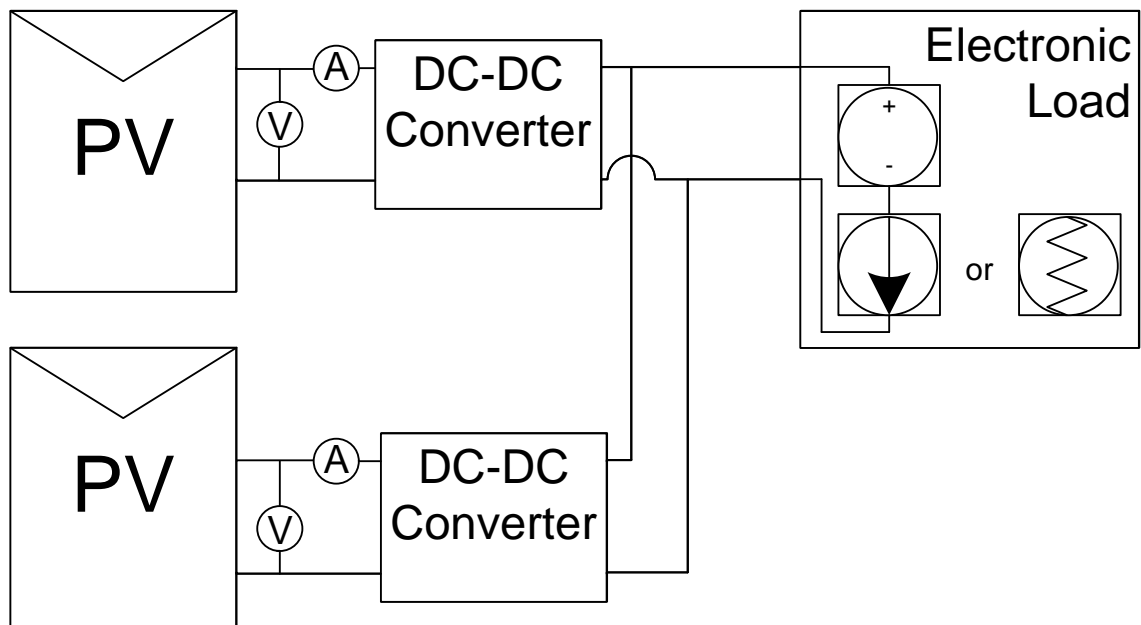
Figure 4.1. System Topology

There are two high-precision multimeters, Fluke 8845As, either used as both a voltmeter and an ammeter on the input of a single full-bridge converter. The individual full-bridge converters are connected in parallel to an electronic load, an Agilient N3300A, which is also used to measure the output voltage and output current.

Figure 4.2. Physical Experimental Setup

For the solar testing, Blue Hawk 4 mil thick, heavy-duty plastic sheeting was cut into smaller sheets. These were placed on top of the solar panels in order to provide varying levels of insolation to the solar panels. There were six different levels of insolation tested where there were unshaded, some partial shading, and full shading of an

individual panel. Figure 4.3 shows the physical setup to simulate a uniform insolation

over a solar panel.

Figure 4.3. Physical Setup of Uniform Insolation

4.2. EXPERIMENTAL RESULTS

In this section, the results for unshaded, partial shading and full shading are

shown. These include the current versus voltage (I-V) and power versus voltage (P-V)

waveforms along with maximum power point data tables. More results may be found in

Appendix D.

Figure 4.4 shows the current versus voltage (I-V) curves for the unshaded condition. Figure 4.5 shows the power versus voltage (P-V) curves for the unshaded condition. These figures demonstrate that the two converter outputs are nearly identical for unshaded conditions.
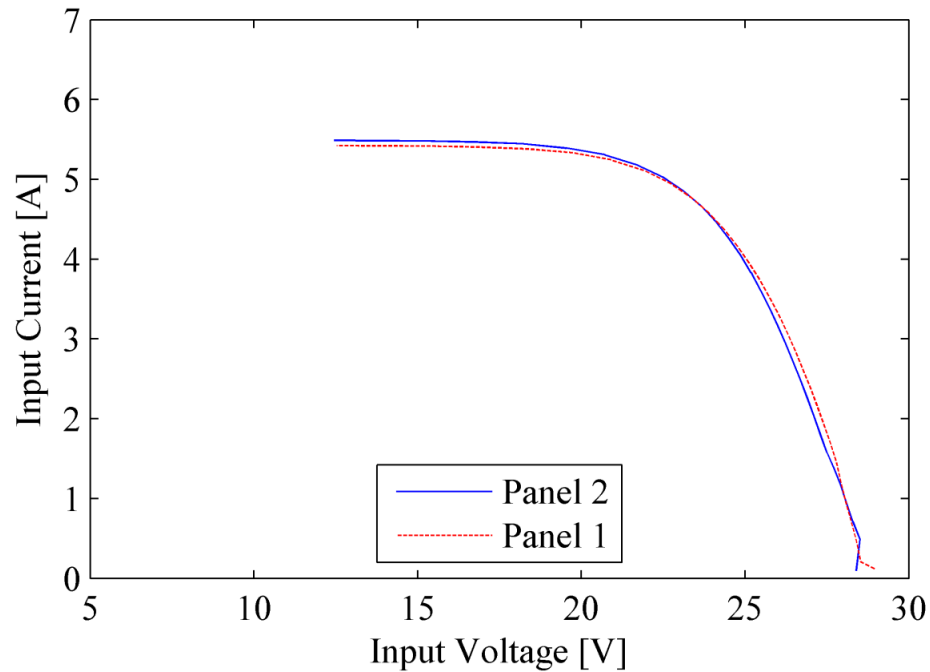
Figure 4.4. Input I-V Waveforms Unshaded

The values of the maximum power, the voltage at the maximum power point, and the current at the maximum power point can be seen in Table 4.1. Included are the insolation of the unshaded panel, the temperature of each panel, the current, voltage and power at the total maximum power point for each panel.
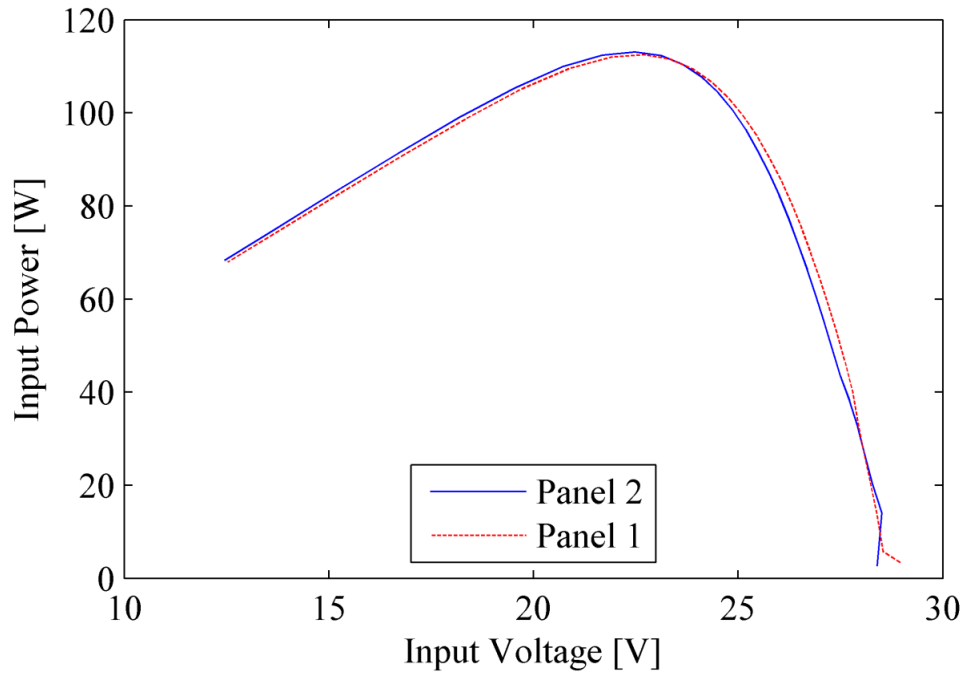
Figure 4.5. Input P-V Waveforms Unshaded

Table 4.1. Solar MPP Data for Unshaded Conditions

	Temp. (°C)	Insolation (W/m^2)	I_{mpp} (A)	V_{mpp} (V)	P_{mpp} (W)	I_{in} @ Total MPP	V_{in} @ Total MPP	P_{in} @ Total MPP
Panel 1	106	-	4.958	22.69	112.5	4.958	22.69	112.5
Panel 2	96	-	5.033	22.48	113.13	5.033	22.48	113.1
Total	-	760	1.063	195.8	208.2	-	-	-

The data shows that the two panels with their individual converters operate nearly the same. Also the data shows that the maximum power point of each individual panel is near the maximum power point of the entire system. This is expected from the results in Section 3.

Figure 4.6 shows the power vs. voltage relationship for the inputs of the two converters and the paralleled output of the converters for unshaded conditions. From the plots, the total maximum power point can easily be determined and occurs at the same instance as the maximum power points of each individual panel.
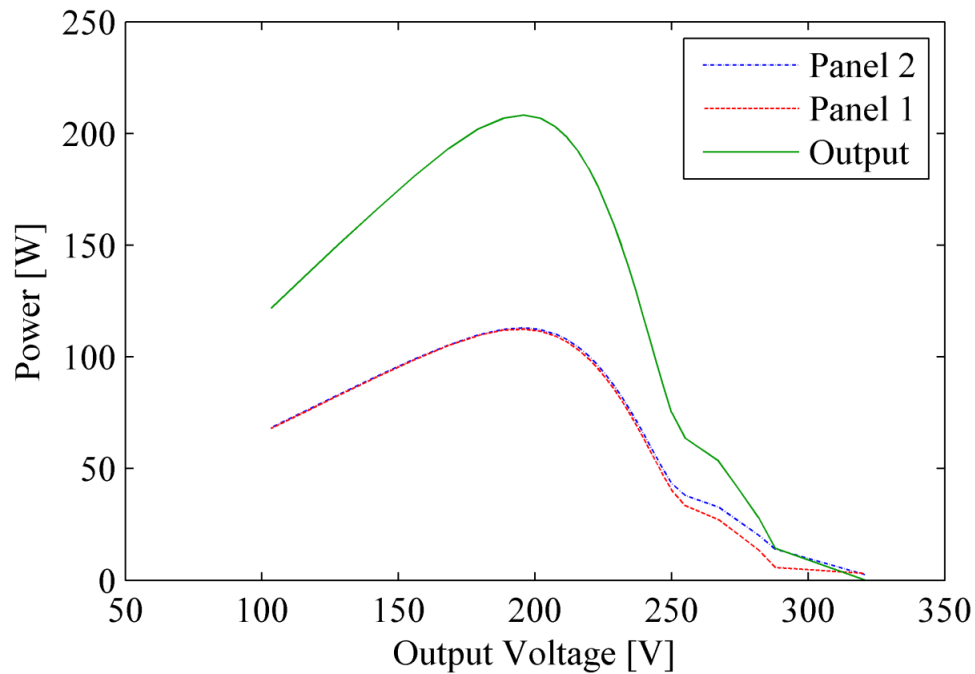
Figure 4.6. Total P-V Waveforms Unshaded

Figure 4.7 shows the power vs voltage relationship from Figure 4.6 with maximum power points added for each of the inputs and the paralleled output of the converters. The maximum power points all occur at the same output voltage on the curve, which is expected.
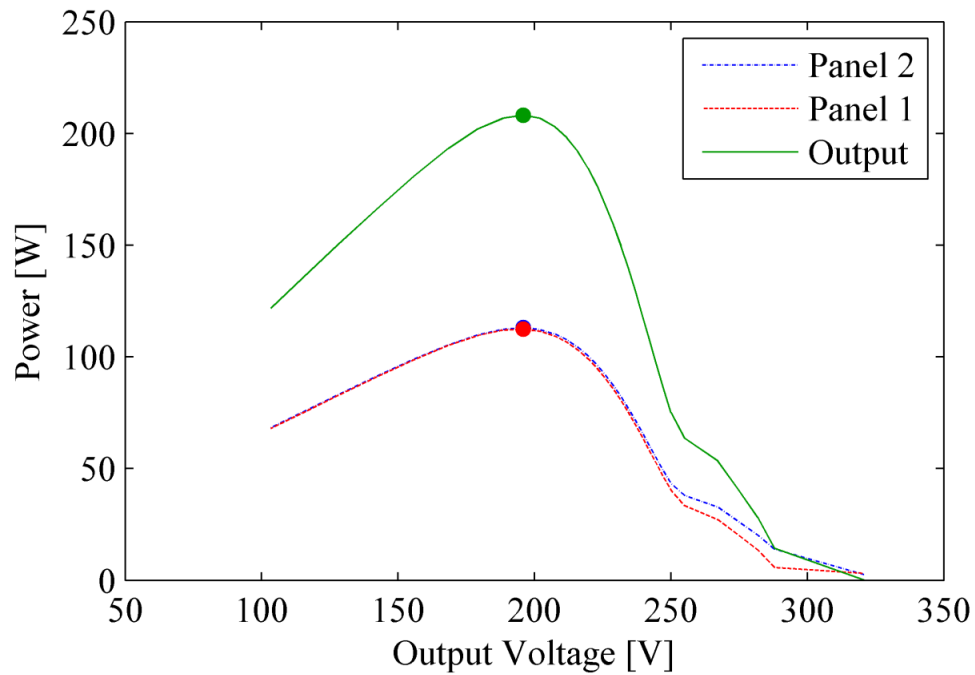
Figure 4.7. Total P-V Waveforms Unshaded with Maximum Power Points

Figure 4.8 shows the efficiency vs. the output current for the unshaded conditions. The peak efficiency was 92.41%. The average efficiency was 90.25% after the first measurement.

Figure 4.9 shows the input current vs. input voltage when one panel is partially occluded, resulting in approximately 50% insolation. Figure 4.10 shows the power vs. output voltage relationships for the inputs of the two converters and the paralleled output of the converters for partially shaded case.
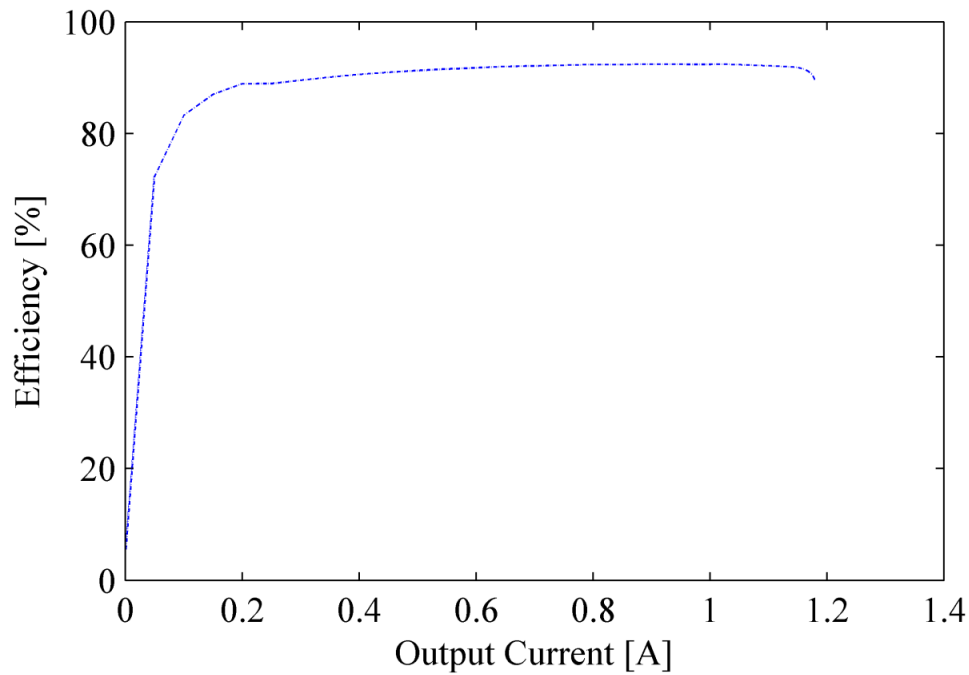
Figure 4.8. Total System Efficiency for Unshaded Conditions

As above in Table 4.1, the values of the maximum power, the voltage at the maximum power point, and the current at the maximum power point can be seen in Table 4.2. Included are the insolation of the unshaded panel, the temperature of each panel, the current, voltage and power at the total maximum power point for each panel.

Figure 4.11 shows the power vs voltage relationship from Figure 4.9 with maximum power points added for each of the inputs and the paralleled output of the converters. At the output voltage where the output power reaches its maximum, the unshaded panel is within 2.02% of its maximum power and the shaded panel is within 1.28% of its maximum power. This shows that the individual panel outputs are well within 5% of their individual maxima when the array power is maximized, despite differing insolation.
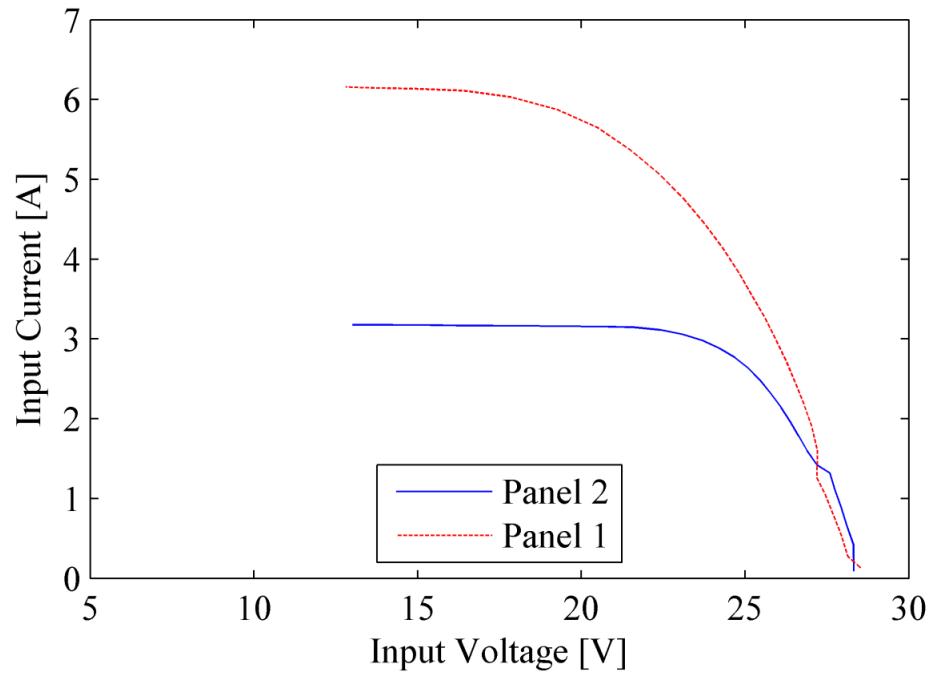
Figure 4.9. Input I-V Waveforms with Partial Shading

Table 4.2. Solar MPP Data for Partial Shaded Conditions

	Temp. (°C)	Insolation (W/m^2)	I$_{mpp}$ (A)	V$_{mpp}$ (V)	P$_{mpp}$ (W)	I$_{in}$ @ Total MPP	V$_{in}$ @ Total MPP	P$_{in}$ @ Total MPP
Panel 1	115	-	5.656	20.47	115.8	5.070	22.38	113.5
Panel 2	87	-	2.980	23.71	70.66	3.115	22.39	69.76
Total	-	830	0.8652	195.3	169.0	-	-	-

Figure 4.12 shows the efficiency vs. the output current for the partially shaded conditions. The peak efficiency was 92.25%. The average efficiency was 89.96% after the first measurment.
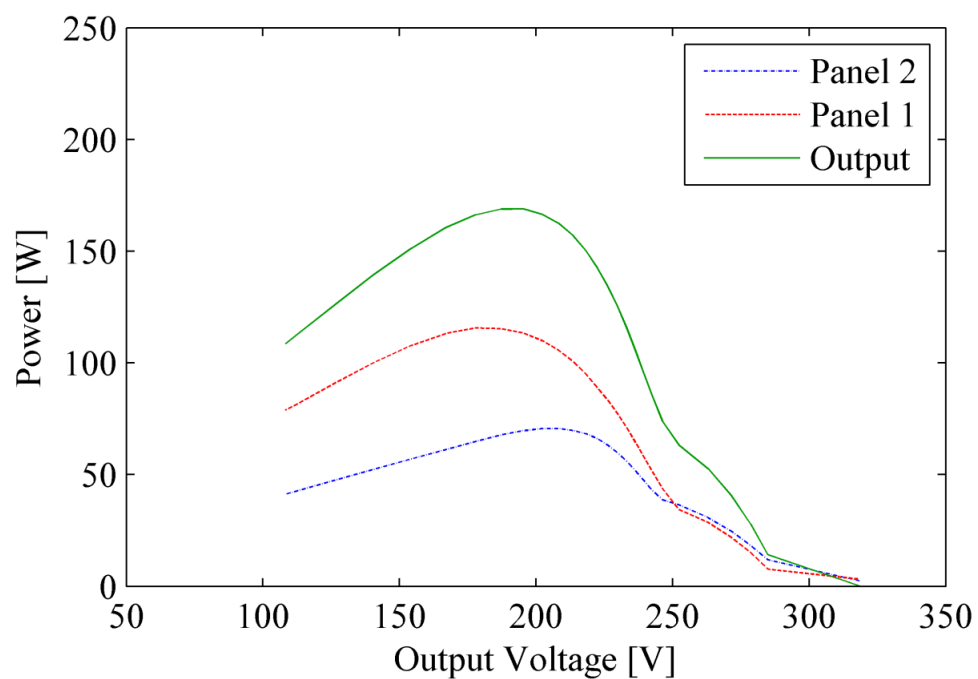
Figure
4.10. Total P-V Waveforms with Partial Shading

Figure 4.13 shows the input current vs. input voltage when one panel is fully shaded, resulting in approximately 30% insolation. Figure 4.14 shows the power vs. output voltage relationships for the inputs of the two converters and the paralleled output of the converters for fully shaded case.

At the output voltage where the output power reaches its maximum, the unshaded panel is within 0.5% of its maximum power and the shaded panel is within 11.2% of its maximum power.

As the insolation is decreased past 50%, the shaded panel drops out of the 5% range desired. The difference in power from the maximum power point at full shaded conditions is 11.19%, which is over double the objective. At insolation levels where the

shaded panel is out of the 5% range, the characteristics of the unshaded panel dominate

the total system power characteristics.
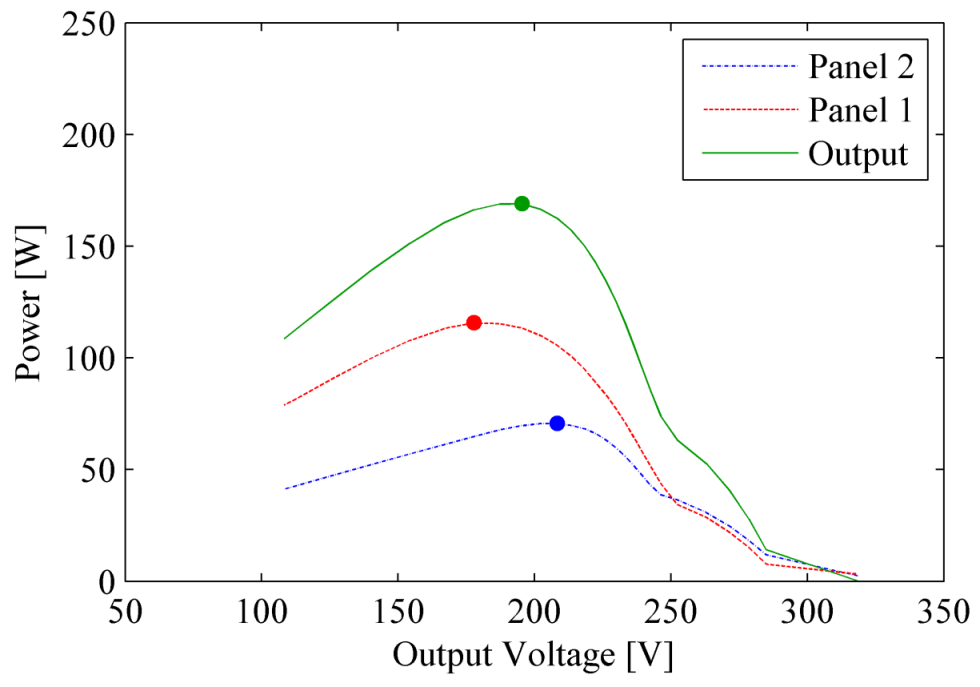
Figure 4.11. Total P-V Waveforms Partial Shading with Maximum Power Points

The difference in power from the maximum power point is less than 2.05% for the

unshaded panel for all shading conditions on the other panel.

Figure 4.15 shows the power vs voltage relationship from Figure 4.13 with

maximum power points added for each of the inputs and the paralleled output of the

converters.
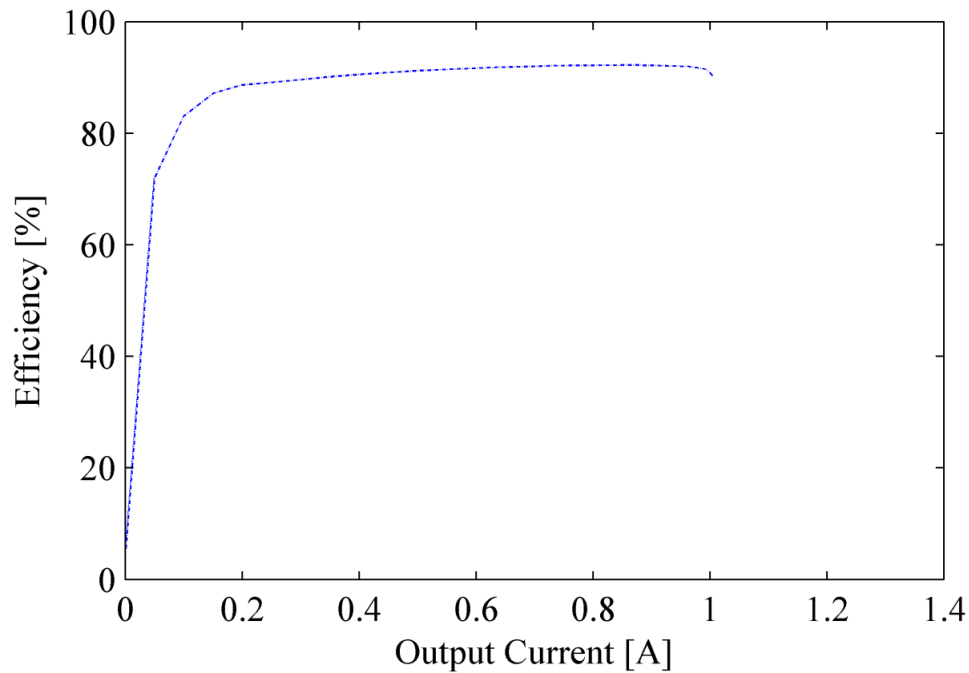
Figure 4.12. Total System Efficiency with Partial Shading

As above in Table 4.1, the values of the maximum power, the voltage at the maximum power point, and the current at the maximum power point can be seen in Table 4.3. Included are the insolation of the unshaded panel, the temperature of each panel, the current, voltage and power at the total maximum power point for each panel.

Figure 4.16 shows the efficiency vs. the output current for the partially shaded conditions. The peak efficiency was 92.44%. The average efficiency was 89.92% after the first measurement.
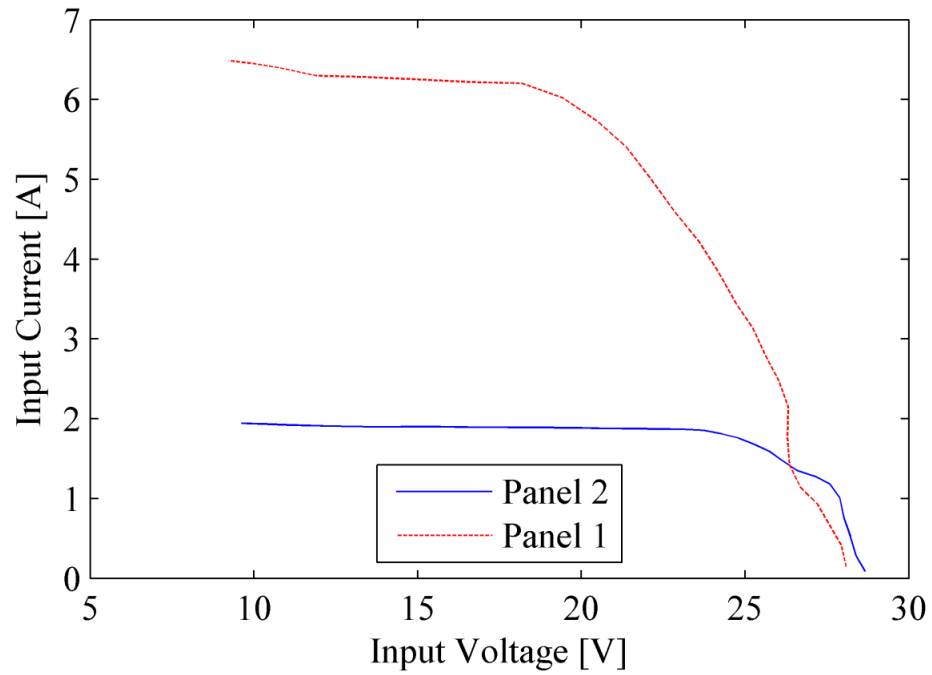
Figure 4.13. Input I-V Waveforms with Full Shading
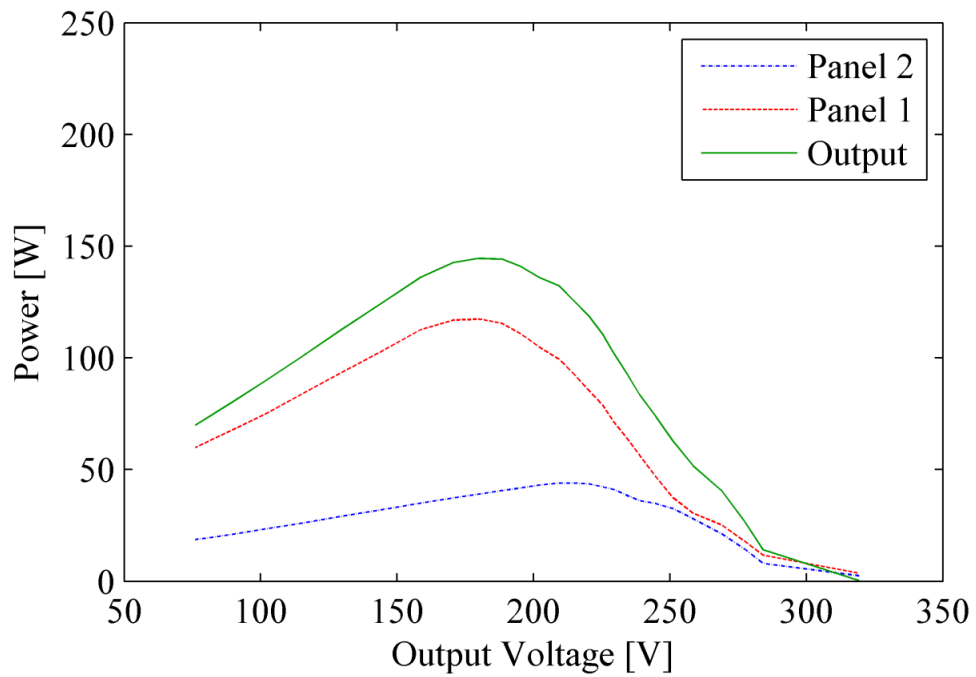
Figure 4.14. Total P-V Waveform with Full Shading

Table 4.3. Solar MPP Data for Full Shaded Conditions

	Temp. (°C)	Insolation (W/m^2)	I_{mpp} (A)	V_{mpp} (V)	P_{mpp} (W)	I_{in} @ Total MPP	V_{in} @ Total MPP	P_{in} @ Total MPP
Panel 1	100	-	6.082	19.83	120.6	5.790	20.78	120.3
Panel 2	74	-	1.831	24.48	44.83	1.889	21.07	39.81
Total	-	880	0.8079	182.9	147.8	-	-	-
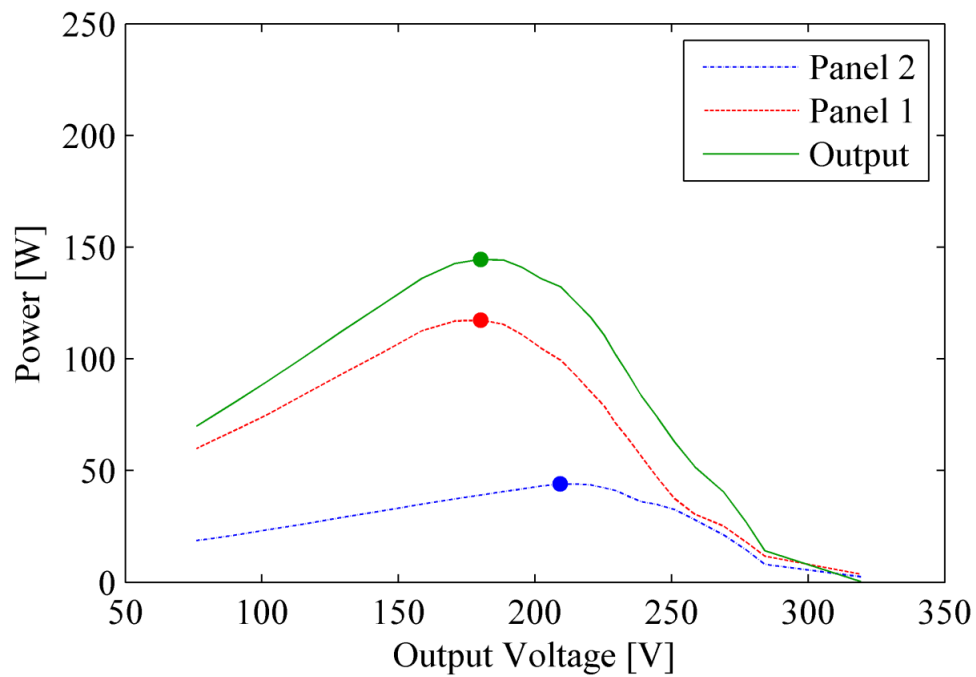
Figure 4.15. Total P-V Waveform with Full Shading with Maximum Power Points
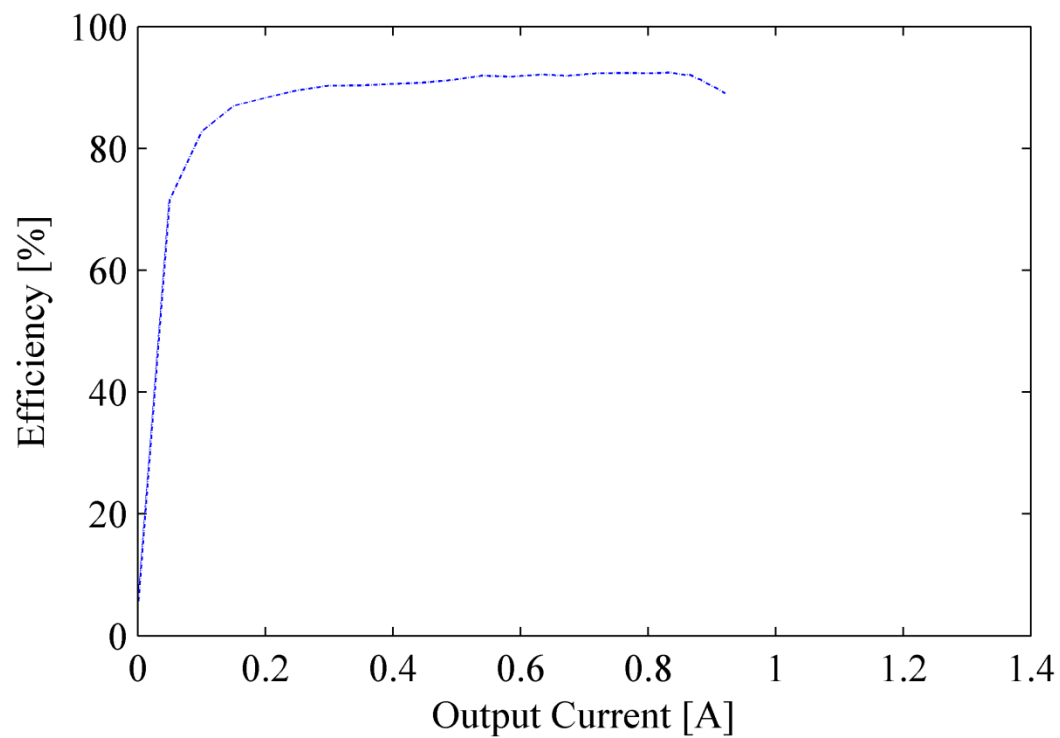
Figure 4.16. Total System Efficiency with Full Shading

The data tables for all of the different insolation trials and the figures for all of the different insolation trials are located in Appendix D.

5. CONCLUSIONS AND FUTURE WORK

A new approach to PV arrays was investigated. Each panel has an integrated module-level power converter with a fixed voltage gain. The output of the converters may be directly connected to a grid-tie inverter. This will allow individual panels to operate much closer to their respective maximum power points than panels in a conventional series-connected array.

The design of an auxilary circuit to supply gate drivers with gate signals and power is presented. The design and implementation of a Labview interface for automating the experimental process of setting the electronic load and taking measurements was discussed. The use of supplementary devices such as the pyranometer and thermocouples was discussed.

The design of a full-bridge, buck-derived, isolated converter is presented. The design and construction of a transformer for use with the full-bridge converter is covered, as well as the novel topology utilized to increase converter efficiency. The simulation results show that a high efficiency converter is possible if skin and proximity effects are limited and transformer construction is improved.

Analysis of both field data and random insolation indicate that the new approach does increase power generation and therefore system efficiency. Solar testing shows that the topology does improve system performance overall independent of insolation levels on one of the panels. With a higher efficiency converter, the individual maxima will more closely coincide with the total maximum power point of the system. Even with less efficienct converters, the unshaded panel's characteristics govern the total system's characteristics, rather than the shaded panel limiting outputs.

Future work should include the introduction of two new gate signals to control Q3 and Q4 as seen in Section 3.1. These new gate signals would have a phase shift from the gate signals on Q1 and Q2. This would allow the voltage on the MOSFETs to reach zero and achieve zero-voltage switching, possibly increasing efficiency. Further experimental testing could then be done to measure the increase in efficiency. If bench testing proves successful, the next step would be to do solar testing and measure the efficiency increase on both converters. Also, checking the difference in power from the maximum for both converters at maximum output power to ensure that the converters are operating at their individual maxima independent of insolation levels. Finally, the system should be scaled to a large PV array and connected to a grid-tie inverter.

APPENDIX A.

PRINTED CIRCUIT BOARD DESIGN

This appendix includes the schematics and board layouts of the printed circuit boards described in Section 2.1 and Section 3.1. The schematic diagram is broken into multiple sections and shown in Figures A.1 through A.4 for clarity.
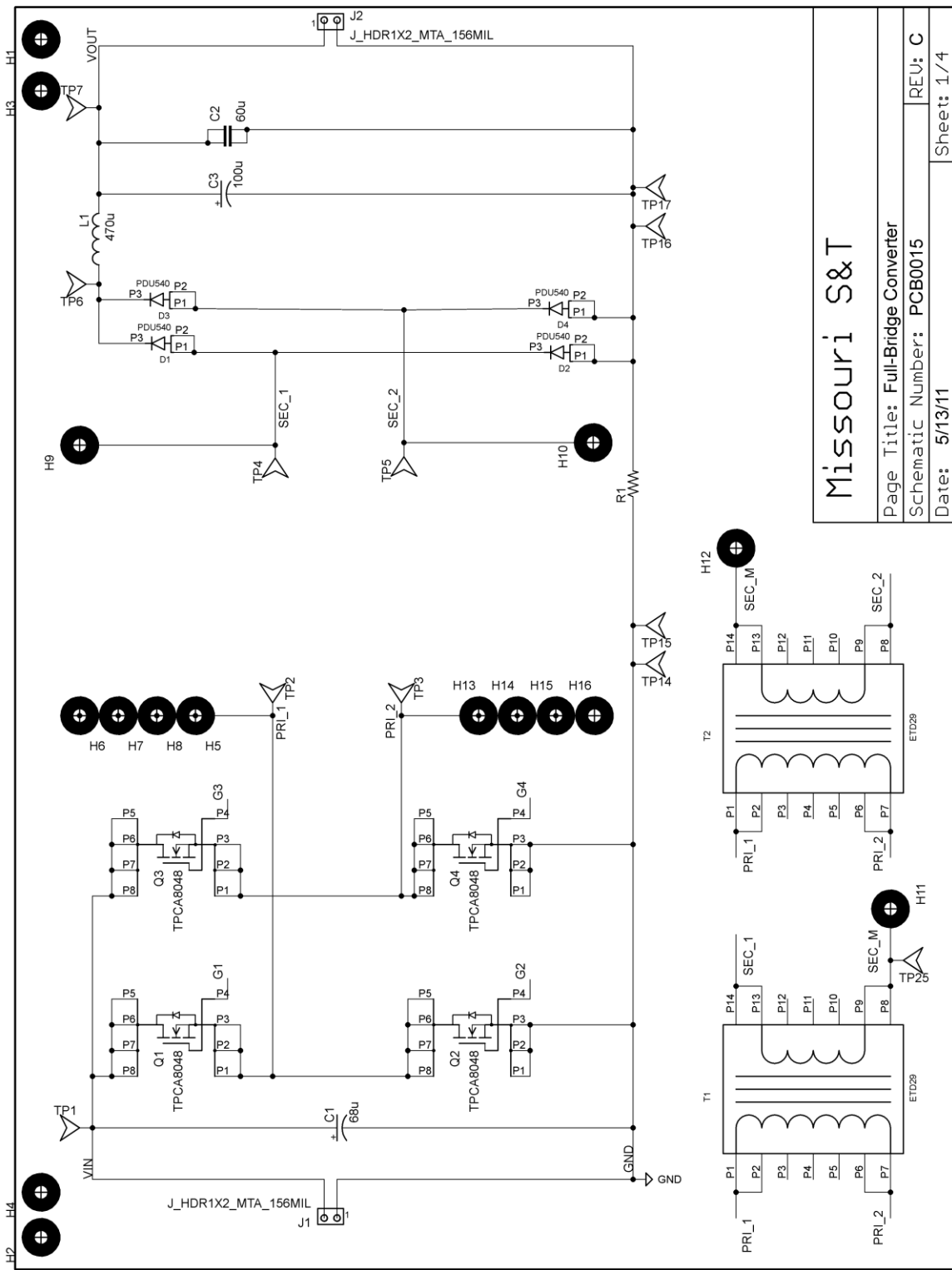
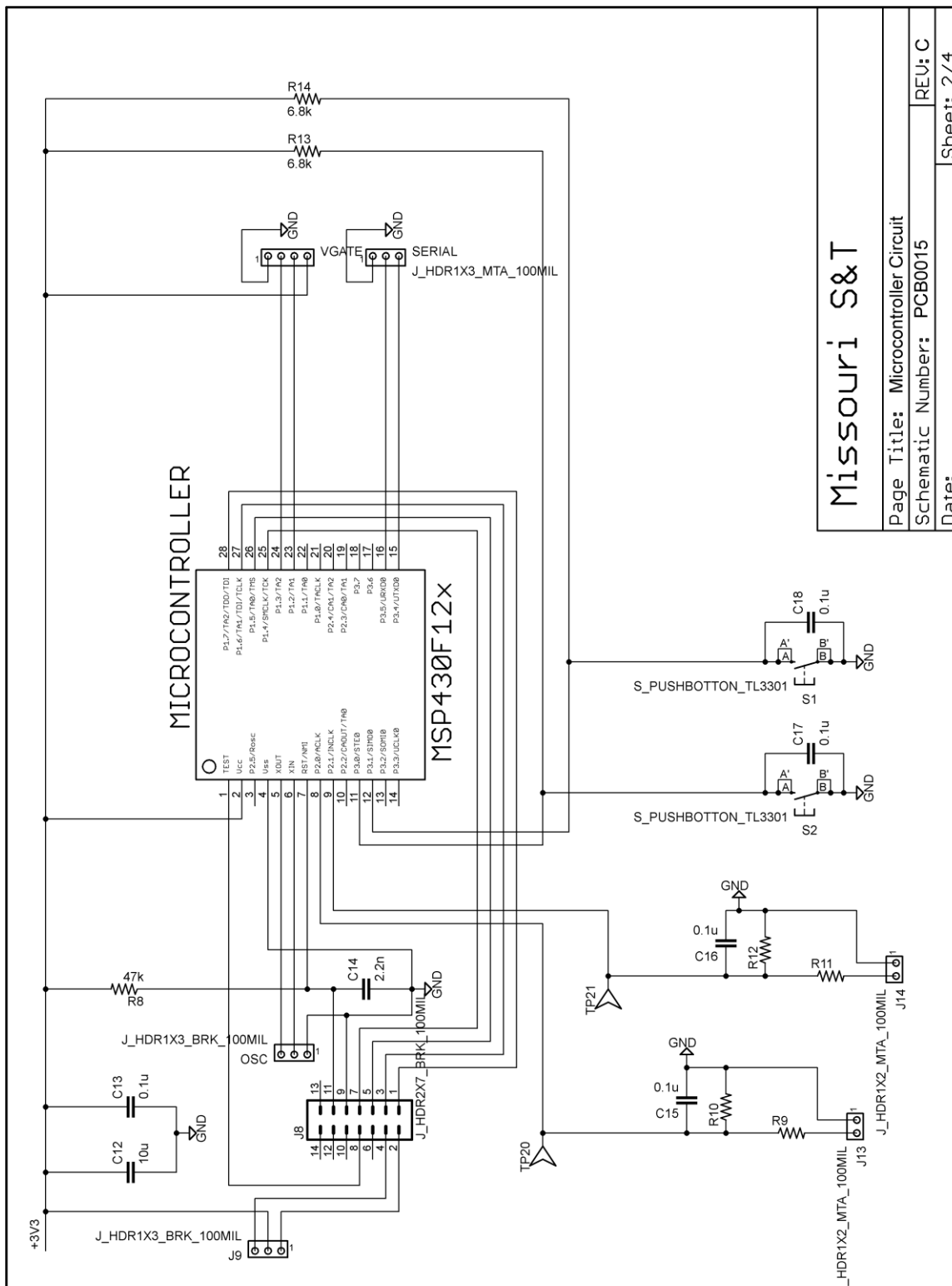Figure A.1. Sheet 1 of Printed Circuit Board Schematic

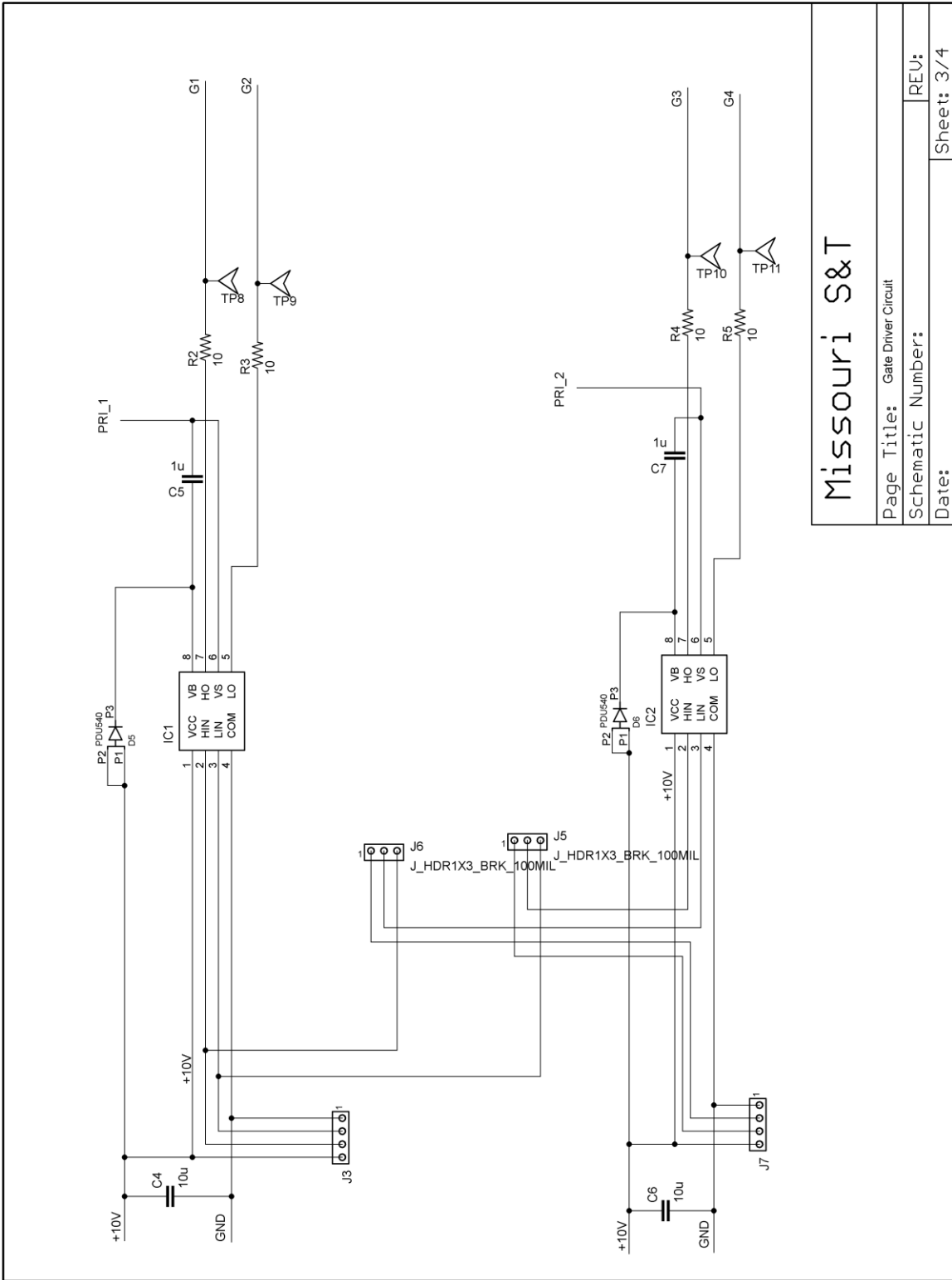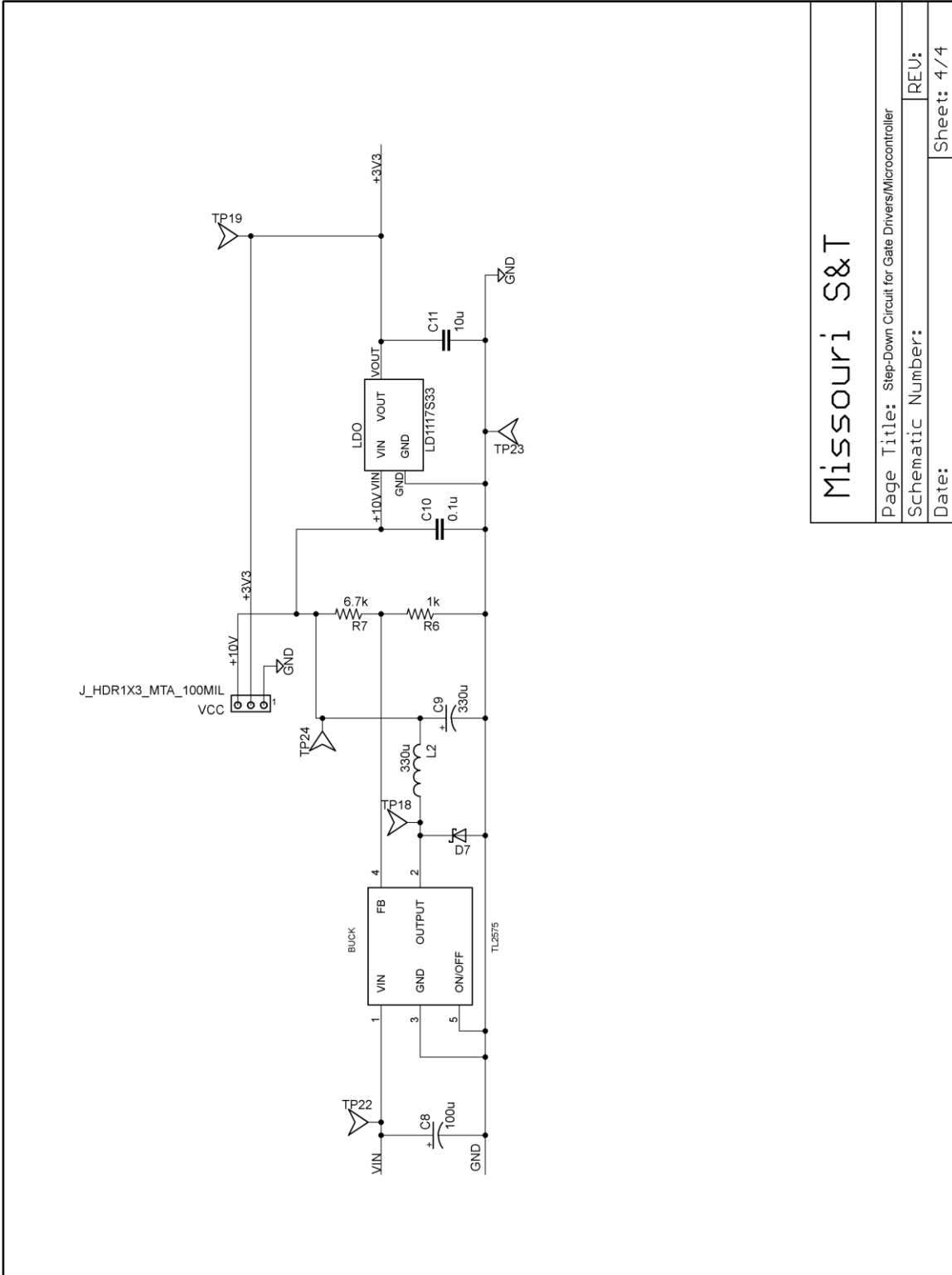Figure A.2. Sheet 2 of Printed Circuit Board Schematic

Figure A.3. Sheet 3 of Printed Circuit Board Schematic

Figure A.4. Sheet 4 of Printed Circuit Board Schematic
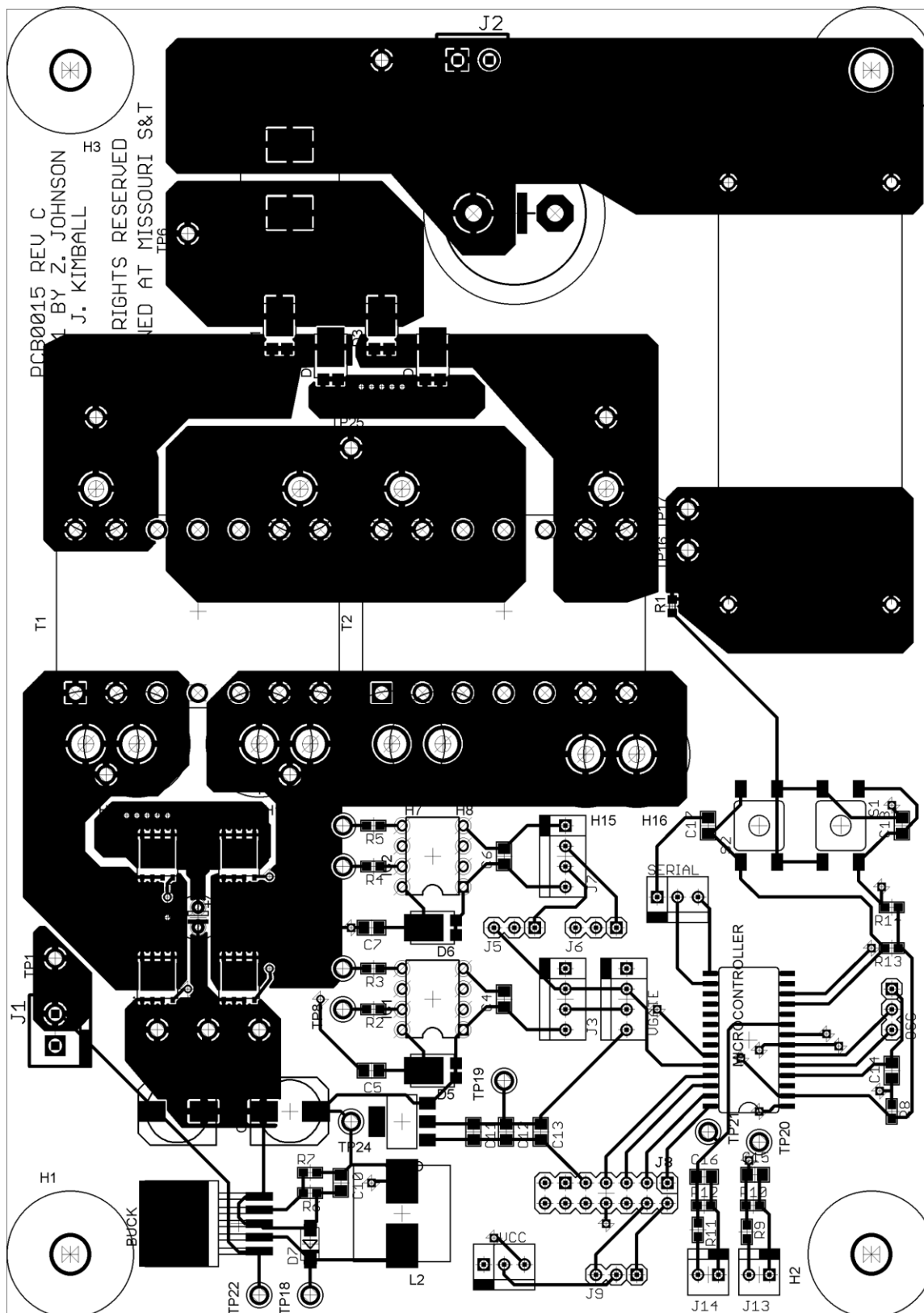
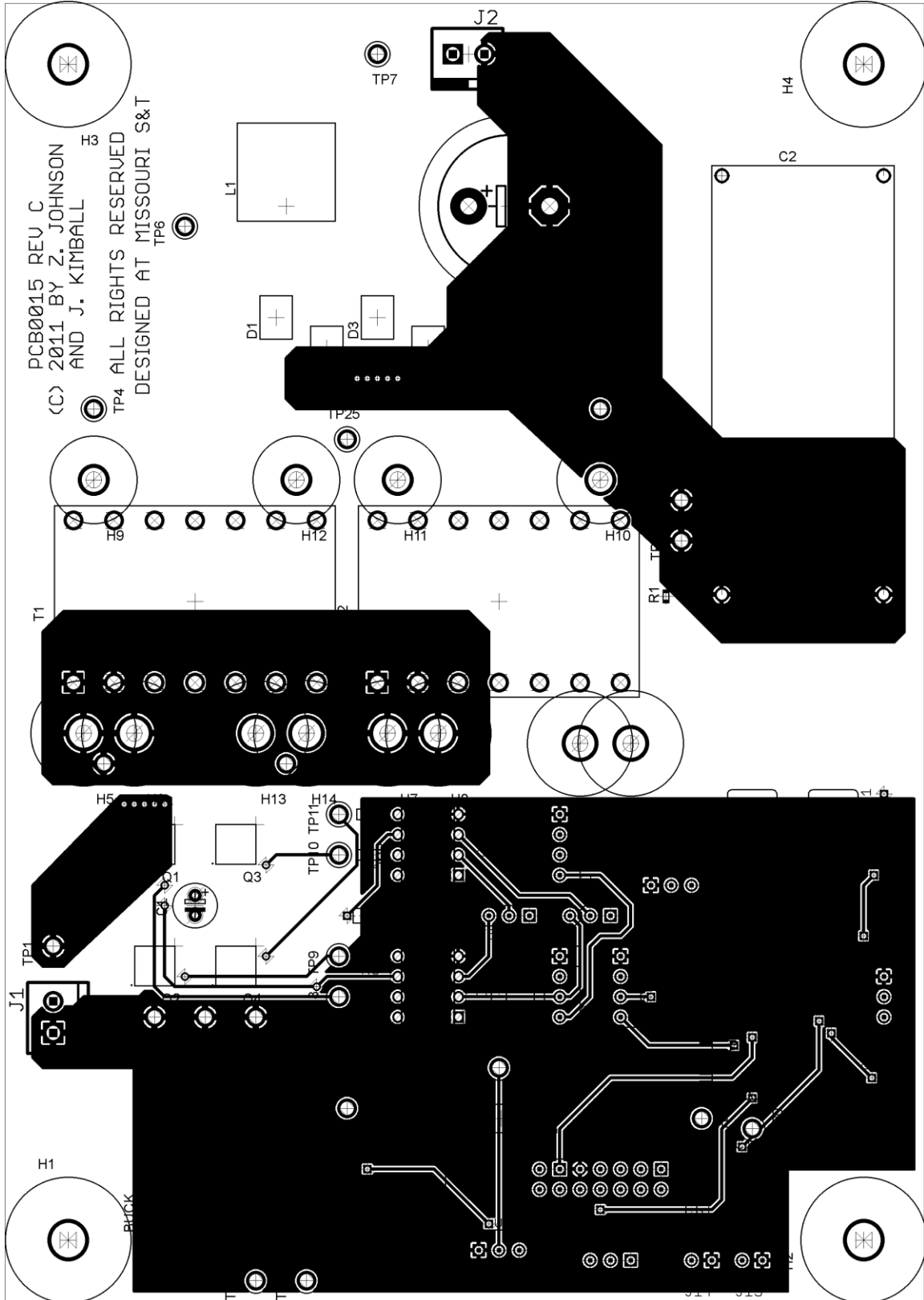Figure A.5. Physical Board Layout of Top Layer

Figure A.6. Physical Board Layout of Bottom Layer

APPENDIX B.

MICROCONTROLLER CODE FOR PWM GATE SIGNALS

```
WDTCTL = WDTPW + WDTHOLD;           // Stop WDT
DCOCTL |= 0xE0;                                         // Set DCO = 7
BCSCTL1 |= 0x07;                                        // Set RSEL = 7
P1DIR |= 0x0C;                  // P1.2 and P1.3 output
P1SEL |= 0x0C;                  // P1.2 and P1.3 TA1/2 otions
CCR0 = 26;                        // PWM Period/2
CCTL1 = OUTMOD_6;                    // CCR1 toggle/set
CCR1 = 15;                       // CCR1 PWM duty cycle
CCTL2 = OUTMOD_2;                    // CCR2 toggle/reset
CCR2 = 11;                       // CCR2 PWM duty cycle
TACTL = TASSEL_2 + MC_3;             // SMCLK, up-down mode
_BIS_SR(LPM0_bits);               // Enter LPM0
```

APPENDIX C.

LABVIEW PROGRAM

This appendix includes the front panel view and the block diagram of the Labview program described in Section 2.2. The block diagram is broken into multiple sections and shown in Figures C.2 through C.4 for clarity.
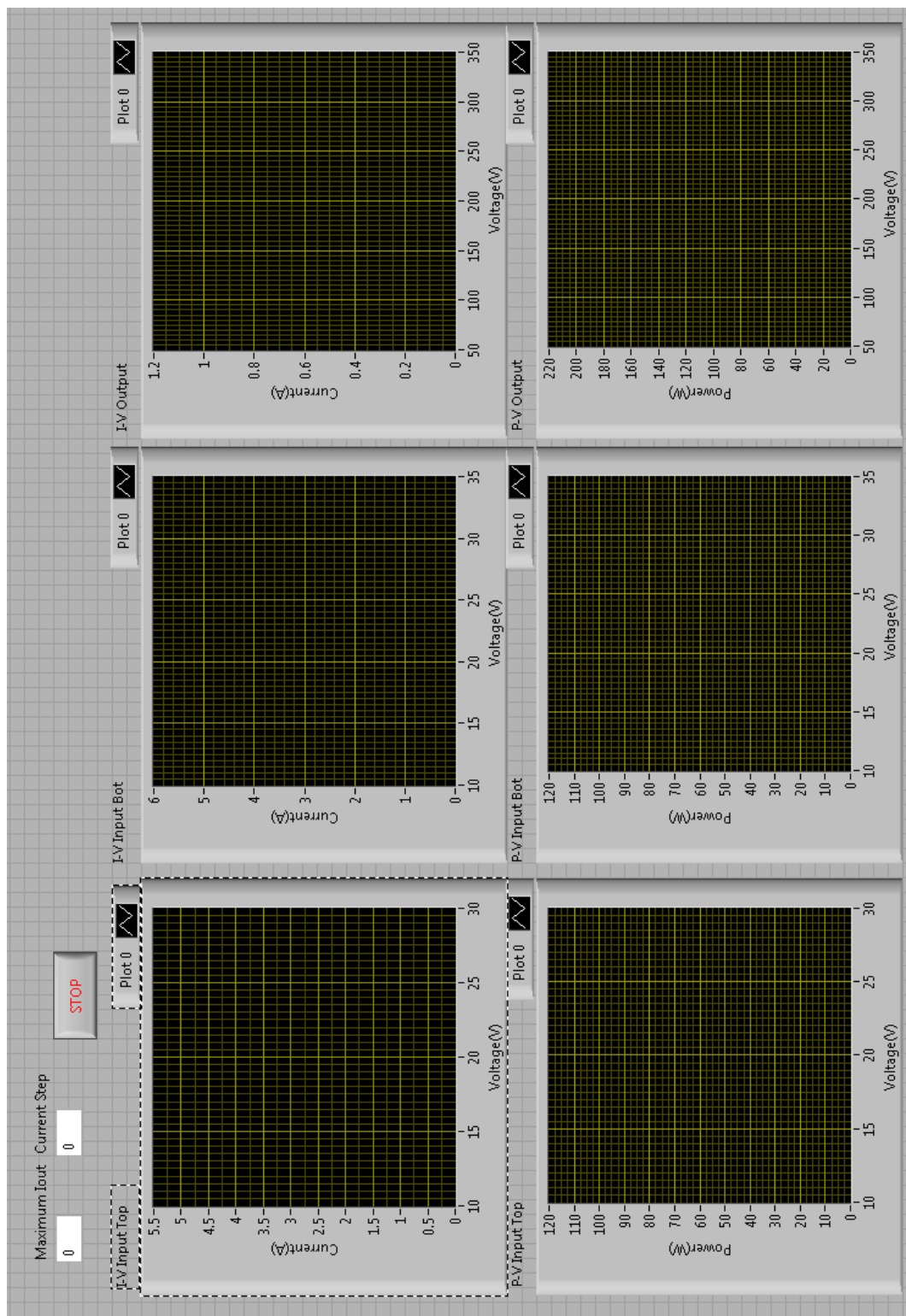
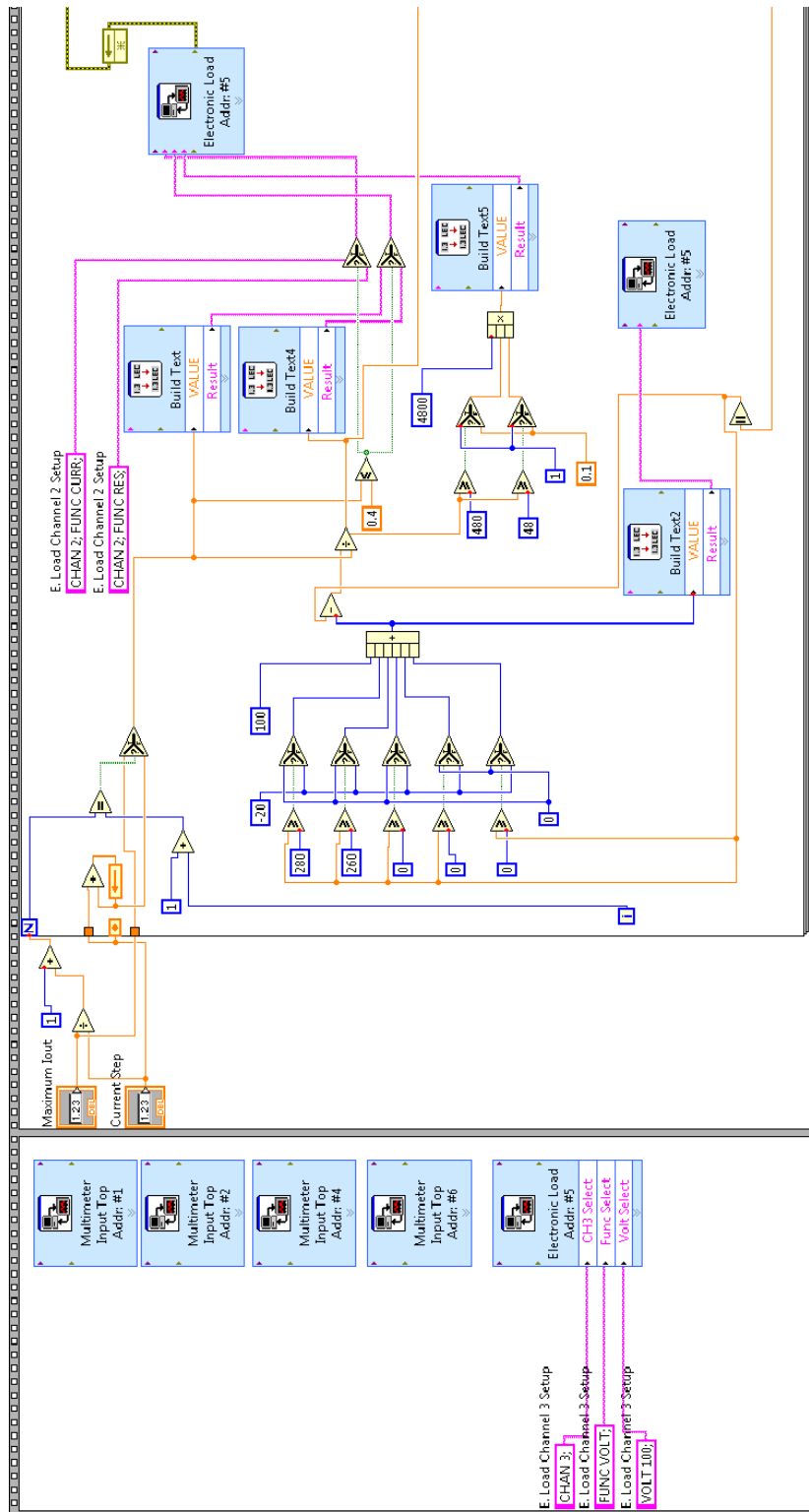Figure C.5.1. Labview Human-Machine Interface
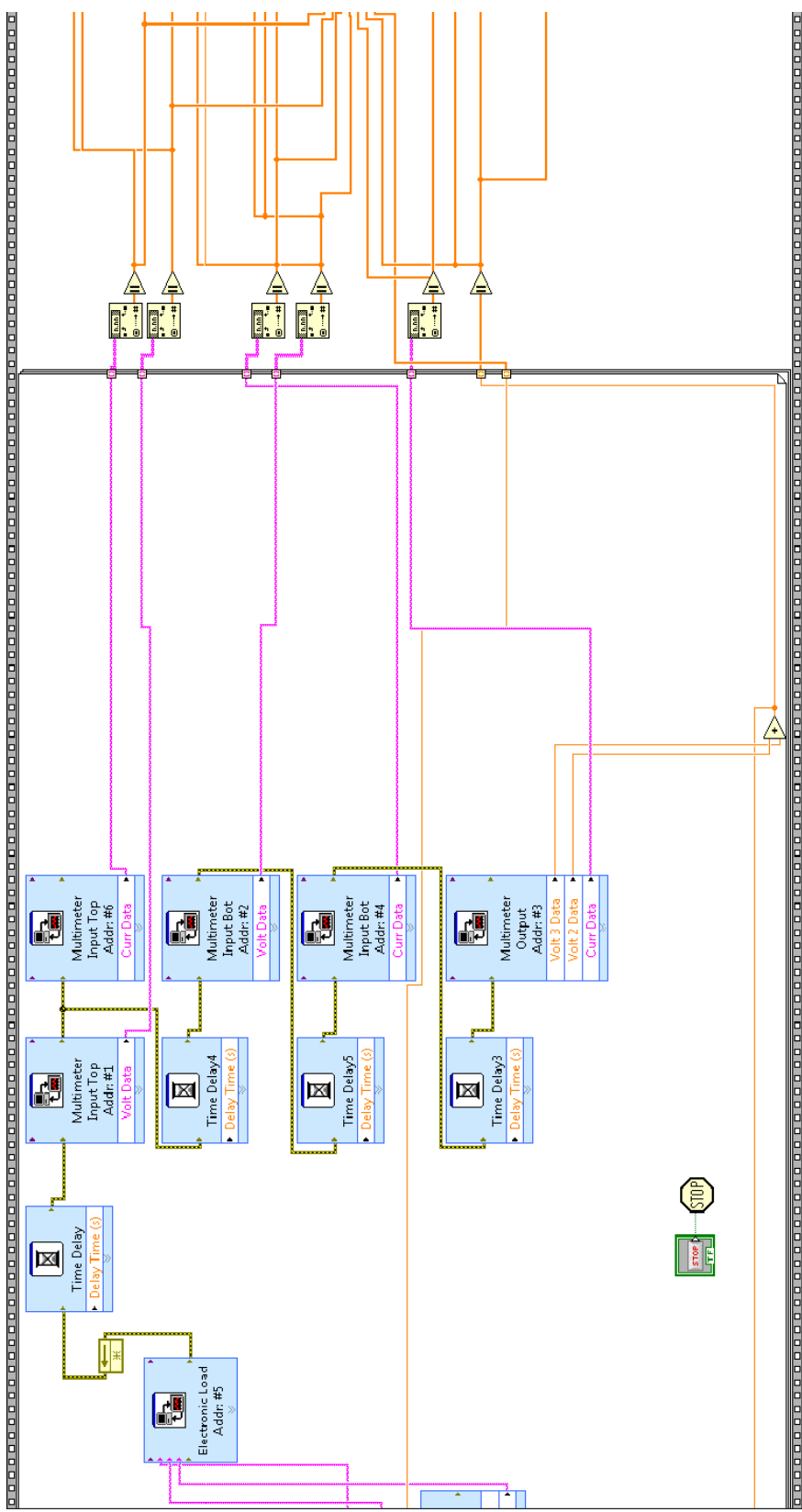
Figure C.2. Labview Block Diagram
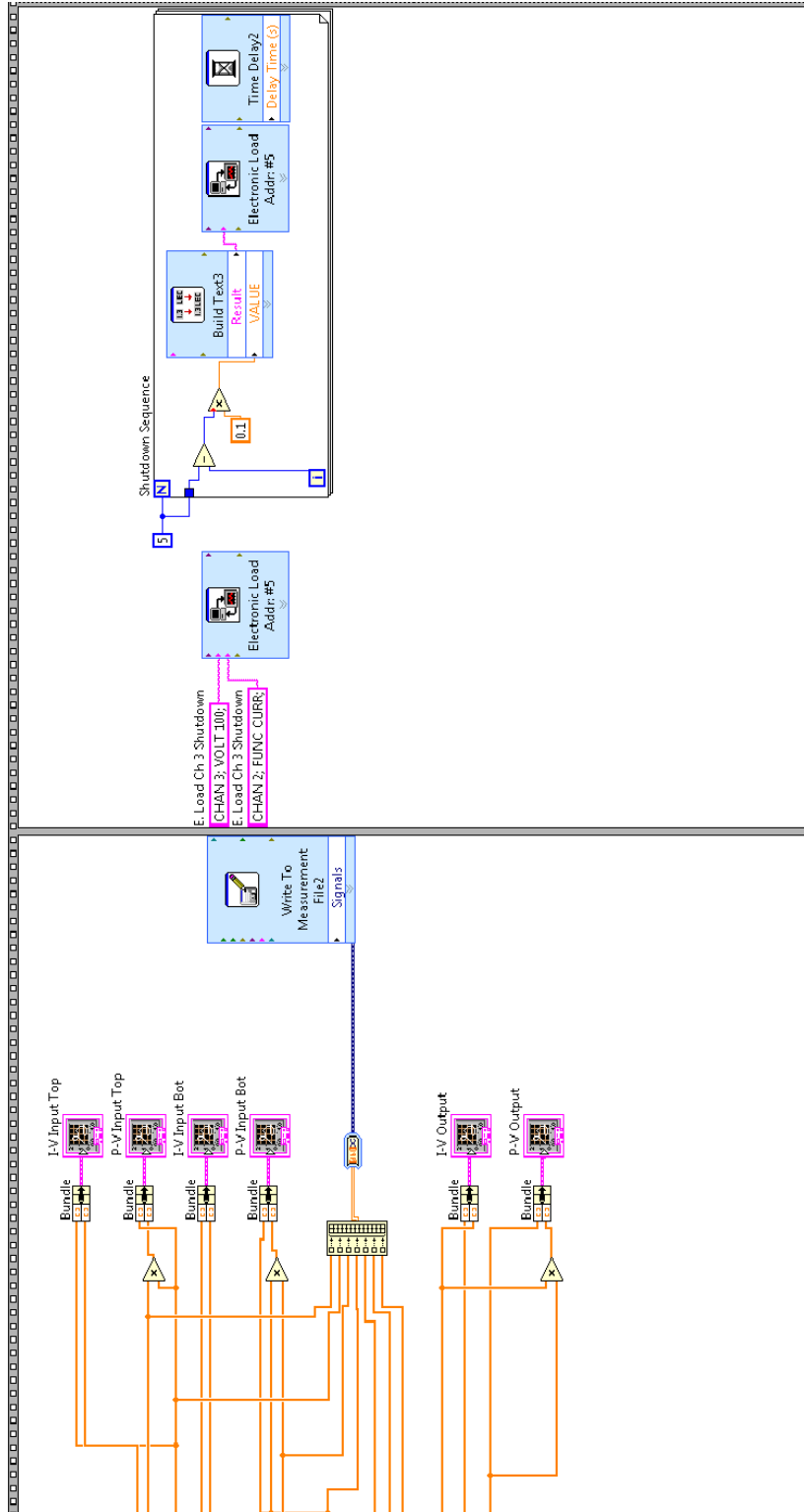
Figure C.3. Labview Block Diagram Continued

Figure C.4. Labview Block Diagram Continued

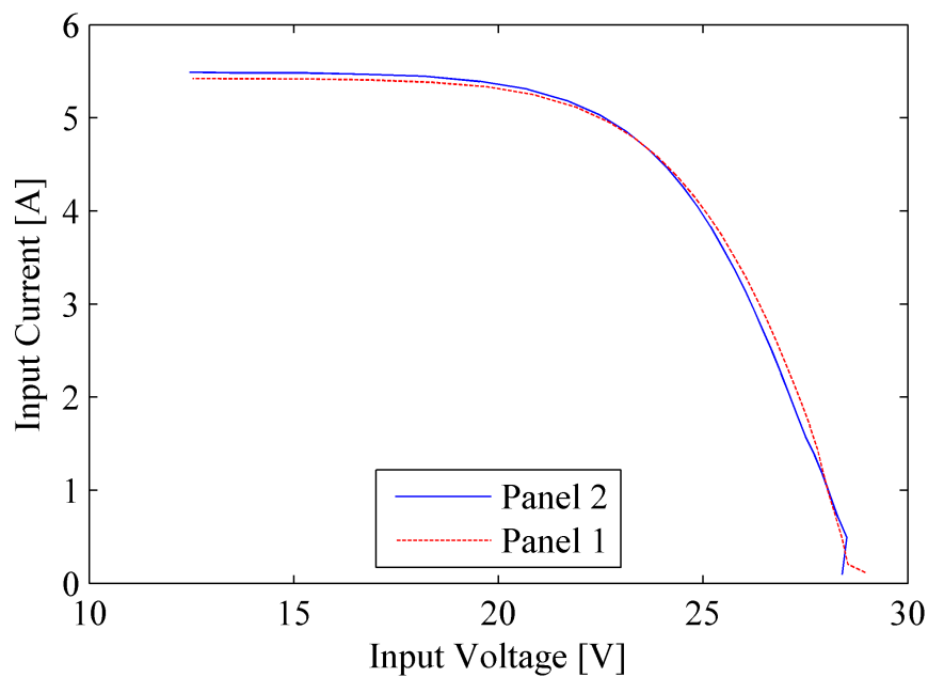APPENDIX D.

SOLAR DATA TABLES AND FIGURES

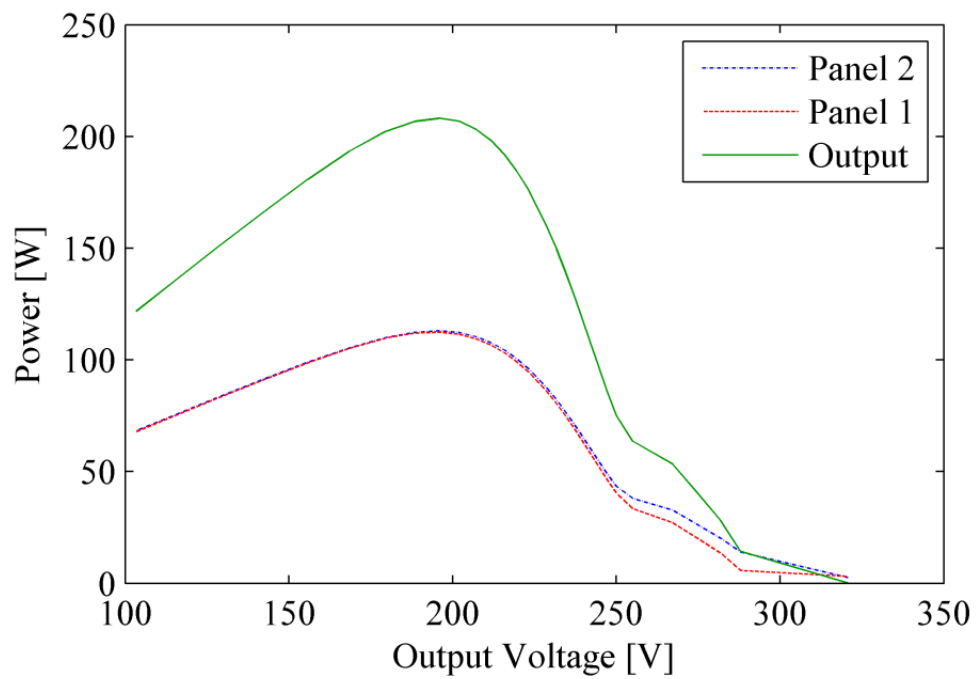Figure D.1. Input I-V Waveforms for 0 Sheets/Unshaded

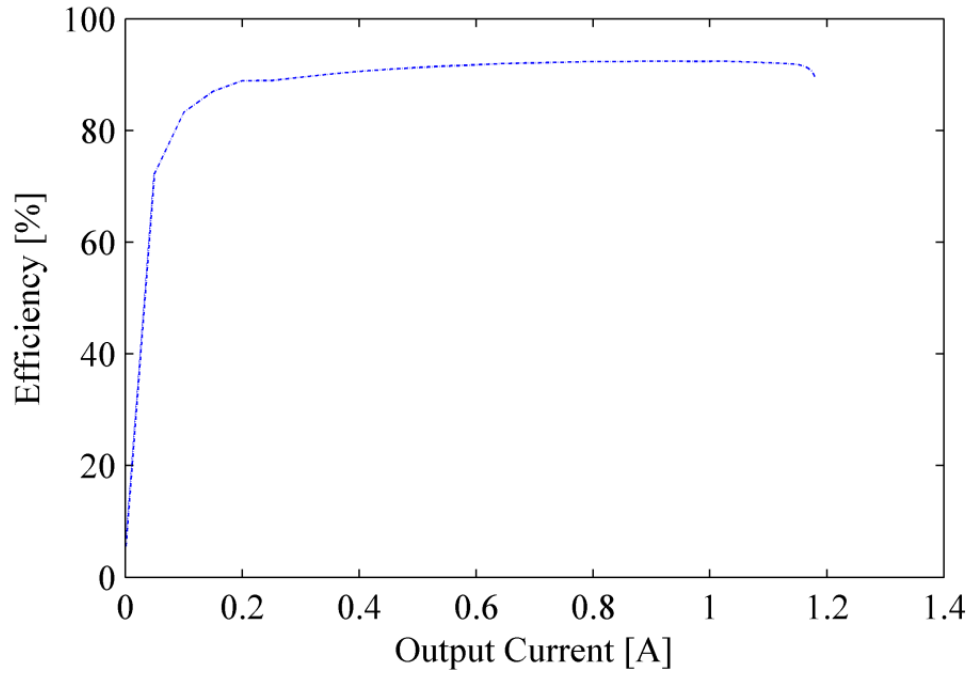Figure D.2. Total P-V Waveforms for 0 Sheets/Unshaded

Figure D.3. Efficiency Waveforms for 0 Sheets/Unshaded

Table D.1. Solar MPP Data for 0Sheets/Unshaded

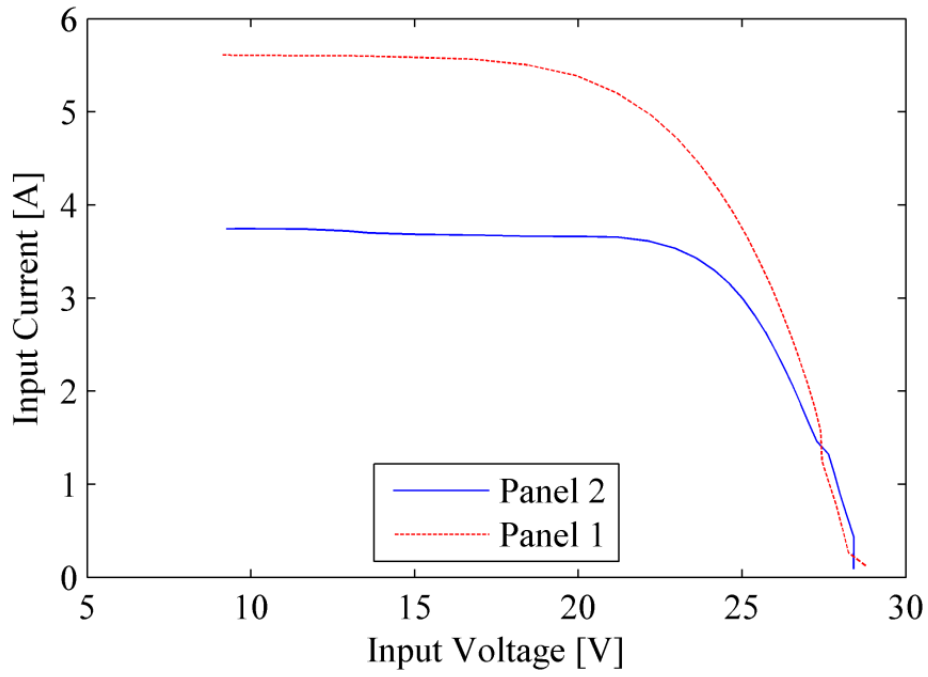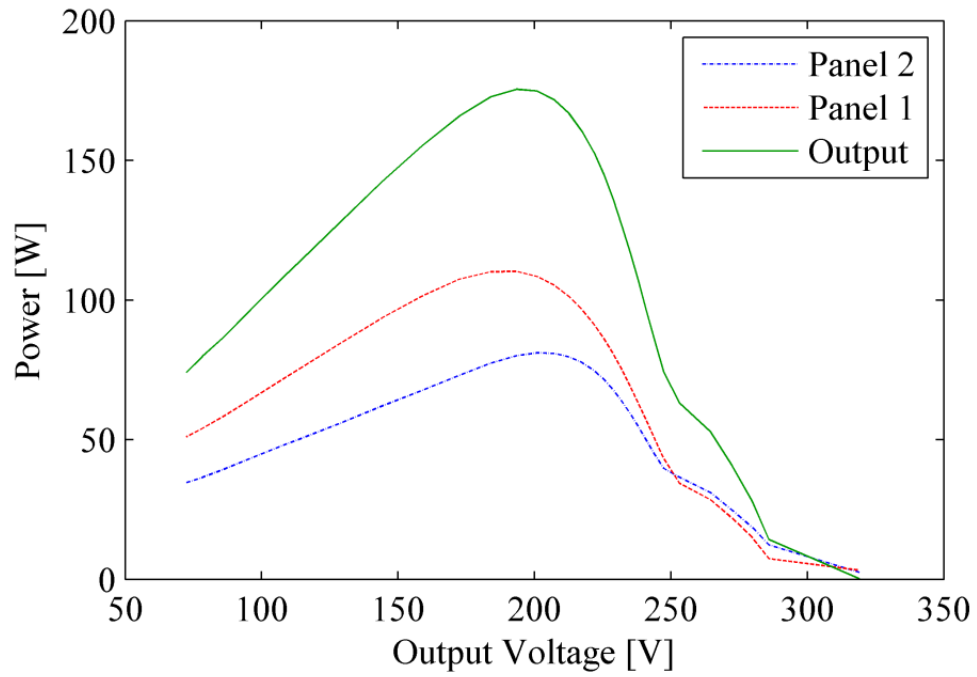|	Temp. (°C)	Insolation (W/m^2)	I$_{mpp}$ (A)	V$_{mpp}$ (V)	P$_{mpp}$ (W)	I$_{in}$ @ Total MPP	V$_{in}$ @ Total MPP	P$_{in}$ @ Total MPP
Panel 1	41.11	-	4.958	22.69	112.5	4.958	22.69	112.5
Panel 2	35.56	-	5.032	22.48	113.1	5.033	22.48	113.1
Total	-	760	1.063	195.8	208.2	-	-	-

Figure D.4. Input I-V Waveforms with 2 Sheets

Figure D.5. Total P-V Waveforms with 2 Sheets
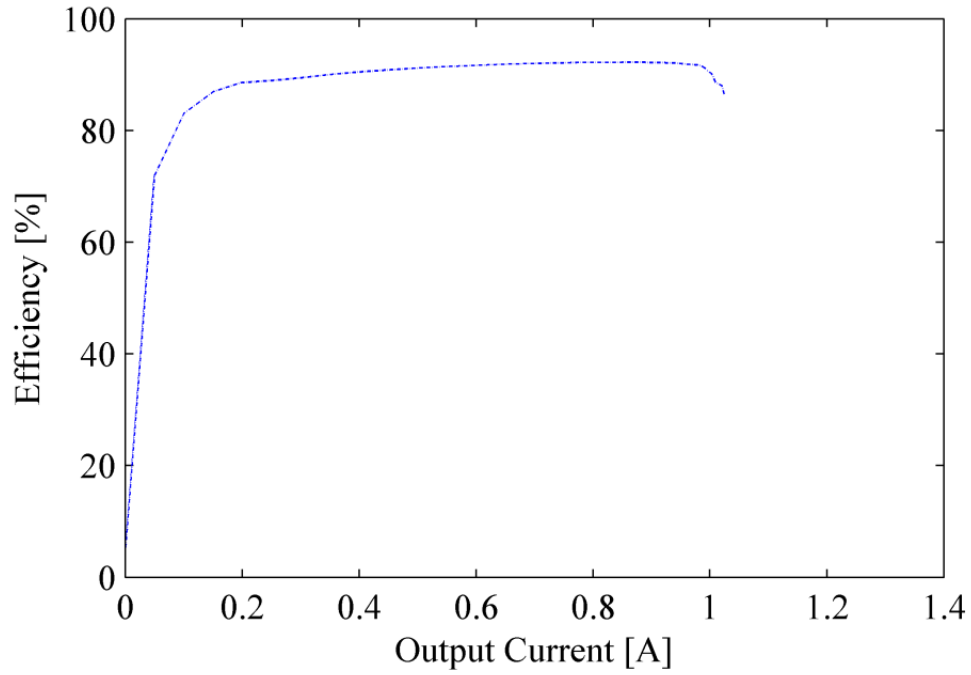
Figure D.6. Efficiency Waveform with 2 Sheets

Table D.2. Solar MPP Data for 2 Sheets

	Temp. (°C)	Insolation (W/m^2)	I_{mpp} (A)	V_{mpp} (V)	P_{mpp} (W)	I_{in} @ Total MPP	V_{in} @ Total MPP	P_{in} @ Total MPP
Panel 1	41.11	-	4.968	22.21	110.4	4.968	22.21	110.4
Panel 2	35.56	-	3.535	22.96	81.17	3.613	22.18	80.12
Total	-	770	0.908	193.3	175.5	-	-	-

Figure D.7. Input I-V Waveforms with 4 Sheets
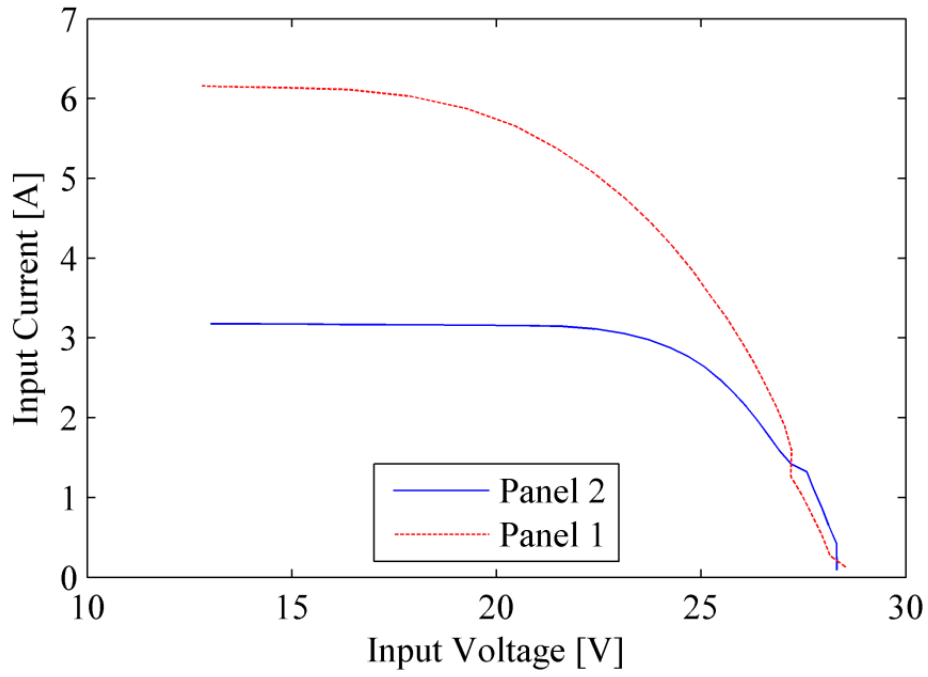

Figure D.8. Total P-V Waveforms with 4 Sheets

Figure D.9. Efficiency Waveform for 4 Sheets

Table D.3. Solar MPP Data for 4 Sheets

	Temp. (°C)	Insolation (W/m^2)	I_{mpp} (A)	V_{mpp} (V)	P_{mpp} (W)	I_{in} @ Total MPP	V_{in} @ Total MPP	P_{in} @ Total MPP
Panel 1	46.11	-	5.656	20.47	115.8	5.070	22.38	113.5
Panel 2	30.56	-	2.980	23.71	70.66	3.115	22.39	69.76
Total	-	830	0.865	195.3	169.0	-	-	-

Figure D.10. Input I-V Waveforms for 6 Sheets
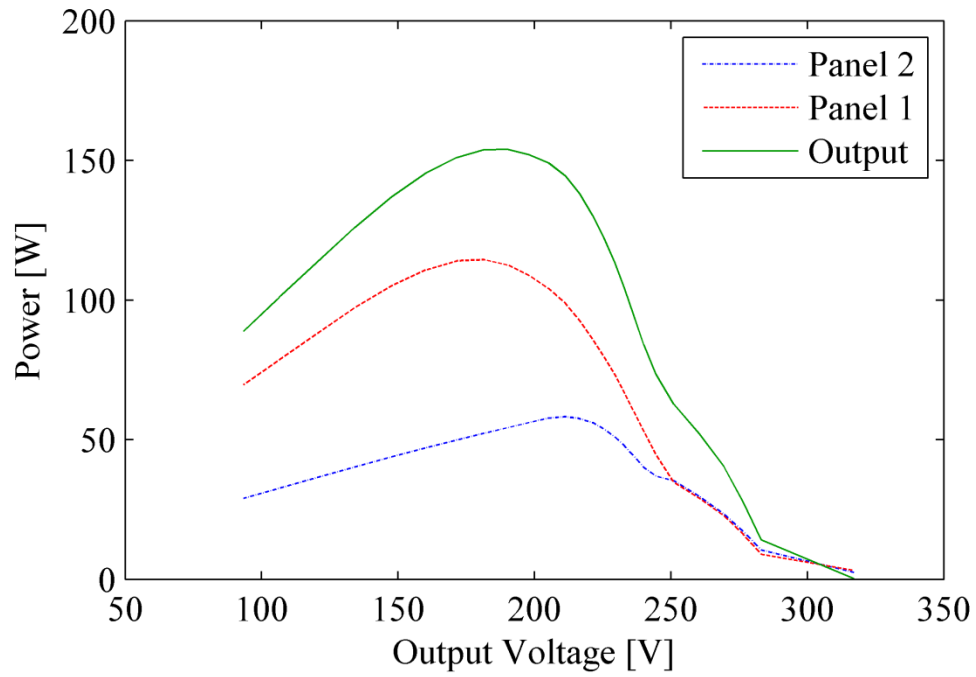
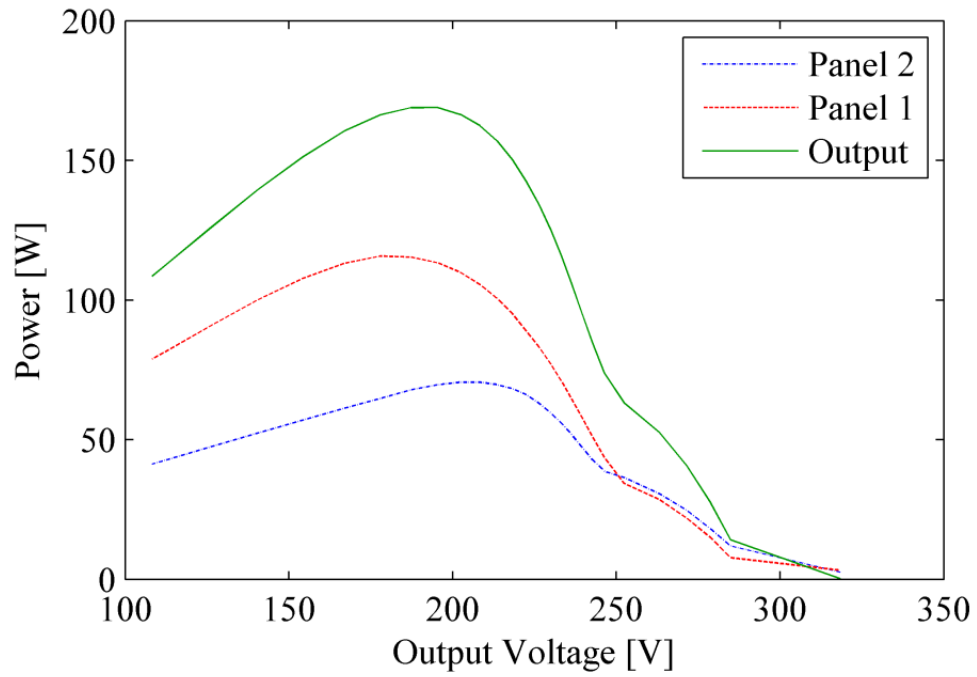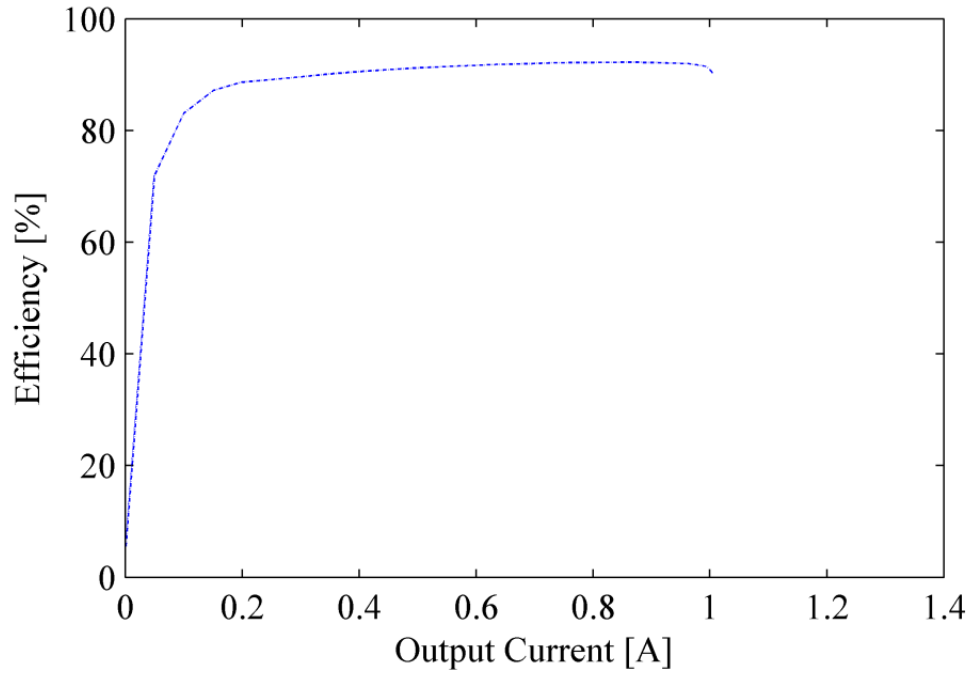Figure D.11. Total P-V Waveforms for 6 Sheets

Figure D.12. Efficiency Waveforms for 6 Sheets

Table D.4. Solar MPP Data for 6 Sheets

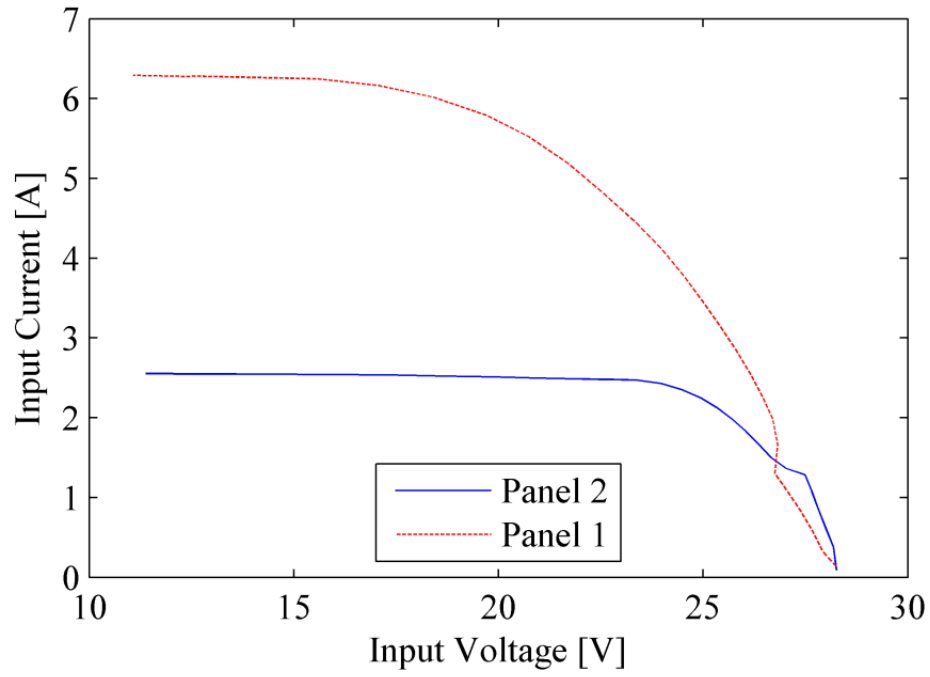|	Temp. (°C)	Insolation (W/m^2)	I$_{mpp}$ (A)	V$_{mpp}$ (V)	P$_{mpp}$ (W)	I$_{in}$ @ Total MPP	V$_{in}$ @ Total MPP	P$_{in}$ @ Total MPP
Panel 1	47.22	-	5.520	20.75	114.6	5.187	21.71	112.6
Panel 2	27.78	-	2.431	23.98	58.30	2.490	21.85	54.40
Total	-	820	0.809	190.2	154.0	-	-	-

Figure D.13. Input I-V Waveforms for 8 Sheets

Figure D.14. Total P-V Waveforms for 8 Sheets
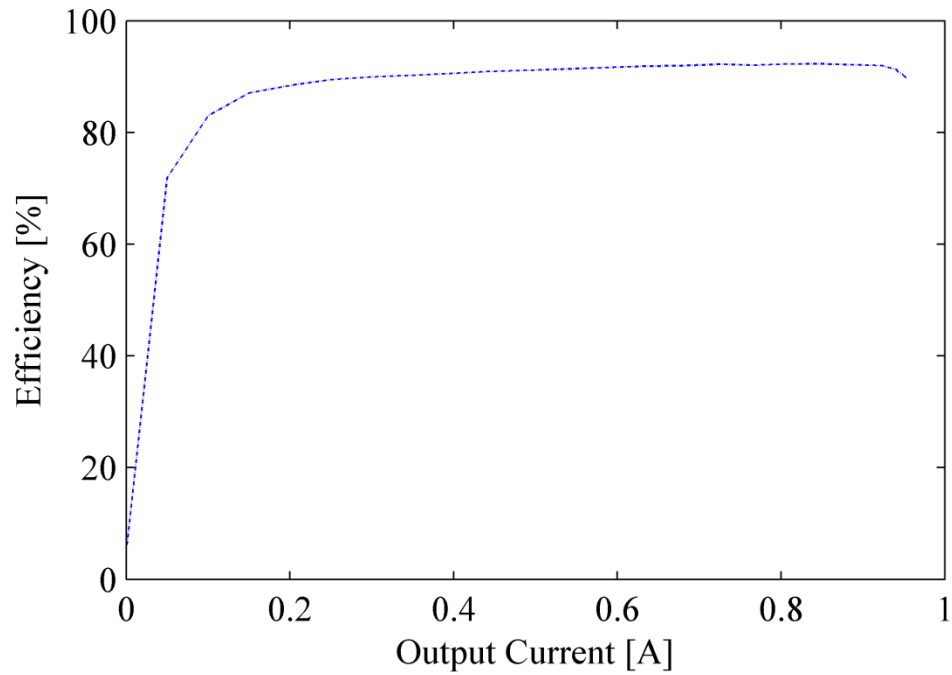
Figure D.15. Efficiency Waveform for 8 Sheets

Table D.5. Solar MPP Data for 8 Sheets

	Temp. (°C)	Insolation (W/m^2)	I$_{mpp}$ (A)	V$_{mpp}$ (V)	P$_{mpp}$ (W)	I$_{in}$ @ Total MPP	V$_{in}$ @ Total MPP	P$_{in}$ @ Total MPP
Panel 1	47.22	-	5.779	20.25	117.0	5.454	21.22	115.8
Panel 2	26.11	-	2.179	23.66	51.55	2.207	21.45	47.35
Total	-	870	0.808	186.3	150.5	-	-	-
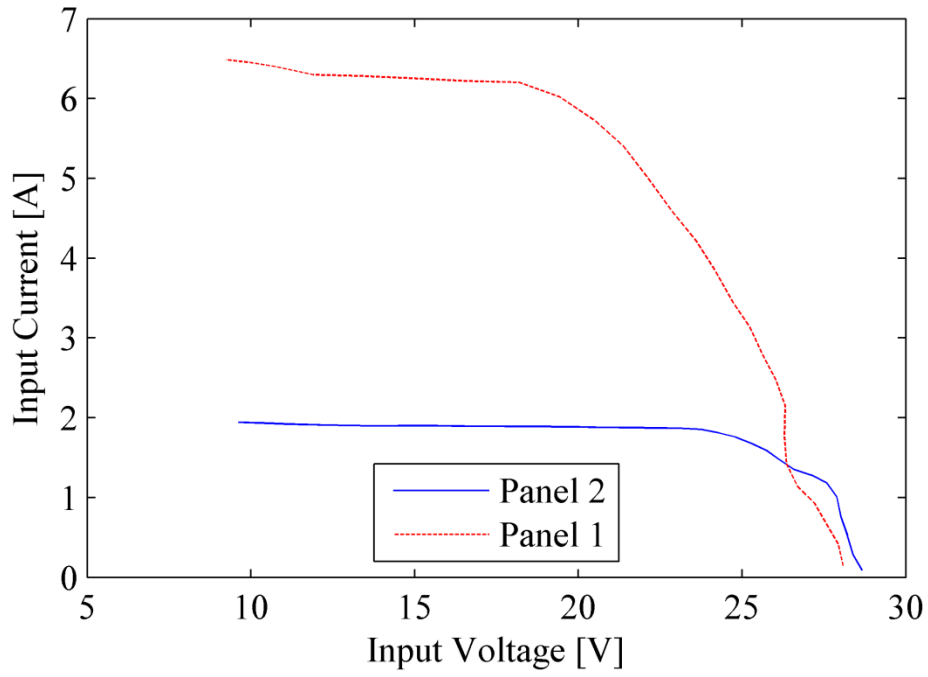
Figure D.16. Input I-V Waveforms for 10 Sheets
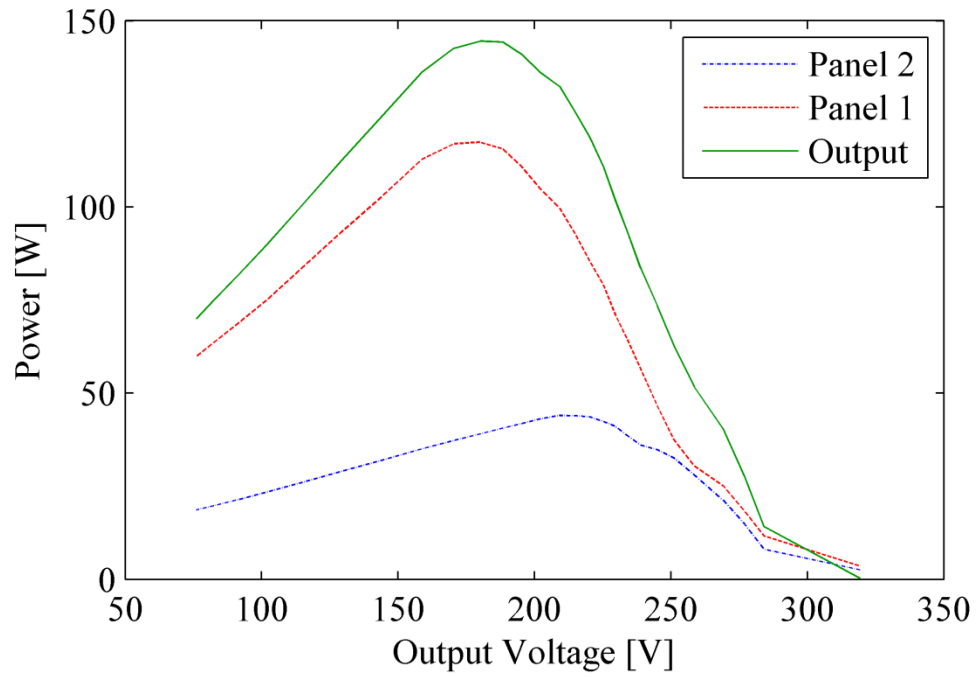
Figure D.17. Total P-V Waveforms for 10 Sheets
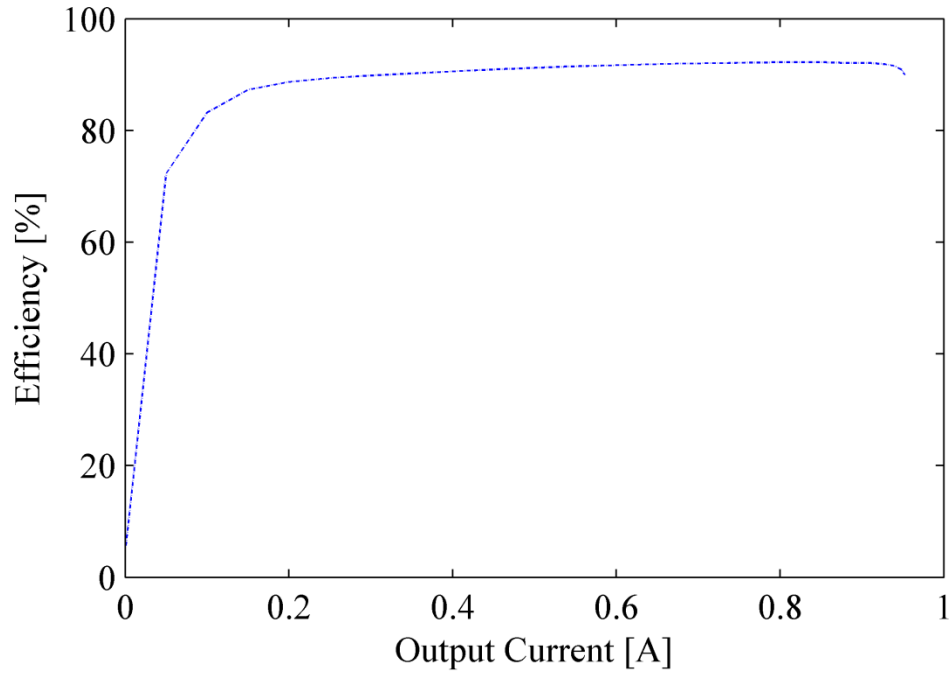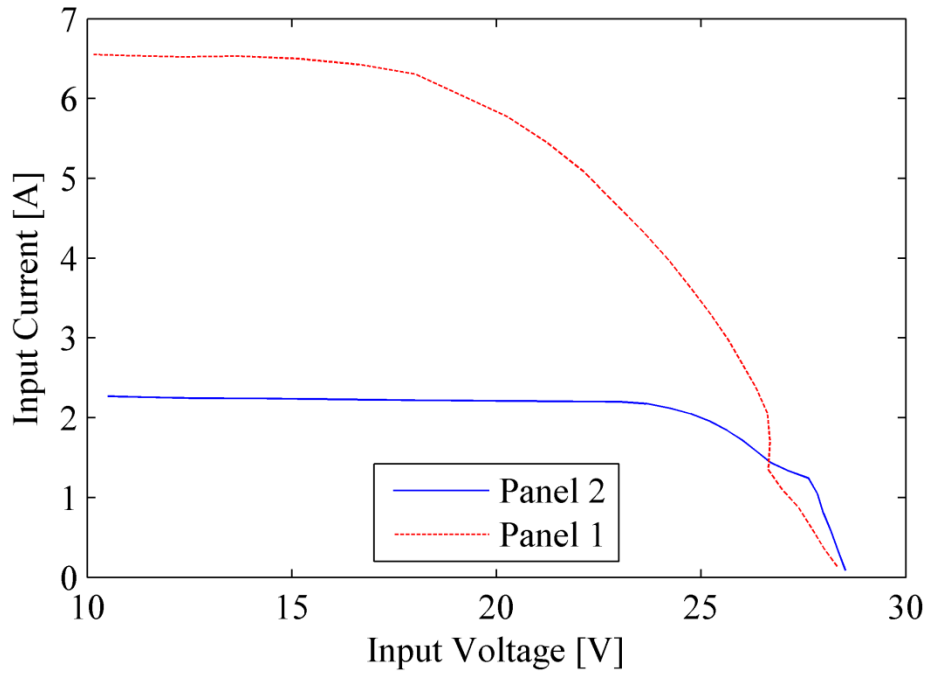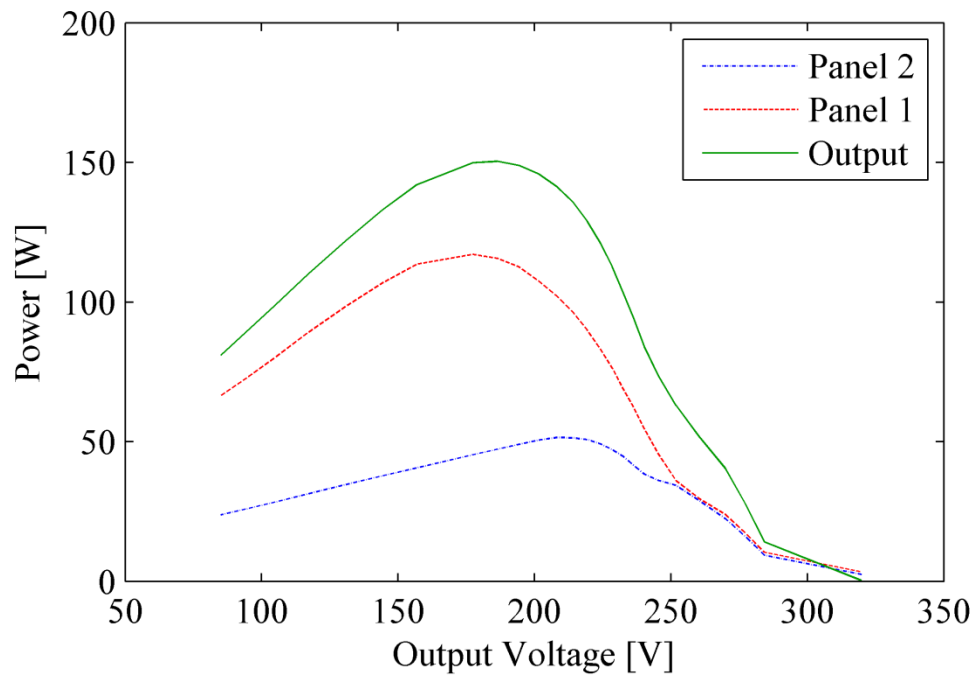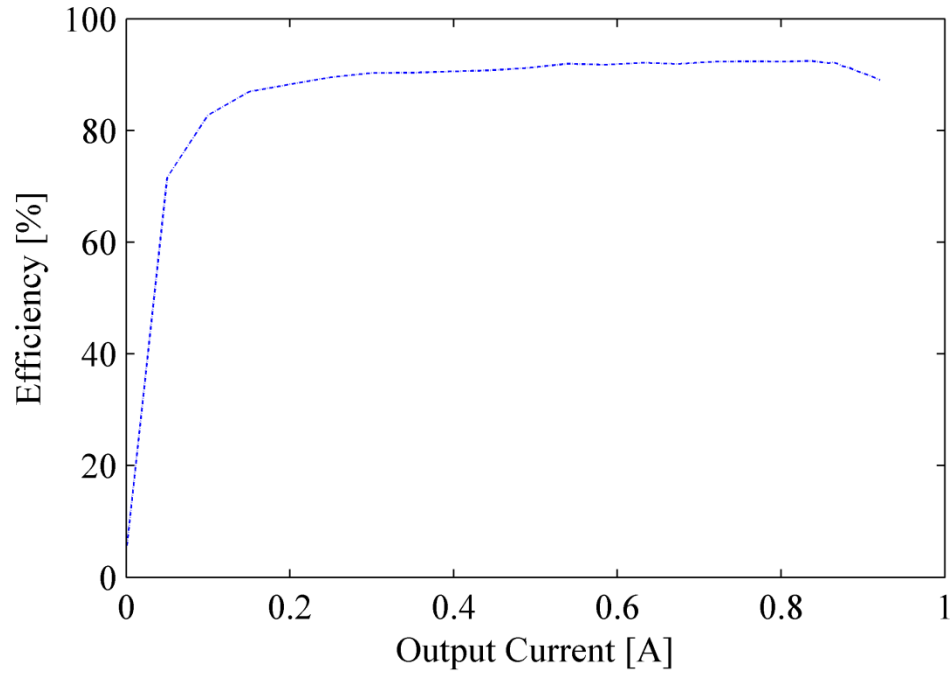
Figure D.18. Efficiency Waveform for 10 Sheets

Table D.6. Solar MPP Data for 10 Sheets

	Temp. (°C)	Insolation (W/m^2)	I_{mpp} (A)	V_{mpp} (V)	P_{mpp} (W)	I_{in} @ Total MPP	V_{in} @ Total MPP	P_{in} @ Total MPP
Panel 1				20.47639				
	43.33	-	5.736		117.5	5.736	20.48	117.5
Panel 2	25	-	1.856	23.74	44.06	1.882	20.79	39.13
Total	-	870	0.803	180.1	144.6	-	-	-

Table D.7. Summarized Solar Data

Shading	Maximum Output Power (W)	Power from Unshaded at Max Pout (W)	Unshaded Max Power (W)	Power from Shaded at Max Pout (W)	Shaded Max Power (W)	Temp. Difference (°C)
0 Sheets	208.229	112.526	112.526	113.129	113.129	5.55
2 Sheets	175.539	110.3668	110.366	80.12382	81.1723	5.55
4 Sheets	169.014	113.4539	115.794	69.75764	70.6625	15.55
6 Sheets	154.029	112.6064	114.559	54.39827	58.2960	19.44
8 Sheets	150.478	115.7696	117.054	47.34713	51.5539	21.11
10 Sheets	144.598	117.4569	117.456	39.12618	44.0560	18.33

BIBLIOGRAPHY

[1]   D. Sera, R. Teodorescu, and P. Rodriguez, "PV panel model based on datasheet values," in *Proc. Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, 2007, pp. 2392-2396.

[2]   J. Yuncong, J. A. A. Qahouq, and M. Orabi, "Matlab/Pspice hybrid simulation modeling of solar PV cell/module," in *Proc. Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, 2011, pp. 1244-1250.

[3]   A. Kajihara and A. T. Harakawa, "Model of photovoltaic cell circuits under partial shading," in *Proc. Industrial Technology, 2005. ICIT 2005. IEEE International Conference on*, 2005, pp. 866-870.

[4]   H. Patel and V. Agarwal, "MATLAB-Based Modeling to Study the Effects of Partial Shading on PV Array Characteristics," *Energy Conversion, IEEE Transactions on*, vol. 23, pp. 302-310.

[5]   J. Young-Hyok, K. Jun-Gu, P. Sang-Hoon, K. Jae-Hyung, and W. Chung-Yuen, "C-language based PV array simulation technique considering effects of partial shading," in *Proc. Industrial Technology, 2009. ICIT 2009. IEEE International Conference on*, 2009, pp. 1-6.

[6]   M. C. Di Vincenzo and D. Infield, "Artificial Neural Network for real time modelling of photovoltaic system under partial shading," in *Proc. Sustainable Energy Technologies (ICSET), 2010 IEEE International Conference on*, 2010, pp. 1-5.

[7]   W. Saranrom and S. Polmai, "The efficiency improvement of series connected PV panels operating under partial shading condition by using per-panel DC/DC converter," in *Proc. Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2011 8th International Conference on*, 2011, pp. 760-763.

[8]   G. Lijun, R. A. Dougal, L. Shengyi, and A. P. Iotova, "Parallel-Connected Solar PV System to Address Partial and Rapidly Fluctuating Shadow Conditions," *Industrial Electronics, IEEE Transactions on*, vol. 56, pp. 1548-1556.

[9]   L. Wuhua and H. Xiangning, "Review of Nonisolated High-Step-Up DC/DC Converters in Photovoltaic Grid-Connected Applications," *Industrial Electronics, IEEE Transactions on*, vol. 58, pp. 1239-1250.

[10] L. Jong Pil, M. Byung Duk, K. Tae Jin, Y. Dong Wook, and L. Byung Kuk, "A Novel Topology for Photovoltaic Series Connected DC/DC Converter with High Efficiency Under Wide Load Range," in *Proc. Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, 2007, pp. 152-155.

[11] A. Hensel, C. Wilhelm, and D. Kranzer, "Development of a boost converter for PV systems based on SiC BJTs," in *Proc. Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-7.

[12] M. Lin, S. Kai, R. Teodorescu, J. M. Guerrero, and J. Xinmin, "An integrated multifunction DC/DC converter for PV generation systems," in *Proc. Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, 2010, pp. 2205-2210.

[13] I. Sefa, x, and S. zdemir, "Multifunctional interleaved boost converter for PV systems," in *Proc. Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, 2010, pp. 951-956.

[14] A. Bellini, S. Bifaretti, and V. Iacovone, "A Zero-Voltage transition full bridge DC-DC converter for photovoltaic applications," in *Proc. Power Electronics Electrical Drives Automation and Motion (SPEEDAM), 2010 International Symposium on*, 2010, pp. 448-453.

[15] H. Guan-Chyun, L. Jung-Chien, L. Ming-Huei, W. Jia-Perng, and H. Tsai-Fu, "A study on full-bridge zero-voltage-switched PWM converter: design and experimentation," in *Proc. Industrial Electronics, Control, and Instrumentation, 1993. Proceedings of the IECON '93., International Conference on*, 1993, pp. 1281-1285 vol.2.

[16] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in *Proc. Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990., Fifth Annual*, 1990, pp. 275-284.

[17] J. Seong-Jeub and C. Gyu-Hyeong, "A zero-voltage and zero-current switching full bridge DC-DC converter with transformer isolation," *Power Electronics, IEEE Transactions on*, vol. 16, pp. 573-580.

[18] B. Yan, L. Sheng, J. Jiuchun, and Z. Weige, "Research and improvement of a zero-voltage zero-current switching full-bridge converter," in *Proc. Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 825-829.

[19] A. Jangwanitlert, K. J. Olejniczak, and J. C. Balda, "An improved zero-voltage and zero-current-switching PWM full-bridge DC-DC converter," in *Proc. Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE*, 2003, vol. 2, pp. 1685-1690 Vol.2.

[20]   Ting Ting Song and Nianci Huang, "A novel zero-voltage and zero-current-switching full-bridge PWM converter," in *Proc. Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, 2003, vol. 2, pp. 1088-1092 vol.2.

[21]   U. Badstuebner, J. Biela, and J. W. Kolar, "Design of an 99%-efficient, 5kW, phase-shift PWM DC-DC converter for telecom applications," in *Proc. Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, 2010, pp. 773-780.

[22]   W. Xinke, C. Huiming, Z. Junming, and Q. Zhaoming, "An improved high efficiency full bridge ZVS DC-DC converter with overall load range soft switching," in *Proc. Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, 2004, vol. 2, pp. 1605-1611 Vol.2.

[23]   L. Jong-Pil, M. Byung-Duk, K. Tae-Jin, Y. Dong-Wook, and Y. Ji-Yoon, "A Novel Topology for Photovoltaic DC/DC Full-Bridge Converter With Flat Efficiency Under Wide PV Module Voltage and Load Range," *Industrial Electronics, IEEE Transactions on*, vol. 55, pp. 2655-2663.

[24]   J. Huusari and T. Suntio, "Current-fed quadratic full-bridge converter for PV systems interfacing: Static operation," in *Proc. Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-10.

[25]   Texas Instruments, "TL2575, TL2575HV 1-A Simple Step-Down Switching Voltage Regulators (Rev. B)," accessed on November 8, http://www.ti.com/lit/ds/slvs638b/slvs638b.pdf.

[26]   STMicroelectronics, "Adjustable and Fixed Low Drop Positive Voltage Regulator," accessed on November 8, http://www.st.com/internet/com/TECHNICAL_RESOURCES/TECHNICAL_LITERATURE/DATASHEET/CD00000544.pdf.

[27]   Texas Instruments, "MSP430(tm) Hardware Tools User's Guide (Rev. F)," accessed on November 8, http://www.ti.com/lit/ug/slau278f/slau278f.pdf.

[28]   Texas Instruments, "MSP430F11x2, MSP430F12x2 Mixed Signal Microcontroller (Rev. D)," accessed on November 8, http://www.ti.com/lit/ds/slas361d/slas361d.pdf.

[29]   Texas Instruments, "MSP430x1xx Family User's Guide (Rev. F)," accessed on November 8, http://www.ti.com/lit/ug/slau049f/slau049f.pdf.

[30]   C. W. T. McLyman, *Magnetic core selection for transformers and inductors: a user's guide to practice and specification*. New York: M. Dekker, 1982.

VITA

Zachary Scott Johnson was born on August 26, 1986 in Kansas City, Missouri. On graduating from Lee's Summit High School in 2005, he enrolled in the University of Missouri-Rolla, which is now the Missouri University of Science and Technology. He received the Bachelor's of Science degree in Electrical Engineering from Missouri S&T in 2009, the Bachelor's of Science degree in Computer Engineering from Missouri S&T in 2009, and the Master's of Science degree in Electrical Engineering from Missouri S&T in 2012.