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THERMAL RUNAWAY
IN
POWER TRANSISTORS

BY

JERRY H. LEE, 1943

A

THESIS

Submitted to the Faculty of the

UNIVERSITY OF MISSOURI - ROLLA

in Partial Fulfillment of the Requirements for the

Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

Rolla, Missouri

1968

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Approved by

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C. Y. Ho

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ABSTRACT

Considerable work has been done on the theory of thermal runaway and the relationship between transistor junction temperature and collector power dissipation. The first part of this thesis is a review of literature. An equation for the normalized junction temperature and its peak value is developed. From this equation, the junction temperature at the thermal runaway point for a given maximum power dissipation could be determined. The second part of this thesis is experimental. The author examined the thermal runaway points for eight different transistors in the basic common emitter class A circuit which operated under no signal DC conditions.

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LIST OF SYMBOLS

T_J ... transistor junction temperature

I_{CO} ... I_{CBO} cut-off collector current

V_{eb} ... voltage drop between emitter and base

S ... stability factor

ΔT ... increment of temperature

P_C ... collector power dissipation

θ_{th} ... total thermal resistance from transistor case to ambient

a ... ratio of the collector current to emitter current

E_{CC} ... collector DC bias

E_{BB} ... base DC bias

W ... parameter

A ... parameter

K ... temperature coefficient of I_{CO}

k ... temperature coefficient of V_{eb}

k^* ... normalized collector power dissipation

ΔT^* ... normalized junction temperature

e ... constant

K^* ... normalized temperature coefficient of I_{CBO}

T_A ... ambient temperature

I_C ... collector current

I_E ... emitter current

I_B ... base current

T_{th} ... thermal loop gain

I_{CA} ... collector current at operating point

R_e ... emitter resistance

R_L ... load resistance

R_b ... base resistance

R_T ... the total resistance of emitter and collector circuit

P_C^* ... normalized collector power dissipation

$(E_{CC})_{th}$... collector power supply at thermal runaway

h_{FE} ... short circuit current gain

θ_{J-C}... thermal resistance from the junction to transistor case

θ_{C-S}... thermal resistance from the transistor case to heat sink

θ_{S-A}... thermal resistance from the heat sink to ambient

$r_{bb'}$... the ohmic resistance between the active base region, B', of the transistor and the external base lead, B.

∂ ... partial differential operator

δ ... difference operator

θ ... thermal resistance

P_{diss}... collector power dissipation

CHAPTER I

INTRODUCTION AND REVIEW OF THE LITERATURE

A. Thermal Requirements for Circuit Design

In the design of a transistor amplifier circuit, there are two thermal requirements which must be met for satisfactory transistor operation.

1) The greatest instantaneous heat released at the junction must flow through the thermal impedance at the highest ambient temperature ever encountered without raising the junction above its maximum rated temperature. In other words:

$$T_{(junction)}^{(Max)} = T_{(ambient)}^{(Max)} + \Delta T_{(J-A)}^{(Max)}$$

2) The circuit must be stabilized against thermal runaway.

For requirement 1, if the junction temperature is higher than its maximum rated temperature, then the transistor will be burned up.

For requirement 2, the power dissipation at the collector junction increases the junction temperature T_J and hence causes shifts in both I_{CO} and V_{eb} , therefore some of the transistor parameters would also be changed.

These shifts of operating point Q and transistor parameters will cause some error in transistor amplifier circuit calculations if we assumed the collector junction remained at the ambient temperature.

The shifts in T_J and in the Q-point are dependent upon the value of stability factor S ($= \frac{\partial I_C}{\partial I_{CO}}$) ; if it is small then the shifts will be small and we do not need to take

care of the increases of junction temperature. But if S is large, then the circuit may be in an unstable condition for which ΔT ($= T_J - T_A$) will be large and thermal runaway may occur.

B. Definition of Thermal Runaway

Thermal runaway may be explained as a chain of events related to the transistor junction temperature, cut-off collector current, and collector current. Therefore a rise in junction temperature alters the transistor parameters in a direction that will increase cut-off collector current I_{CBO} . This increased cut-off collector current, in turn increases the collector current, this increased collector current may increase collector power dissipation and junction temperature. This cycle repeats until finally the transistor junction temperature reaches a point at which the collector current goes up infinitely.

We may conclude that thermal runaway consists of a repetition of the following three physical process:

1) A change in I_C results in a change in P_{diss} .

2) A change in P_{diss} results in a change in T_J .

3) A change in T_J results in a change in I_C .

These statements can be further illustrated by the block diagram of Fig. 1. where it is noted that:

$$\delta T_J = \theta_{th} \cdot \delta P_C$$

$$\delta I_{CO} = \frac{\partial I_{CO}}{\partial T_J} \cdot \delta T_J$$

$$\delta I_C = \frac{\partial I_C}{\partial I_{CO}} \cdot \delta I_{CO} = S \cdot \delta I_{CO}$$

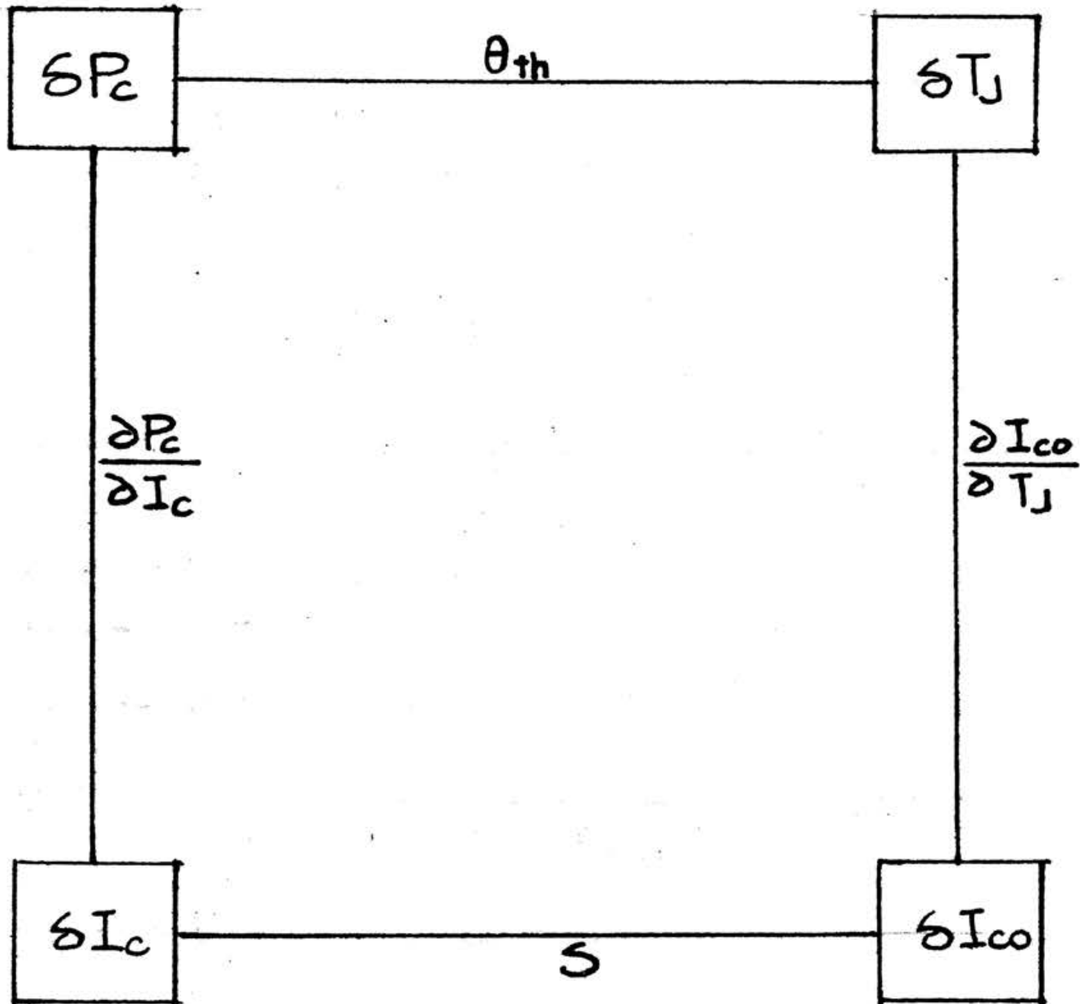

Figure 1. Illustrating positive feedback associated with thermal runaway.

$$\delta P_C = \frac{\partial P_C}{\partial I_C} \cdot \delta I_C$$

Hence the modulus of the thermal loop gain T_{th} of the system is deduced from Fig. 1. to be

$$T_{th} = \theta_{th} \cdot S \cdot \frac{\partial I_{CO}}{\partial T_J} \cdot \frac{\partial P_C}{\partial I_C}$$

If T_{th} is equal to or greater than unity then the system becomes unstable, i.e. , the transistor circuit is under the thermal runaway condition.

C. Discussion of Thermal Equation in General DC Bias Circuit

From the mathematical derivation* for a typical transistor DC bias circuit, we may finally obtain the temperature change to be

$$\Delta T = \frac{\theta P_A}{1 - \theta VS(k/(R_e + R_b) + I_{COA} / K)} \quad \text{(if } \Delta T \text{ is small)}$$

where $V = (E_{CC} - 2 I_{CA}R_T)$, $R_T = R_e + R_L$

If V is negative, then ΔT will always decrease; if V is positive and S is too large, then ΔT may become infinite and thermal runaway will occur.

Therefore by the restriction on V for stability, it is evident that for $V > 0$, i.e. , $(E_{CC} - 2 I_{CA}R_T) > 0$

then $\frac{E_{CC}}{2R_T} > I_{CA}$.

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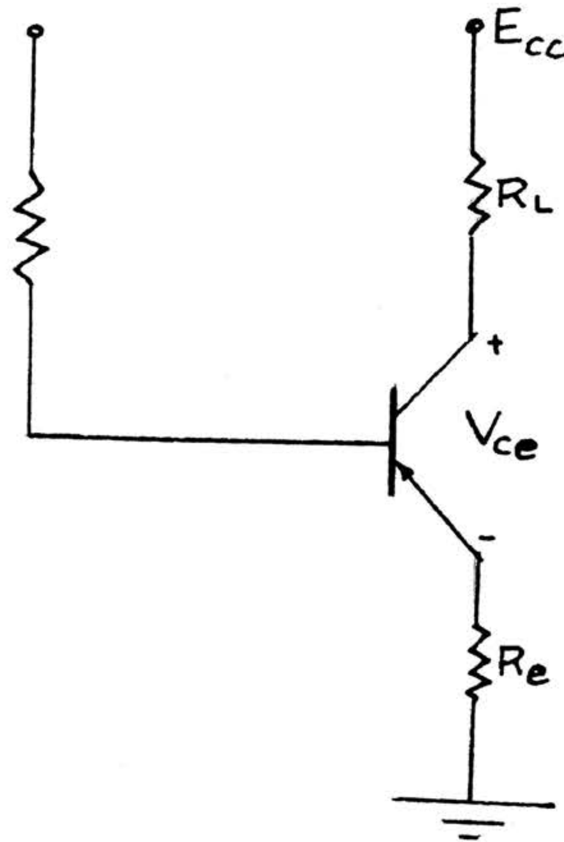
* Refer to Appendix I



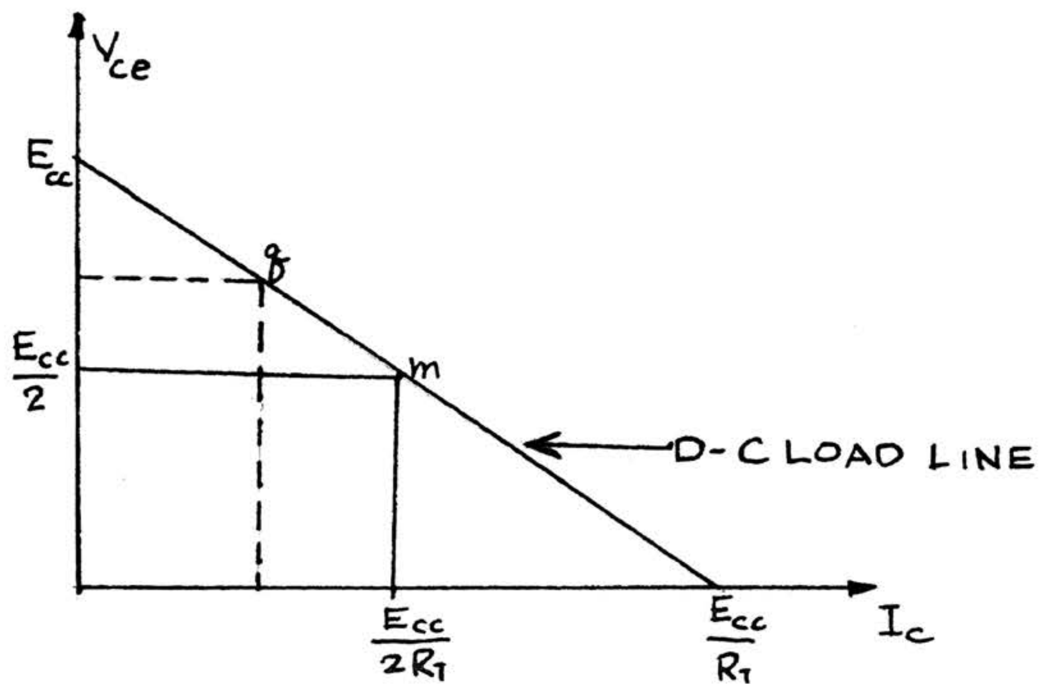


Figure 2. D-C circuit and V_{ce} vs I_C for d-c circuit.

Refer to Fig. 2. This inequality shows that an operating point q at V_{ce} greater than one-half the supply voltage E_{CC} will give a large temperature increase and more bias shifts than we may expect by calculating ΔT as just $P\theta$, and thermal runaway may occur at that point. In other words, for stable operation, the operating point indicated in Fig. 2. should be below the mid-point m, i.e. V_{ce} at operating point has to be smaller than one-half the supply voltage.

CHAPTER II

THERMAL RUNAWAY IN CLASS A OPERATION

In general, thermal runaway is not of importance except in class A amplifier operation, for example, in transformer coupled power output stages, where the load and emitter resistance are negligibly small and almost the entire supply voltage is across the transistor. If the input circuit is also transformer coupled, then by the equation for stability factor

$$S = \frac{R_e + R_b}{R_e + R_b(1 - a)}^{*}, \quad \text{therefore } S = 1 \text{ and the circuit}$$

is possible in a stable condition.

For convenience, we may construct a thermal circuit as shown in Fig. 3.

Various definitions and assumptions concerning the circuit are as follows:

1) The system operates under class A, no input signal conditions.

2) The voltage drops across R_L and R_e are negligible compared with the supply voltage, so that $V_{ce} = E_{CC}$.

3) I_C' is the collector current with no I_{CO} flowing, i.e. , at $T = T_A$.

4) $P_C' = E_{CC} I_C'$ is the collector power with no I_{CO} flowing.

5) θ is overall thermal resistance from junction to

---

* Refer to Appendix I

ambient.

6) $P_C = E_{CC} I_C$ is the total collector power.

7) $\Delta T = T_J - T_A = \theta P_C$ is the difference between the actual junction temperature and ambient temperature.

8) $\Delta V_{eb} = - k \Delta T$ where $k = - 2.5$ mv /°C

9) $I_{CO2} = I_{CO1} \cdot \exp\left(\frac{\Delta T}{K}\right)$ where K is a constant that governs the rate of increase of I_{CO} with temperature.

10) Thermal capacitances are ignored.

11) I_{CO1} is the I_{CO} at the ambient temperature, that is when $\Delta T = 0$.

12) $W = E_{CC} \cdot I_{CO1} \cdot S$

13) $A = \frac{a \cdot E_{CC} \cdot S \cdot k}{R_e + R_b}$

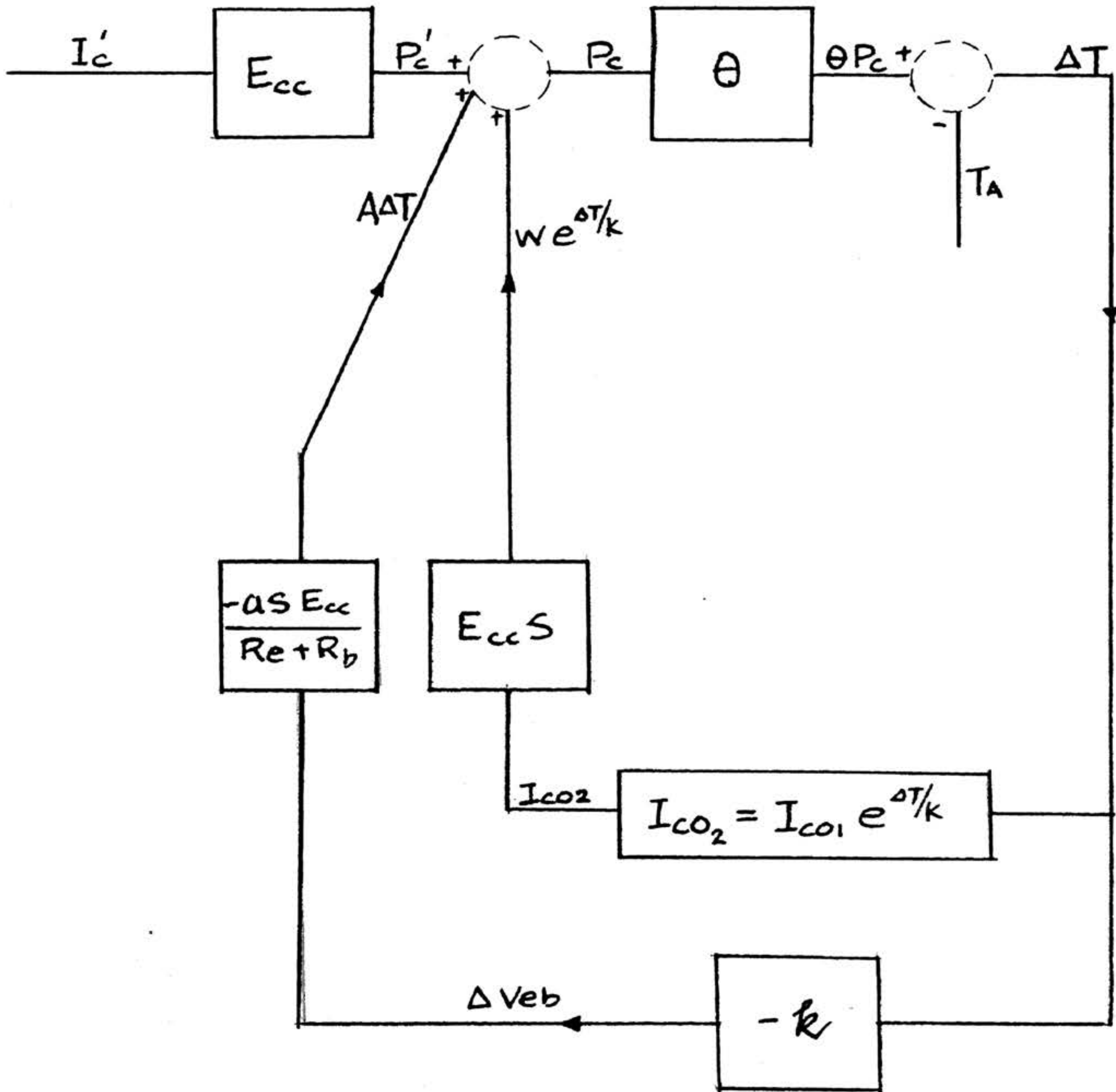


Figure 3. Block diagram of thermal feedback.

Now from the thermal circuit

$$\Delta T = (\theta P_C') + (A\theta) \Delta T + \theta W \exp (\Delta T / K)$$

Solve for ΔT to obtain

$$\Delta T = \frac{P_C'\theta + \theta W \exp (\Delta T / K)}{1 - A\theta} \tag{1}$$

If we assume that a bias compensation, such as diode compensation, has been employed to remove the effect of the variation in the emitter-base junction voltage with temperature, then $A = 0$ and

$$\Delta T = \theta P_C' + \theta W \exp (\Delta T / K) \tag{1-a}$$

By maximizing $P_C'\theta$ with respect to ΔT, we obtain the peak value of ΔT and $\theta P_C'$.

$$(P_C'\theta)_{Peak} = \Delta T_{Peak} - K \tag{2}$$

By picking a different value of K, and using $W\theta$ as a parameter we could generate a family of ($P_C'\theta$) vs ΔT curves and Equation (2) serves as a locus of points at which thermal runaway occurs.

For simplicity, we may normalize equation (1-a) with respect to $W\theta$ to obtain

$$\frac{\theta P_C'}{W\theta} = \frac{\Delta T}{W\theta} - \exp \left(\frac{\Delta T / \theta W}{K / \theta W} \right)$$

$$P_C^* = \Delta T^* - \exp (\Delta T^* / K^*) \tag{3}$$

The slope of all curves is

$$\frac{d P_C^*}{d \Delta T^*} = 1 - \frac{1}{K^*} \exp (\Delta T^* / K^*)$$

At $\Delta T^* = 0$,

$$\frac{d\,P_C^*}{d\,\Delta T^*} = 1 - \frac{1}{K^*}$$ -------- slope initially of all curves

At $\Delta T^* = 0$ for Equation (3)

$$P_C^* = -1$$

Maximum P_C^* occurs when $1 = \frac{1}{K^*} \exp (\Delta T^* / K^*)$

or $K^* = \exp (\Delta T^* / K^*)$

Thus $\Delta T^* = K^* \ln (K^*)$ (4)

Substituting (4) into Equation (3)

then $(P_C^*)_{Max} = (\Delta T^*) - K^*$ (5)

which is zero at $\Delta T^* = K^*$

when $\Delta T^* = 0$.

Then $(P_C^*)_{Max} = - K^*$

From Equation (3) when $P_C^* = 0$

$$\Delta T^* = \exp (\Delta T^* / K^*)$$

or

$$\frac{\Delta T}{W\theta} = \exp (\Delta T^* / K^*)$$

At the condition of $P_C^* = 0$, when thermal runaway occurs from Equation (5) then $\Delta T = K$

therefore

$$\frac{\Delta T}{W\theta} = e$$

and $W\theta = \frac{\Delta T}{e}$

From the discussion above two boundary conditions for safe operation were obtained. As in Fig. 4, for a given K, the stable operation region is between these two lines and

each value of parameter $W\theta$ corresponds to a new ΔT.

Furthermore, rewrite Equation (3) and Equation (4) together

$$P_C^* = \Delta T^* - \exp(\Delta T^* / K^*)$$

$$\Delta T^* = K^* \ln(K^*) \tag{5}$$

They are two dependent-variable simultaneous equations with K^* as a parameter. Theoretically it is possible to eliminate K^* between them but because of the nonlinearity of the equations, we can not do better than using the numerical method to draw a curve of $(P_C^*)_{Max}$ vs ΔT^* as shown in Fig. 5. from which we can see the relationship between $(P_C^*)_{Max}$ and $(\Delta T^*)_{Max}$.

By using this curve one may predict the junction temperature at thermal runaway when collector power dissipation is given for any kind of transistor.

If the bias compensation scheme is omitted, so that $A \neq 0$, then we have the $A\theta$ term in Equation (1).

Thus $P_C'\theta = (1 - A\theta)\Delta T - W\theta \exp(\Delta T/K)$

which can be written as

$$\frac{\theta P_C'/(1 - A\theta)}{W\theta/(1 - A\theta)} = \frac{\Delta T}{W\theta/(1 - A\theta)} - \exp(\Delta T/K)$$

when normalized, this becomes

$$\frac{P_C'\theta}{W\theta} = P_C^* = \Delta T^* - \exp(\Delta T^*/K^*)$$

where $K^* = \dfrac{K}{W\theta/(1 - A\theta)}$

Using the same procedure as before, we finally could

obtain the curves as shown in Fig. 4. and Fig. 5. respectively.

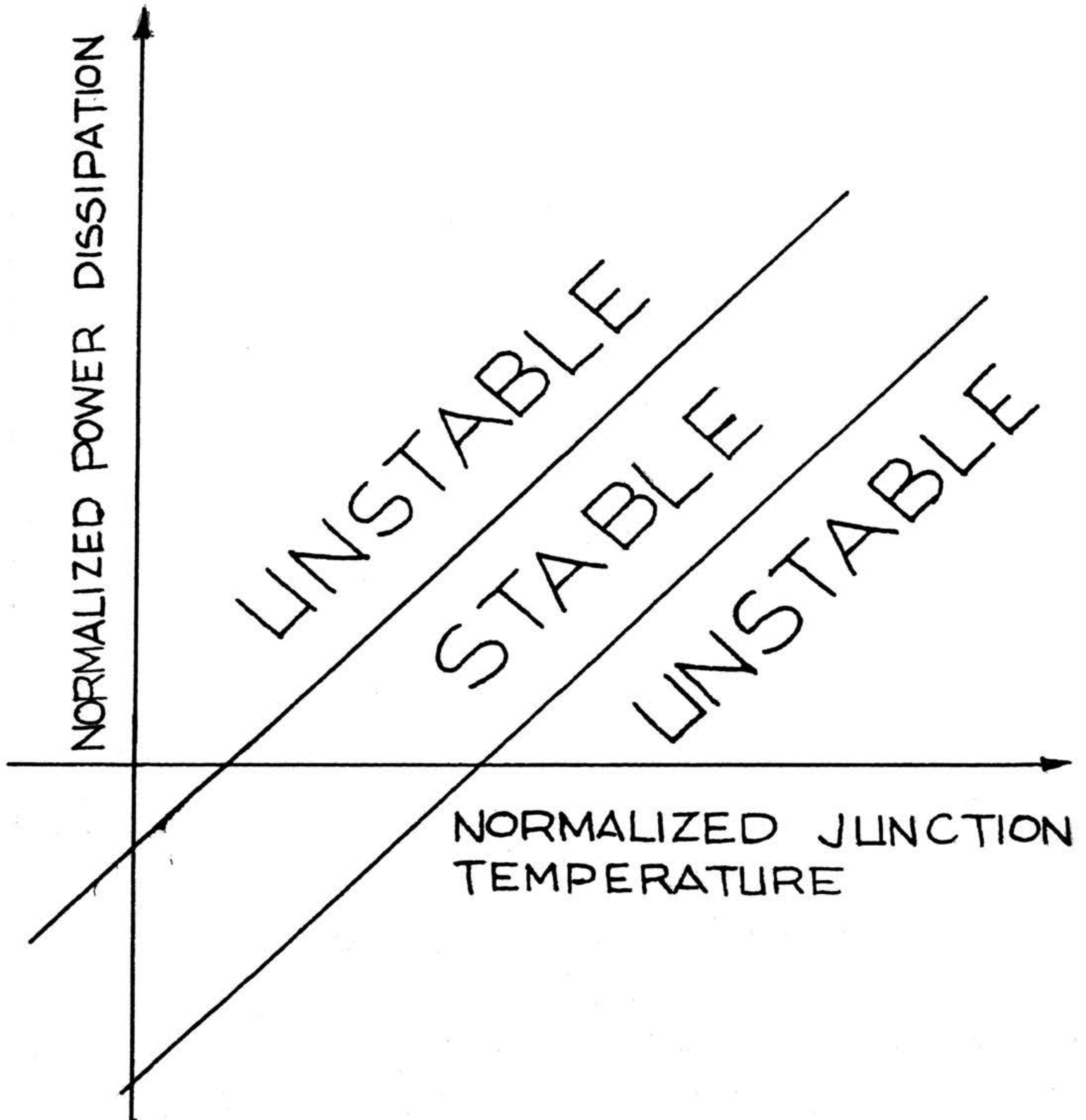


Figure 4. Normalized junction temperature vs power dissipation curve with K^* as a parameter.

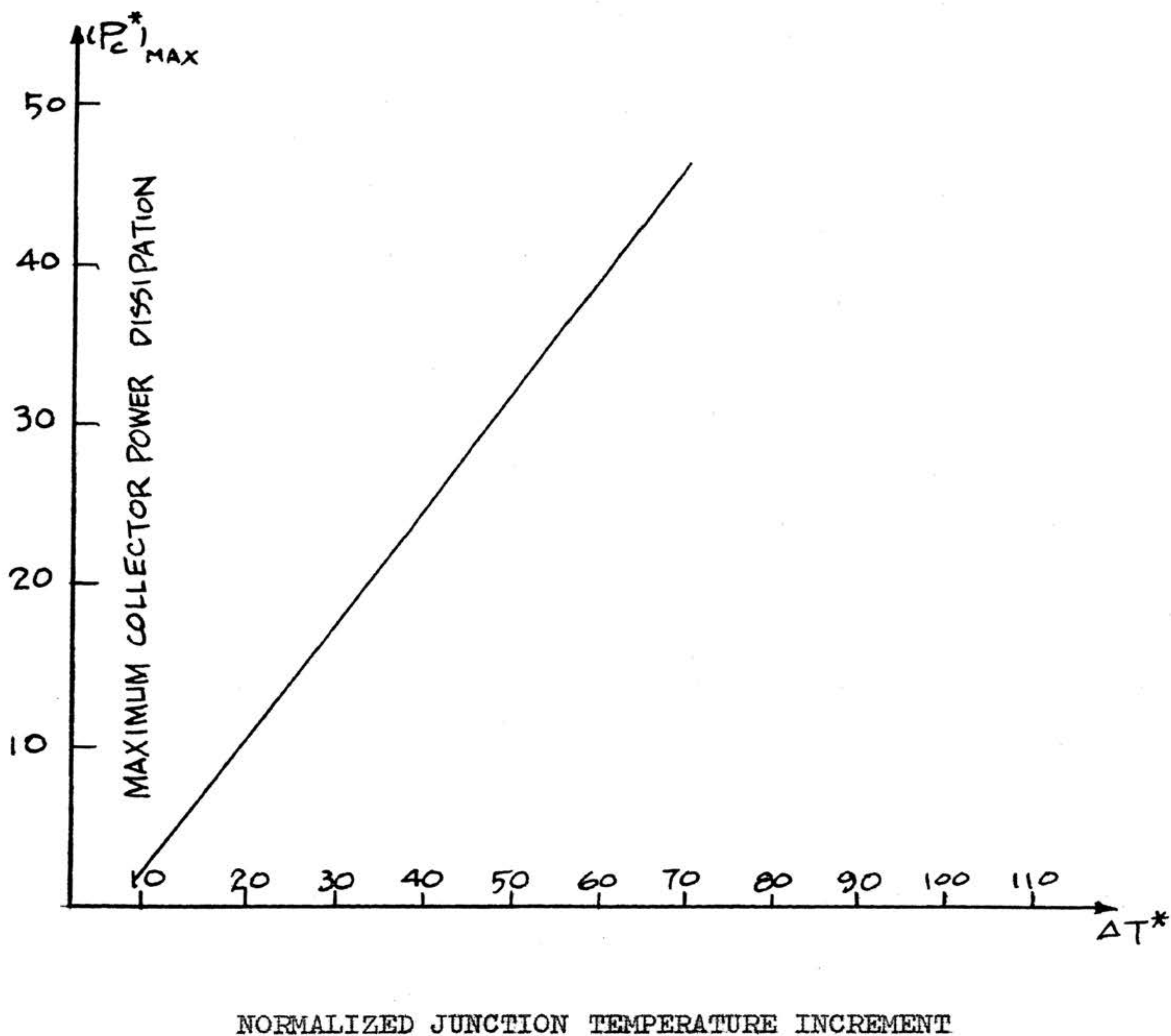


Figure 5. Normalized maximum power dissipation at thermal runaway vs normalized junction temperature.

CHAPTER III

EXPERIMENTAL

A. Objectives

The objectives of the experimental measurements are to obtain the transistor junction temperatures at the thermal runaway points for several different power transistors in the same common-emitter DC bias circuit, and to compare them with the theoretical values given in Fig. 5.

B. Design of the Circuit

Because of the intention to induce thermal runaway, it is necessary to build up an unstable circuit, which means to make the stability factor as large as possible. For making S large, we may operate the transistor circuit as a class A amplifier with high input resistance. Furthermore, since the maximum power is dissipated in the transistor with no signal present, we only need to examine thermal runaway in the DC circuit.

When the transistor is operating, collector dissipation power increases, which in turn increases the junction temperature, which causes heat to be generated within the semiconductor. In order to reduce the junction temperature, a heat sink is required to direct heat from the junction into the ambient air. For the objectives of this experiment, a heat sink that is just big enough to induce thermal runaway is used. Also, in order to reduce the high thermal impedance of an air gap present between the mating surface of the semiconductor case and the heat sink surface, a type

120 thermal joint compound is used.

C. Equipment

1) 1 microammeter

2) 3 DC power supplies (one range 0-40 V for base bias, 2 range 0-32 V are in series for collector bias).

3) 2 ammeters (0-1 amp.)

4) Oven

5) Transistor parameter tester

D. Material

1) 1 thousand-ohm resistor

2) 2 one-ohm resistors

3) Power transistor types: 2N2142, 2N2143, 2N2144, 2N2145, 2N1359, 2N1360, 2N1529, 2N1530.

4) 120 silicon joint compound

5) Heat sinks: NC621, NC403

E. Procedure

1) Measuring I_{CBO}

In order to determine the temperature coefficient of I_{CBO} for a specified transistor, several values of I_{CBO} at different temperature are required.

Set the transistor circuit board as indicated in Fig. 7 into the oven, then start to increase the temperature from the ambient. In order to keep the temperature of the oven constant for a sufficiently long time at each step, one must keep rotating the knob forward and backward. After the scale indicated that the temperature of the oven is nearly constant, record the value of current

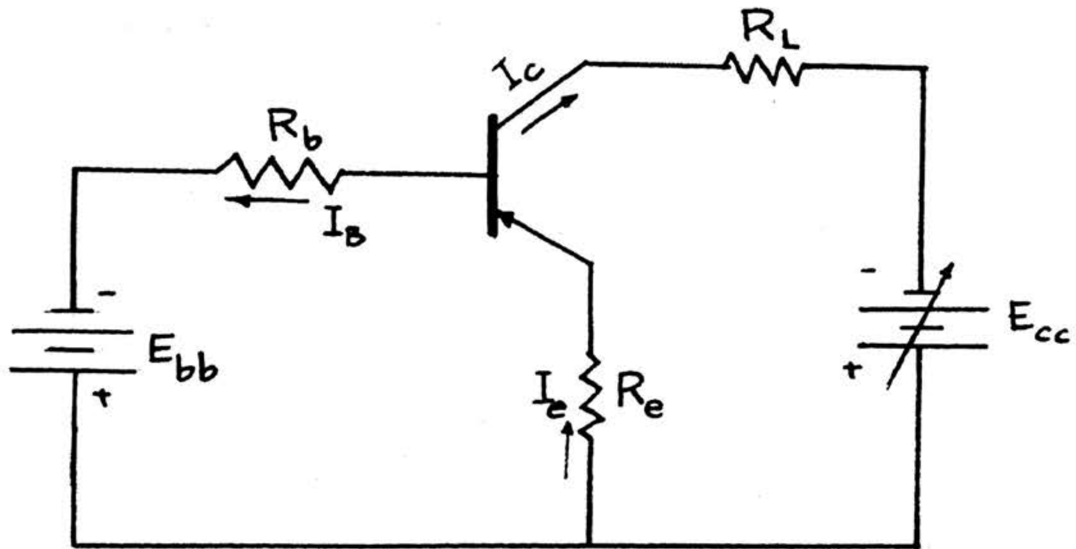


Figure 6. Common emitter DC bias circuit.

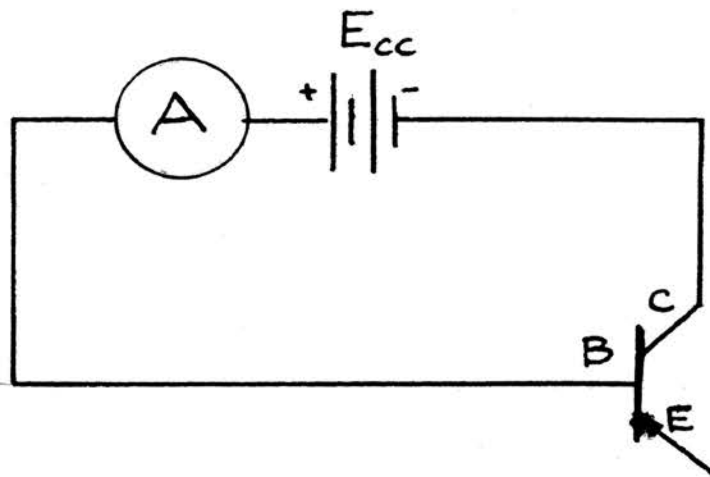


Figure 7. Cut-off collector current measuring circuit.

flowing through the microammeter. Repeat the same procedure at several different temperature.

2) Testing of the transistor short-circuit current gain

By using the transistor parameter tester, the short circuit current gain for a specified transistor at ambient temperature is obtained.

3) Setting the bias

Connect a one-thousand ohm resistor in the base circuit and apply a reverse bias E_{BB} which has the value only a little bit larger than V_{be} , that has been given by manufacturer's data. Then connect the two-ohm resistors in both emitter and collector circuits.

4) Apply a DC power supply into the collector circuit as reverse bias. Record the collector current at that instant and after five minutes, then increase E_{CC} to a new value. Repeat the same procedure at each step. When the thermal runaway point is approached, the collector current will go up gradually for a given bias, and at thermal runaway the collector current is increased very rapidly. One should watch the increment very carefully and shut down the system before the maximum allowable collector current has been reached, otherwise the transistor will be burned up.

5) Since the collector current used in Equation (1) is the one with no I_{CBO} flowing, in other words, it is the collector current at $T = T_A$, the collector current corresponding to the collector DC bias which would induce

thermal runaway has to be examined again. Wait until the elements of the circuits are completely cooled down to ambient temperature, then turn on the system and set the collector bias at $(E_{CC})_{th}$ * and record the collector current at that instant accordingly.

6) Using eight power transistors and repeating the same procedure eight times, eight thermal runaway points were obtained.

7) Calculate the junction temperature by using the values of $P'\theta = E_{CC} \cdot I_C \cdot \theta_T$, k, K, I_{CBO} , h_{FE} , in Equation (1). The IBM 360-50 computer was used to solve this nonlinear equation.

---

* $(E_{CC})_{th}$ represents the collector DC bias voltage at which thermal runaway occurs.

F. Results

TYPE	E_{cc} VOLT	I_c AMP	θ_T OHM	I_{CBO} μA T=18°C	K °C	h_{FE} T=18°C	$P_c\theta$ WATT	ΔT °C EXPER	ΔT °C THEOR	ERROR %
2N-2142	45	0.35	3.1	40	17.8	75	48.8	64.3	68.7	6.56
2N-2143	27	0.245	5.8	45	18.2	95	38.4	48.9	54.1	9.50
2N-2144	28	0.256	5.8	26	15.3	80	41.9	54.8	59.4	8.00
2N-2145	30	0.282	5.8	18	16.5	95	49.0	65.4	69.1	4.60

REMARK 1) ASSUME h_{FE} CONSTANT

2) THEORETICAL VALUES OF ΔT ARE OBTAINED FROM SOLVING THE EQ. (5) FOR A GIVEN $P_c\theta$

TABLE 2-1

EXPERIMENAL RESULTS FOR TRANSISTORS 2N2142, 2N2143, 2N2144, 2N2145

TYPE	E_{cc} VOLT	I_c AMP	θ_T OHM	I_{CBO} μA T=18°C	K °C	h_{FE} T=18°C	$P_c\theta$ WATT	ΔT °C EXPER	ΔT °C THEOR	ERROR %
2N-1359	30	0.12	5.4	335	24.4	40	19.4	26.1	27.3	5.2
2N-1360	24	0.22	5.4	51	17.5	140	28.5	37.7	40.0	6.0
2N-1529	32	0.32	5.4	30	16.5	35	55.3	71.5	77.1	7.2
2N-1530	23	0.35	5.4	61	14.4	90	43.6	57.5	61.4	6.35

TABLE 2-2

EXPERIMENTAL RESULTS FOR TRANSISTORS 2N1359, 2N1360, 2N1529, 2N1530

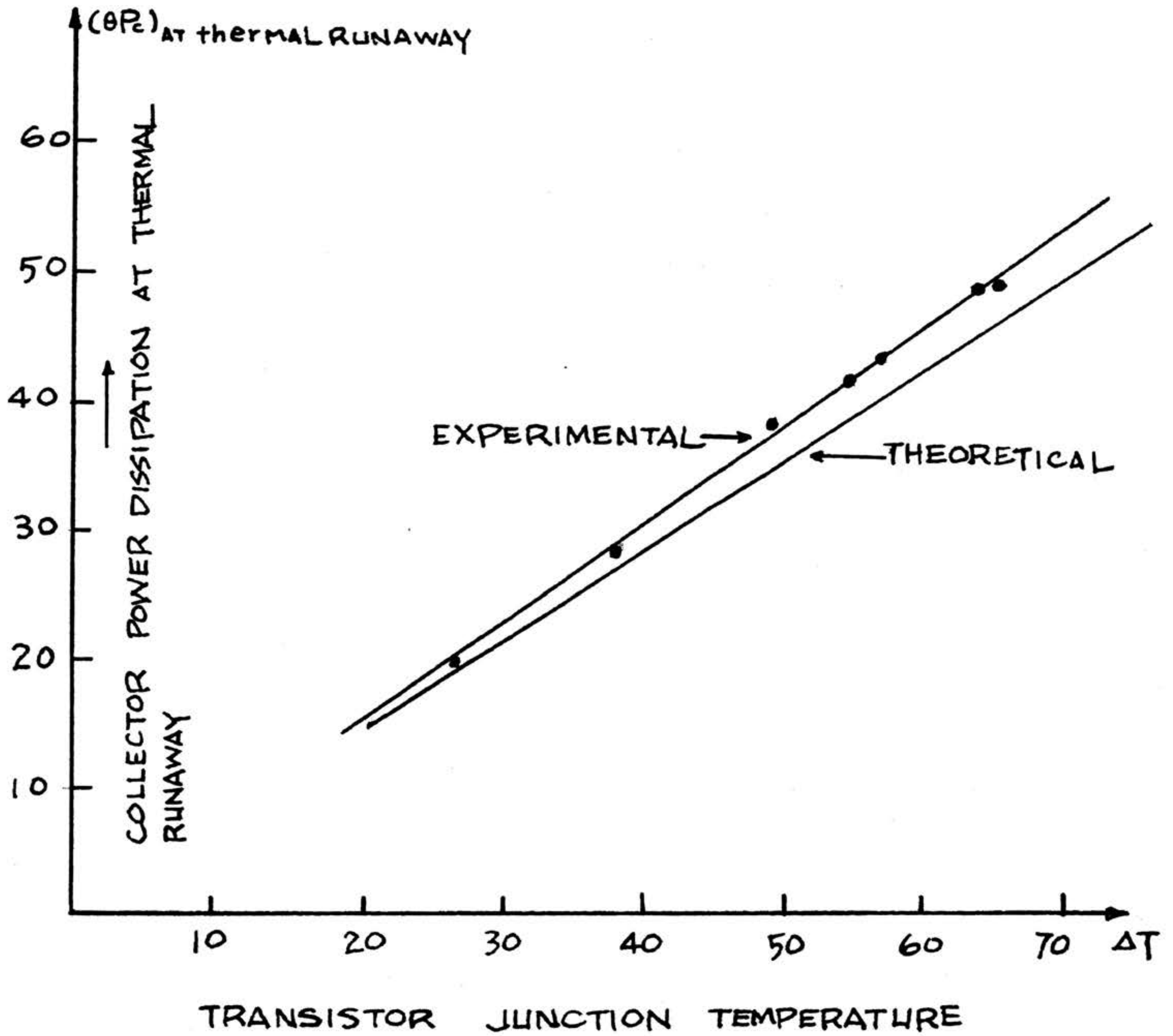


Figure 8. Comparison of experimental and theoretical curves for $(\theta P_C)_{Max}$ vs ΔT.

CHAPTER IV

DISCUSSION AND CONCLUSIONS

There are several problems inherent in calculating the junction temperature.

The first is unavoidable when the devices are considered over a wide range of input parameters. It involves the necessity of assuming that the transistor parameters such as a or $r_{bb'}$ are constant with temperature and with the operating point. For example, when thermal runaway is approached, I_C increases which normally decreases a; on the other hand, the temperature increases which normally increases a. If no emitter resistance or a very small emitter resistance is employed, the stability factor S is equal to $(1 + h_{FE})$, so that small changes in a will have large effects upon the runaway point.

In this experiment it is impossible to obtain the exact value of h_{FE} and hence a at each bias step; of course one may use the fundamental current identity for common emitter transistor circuit to solve for a,

i.e. , $I_C = a I_E + I_{CO}$

By using this equation, the author has met the following difficulty.

1) Since the value of a is very nearly equal to 1, and also I_{CO} is a very small value, thus I_C and I_E may be very close. Therefore it is hard to obtain the exact difference between I_E and I_C just by using a common current meter or a oscilloscope. If they are not the exact value, then large

error will be induced.

2) Since the coefficient K is variable at each temperature for a given transistor, the cut off current I_{CBO} obtained from the equation $I_{CO2} = I_{CO1} \exp(\Delta T / K)$ is unreliable. Thus it is evident that the value of h_{FE} is difficult to estimate exactly from the discussion above. The only way to handle this problem seems to involve some assumptions on h_{FE}.

The first assumption made on h_{FE} is by assuming that $h_{FE} = (h_{FE})_{T=T_A} \cdot 2^{(\Delta T/50)}$ and neglecting the influence of I_C. This assumption is based on the investigation that the short-current gain will be doubled for each 50°C increase for a germanium semiconductor, in general.

In order to check the accuracy of this assumption, one transistor was selected arbitrarily and used in the common emitter DC circuit shown in Fig. (9).

Having properly biased the circuit, put the transistor circuit board into the oven and heat it up from 20°C to 70°C. Record the values of I_C and I_B for each 10°C increment. Then applying them into the equation

$$h_{FE} = \frac{I_C}{I_B}$$

the current gains at each temperature level were obtained.*

By comparision with the assumption made on the h_{FE} variation with temperature, a standard error of 11% was found*.

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* See Appendix II

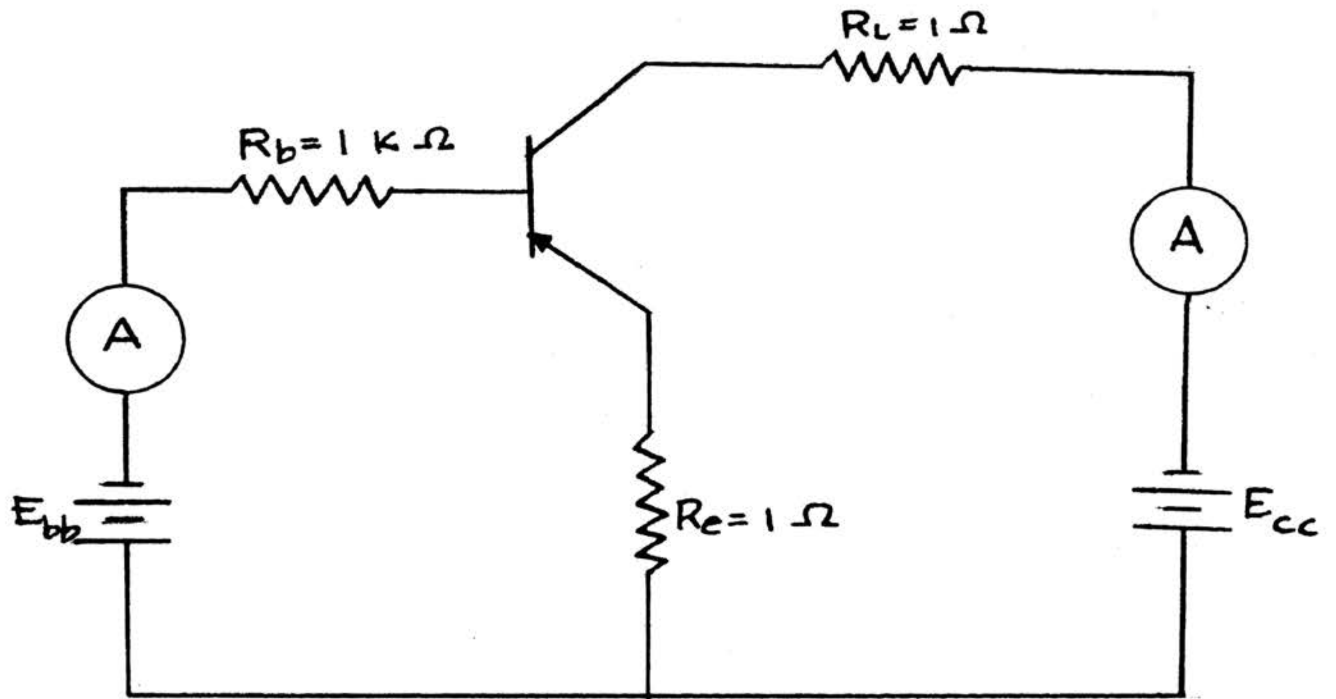

Figure 9. Common emitter circuit for measuring h_{FE}.

Upon using this assumption, for minimum error, the average value of K was used for calculating the junction temperature, quite satisfactory results have been obtained*.

But because the influence of collector current on the variation of h_{FE} could not be neglected, the only reasonable approach appears to be to assume the fall-off in h_{FE} from increased current density will compensate for the increase due to increased temperature. In other words, h_{FE} is assumed to be unchanged during the whole operating process —— this is the second assumption made on h_{FE}. After carefully examining this problem, it seems that the second assumption is more reasonable.

Also for inducing the minimum error, the minimum value of K was used instead of average K. The result by using this assumption is given on pages 20, and 21.

The second problem is the one of determining what values to use for θ_T, k, K.

The semiconductor manufacturer normally gives the thermal resistance from the junction to the transistor case θ_{J-C}. The heat sink manufacturer gives the thermal resistance from the heat sink to ambient θ_{S-A}. The only thing remaining to examine is the thermal resistance from transistor case to heat sink θ_{C-S}. Because of the dependence of the flatness of the heat sink surface and semiconductor surface when using 120 joint compound for a

---

* See Appendix II

given semiconductor case style, it is unexpected to estimate an exact value of θ_{C-S} .

An average value of θ_{C-S} for different degrees of flatness was selected in this experiment. Of course, some small error was induced.

As regard to k, for simplicity no attempt was made to measure k. It is desirable to assume k to be -2.5 mv/°C for each transistor. The reason for using this assumption is that k will not influence the junction temperature appreciably in this experiment.

Because of the difficulty of keeping the temperature of the oven constant when measuring I_{CBO} , different values of K were introduced for each measurment. Joyce & Clark [1] suggest that one should assume the lowest expected value for K. By using this suggestion and assuming h_{FE} constant during the whole process, a set of tabulated data and diagrams were obtained as shown on page 20, 21, and 22.

All in all, these considerations add up to make a certain amount of guesswork. Therefore, the error between the experimental and theoretical results for each transistor is in the range of 5-10 %.

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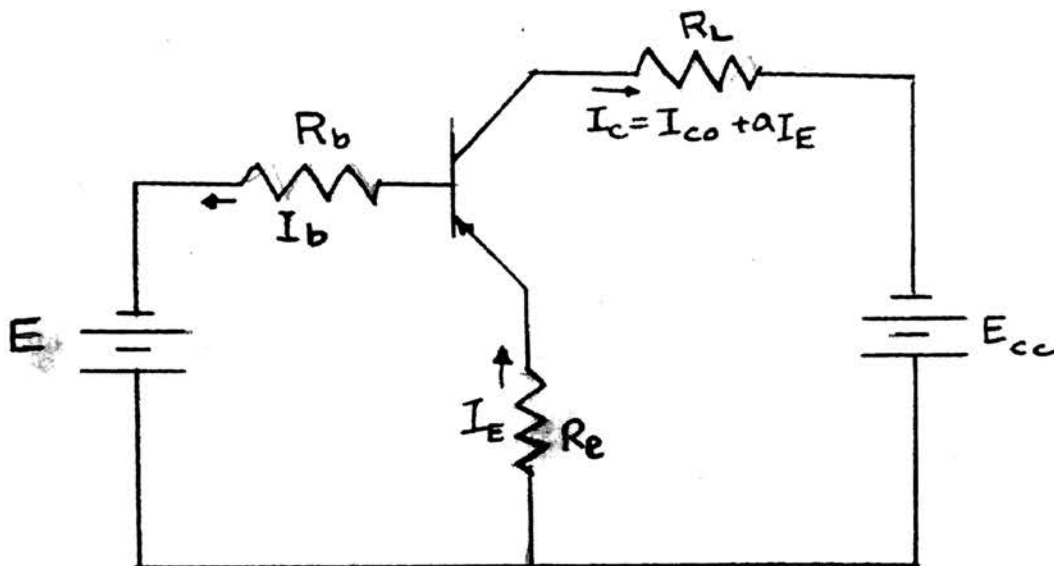
APPENDIX I

DERIVATION OF THERMAL EQUATION



$$I_C = a\ I_E + I_{CO} \qquad (1)$$

$$I_B = (1-a)\ I_E - I_{CO} \qquad (2)$$

For the input circuit

$$E = R_e I_E + V_{eb} + ((1-a)\ I_E - I_{CO})\ R_b$$

$$= (R_e + (1-a)\ R_b)\ I_E + V_{eb} - I_{CO} R_b$$

Therefore

$$I_E = \frac{E - V_{eb}}{R_e + (1-a)\ R_b} + \frac{I_{CO}\ R_b}{R_e + (1-a)\ R_b}$$

Let $$I_{E1} = \frac{E - V_{eb1}}{R_e + (1-a)\ R_b} + \frac{I_{CO1}\ R_b}{R_e + (1-a)\ R_b}$$

$$I_{E2} = \frac{E - V_{eb2}}{R_e + (1-a)\ R_b} + \frac{I_{CO2}\ R_b}{R_e + (1-a)\ R_b}$$

therefore

$$\Delta I_E = I_{E2} - I_{E1} = \frac{-\Delta V_{eb}}{R_e + (1-a)\ R_b} + \frac{\Delta I_{CO}\ R_b}{R_e + (1-a)\ R_b}$$

where $\Delta V_{eb} = V_{eb2} - V_{eb1}$

$$\Delta I_{CO} = I_{CO2} - I_{CO1}$$

From (1) we obtain the variation equation for ΔI_C

$$\Delta I_C = a\,\Delta I_E + \Delta I_{CO} \qquad (3)$$

Substitute ΔI_E into (3)

$$\Delta I_C = \frac{-a\ \Delta V_{eb}}{R_e + (1-a)\ R_b} + \frac{a\ \Delta I_{CO}\ R_b}{R_e + (1-a)\ R_b} + \Delta I_{CO}$$

$$= \frac{-a\ \Delta V_{eb}}{R_e + (1-a)\ R_b} + \frac{(R_e + R_b)\ \Delta I_{CO}}{R_e + (1-a)\ R_b}$$

By definition

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{R_e + R_b}{R_e + (1-a)\ R_b}$$

therefore

$$\Delta I_C = \frac{-a\ \Delta V_{eb}(R_e + R_b)}{(R_e + (1-a)\ R_b)(R_e + R_b)} + S\,\Delta I_{CO}$$

$$= \frac{-a\ S\ \Delta V_{eb}}{R_e + R_b} + S\,\Delta I_{CO}$$

Let $I_C = I_{CA} + \Delta I_C$

$$\Delta V_{eb} = -\ k\,\Delta T$$

$$\Delta I_{CO} = I_{COA}(\ e^{\Delta T/K} - 1\ )$$

$$R_e + R_L = R_T$$

Then $P_C \cong E_{CC} \cdot I_C - I_C^2 (R_L + R_e)$

$$= (I_{CA} + \Delta I_C)(E_{CC} - (I_{CA} + \Delta I_C) R_T)$$

$$= (I_{CA}E_{CC} - I_{CA}^2 R_T) + \Delta I_C(E_{CC} - 2 I_{CA}R_T - \Delta I_C R_T)$$

Now $P_A = I_{CA}E_{CC} - I_{CA}^2 R_T$

and in general $2 I_{CA} >> \Delta I_C$ in any circuit for good stability, so that the $\Delta I_C^2 R_T$ term may be dropped.

Let $V = E_{CC} - 2 I_{CA} R_T$

therefore

$$P_C = P_A + \Delta I_C V$$

Since $\Delta T = \theta P_C$

then $$\Delta T = \theta P_A + \theta VS \left(\frac{k \Delta T}{R_e + R_b} + I_{COA}(e^{\Delta T/K} - 1)\right) \qquad (4)$$

for $S \longrightarrow 1$ then ΔT will be small

If $\frac{\Delta T}{K} < 0.3$ then $e^{\Delta T/K} - 1 = \frac{\Delta T}{K}$

Making this substitution into Equation (4) gives the thermal equation

$$\Delta T = \frac{\theta P_A}{(1 - \theta VS (k/(R_e + R_b) + I_{COA}/ K)}$$

APPENDIX II

EXPERIMENTAL DATA AND RESULTS BY USING THE ASSUMPTION $h_{FE2} = h_{FE1} \cdot 2^{\Delta T/50}$

TYPE	E_{CC} VOLT	I_C AMP	θ_T OHM	I_{CBO} μA T= 18°C	K °C	h_{FE} T=18°C	$P_C\theta$ WATT	ΔT °C EXPER	ΔT °C THEOR	ERROR %
2N-2142	45	0.35	3.1	40	23	75	48.8	62.1	68.9	9.7
2N-2143	27	0.245	5.8	45	25.7	95	38.4	48.8	54.1	9.5
2N-2144	28	0.256	5.8	26	20	80	41.9	54.5	59.4	8.0
2N-2145	30	0.282	5.8	18	22.5	95	49	65.4	69.1	4.6

TABLE A-1

DATA AND RESULTS BY USING THE ASSUMPTION $h_{FE2}=h_{FE1} \cdot 2^{\Delta T/50}$ FOR TRANSISTORS 2N2142, 2N2143, 2N2144, 2N2145

TYPE	E_{CC} VOLT	I_C AMP	θ_T OHM	I_{CBO} µA T=18°C	K °C	h_{FE} T=18°C	$P_C\theta$ WATT	ΔT °C EXPER	ΔT °C THEOR	ERROR %
2N-1359	30	0.12	5.4	335	28	40	19.4	28.7	27.3	5.2
2N-1360	24	0.22	5.4	51	22.4	140	28.5	37.6	40.0	6.0
2N-1529	32	0.32	5.4	30	21.5	35	55.3	67.7	77.1	13.8
2N-1530	23	0.35	5.4	61	26.5	90	43.5	57.6	61.4	6.35

TABLE A-2

DATA AND RESULTS BY USING THE ASSUMPTION $h_{FE2} = h_{FE1} \cdot 2^{\Delta T/50}$ FOR TRANSISTORS 2N1359, 2N1360, 2N1529, 2N1530

APPENDIX III

EXPERIMENTAL RESULTS OF CHECKING THE ACCURACY OF EQUATION $h_{FE2} = h_{FE1} \cdot 2^{\Delta T/50}$

T °C	MA I_b	MA I_C	h_{FE}	NORMALIZED h_{FE}	$2^{\Delta T/50}$	DIFF.
40	0.748	115	154	1	1	0
50	0.745	121	162	1.05	1.14	0.09
60	0.730	139	191	1.25	1.32	0.07
70	0.730	153	210	1.36	1.49	0.13
80	0.715	183	257	1.67	1.82	0.15
90	0.690	207	299	1.94	2	0.06

Table A-3 Experimental data of short circuit current gain h_{FE} by using transistor 2N2145

$$\text{Standard Error} = \sqrt{\frac{(0.09)^2+(0.07)^2+(0.13)^2+(0.15)^2+(0.06)^2}{5}}$$

$$= \sqrt{\frac{0.0081 + 0.0049 + 0.0169 + 0.0225 + 0.0036}{5}}$$

$$= 11\ \%$$

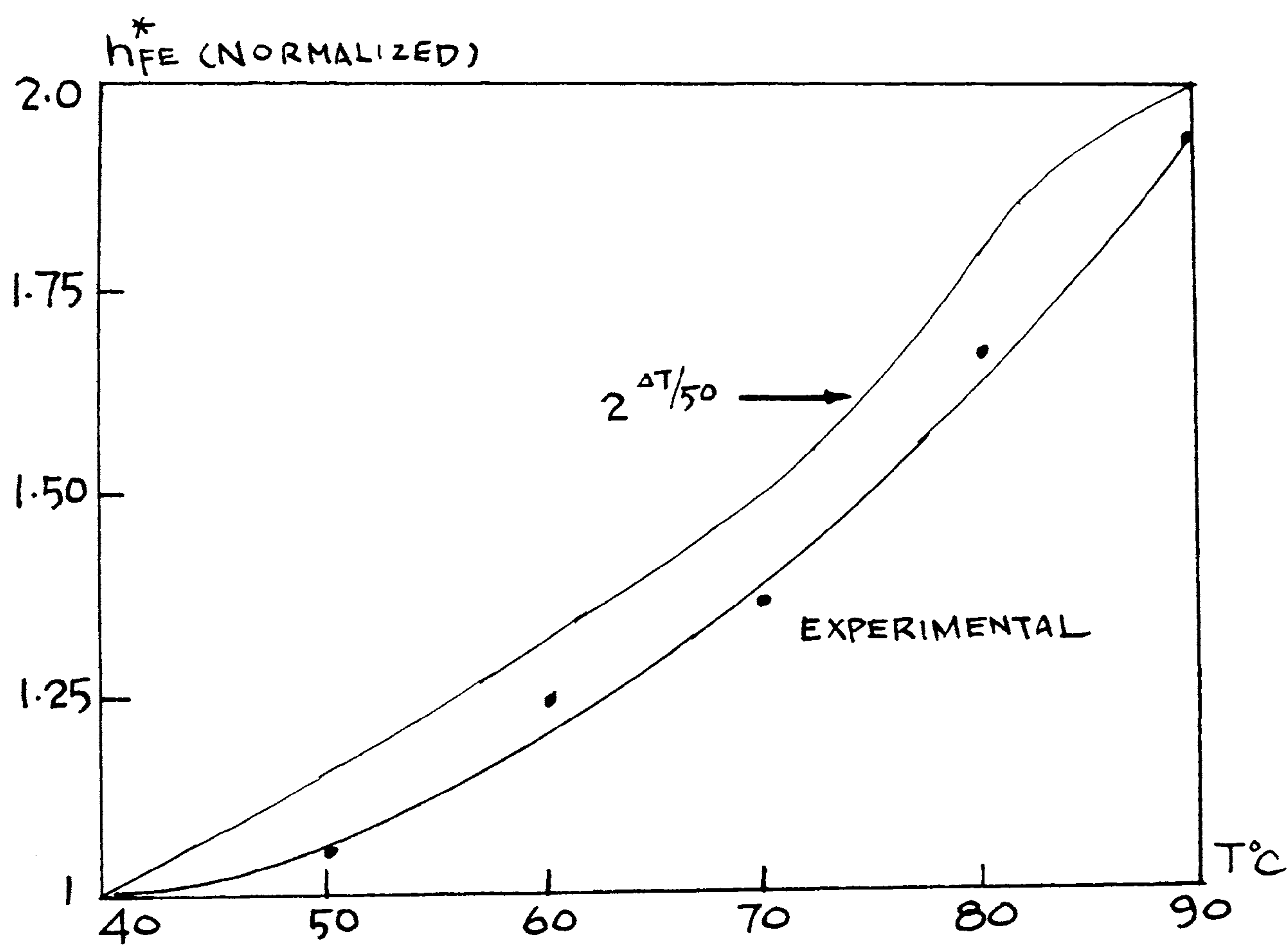


Figure A-1. Comparison of equation $h_{FE2} = h_{FE1} \cdot 2^{\Delta T/50}$ and experimental results.

APPENDIX IV

THE WATFOR PROGRAM FOR SOLVING THE NONLINEAR THERMAL EQUATION

```
    /WAT4  EE120171,TIME=1,PAGES=10  D                  JERRY H LEE
    C      EE120171    JERRY H LEE
    C      TRANSISTOR TYPE 2N2142,2N2143,2N2144,2N2145,2N1359,
    C      2N1360,2N1529,2N1530
 1         DIMENSION AK(10),B(10),E(10),P(10),CI(10),AI(10)
 2         F(X)=X-(PC+W*EXP(X/Q))/(1-AA)
 3         G(X)=(PC+W*EXP(X/Q))/(1-AA)
 4         READ(1,1) (E(I),I=1,8)
 5         READ(1,1) (P(I),I=1,8)
 6         READ(1,1) (B(I),I=1,8)
 7         READ(1,1) (AK(I),I=1,8)
 8         READ(1,1) (CI(I),I=1,8)
 9         READ(1,5) (AI(I),I=1,8)
10         READ(1,7) RE,RB,AKK
11       1 FORMAT(8F10.5)
12       5 FORMAT(8F10.6)
13       7 FORMAT(3F10.5)
14         DO 10 N=1,8
15         R=E(N)
16         RR=AI(N)
17         T=P(N)
18         WRITE(3,100) E(N),CI(N),AI(N),AK(N),P(N),B(N)
19     100 FORMAT(15X,6F14.7//)
20         A=B(N)/(1+B(N))
21         S=(RE+RB)/(RE+RB*(1-A))
22         W=E(N)*S*AI(N)*P(N)
23         AA=(A*E(N)*S*AKK*P(N))/(RE+RB)
24         PC=E(N)*CI(N)*P(N)
25         Q=AK(N)
26         BO=B(N)
```

```
    C       USING ITERATION METHOD TO SOLVE A NONLINEAR EQ.
    C       CHOOSING AN INITIAL VALUE
27          X=40.
28          Y=F(X)
29          DO 30 M=1,150
30          X1=G(X)
31          Y=F(X1)
32          IF(ABS(X)-X) .LT. 1.E-3) GO TO 20
33       30 X=X1
34       20 WRITE(3,200) PC,X1
35      200 FORMAT(15X,'COLL DISS='F14.7,3X,'JUNC TEMP(EXPER)='
           1F14.7//)
36       10 CONTINUE
37          STOP
38          AND
```

VITA

The author was born on October 2, 1943, in Kan-su, China. He received his primary and high school education in Taipei, Taiwan, China. He received his college education in National Taiwan University, Taiwan, China, and obtained a B.S. degree in Electrical Engineering in June 1965. He came to the United States in October 1966 and enrolled in the Graduate School of The University of Missouri at Rolla in January, 1967.

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