Improved Harmonic Performance of Seven-level CHB Inverter using Multicarrier Modulation and Varying Modulation Index

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***Abstract*— This paper proposed the design of a multicarrier modulation with symmetrical voltage input of a single phase seven-level cascaded H-Bridge multilevel inverter (CHBI). The selection of the topology is mainly due to the easy implementation as well as presence of lesser components. The simulation design of the inverter is done by using MATLAB Simulink. The modulation control technique for the power switches of the inverter is the multicarrier PWM technique which focuses specifically on PD technique. The modulation index is varied and the results are measured in terms of THD. The results obtained are analyzed and discussed in this article. The results indicate that the THD is decreasing for increasing values of modulation index.**

***Index Terms*— Cascaded H-Bridge; Multicarrier; Multilevel Inverter; Pulse Width Modulation.**

I. INTRODUCTION

Industrial applications which uses medium voltage and high power applications had dramatically increased in recent decades, thus power converters such as inverters are vastly utilized to produce to desired voltage and power requirements. Inverters, in power electronics, are devices that can convert Direct Current (DC) to Alternating Current (AC). Using the basis of inverter circuitry, the first model of multilevel inverter was constructed in the late 1975. The "multilevel" term is closely related to the stepped voltage generated at the output waveform. Generally, multilevel inverters as power electronic systems are aimed to generate a sinusoidal voltage output from a number of DC sources. The DC sources can be batteries, fuel cell, solar cells, ultra-capacitors and etc. [1]. Reducing the harmonic components from the generated output waveform is the primary advantage of the multilevel inverters. The harmonic distortion of the sinusoidal output waveform will further decrease with increasing levels of stepped voltage. Nowadays, pulse width modulation is amongst the popular choices for control strategy in the field of modern power electronics [1-3].

The application of multilevel inverter compared to the conventional two-level inverter in the medium and high voltage grid are increasing over the years due to the numerous advantage provided by the multilevel inverter such as CHBI. The main advantage offered by the multilevel inverter is the increasing number of n levels which enables the generation of higher voltage levels as well as further reduce the harmonic distortion in the output voltage and current. Therefore, the multilevel inverter produces lower THD in terms of performance. Besides that, the semiconductor power device for multilevel inverters operates at a relatively lower switching frequency resulting in the reduction of switching losses. Moreover, the lower switching frequency of the multilevel inverter such as CHBI ensures that the switching action of the semiconductor device is at a lower rate in order to reduce the voltage change rate, dv/dt stress. When the dv/dt stress reduces, the electromagnetic interference (EMI) or electromagnetic compatibility (EMC) issues will also be lessen [4-6].

II. MULTILEVEL INVERTER

A. *Cascaded H-Bridge Inverter (CHBI)*

The Cascaded H-Bridge Inverter (CHBI) topology as shown in Figure 1, unlike other topologies, consists of a cascade of low voltage single phase H-bridge inverters connected in series [3]. Each of the single phase H-bridges comprises of an independent and isolated DC source where the CHBI will be categorized as symmetrical if the DC sources are of the same voltage values and asymmetrical if the DC sources are of different voltage values [7]. For symmetrical CHBI, the output level can be defined by Eq. 1:

$$\text{Output level, } m = 2N + 1 \quad (1)$$

Where N is the number of single phase H-bridge units in the CHBI topology.

Three different levels of output voltage can be generated by each individual single phase H-bridges which is $+V_{dc}$, 0 or $-V_{dc}$. The generation of the output voltage levels is based on the proper switching combinations of switches S1 - S4.

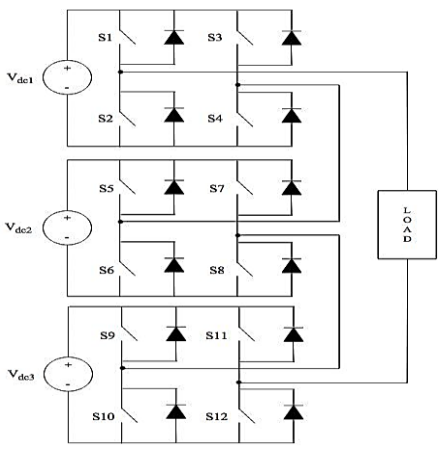


Figure 1: Seven-Level CHBI Topology

Switches S1 and S4 are turned on to produce the output voltage of $+V_{dc1}$ while the switches S2 and S3 are turned on to generate $-V_{dc1}$ output voltage. In order to yield 0V output, either pair switches S1 and S3 or S2 and S4 are turned on simultaneously. For the seven-level CHBI, since the individual H-bridges are connected in series for the same phase, therefore the synthesized AC output voltage is the sum of the individual H-bridge converter output and can be represented by the mathematical equation, Eq 2. [4-6]:

$$V_{O,AC} = V_{O,1} + V_{O,2} + V_{O,3} \quad (2)$$

Where: $V_{O,1}$ is the output voltage of the first H-bridge unit with DC source V_{dc1};
$V_{O,2}$ is the output voltage of the second H-bridge unit with DC source V_{dc2};
$V_{O,3}$ is the output voltage of the third H-bridge unit with DC source V_{dc3}

Hence, the possible voltage outputs for the seven-level cascaded H-bridge inverter are $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$ and $-3V_{dc}$. The switching states of switches and the predicted stages-output waveform are shown in Table 1 and Figure 2 respectively.

Table 1
Switching States of Switches

S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Output Voltage
0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	1	0	0	1	V_{DC}
0	1	0	1	1	0	0	1	1	0	0	1	$2V_{DC}$
1	0	0	1	1	0	0	1	1	0	0	1	$3V_{DC}$
0	1	0	1	1	0	0	1	1	0	0	1	$2V_{DC}$
0	1	0	1	0	1	0	1	1	0	0	1	V_{DC}
0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	1	0	$-V_{DC}$
1	0	0	1	0	1	1	0	0	1	1	0	$-2V_{DC}$
0	1	1	0	0	1	1	0	0	1	1	0	$-3V_{DC}$
1	0	0	1	0	1	1	0	0	1	1	0	$-2V_{DC}$
0	1	0	1	0	1	0	1	0	1	1	0	$-V_{DC}$
0	1	0	1	0	1	0	1	0	1	0	1	0

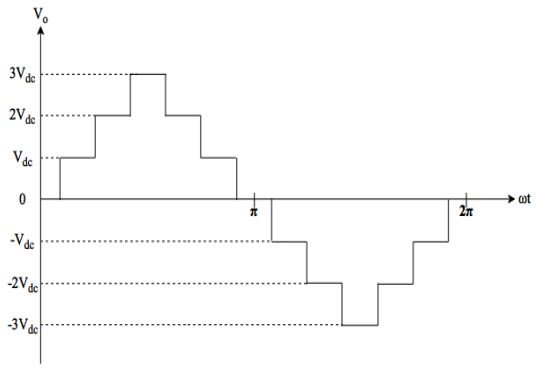


Figure 2: Output Voltage Waveform for Single Phase Seven-Level CHBI

B. *Pulse Width Modulation (PWM)*

The multicarrier PWM technique utilizes the comparison of a single sinusoidal reference or modulating signal with multiple high switching frequency carrier signals obtained through disposition or shifting. The frequency of the reference signal is usually significantly lower than the carrier signal [6]. In general, the number of carrier signals needed for the multicarrier PWM follows the expression of (m-1) where m represents the level of the multilevel inverter. Multicarrier PWM can be categorized into two types [3] mainly known as phase-shifted modulation and level-shifted modulation. The level-shifted modulation can be further divided into three types namely Phase Disposition (PD), Phase Opposition Disposition (POD) and Alternate Phase Opposition Disposition (APOD). Figure 3 shows the (m-1) carrier signal waveforms for the PD PWM method.

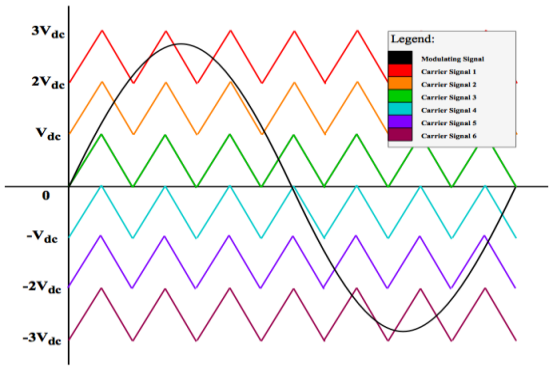


Figure 3: PD PWM with (m-1) Carrier Signal Waveforms

C. *Harmonic Distortion*

The Total Harmonic Distortion (THD) is the summation of the harmonic distortions due to the distortion factor and can be used to define voltages or currents. The quality of the waveform produced can be calculated and expressed in terms of THD [3] as shown in the Eq. 3.

$$THD_v = \frac{\sqrt{\sum_{n=2}^{\infty}(V_{n,RMS})^2}}{V_{1,RMS}} \quad (3)$$

Where: $V_{n,rms}$ is the RMS voltage of the n^{th} harmonic component;
$V_{1,rms}$ is the RMS voltage of the fundamental frequency.

III. Proposed Method - Multicarrier Pulse Width Modulation

This paper used PD modulation method, where the carrier signal is offset vertically. The carrier signal is offset such that all (m-1) carrier signals are in phase to each other. The proposed method is divided into the inverter model and the modulation model as shown in Figure 4 and Figure 5. The seven-level CHBI utilizes isolated and symmetrical DC power sources. The power device used for the simulated inverter model is the Metal Oxide Semiconductor Field Effect Transistor. (MOSFET). The simulation parameters are such that each DC power sources are of 100V (Vdc1=Vdc2=Vdc3=100V) and the load which consists of resistive and inductive components which are of 15 Ω and 0.8 H respectively (R= 15 Ω and L= 0.8 H).

IV. SIMULATION RESULTS

The generated gate pulse, the output voltage and the harmonic performance of the inverter are verified using the FFT analysis, which is shown in Figure 6. The generated gate pulse is shown for the positive cycle in Figure 6(a) while the output voltage corresponding to the switching sequence is shown in Figure 6(b). The percentage THD for the seven-level CHB inverter is obtained using FFT analysis and is plotted with voltage magnitude of harmonic components (Mag) against harmonic order as shown in Figure 6(c).

A. Improved Harmonic Performance at Different Modulation Indices

The modulation index, M_a, is then varied (by altering the amplitude of the modulating sine wave) for every interval of 0.1 (0.1 to 1.0). For every 0.1 modulation index, the harmonic performance and the output voltage of the seven-level CHBI is analyzed and the results are tabulated in Table 2. Table 2 indicates that the percentage THD of the inverter decreases for increasing M_a. The relationship between the M_a and percentage THD is plotted using line of best-fit and is illustrated in Figure 7. The output voltage level also indicates changes from three-level to seven-level as the M_a increases. The percentage THD and voltage levels for modulation index 0.3 and 0.7 are illustrated in Figure 8.

Table 2
Harmonic Performance and Output Voltage Level by Varying the Modulation index

M_a	A_m	A_c	THD (%)	Voltage Level
1.00	6.00	1	18.11	Seven levels
0.90	5.40	1	22.84	
0.80	4.80	1	24.37	
0.70	4.20	1	24.01	
0.60	3.60	1	33.04	Five levels
0.50	3.00	1	39.96	
0.40	2.40	1	44.27	
0.30	1.80	1	69.51	Three levels
0.20	1.20	1	102.99	
0.10	0.60	1	211.07	

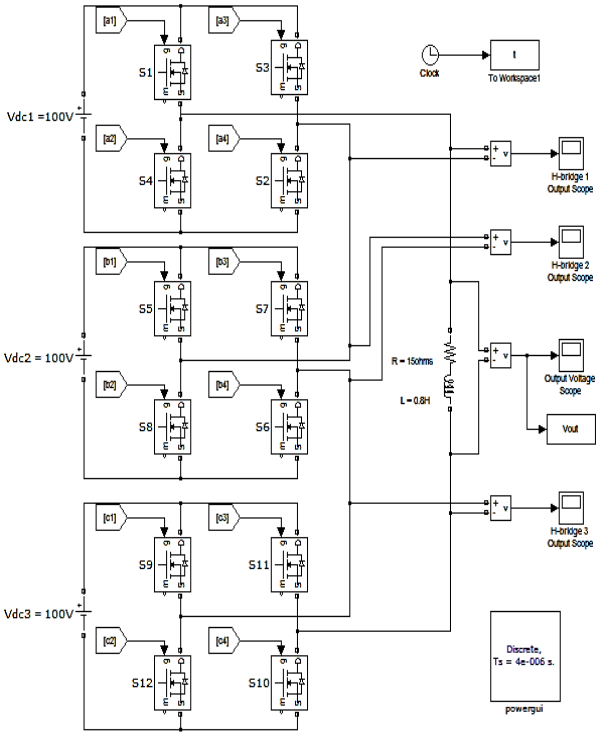


Figure 4: Proposed Inverter Model

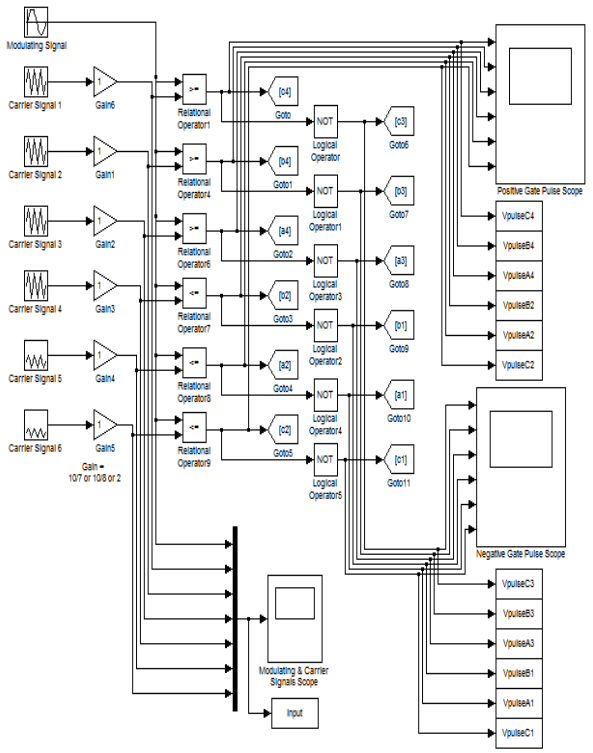
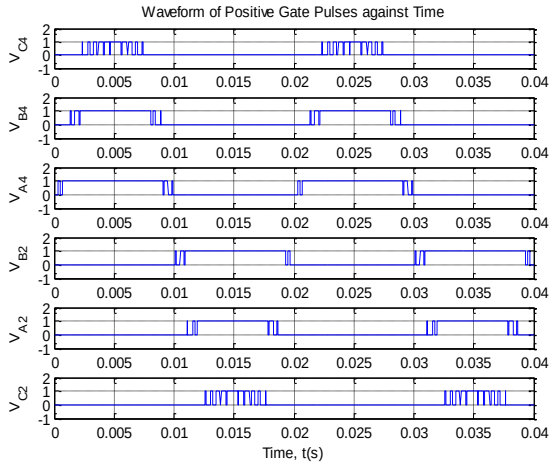
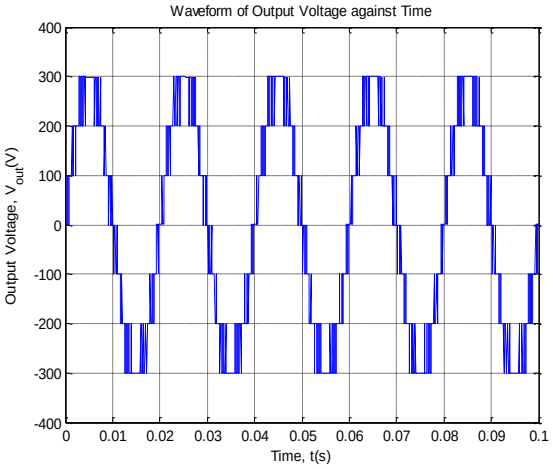


Figure 5: Proposed Multicarrier PD PWM Generation



(a)



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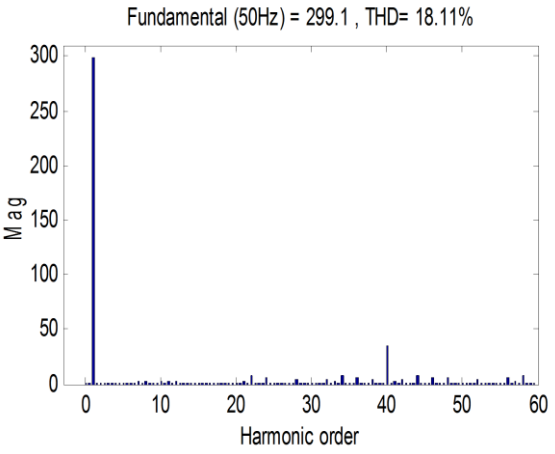


(c)

Figure 6: Output for 7-level CHB Inverter: (a) Gate Pulse Generation, (b) Stages of output Voltage, and (c) Harmonic presents using FFT Analysis

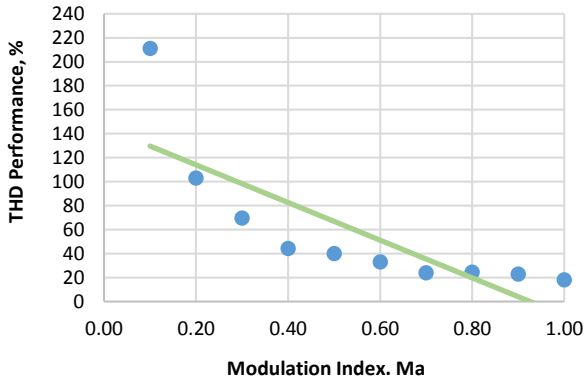
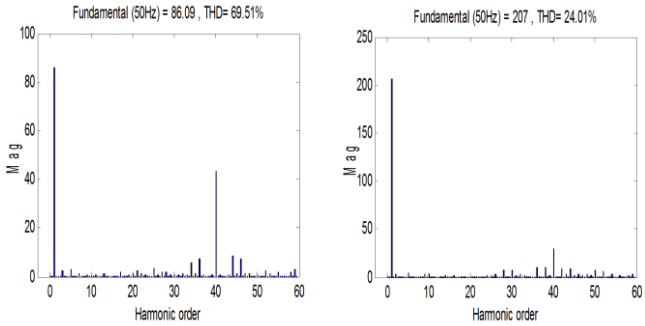
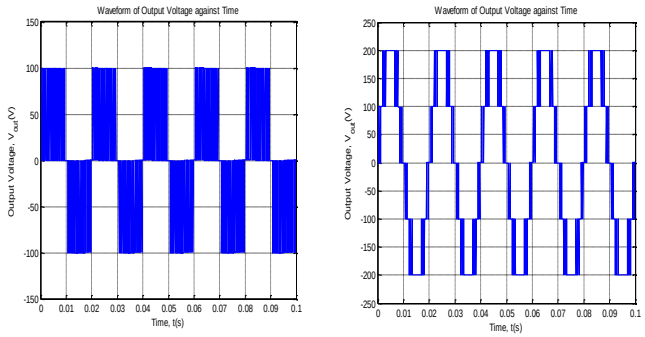


Figure 7: Relationship Trend between harmonic presents and modulation index using line of best fit.



(a)



(b)

Figure 8: Simulation results for Ma = 0.3 and Ma = 0.7 for: (a) Harmonic performance using FFT analysis (b) Stages of Output Voltage

V. CONCLUSION

On the whole, this paper was successfully described the fundamentals of the seven-level CHBI inverter. The CHBI topology exhibits various advantages including the modular structure as well as easy implementation despite the requirement of additional isolated DC supply for each H-bridge unit. The modulation technique selected in the simulation of the seven-level CHBI is the multicarrier PWM technique specifically the PD PWM control technique. The reduction of THD is inversely proportional to the number of level of the multilevel inverter. The analysis from the simulation reveals that the varying of modulation index from 0.1 to 1.0 will result in the reduction of THD as well as the change in output voltage levels.

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