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A comparative study of capacitor voltage balancing techniques for flying capacitor multi-level power electronic converters

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Department:

A COMPARATIVE STUDY OF CAPACITOR VOLTAGE BALANCING TECHNIQUES FOR FLYING CAPACITOR MULTI-LEVEL POWER ELECTRONIC CONVERTERS

by

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ABSTRACT

With the advent of multilevel converters for high power applications in industry, a need to develop simpler topologies and control techniques has arisen. The flying capacitor multilevel inverter (FCMLI) is one such topology which is gaining popularity in recent years with many advantages such as extra ride-through capabilities because of the capacitor storage, redundancy in switching states, low common mode voltage ratio, improved power quality, etc. In this thesis, different basic multilevel converter topologies and their advantages and applications are discussed. The thesis mainly focuses on single-phase five-level FCMLI topology. Different control techniques for capacitor voltage regulation like staircase modulation, and PWM techniques including phase disposition PWM (PDPWM), and natural balancing technique are implemented. The disadvantages of these methods are discussed. To overcome these, a new method called the split natural balancing technique which is based on the Unipolar PWM method is proposed in this thesis. In addition, a feedback control technique called amplitude modulation adjustment (AMA) method is devised to regulate the voltage across capacitors around the desired value irrespective of their initial values. Harmonic analysis of the output voltage for all the implemented methods is performed and compared.

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NOMENCLATURE

Symbol	Description
V_{dc}	Input dc voltage
S_{a1}	Switch 1 on leg *a*
S_{a1}'	Complementary switch to switch S_{a1} on leg *a*
S_{a2}	Switch 2 on leg *a*
S_{a2}'	Complementary switch to switch S_{a2} on leg *a*
S_{b1}	Switch 1 on leg *b*
S_{b1}'	Complementary switch to switch S_{b1} on leg *b*
S_{b2}	Switch 2 on leg *b*
S_{b2}'	Complementary switch to switch S_{b2} on leg *b*
V_{ca}	Voltage across the capacitor C_a on leg *a*
V_{cb}	Voltage across the capacitor C_b on leg *b*
V_{ag}	Voltage on leg *a*
V_{bg}	Voltage on leg *b*
V_{ab}	Output voltage across the RL load
i_{load}	Current through the RL load
i_{ca}	Current through the capacitor C_a
i_{cb}	Current through the capacitor C_b
p	Ratio of input dc voltage to the capacitor voltage
θ	Firing angle
M	Modulation index (ratio of amplitude of fundamental component of output voltage to the input voltage
P	Output power

Φ	Power factor angle
f_c	Carrier frequency
f_{ref}	Reference frequency
m_f	Frequency modulation index (ratio of carrier frequency to reference frequency)
m_a	Amplitude modulation index (ratio of reference peak to peak amplitude to dc source voltage)
N	Number of pairs of complementary switches per leg
m_{csi}	Amplitude of carrier signal i
m_{ref}	Reference amplitude
k_i	Factor by which the amplitude of carrier signal '*i*' is changed (ratio of carrier signal amplitude to reference amplitude)

1. INTRODUCTION

1.1 BASIC CONCEPT

The need for high power apparatus in industry has increased in recent years. Multilevel converters have developed as easy alternatives for such power requirements [1-4]. Mostly used in medium voltage applications, multilevel converters have gained prominence since it is not feasible to connect a single power semiconductor switch directly to the grid. There are other advantages of multilevel converters such as their capability to be easily interfaced with the renewable energy sources such as solar power, wind power, and fuel cells [5, 6].

Multilevel converters consist of a group of semiconductor switches, like IGBTs, and a set of voltage source components like capacitors or independent sources. The basic concept of these converters depends on using this series of switches and sources to synthesize a stepped or staircase output voltage waveform. Therefore, they reduce the voltage stress on each device or component used [7]. Multilevel converters play a significant role in enhancing the quality of high power distribution networks, power conditioning systems, variable speed drive systems etc because of the availability of higher number of voltage levels at the output. This helps in reducing the size of switching components which can be operated at lower switching frequencies [8].

However, multilevel converters have their own disadvantages. Voltage sharing may not be as desired under all conditions because of the series connection of the switching devices.

1.2 MULTILEVEL POWER ELECTRONIC TOPOLOGIES

The number of switches in a multilevel converter depends on the number of voltage levels required in the output. Based on the arrangement of switches and passive sources, there are four basic types of multilevel converter topologies [9-11]. They are:

i) Diode-Clamped

ii) Cascaded H-Bridge Cell

iii) Flying Capacitor

iv) Switched Capacitor

1.2.1. Diode-Clamped Multilevel Inverters. Diode-clamped inverters are one of the earliest designed topologies of multilevel inverters [12-14]. Figure 1.1 shows a single-phase five-level diode-clamped inverter. The two capacitors connected in the circuit split input voltage V_{dc} to obtain the midpoint voltage of the input. In a three level topology, the common point of capacitors is connected to the ground. Therefore, this circuit can also be called the neutral point clamped inverter. Diodes D_1 and D_2 present in the circuit help with clamping dc voltage V_{dc} to obtain different output voltage levels. There are nine allowable switching states for the given circuit to obtain five different output voltage levels $+V_{dc}$, $+V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$ [5] as shown in Table 1.1. It has to be noted that switch pairs S_{a1} and S_{a1}', and S_{a2} and S_{a2}' are complementary to each other. Similarly, switch pairs S_{b1} and S_{b1}', and S_{b2} and S_{b2}' are complementary to each other.

The number of switches, capacitors, and diodes required in the circuit increases with the number of output voltage levels desired. For every additional level of voltage, it requires an extra pair of complementary switches is required in each limb of the circuit and also additional capacitors and clamping diodes. However, in such cases, voltage

balancing of the capacitors and the cost of diodes become a practical problem [8]. Another disadvantage of diode-clamped multilevel inverters is that they need high voltage rating diodes to block the reverse voltages [9].

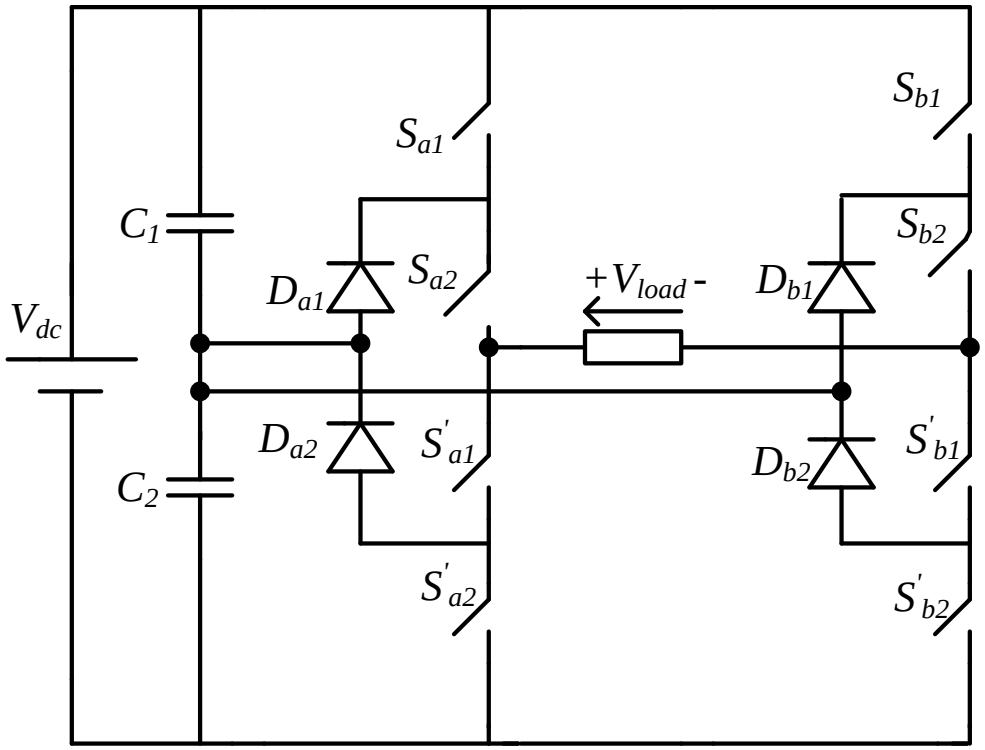


Fig. 1.1. Five-level diode-clamped inverter

Table 1.1
Possible switching states for the diode-clamped inverter

S_{a1}	S_{a2}	S_{a1}'	S_{a2}'	S_{b1}	S_{b2}	S_{b1}'	S_{b2}'	V_{load}
0	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	0	0
1	1	0	0	1	1	0	0	0
0	1	1	0	0	0	1	1	$+V_{dc}/2$
1	1	0	0	0	1	1	0	$+V_{dc}/2$
1	1	0	0	1	1	0	0	$+V_{dc}$
0	1	1	0	1	1	0	0	$-V_{dc}/2$
0	0	1	1	0	1	1	0	$-V_{dc}/2$
0	0	1	1	1	1	0	0	$-V_{dc}$

1.2.2. Cascaded H-Bridge Cell Multilevel Inverters. Cascaded H-bridge cell multilevel inverter topology [15-17] is a series connection of two or more individual full-bridge inverters. Figure 1.2 shows a single-phase, five-level cascaded H-bridge cell inverter realized by connecting two three level conventional full bridge inverters in series. Switch pairs S_{a1} and S_{a1}', and S_{a2} and S_{a2}' are complementary to each other. Similarly, switch pairs of the other full bridge inverter S_{b1} and S_{b1}', and S_{b2} and S_{b2}' are complementary to each other. The switching states are as shown in Table 1.2. The different voltage levels that can be obtained at the output terminals are $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, $-2V_{dc}$. If the dc voltage sources in both the inverter circuits connected in series are not equal to each other, then nine levels can be obtained at the output terminals. The

number of levels in the output voltage can be increased by two by adding an identical inverter in series.

Cascaded H-bridge cell inverters use the least number of power electronic devices when compared to any other topology. However, they require isolated power sources in each cell which in turn requires a large isolating transformer [8].

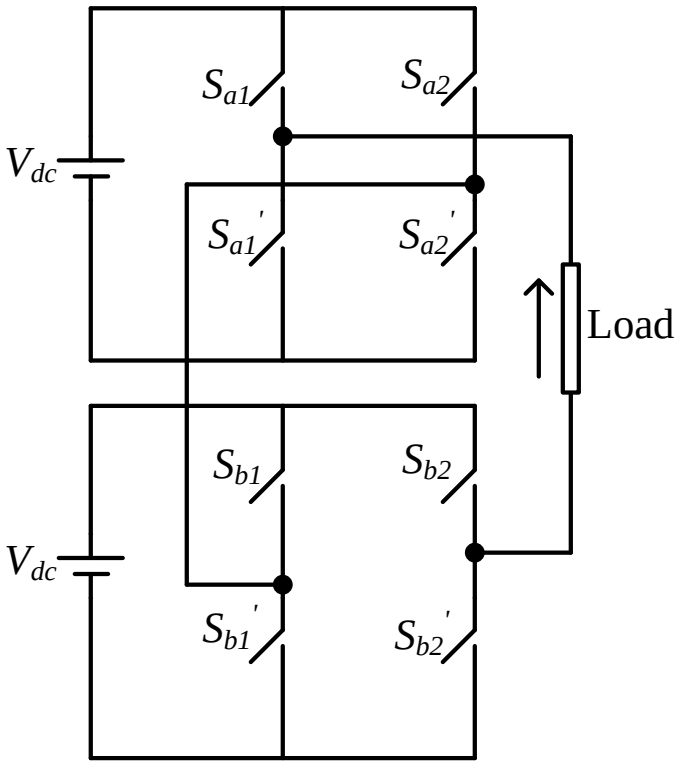


Fig. 1.2. Five-level cascaded H-bridge-cell inverter

Table 1.2
Possible switching states for cascaded H-bridge cell inverter

S_{a1}	S_{a2}	S_{a1}'	S_{a2}'	S_{b1}	S_{b2}	S_{b1}'	S_{b2}'	V_{load}
1	0	0	1	0	1	1	0	0
1	0	1	0	1	0	1	0	0
1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	0	1	0
1	0	0	1	1	0	1	0	$+V_{dc}$
1	0	0	1	0	1	0	1	$+V_{dc}$
1	0	1	0	1	0	0	1	$+V_{dc}$
0	1	0	1	1	0	0	1	$+V_{dc}$
1	0	0	1	1	0	0	1	$+2V_{dc}$
0	1	1	0	1	0	1	0	$-V_{dc}$
0	1	1	0	0	1	0	1	$-V_{dc}$
1	0	1	0	0	1	1	0	$-V_{dc}$
0	1	0	1	0	1	1	0	$-V_{dc}$
0	1	1	0	0	1	1	0	$-2V_{dc}$

1.2.3. Flying Capacitor Multilevel Inverters. The diodes in the diode-clamped topology can be replaced by clamping capacitors or floating capacitors to clamp the voltages. Such a topology is called flying capacitor multilevel inverter (FCMLI). FCMLI topologies are relatively new compared to the diode-clamped or the cascaded H-bridge

cell inverter topologies [18, 73]. Redundancy in the switching states is available by using flying capacitors instead of clamping diodes. This redundancy can be used to regulate the capacitor voltages and obtain the same desired level of voltage at the output [19]. Figure 1.3 shows a single-phase five-level FCMLI topology. The voltage across the capacitors is considered to be half of Dc source voltage V_{dc}. The output voltage consists of five different voltage levels + V_{dc}, V_{dc}/2, 0, -V_{dc}/2, and - V_{dc}. Similar to the other multilevel converter topologies, FCMLI also has complementary switch pairs. In the present considered circuit, switches S_{a1} & $S_{a1}^{'}$, and S_{a2} & $S_{a2}^{'}$ are complementary to each other. Similarly on the other limb, switches S_{b1} & $S_{b1}^{'}$, and S_{b2} & $S_{b2}^{'}$ are complementary to each other. The switching states available for such a topology are higher than that of the diode-clamped which can be observed from Table 1.3. The number of voltage levels at the output can be increased by adding a pair of complementary switches and a capacitor. However, all the capacitors used in such topologies must be rated identically which can prove to be expensive and bulky in size.

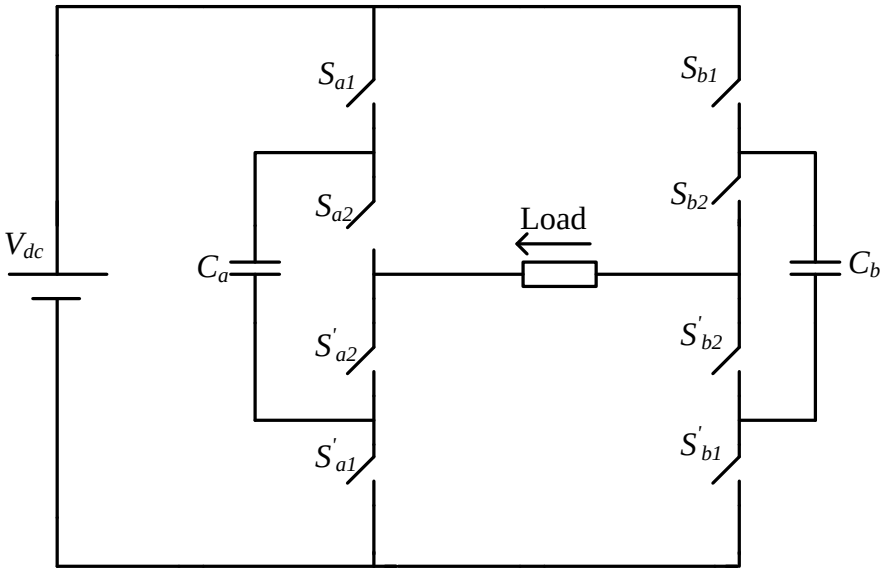


Fig. 1.3. Single-phase five-level FCMLI topology

Table 1.3.
Possible switching states for FCMLI topology

S_{a1}	S_{a2}	S_{a1}'	S_{a2}'	S_{b1}	S_{b2}	S_{b1}'	S_{b2}'	V_{load}
1	1	0	0	1	1	0	0	0
1	0	1	0	1	0	1	0	0
1	0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	0	0
0	1	0	1	0	1	0	1	0
0	0	1	1	0	0	1	1	0
1	1	0	0	1	0	1	0	$+V_{dc}/2$
1	1	0	0	0	1	0	1	$+V_{dc}/2$
1	0	1	0	0	0	1	1	$+V_{dc}/2$
0	1	0	1	0	0	1	1	$+V_{dc}/2$
1	1	0	0	0	0	1	1	$+V_{dc}$
1	0	1	0	1	1	0	0	$-V_{dc}/2$
0	1	0	1	1	1	0	0	$-V_{dc}/2$
0	0	1	1	0	1	0	1	$-V_{dc}/2$
0	0	1	1	1	0	1	0	$-V_{dc}/2$
0	0	1	1	1	1	0	0	$-V_{dc}$

The major challenge in the flying capacitor multilevel inverter topologies is the voltage regulation across the capacitors. The switching states and the polarity of load current cause the capacitors either to charge or discharge since the current can flow

through more than one capacitor. Therefore, the appropriate selection of switching states becomes a priority in FCMLI topologies.

1.2.4. Comparison of Different Multilevel Topologies. Table 1.4 shows the basic comparison of various aspects of different multilevel topologies discussed above. It can be observed that for obtaining the same number of levels of voltage at the output, different topologies need different number of sources, diodes, capacitors etc. Other parameters like cost and size of components depend on their rating and requirement. Suitability of topology is mostly application oriented.

Table 1.4
Comparison between various multilevel topologies

Topology / Aspect	Diode-clamped Multilevel	Cascaded H-bridge Cell Multilevel	Flying Capacitor Multilevel
No. of Voltage Levels at the Output	5	5	5
No. of Switches	8	8	8
No. of Sources	1	2	1
No. of Capacitors	2	None	2
No. of Clamping Diodes	4	None	None
No. of Possible Switching States	9	16	16

More topologies of multilevel inverters can be developed as a combination of one or more of the above mentioned topologies. For example, in [20] F. Z. Peng claims to have developed a generalized multilevel inverter which uses capacitors and diodes in a

cascaded H-bridge topology. Many other topologies can be derived from such a topology. Figure 1.4 shows the five-level topology of such a generalized multilevel inverter. Such a topology can also be called as a switched capacitor multilevel converter. In this topology, it can be observed that when switches S_{b1} and S_{b3} are turned ON, capacitor C_{a1} is in parallel to capacitor C_{b1} when switches S_{b2} and S_{b4} are turned ON, then capacitor C_{a1} is in parallel to capacitor C_{b2}. So, the output available at the terminals of leg *b* can be a combination of the sum of capacitor voltages C_{a1}, C_{b1}, and C_{b2}. This topology proves to possess more efficient self balancing capabilities than the other conventional topologies.

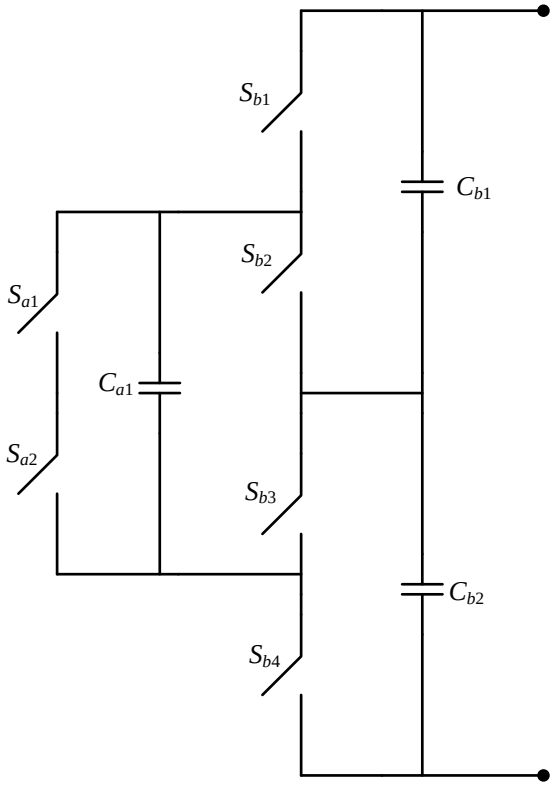


Fig. 1.4. Five-level generalized multilevel topology

Yet another multilevel topology can be a mixed-level hybrid multilevel converter [21-25]. The full-bridge inverters in a cascaded H-bridge cell inverter can be replaced by diode-clamped or flying capacitor inverters. Such a topology can help in decreasing the number of individual dc voltage sources required in the inverter topology. However, control of such an inverter topology may be difficult because of its mixed-level hybrid structure. As it includes different multilevel inverter topologies incorporated as individual cells of cascaded inverters [5]. An example of a simple hybrid multilevel inverter topology can be shown as a block diagram in Fig. 1.5. It shows an N-level cascaded H-bridge cell multilevel inverter connected in series with an N-level diode-clamped multilevel inverter.

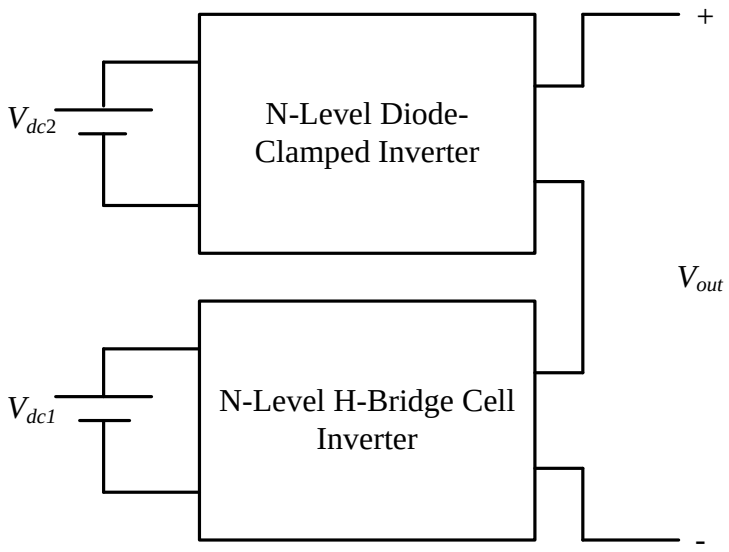


Fig. 1.5. Example for a hybrid multilevel inverter topology

1.3 ADVANTAGES OF MULTILEVEL INVERTERS

The most important aspect of multilevel inverters becomes their ability to produce different levels of output voltage which can be synthesized as a sine waveform. The need for higher power rated switches can be eliminated by using the existing switches in a multilevel topology. The power quality is improved because of the increased number of voltage levels at the output. The common mode voltage is lower in multilevel inverters; therefore, they reduce the stress on the bearings of the motor that is connected to them. In fact, with more advanced control techniques as in [26], the common mode voltage can be completely eliminated in multilevel inverters. Other advantages of multilevel inverters include higher voltage capability, improved electromagnetic compatibility, lower switching losses etc. Specific advantages of different multilevel inverter topologies [9] can be stated as follows:

Diode-clamped inverters:

a) Filters can be avoided because of the increase in the number of voltage levels which reduces the harmonic content of the waveform.

b) As the devices are all operated at fundamental frequency, efficiency of the circuit is high.

c) Easy control

Cascaded H-bridge cell inverters:

a) To obtain the same number of voltage levels at the output terminals, cascaded H-bridge cell inverters require the lowest number of components.

b) Absence of clamping diodes and capacitors allows modularizing the circuit layout.

c) Compatibility to soft switching avoids the usage of bulky snubber circuits which also reduces the losses.

Flying capacitor inverters:

a) Extra ride through capabilities during power outages is possible because of the presence of storage capacitors.

b) Redundancy in the switching states is available which helps in regulating the capacitor voltages.

c) As the number of the levels is increased, filters can be avoided due to low harmonic contents.

1.4. APPLICATIONS OF MULTILEVEL INVERTERS

Several advantages of multilevel inverters as described above make them very promising alternatives in high power and medium voltage applications in industry. Several papers [2, 4, 26, 27] discuss about various industrial applications of multilevel inverters such as input choppers for T13 locomotives in many European countries, medium voltage drives, and adjustable speed drives etc.

Multilevel inverters are becoming popular because of their capability to operate at lower frequencies and therefore, at higher efficiencies. Multilevel inverters also find applications in renewable energy systems [6, 28-32] like fuel cell utilizations, photovoltaic systems, and wind power generation etc for interface with the grid.

Multilevel inverters are also used in aerospace applications where high frequency and low total harmonic distortion (THD) operation is desired. [33] compares the losses in

one such aerospace application and it is observed that there is almost 40% benefit in the losses when an inverter with higher number of voltage levels is used.

An autonomous power generator with diesel engine and permanent magnet synchronous generator which makes use of multilevel inverters is reported in [34]. Usage of multilevel inverters makes the system capable of operating with asymmetrical and non linear three-phase loads.

The next important application of multilevel inverters becomes power conditioning systems [35]. Power conditioning systems are required in almost all renewable energy systems to provide interface with the utility and also to match the characteristics of sources and loads [36]. [37] reports a diode-clamped multilevel inverter connected to the electrical distribution system. This improves the system's ability to control the current demanded and the voltage required to be supplied to the utility and customer respectively. Furthermore, it makes the conditioning system applicable to higher voltage and power levels avoiding the use of bulky transformers.

Applications of multilevel inverters have been extended to low voltage systems as well due to their lower losses and THD. These and reduced voltage derivative dv/dt make them applicable in uninterruptable power supplies (UPS). [38] discusses one such UPS application where a three-level and two four-level multilevel inverters are analyzed and compared for the same purpose.

Most of the major applications of multilevel inverters rest in electric drive systems [17, 26, 39, 40]. These are used in various high speed and voltage traction systems [40-42]. The next area where multilevel inverters are gaining prominence is high power applications like FACTS [3, 43]. Different topologies of multilevel inverters prove

to be more efficient in different applications. For example, cascaded cell multilevel inverters are more used in static compensators (STATCOMs) [44-46] because of their advantages like lower losses, modularity and easier charge balancing techniques. However, diode-clamped and flying capacitor multilevel inverters also proved to be efficient in STATCOM applications because of their larger operating range [47-49]. Diode-clamped inverters are found to be capable in grid connection systems for renewable energy systems [6, 29]. Flying capacitor multilevel inverters find their applications in unified power flow controllers (UPFCs) [50], series and shunt compensation circuits for transmission and distribution systems [51-53], direct torque control (DTC) drives [54] etc because of their various advantages. Diode-clamped inverters are also used in UPFCs [55].

It has to be noted that any multilevel topology may be used in most of these applications though a particular topology might prove to be more efficient for a particular application. Other applications of multilevel inverters include active filters (AFs) [56, 57], dynamic voltage restorers (DVRs), utility adaptors [3], static VAR generators for reactive power control [45, 47], electric vehicle applications [58] and many other medium voltage, high power applications.

1.5. MODULATION AND CONTROL STRATEGIES

Next important thing in multilevel inverters becomes modulation and control strategies for various topologies. Most of these techniques developed may be used as common control methods for any appropriate topology.

To avoid efficiency losses and high switch power dissipation, most of the power electronic converters operate in the switched mode where the switch is either turned OFF, conducting zero current or turned ON, where there is a minimum voltage drop across it. Therefore, power flow control in converters is done by switching between these two transitional states [59].

Several of these controlling strategies are developed from pulse width modulation (PWM) techniques like the phase-shifted PWM, phase-disposition PWM, space vector modulation, etc [36, 60-63]. However, there are other controlling strategies which make use of the redundancy in switching states, delta modulation etc for generating the switching patterns in multilevel inverters [64, 65]. Next sections of this thesis discuss about such modulation and controlling techniques for a single-phase, five-level flying capacitor multilevel inverter modeled as in Fig. 1.3.

1.6. THESIS ORGANIZATION

In this thesis, the concept of multilevel inverters, their basic topologies and applications have been discussed. One such topology, the single-phase five-level flying capacitor multilevel inverter is focused on. Section 2 explains its operation as a seven-level topology with no redundancy and the disadvantages of implementing it in such a mode. To overcome the disadvantages and for availability of redundancy in switching states, the FCMLI considered is operated as a five-level topology in Section 3. It also discusses the staircase modulation technique for capacitor voltage regulation. There are several drawbacks with staircase modulation technique. These are mentioned and the need for simpler techniques as phase disposition sinusoidal PWM and phase shifted

sinusoidal PWM are discussed in Section 4. Section 5 of the thesis discusses the proposed split natural balancing technique for capacitor voltage regulation to avoid the disadvantages associated with PDPWM and natural balancing techniques. Initial voltage of the capacitors if not at the required value, does not provide the desired results. To overcome such a situation, a feedback technique called amplitude modulation technique is discussed in Section 6. This section also talks about the generalization of the proposed methods to higher level flying capacitor multilevel inverter topologies. Harmonic analysis of the output voltage for the implemented control techniques is performed and compared to that of the proposed methods in Section 7. Advantages of the proposed methods are also explained here. Conclusion is presented in Section 8. The units for various parameters shown in the simulation results are seconds (s) for time, volts (V) for output and capacitor voltages, and amperes (A) for load current unless otherwise mentioned.

2. FCMLI WITH NO REDUNDANCY

With some distinct advantages over the other two multilevel topologies such as the absence of clamping diodes and not requiring isolated individual sources, flying capacitor multilevel inverter topologies have gained prominence in industry. Because of the redundancy available to generate the same voltage level in the FCMLI topology, the voltage balancing of capacitors is not an issue. However, some of the redundant states may not be available when the capacitor voltage ratios are changed to increase the number of levels for improving the power quality [66]. A single-phase two-leg FCMLI topology to generate seven levels of voltages is discussed in this section.

2.1. CONVERTER TOPOLOGY

Figure 2.1 shows the two leg FCMLI topology for obtaining the different levels of voltage across the load. Although the dc source voltage sources are shown to be two, it is basically the same source. Initial values of capacitor voltages are considered to be the same and are given by a ratio of the dc source voltage V_{dc}. Switches S & S' on each leg are complementary to each other. These switching states are considered as depicted in Table 2.1.

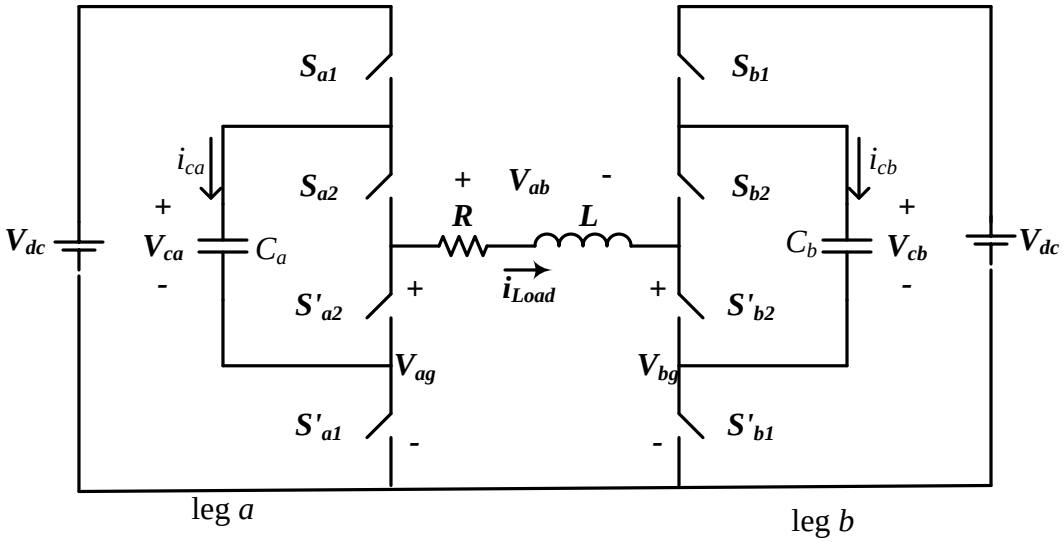


Fig. 2.1. FCMLI topology

Table 2.1
Switching states to determine state indicator

S1	S2	State
ON	ON	3
ON	OFF	2
OFF	ON	1
OFF	OFF	0

Voltage V_{bg} on *leg b* is 180 degrees out of phase with the voltage V_{ag} on leg a. Hence, the resultant voltage V_{ab} across the load is a multi level stair case waveform as shown in Fig. 2.2.

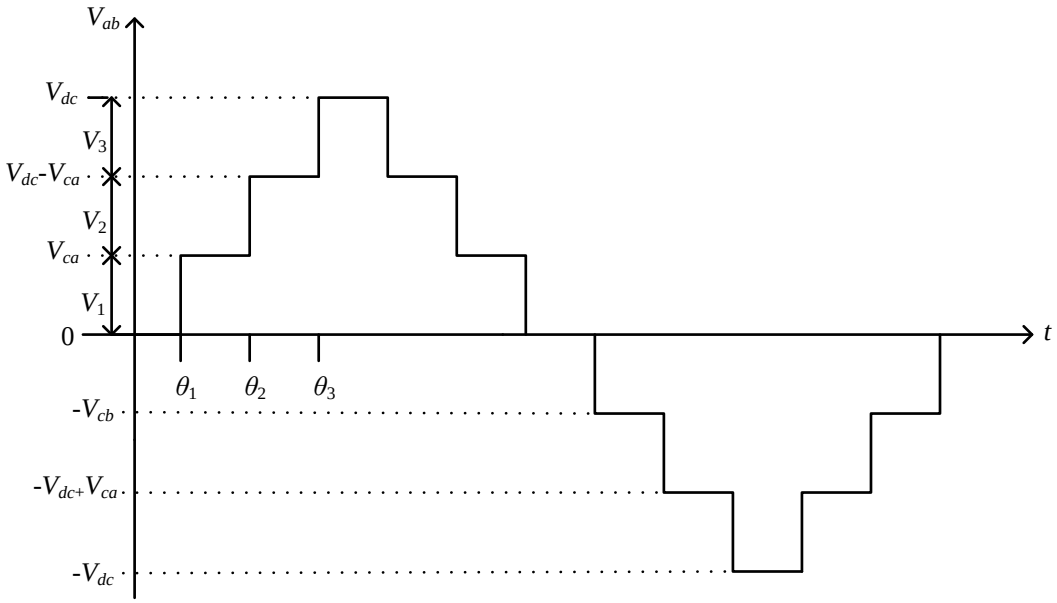


Fig. 2.2. Seven-level staircase voltage V_{ab}

Now that different voltage levels are obtained, the capacitor currents in terms of the load current can be tabulated as in Table 2.2.

Table 2.2
Output voltages and capacitor currents

State	V_{ag}	V_{bg}	i_{ca}	i_{cb}
3	V_{dc}	-V_{dc}	0	0
2	V_{dc}-V_{ca}	-V_{dc}+V_{cb}	i_{Load}	-i_{Load}
1	V_{ca}	-V_{cb}	-i_{Load}	i_{Load}
0	0	0	0	0

The Fourier series of the staircase output voltage (see Fig. 2.2) can be described as:

$$V_{ab}(t) = \sum_{n=1,3,5}^{\infty} \frac{4}{n\pi}(V_1 Cosn\theta_1 + V_2 Cosn\theta_2 + V_3 Cosn\theta_3) Sin(n\omega t) \quad (2.1)$$

Where 'n' is the order of the harmonic and 'ω' is the angular frequency. The voltage levels of the dc sources are equal and labeled to be V_{dc}. Also, the voltage of the capacitors is same and intended to be regulated at $\frac{V_{dc}}{p}$. Accordingly, considering Table 2.2, it can be written:

$$V_1 = \frac{V_{dc}}{p}$$

$$V_1 + V_2 = V_{dc} - \frac{V_{dc}}{p}$$

$$V_1 + V_2 + V_3 = V_{dc}$$

The modulation index in general is defined as:

$$Modulation\ Index\ (M) = \frac{V_m}{V_{dc}} \quad (2.2)$$

where, V_m is the magnitude of the fundamental component of the output voltage.

2.2 THETA CALCULATIONS

Considering only the fundamental component and eliminating the 3rd and the 5th order harmonics, the following equations are used to calculate θ_1, θ_2, and θ_3 for different values of the modulation index *'M'*. Here *'p'* is considered to be three.

$$V_{dc} * M = \frac{4}{\pi}\frac{V_{dc}}{3}(Cos\theta_1 + Cos\theta_2 + Cos\theta_3) \quad (2.3)$$

$$\frac{4}{3\pi}\frac{V_{dc}}{3}(Cos3\theta_1 + Cos3\theta_2 + Cos3\theta_3) = 0 \quad (2.4)$$

$$\frac{4}{5\pi}\frac{V_{dc}}{3}(Cos5\theta_1 + Cos5\theta_2 + Cos5\theta_3) = 0 \tag{2.5}$$

Figure 2.3 shows the graph drawn for the three angles at various modulation indices considering V_{dc} to be 300 V.

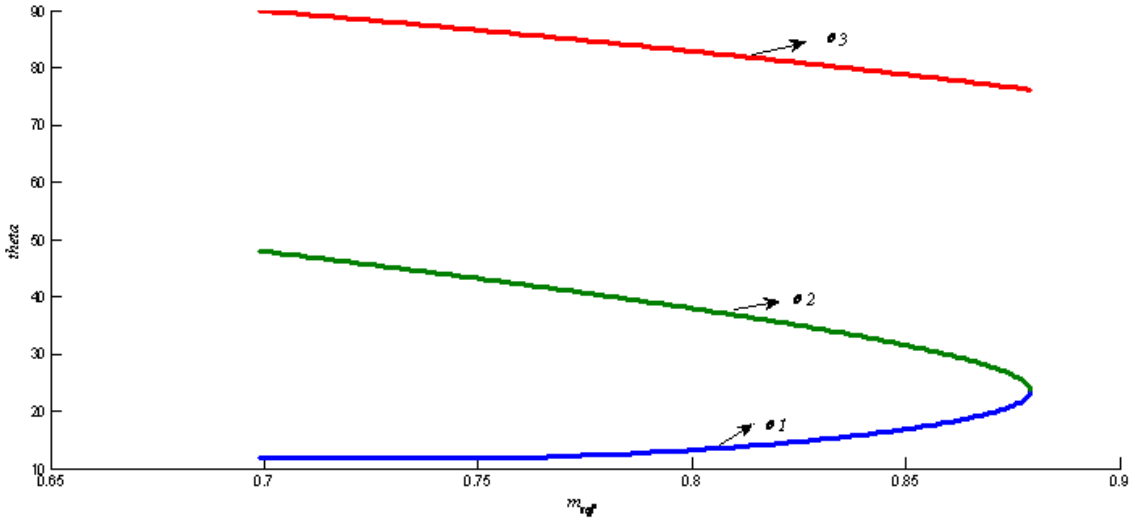


Fig. 2.3. Variation of thetas with the modulation index

Typical values of the angles at M=0.7 & at M=0.877 are as mentioned in Table 2.3:

Table 2.3
Thetas when M=0.7 & M=0.877

Theta / M	θ_1	θ_2	θ_3
M_1=0.7	12	47.92	89.95
M_2=0.877	22	25.19	76.35

2.3. CAPACITOR VOLTAGE CHARACTERISTICS

With these values of firing angles, the capacitor voltages, the output voltage and the load current at different values of power factor were observed under constant power operation of 200 W by varying the load, using MATLAB Simulink. The values of the load resistance and inductance under different power factor conditions and modulation indices are given in Tables 2.4 and 2.5.

Table 2.4
Load resistance (R) and inductance (L) at different power factors when M=0.7

Power Factor	R (Ω)	L (mH)
0.3	6.1224	3.09
0.4	10.884	3.969
0.5	17.006	4.68
0.6	24.48	5.196
0.7	33.33	5.412
0.8	43.537	5.196
0.9	55.102	4.24

Table 2.5
Load resistance (R) and inductance (L) at different power factors when M=0.877

Power Factor	R (Ω)	L (mH)
0.3	9.623	4.87
0.4	17.107	6.23
0.5	26.731	7.368
0.6	38.492	8.168
0.7	52.39	8.507
0.8	68.431	8.168
0.9	86.608	6.676

These values are found from the power calculations and the power factor formulae given by,

$$P = \frac{V_m^2}{R^2 + L^2\omega^2}\frac{R}{2} = 200 \tag{2.6}$$

$$tan\Phi = \frac{L\omega}{R} \tag{2.7}$$

where, *'P'* is the output power, 'Φ' is the power factor angle and *'V_m'* is the magnitude of the fundamental component of the output voltage obtained from equation (2.1). The fundamental frequency is considered to be 1 kHz.

The simulation results showing the capacitor voltages, load current and the output voltage for M=0.7 and M=0.877 at a power factor of 0.8 are shown in Figs. 2.4-2.9, respectively. Capacitor voltage V_{cb} is similar to that of V_{ca}, voltage across the capacitor C_a for both the modulation indices.

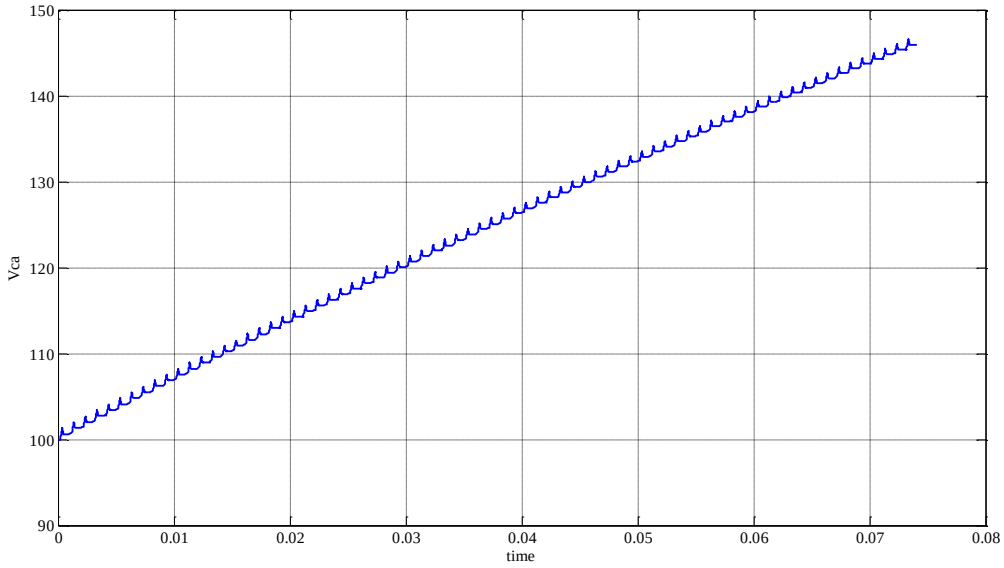


Fig. 2.4. Capacitor voltage V_{ca} at M=0.7 & PF=0.8

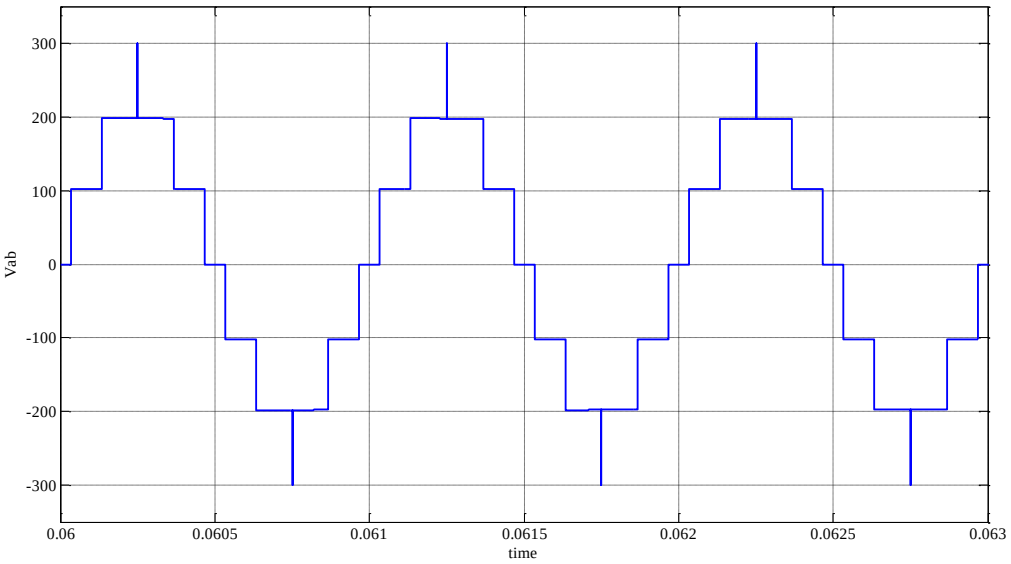


Fig. 2.5. Output Voltage V_{ab} at M=0.7 & PF=0.8

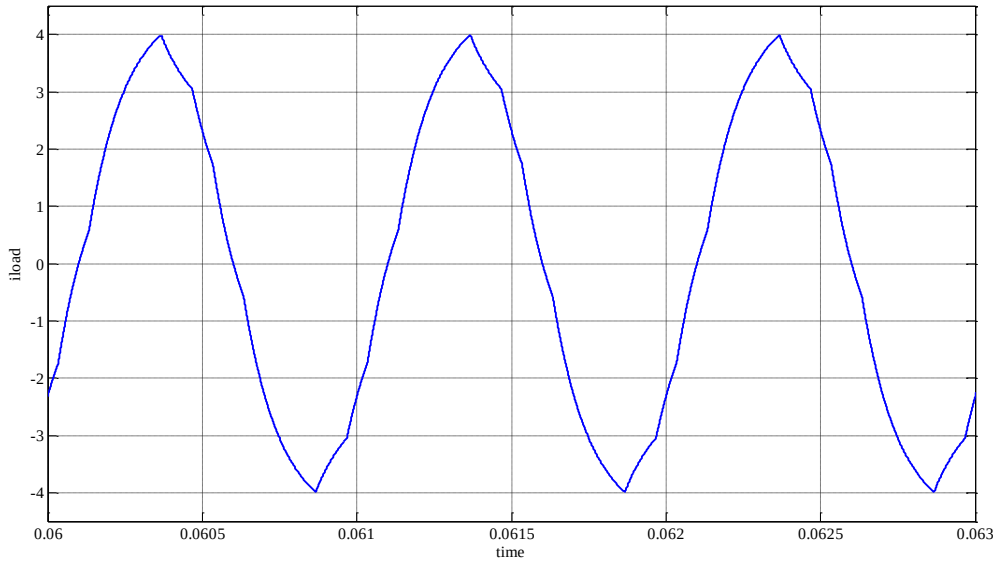


Fig. 2.6. Load current i_{load} at M=0.7 & PF=0.8

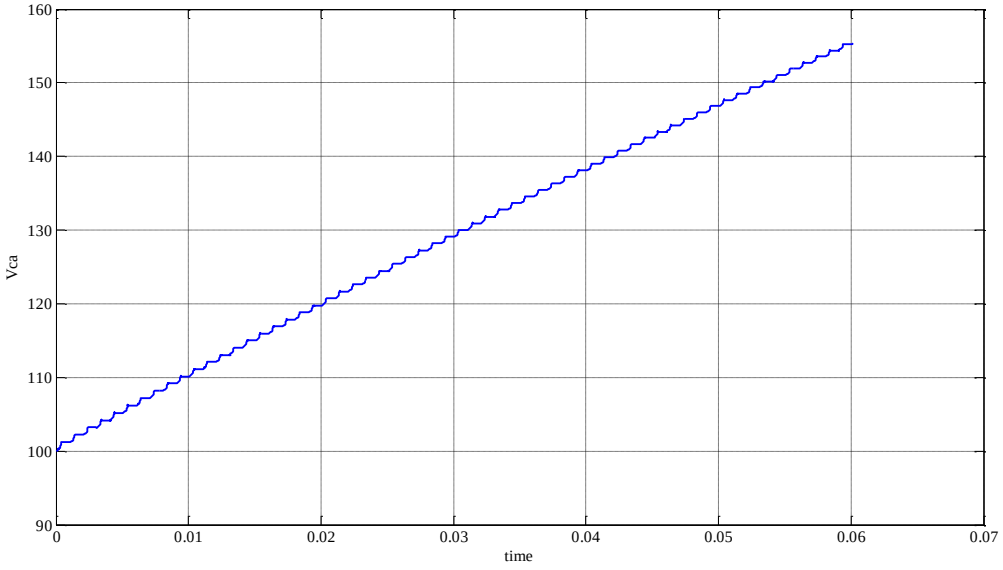


Fig.2.7. Capacitor voltage V_{ca} at M=0.877 & PF=0.8

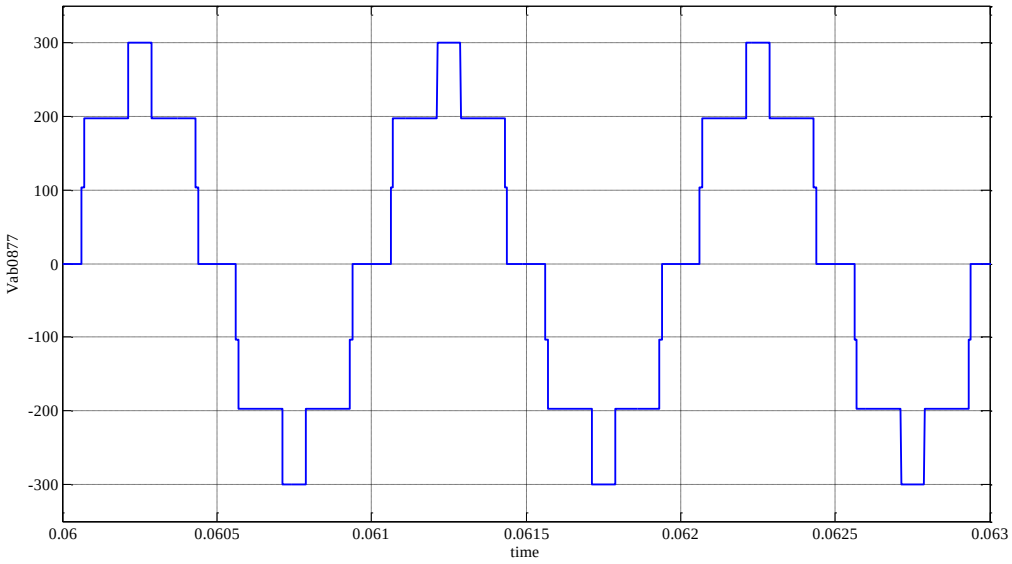


Fig. 2.8. Output Voltage V_{ab} at M=0.877 & PF=0.8

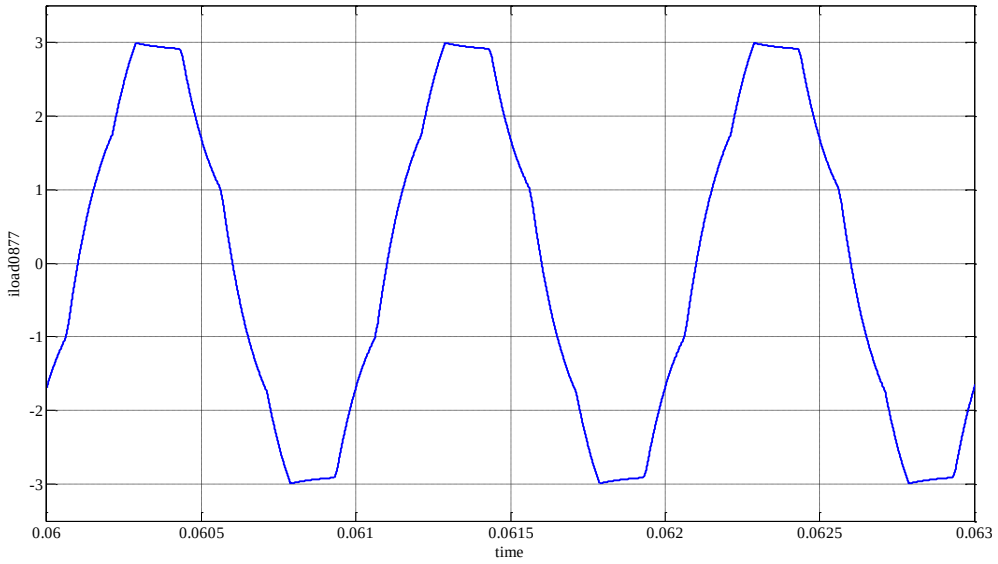


Fig. 2.9. Load current i_{load} at M=0.877 & PF=0.8

Next aspect that was looked into was the effect of power factor on output voltage and load current. Figures 2.10 to 2.13 show the same at power factor 0.7 for two different modulation indices M=0.7 and M=0.877.

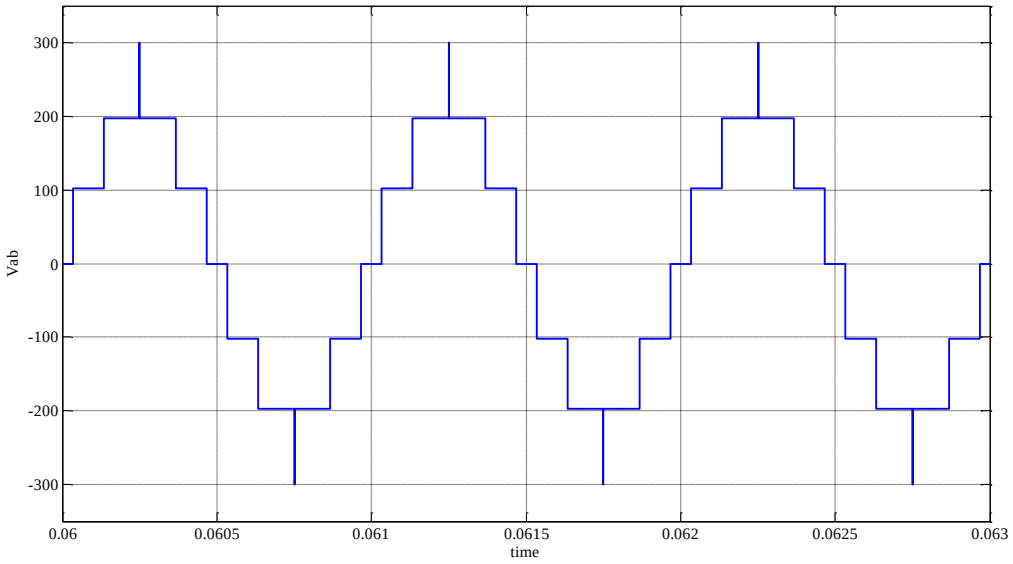


Fig. 2.10. Output voltage V_{ab} at M=0.7 & PF=0.7

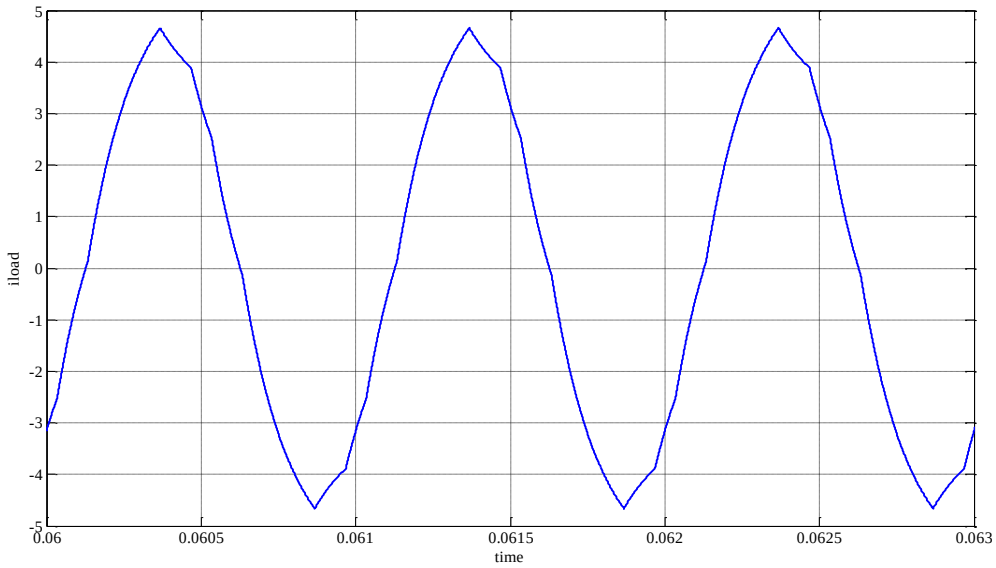


Fig. 2.11. Load current i_{load} at M=0.7 & PF=0.7

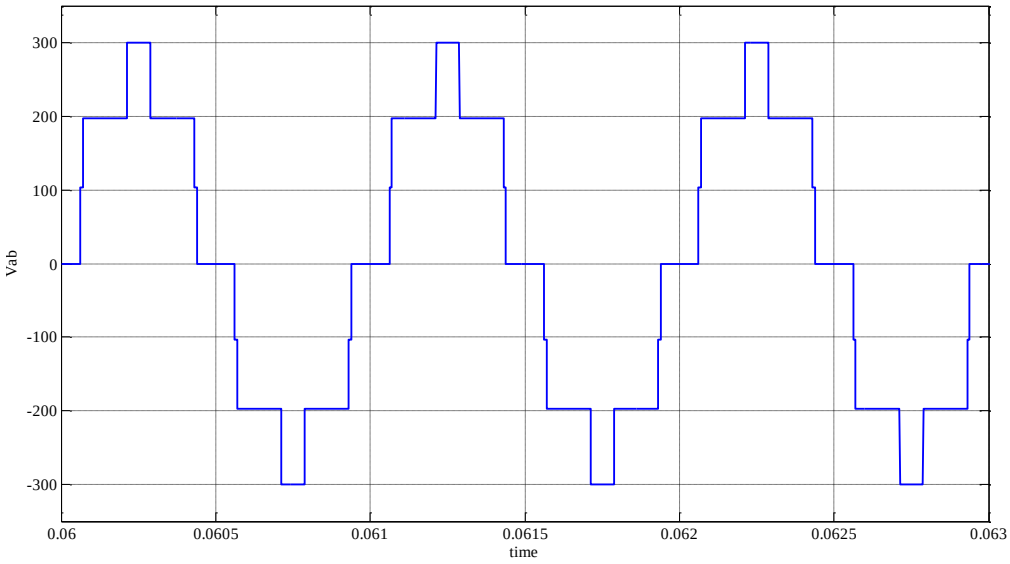


Fig. 2.12. Output voltage V_{ab} at M=0.877 & PF=0.7

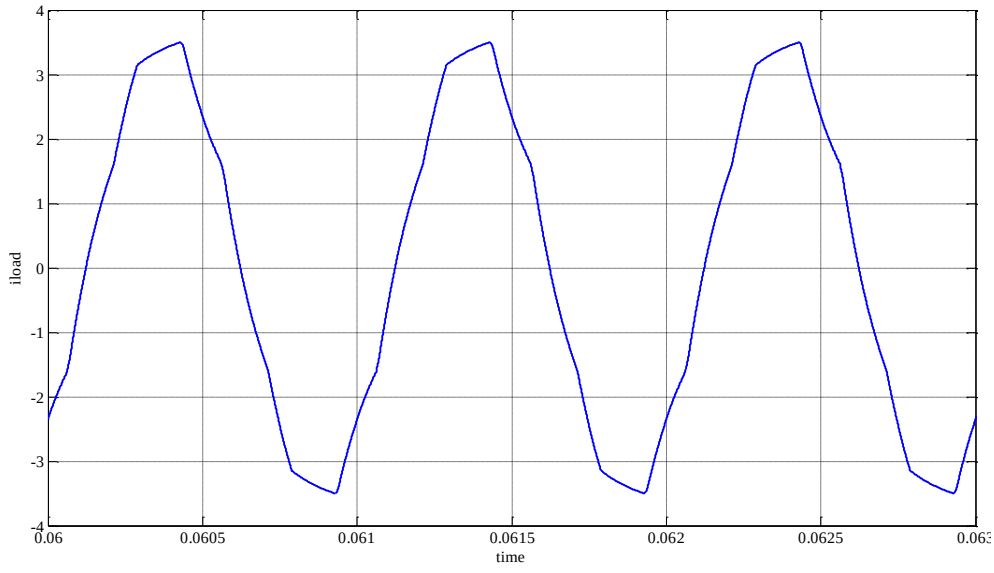


Fig. 2.13. Load current i_{load} at M=0.877 & PF=0.7

2.4 EFFECTS OF MODULATION INDEX, POWER FACTOR AND REDUNDANCY

Figures 2.4-2.13 show the simulation results of the inverter at modulation indices M=0.7 and M=0.877. It can be observed from these that the variation in the modulation index or the power factor does not affect the capacitor voltages. However, variation in the modulation index has noticeable changes on the output voltage and load current characteristics of the FCMLI topology considered.

The main drawback of operating the converter for such higher number of voltage levels is that it does not give the option of redundancy in switching states. This makes the regulation of capacitor voltages difficult. As can be seen in Figs. 2.4 and Fig. 2.7, the capacitor voltages are increasing continuously and are not controlled. Therefore, redundancy plays a vital role in the regulation of the capacitor voltages in a flying capacitor multilevel inverter topology. This calls for reduction in the number of levels in the output voltage. However, it can be an advantage because it makes the capacitor voltage regulation much simpler and easier as Section 3 discusses.

3. STAIRCASE MODULATION FOR FCMLI WITH REDUNDANCY

3.1. FIVE-LEVEL OPERATION OF THE FCMLI TOPOLOGY

The same FCMLI topology shown in Fig. 2.1 of Section 2 is considered. It is being operated as a full bridge arrangement offering five distinct output voltage levels across the load instead of operating as a seven-level inverter This is to make use of the redundant states available for capacitor voltage regulation. The voltage across the capacitors C_a and C_b is going to be regulated at half the dc source voltage (V_{ca}=V_{cb}=V_{dc}/2). Switches S & S' on each leg of the converter are still complementary implying only one of them is ON at any instant of time.

The five output voltage levels obtained across the load are V_{dc}, V_{dc}/2, 0, - V_{dc}/2, - V_{dc}. Table 3.1 shows the different combinations of voltages V_{ag} and V_{bg} on each leg of the converter to obtain all five different output voltage levels. It has to be noted that the redundancy in the switching states discussed in this thesis is per leg. Though, the same level of output voltage can be obtained by a combination of V_{ag} and V_{bg}, only the redundancy on leg a is used for regulating capacitor voltage V_{ca} and the redundancy in the switching states of leg b is used to regulate the capacitor voltage V_{cb}

Table 3.1
Different voltage levels for five-level operation (V_{ca}=V_{cb}=V_{dc}/2)

V_{ab}	V_{ag}	V_{bg}
0	0	0
	V_{dc}-V_{ca}	V_{dc}-V_{cb}
	V_{ca}	V_{cb}
	V_{dc}	V_{dc}
V_{dc}/2	V_{ca}	0
	V_{dc}-V_{ca}	0
	V_{dc}	V_{cb}
	V_{dc}	V_{dc}-V_{cb}
V_{dc}	V_{dc}	0
-V_{dc}/2	0	V_{cb}
	V_{ca}	V_{dc}
	V_{dc}-V_{ca}	V_{dc}
	0	V_{dc}-V_{cb}
-V_{dc}	0	V_{dc}

Circled states in the table are the redundant states to be used. The switching states to obtain these voltage levels on each leg (V_{ag} & V_{bg}) of the converter are shown in Table 3.2 and Table 3.3, respectively.

Table 3.2
Switching states for V_{ag} for five-level operation

S_{a1}	S_{a2}	S'_{a2}	S'_{a1}	V_{ag}
0	0	1	1	0
0	1	0	1	V_{ca}
1	0	1	0	V_{dc}-V_{ca}
1	1	0	0	V_{dc}

Table 3.3
Switching states for V_{bg} for five-level operation

S_{b1}	S_{b2}	S'_{b2}	S'_{b1}	V_{bg}
0	0	1	1	0
0	1	0	1	V_{cb}
1	0	1	0	V_{dc}-V_{cb}
1	1	0	0	V_{dc}

The five level output voltage thus obtained is shown in Fig. 3.1.

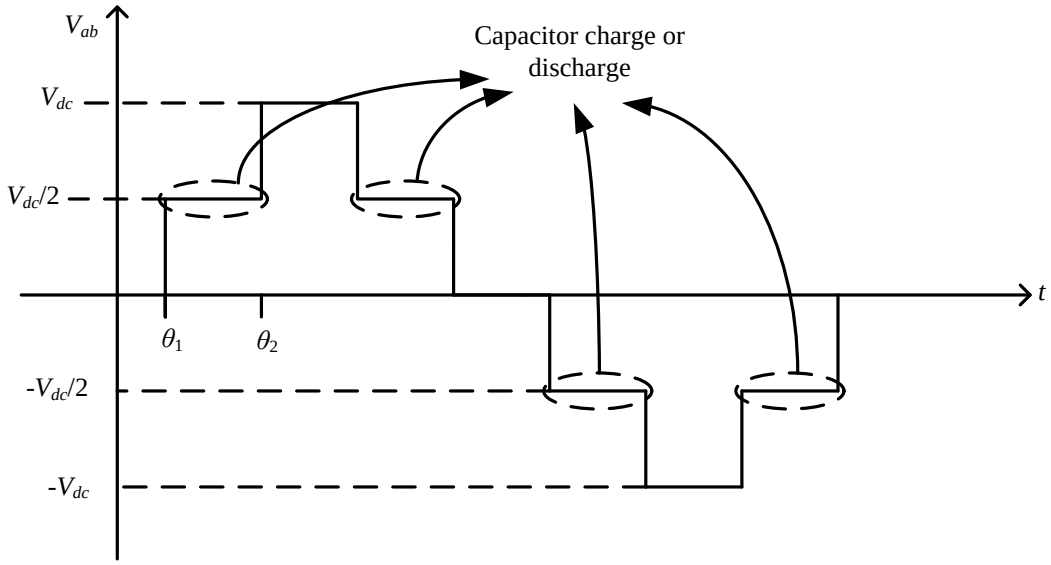


Fig. 3.1. Five-level staircase voltage V_{ab}

3.2 AVAILABILITY OF REDUNDANCY

Maintaining the desired voltage across the capacitors is the main challenge in ensuring proper operation of the inverter. There are several conduction paths that can produce the same voltage levels which will cause charging or discharging of capacitors depending on the overall state of the switches and load current polarity [8]. In the FCMLI topology considered, it can be observed that to obtain the states $V_{dc}/2$ and $-V_{dc}/2$, we have redundancy in switching states in which capacitor voltages appear with opposite polarities (see Table 3.2). This redundancy can be used to choose the path that can provide the best balancing characteristics for the capacitor voltages at any point of time. The ratio of the capacitor voltages can be changed to improve the power quality of the output voltage by increasing the number of output voltage levels. However, this requires the sacrificing of the redundancy in the switching states that helps in the capacitor voltage balancing as discussed in Section 2. Therefore, it has to be a tradeoff between power

quality (with increased number of output voltage levels) and capacitor voltage balancing of the FCMLI topology [66].

3.3 CAPACITOR VOLTAGE BALANCING (STAIRCASE MODULATION)

In order to obtain the desired levels in the output voltage, capacitor voltages should be maintained at a constant voltage level. As seen before, to obtain the same level of output voltage, there is a choice where one state among the available redundant states can be selected. For the topology considered, this can be done by assuming a specific value for the capacitor initial voltage which is equal to the voltage ratio $V_{dc}/2$. By comparing the actual voltages of the capacitors to this value, the switching pattern (turning ON and turning OFF of the switches) is decided. This charges and discharges the capacitors accordingly and thus, balances the internal voltage of the capacitors. Figure 3.2 shows the control used for staircase modulation.

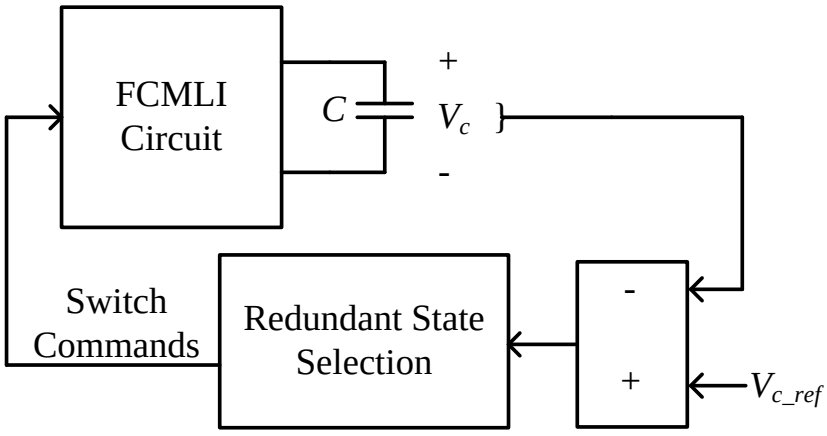


Fig. 3.2. Control strategy for staircase modulation technique

3.4 EFFECTS OF POWER FACTOR

Most of the studies that have been done on FCML converters have assumed the operation at unity power factor or one close to it. Though, power factor has not much effect on the capacitor voltages, it shows a considerable effect on the load current characteristics. At power factors nearing unity, the results are close to the desired results. Figures 3.3-3.6 show the capacitor voltages V_{ca}, and V_{cb} at power factors equal to 0.9 and 0.3, respectively. It can be observed from these figures that there is not much difference in the characteristics of the capacitor voltages with the variation in power factor.

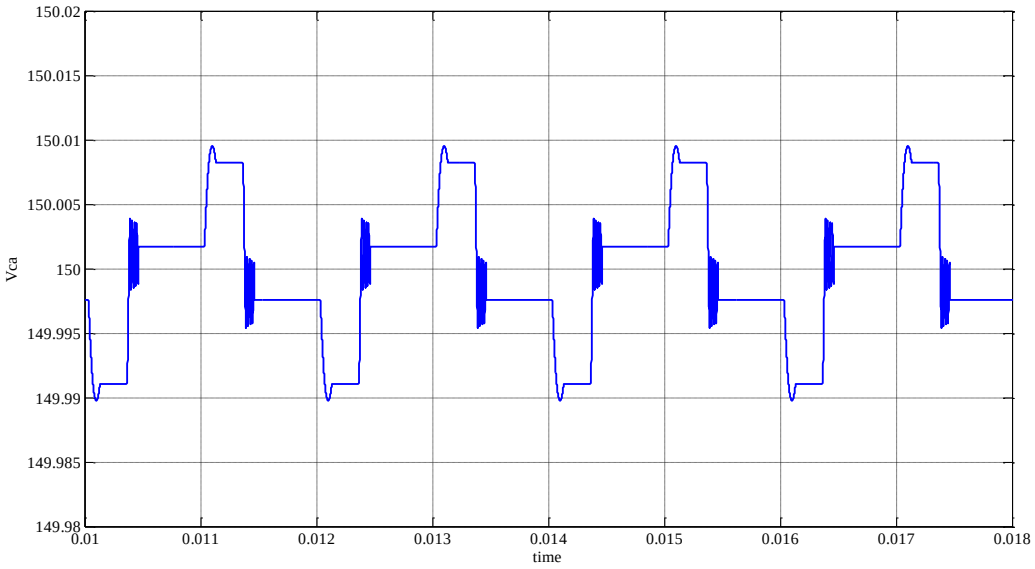


Fig. 3.3. Capacitor voltage V_{ca} at PF=0.9

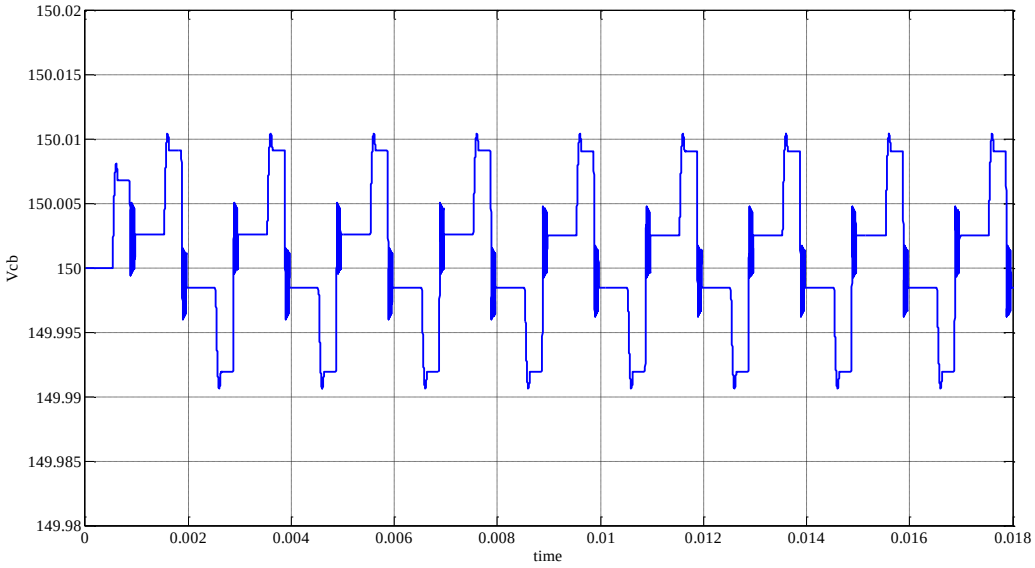


Fig. 3.4. Capacitor voltage V_{cb} at PF=0.9

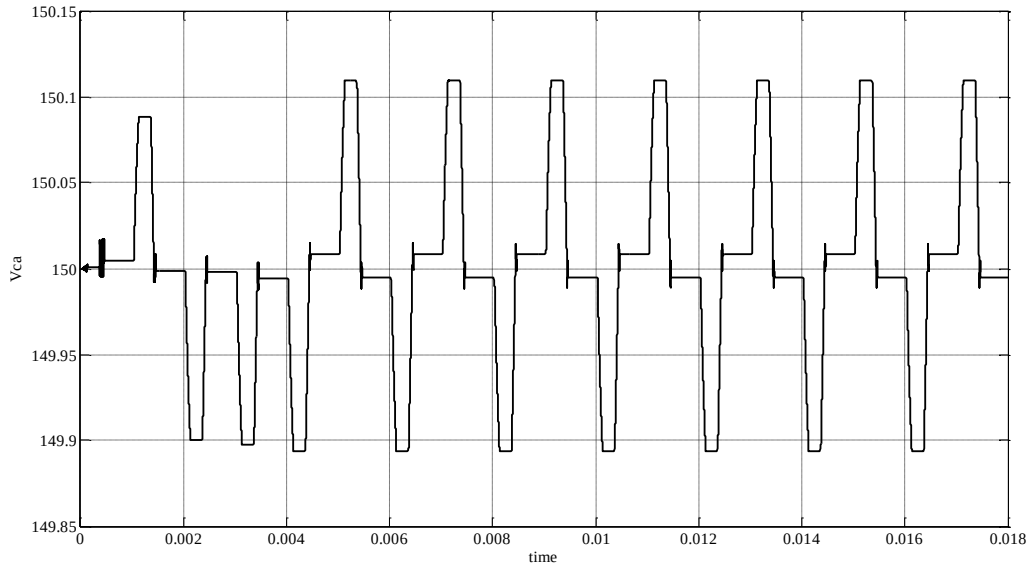


Fig. 3.5. Capacitor voltage V_{ca} at PF=0.3

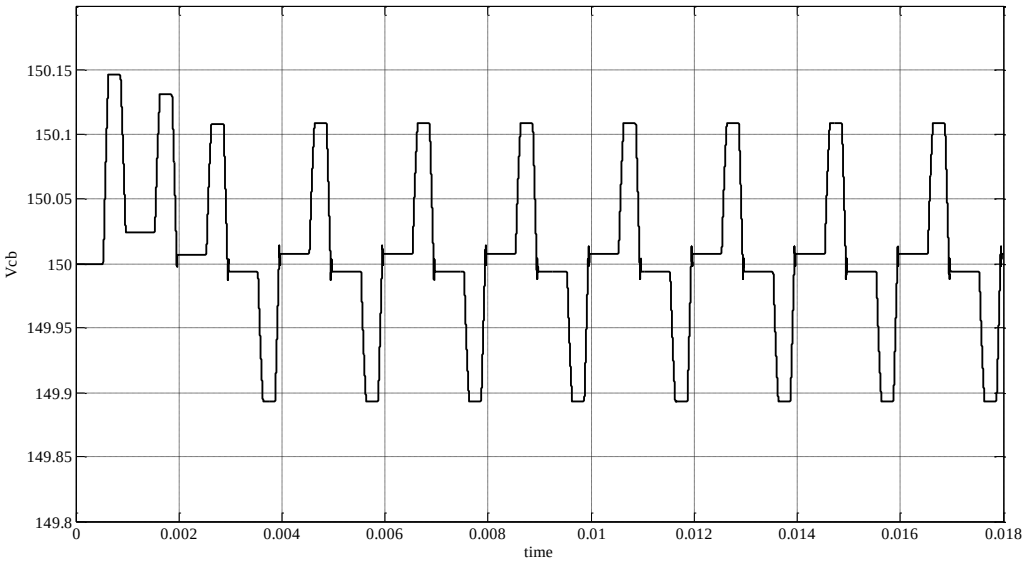


Fig. 3.6. Capacitor voltage V_{cb} at PF=0.3

3.5 OTHER SIMULATION RESULTS

Other important parameters that have to be looked into for the effects of power factor are the output voltage and load current. The simulation results for the five level output voltage V_{ab} and the load current i_{load} at power factors 0.9 and 0.3 are shown in Figs. 3.7 - 3.10, respectively.

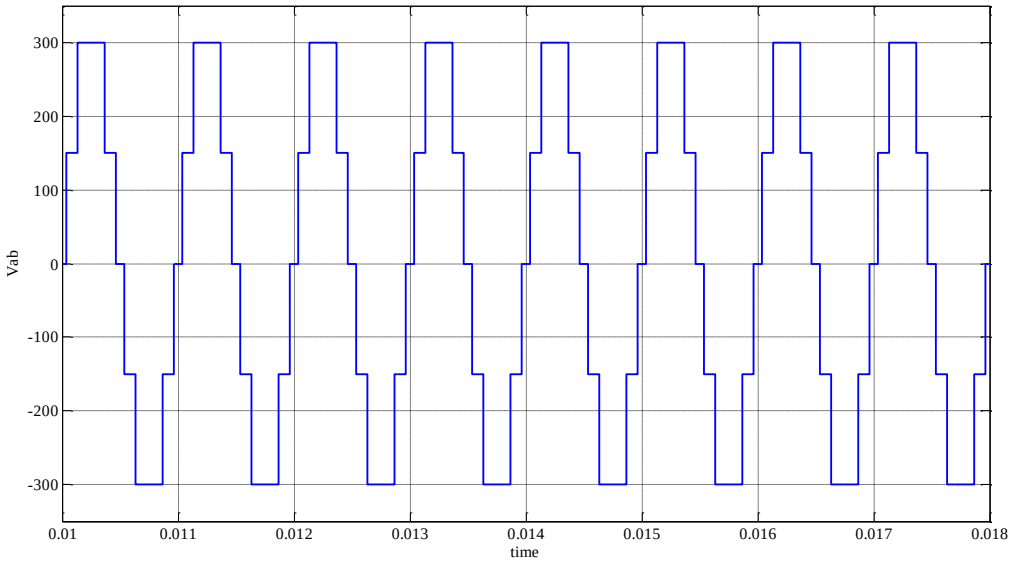


Fig. 3.7. Five level output voltage V_{ab} at power factor 0.9

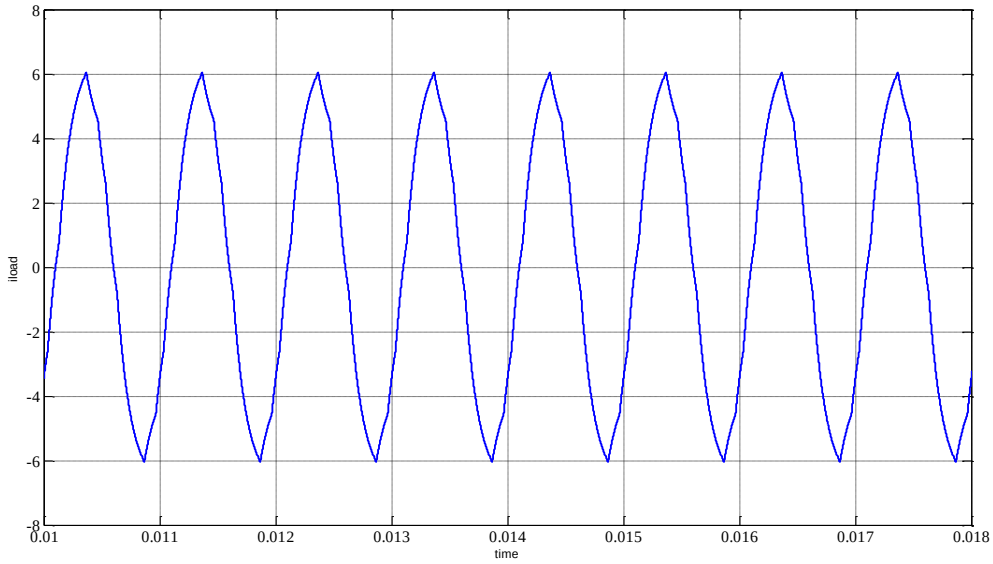


Fig. 3.8. Load current i_{load} at power factor 0.9

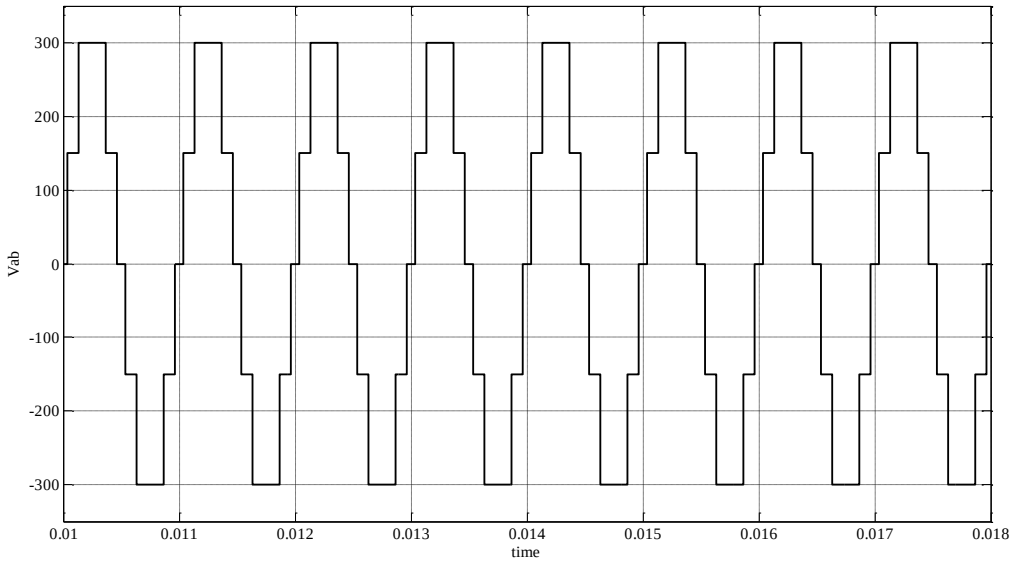


Fig. 3.9. Five level output voltage V_{ab} at power factor 0.3

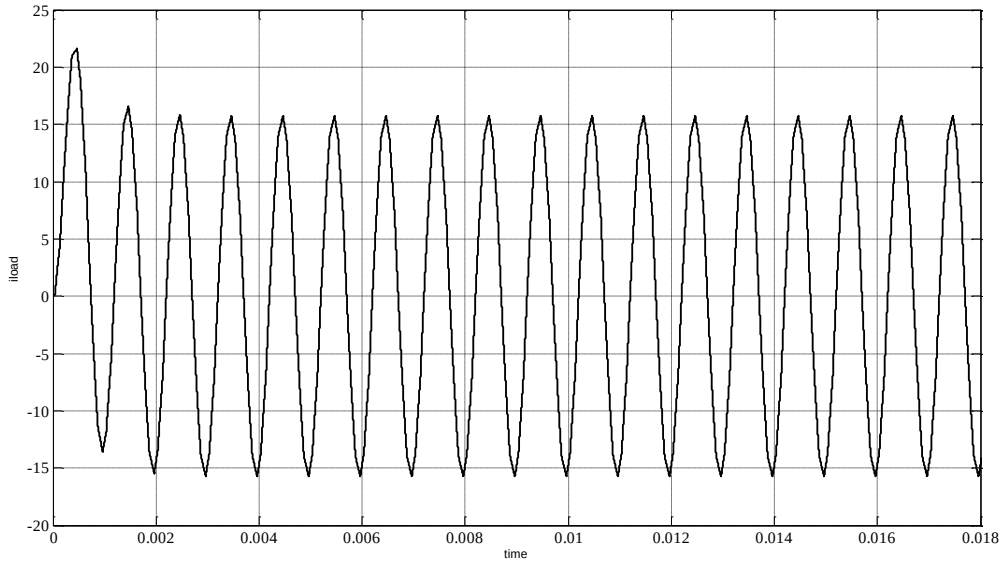


Fig. 3.10. Load current i_{load} at power factor 0.3

It is clear from the figures that there is a change in the amplitude of the load current i_{load}, with the change in power factor. However, this does not very much affect the capacitor voltages or the output voltage characteristics.

Staircase modulation technique requires measuring the voltages of capacitors and the load current polarity. In order to avoid this, easier and simpler methods have been developed based on the PWM techniques especially, the sine-triangle PWM (SPWM) [67-71]. The next sections talk about such methods as phase disposition SPWM (PDPWM), phase shifted SPWM (PSPWM), etc which do not require any capacitor voltage measurements, and the advantages and disadvantages associated with them.

4. PHASE DISPOSITION AND PHASE SHIFTED SINE TRIANGLE PWM

4.1 PWM CONTROL SCHEMES

Many controlling techniques have been developed and implemented of which the PWM control is the most widely used. A significant number of publications have been made on the various ways of implementing this technique [71]. PWM control techniques have been the most feasible control methods of all the FCMLI control schemes. There are many ways in which this PWM control can be implemented based on the type of carrier signal used. The most common among these is using a triangular wave as carrier signal and a sinusoidal signal for reference. Such a technique is called the sine–triangle PWM (SPWM).

This can again be implemented in different ways based on its carrier placement strategy [8]. Older methods used Unipolar modulation technique which used a single carrier that is compared to a sinusoidal reference to generate the two firing pulses of opposite polarity. Another strategy which used a single carrier signal and various distinct sinusoidal signals for reference was proposed in [8]. The sine – triangle PWM is done by dividing the sine wave reference into distinct contiguous bands. This reference is now compared to the triangular carrier signal waves. The number of carrier signals is equal to the number of complementary switch pairs in the inverter topology. Since all the carrier signals are in phase and disposed in bands, this carrier placement strategy is called as the phase disposition (PD) sine triangle PWM. The other carrier placement strategy uses the entire reference range. However, the carrier signals are all out of phase with each other. This scheme is called the phase shifted (PS) PWM.

4.2. PD SINE TRIANGLE PWM

The switching frequency of generated pulses is based on the carrier frequency, and output amplitude depends on the amplitude of the sinusoidal reference signal. Two important controlling parameters of SPWM are frequency modulation index (m_f) and amplitude modulation index (m_a). They are defined as follows:

m_f – ratio of carrier frequency to reference frequency

$$m_f = \frac{f_c}{f_{ref}}$$

m_a – ratio of reference peak to peak amplitude to dc source voltage

$$m_a = \frac{A_{refpk-pk}}{A_{dc}}$$

The common among the various SPWM techniques is the phase disposition (PD) carrier placement strategy which as mentioned earlier, uses the same number of carrier signals as the number of complementary switch pairs. This set of carrier signals are in phase with each other but at different voltage levels. Such a method is used for balancing the voltages of the capacitors in the considered single phase five level FCMLI topology.

Figure 4.1 shows the four triangular carrier signals and the sinusoidal reference signal. The carrier signals are compared to the reference sinusoidal signal to obtain the required control pulses. Figure 4.2 shows the control pulses thus generated.

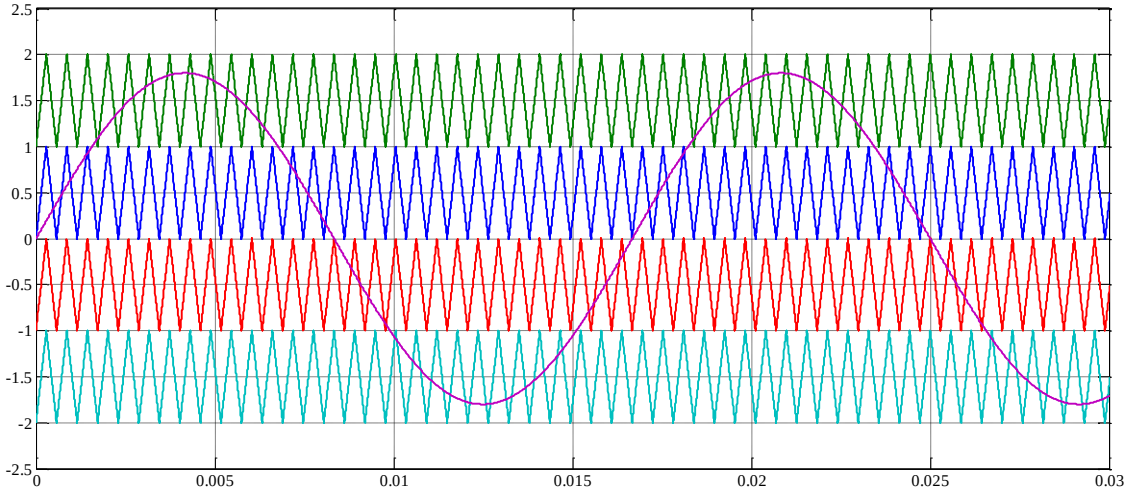


Fig. 4.1. PD SPWM

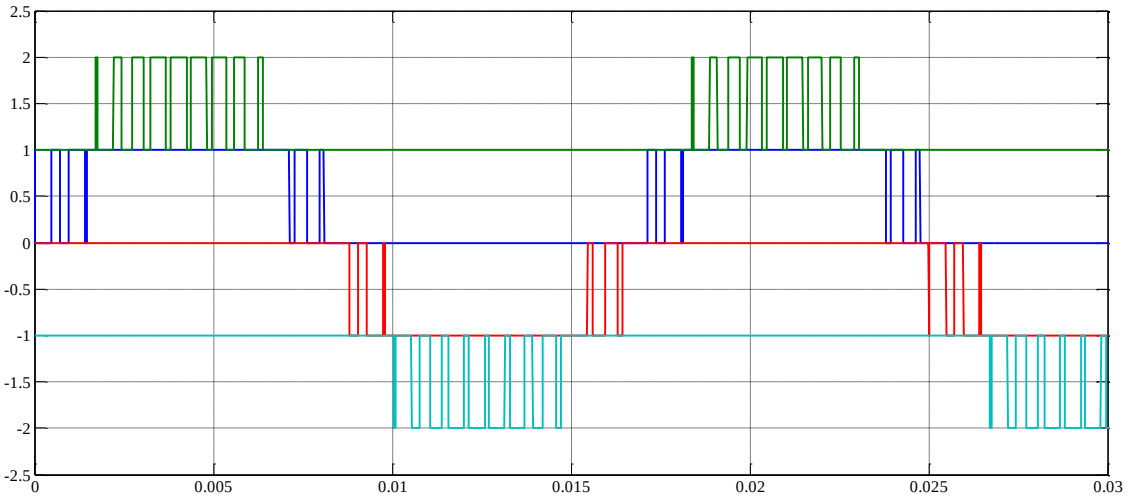


Fig. 4.2. Switching pulses

The frequency and the amplitude modulation indices for the selected PWM control scheme are chosen to be 15 and 0.9, respectively.

$$m_f = \frac{f_c}{f_{ref}} = \frac{900}{60} = 15$$

$$m_a = \frac{A_{refpk-pk}}{A_{dc}} = \frac{1.8}{2} = 0.9$$

Choosing the frequency modulation index to be a multiple of three eliminates the third multiple harmonics across the load [63]. Hence, m_f is chosen to be 15. The output voltage (V_{ab}) obtained across the load consists of the desired five levels. Figures 4.3, and 4.4 show the output voltage across the load and the load current (i_{load}). By using this kind of control technique, the capacitor voltages are very much in balance and regulated over a very small range as can be observed from Figure 4.5 and 4.6. The values for capacitors, and load parameters involved in the FCMLI topology to obtain the simulation results all through this thesis are as mentioned in Table 4.1.

Table 4.1.
Simulation parameters

Parameter	Value
C_a	10 mF
C_b	10 mF
R	20.1087 Ω
L	15.05 mH

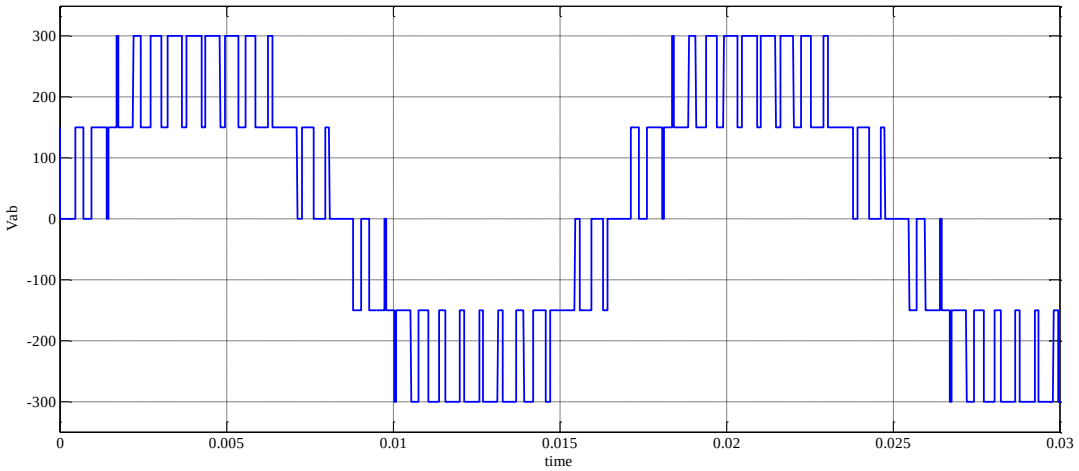


Fig. 4.3. Output voltage V_{ab} with PDPWM

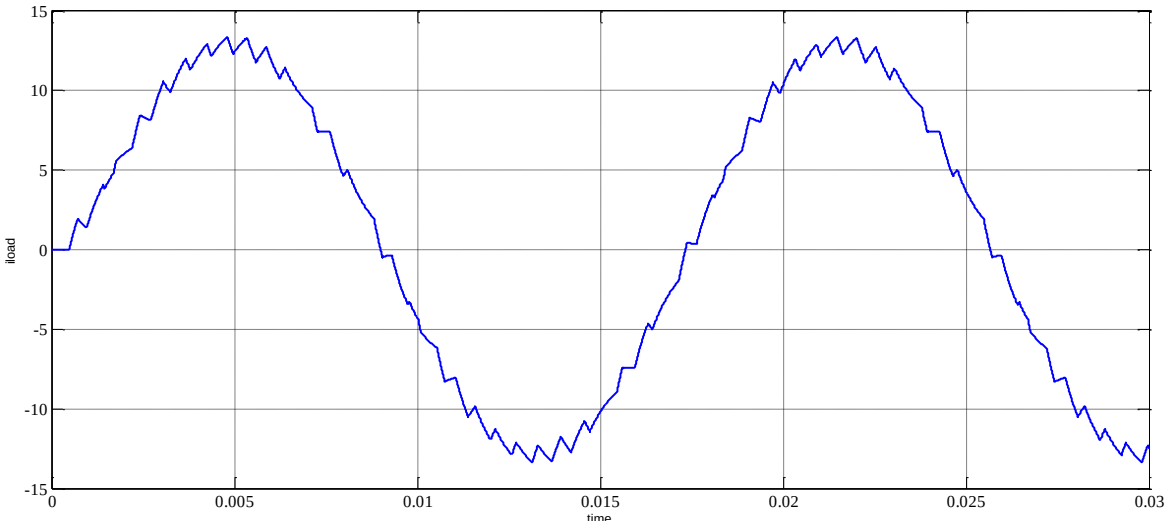


Fig. 4.4. Load current i_{load} with PDPWM

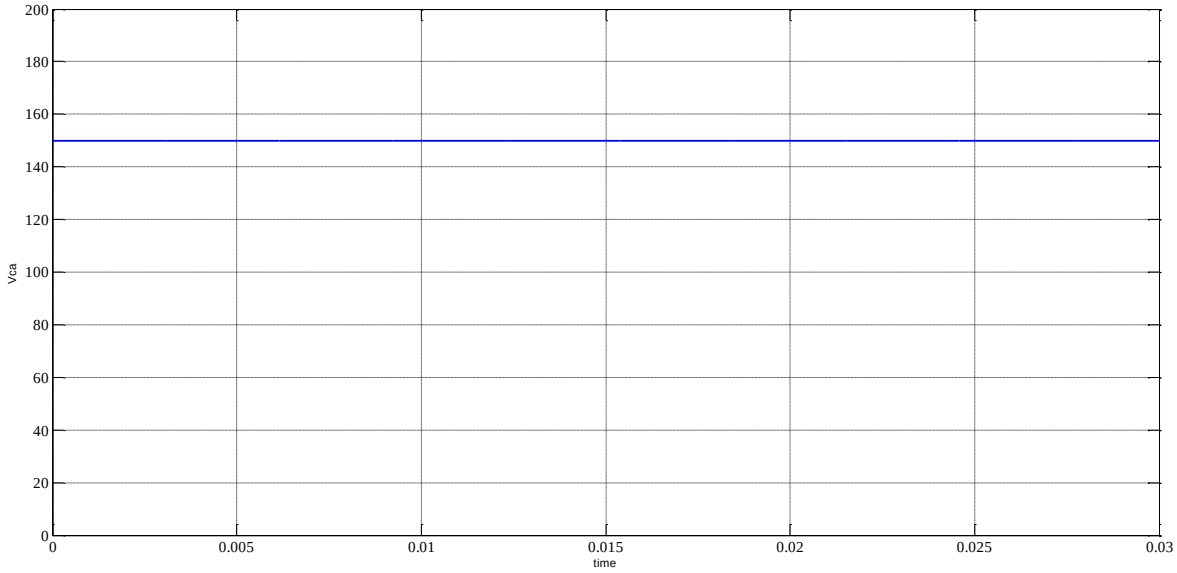


Fig. 4.5. Capacitor voltage V_{ca} with PDPWM

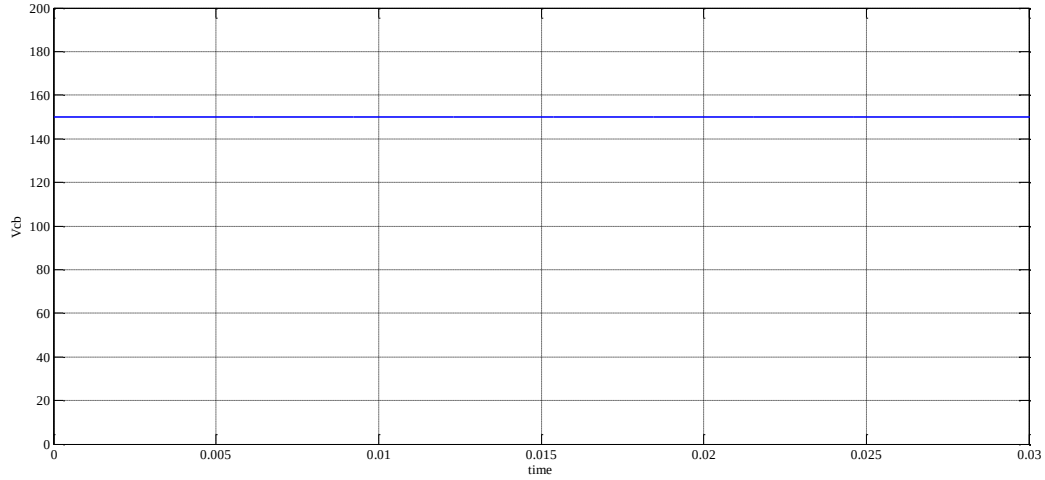


Fig. 4.6. Capacitor voltage V_{cb} with PDPWM

Although PD SPWM technique works well for capacitor voltage regulation, it is not very easy to implement because of the disposition required in the carrier signals. Hence, we can make use of much simpler techniques of flying capacitor voltage balancing like natural balancing technique which makes use of the phase shifted sine-triangle PWM method. This method which is a self-balancing technique that does not

require the measurement of capacitor voltages or load current polarity is implemented on the considered FCMLI topology.

4.3. PHASE SHIFTED PWM (NATURAL BALANCING)

As discussed earlier, capacitor voltage balancing is done by measuring the capacitor voltages and current direction. The appropriate switching states are selected based on the desired output voltage level, capacitor voltages, and current direction. This uses the redundancy in the output voltage levels. Natural balancing method doesn't need these measurements. It is done by using equal duty cycles for every pair of complementary switches in the inverter topology [71-74]. Due to its simplicity, this method has found several applications.

Natural balancing is performed by the phase shifted PWM (PSPWM) in which the carrier waveforms are shifted from each other by a phase equal to $360^{\circ}/N$, where N is the number of pairs of complementary switches per leg. The sinusoidal reference is compared to the carrier waveforms and the corresponding switching states are obtained.

For the FCMLI topology considered, since the number of pairs of complementary switches (N) per leg is 2, the two carrier signals are shifted by a phase of 180° from each other. When the reference signal is greater than carrier signal 1, switch S_{a1} is turned ON. Similarly, when the reference signal is greater than carrier signal 2, then switch S_{a2} is turned ON. A similar PWM method which uses a reference signal with a phase shift of 180° to that of the leg *a* is implemented on leg *b* on the right hand side of the inverter topology to turn switches S_{b1} and S_{b2} ON. The PWM technique used, switching pulses

and output voltages on each leg and across the load are shown in Figs 4.7 to 4.12, respectively.

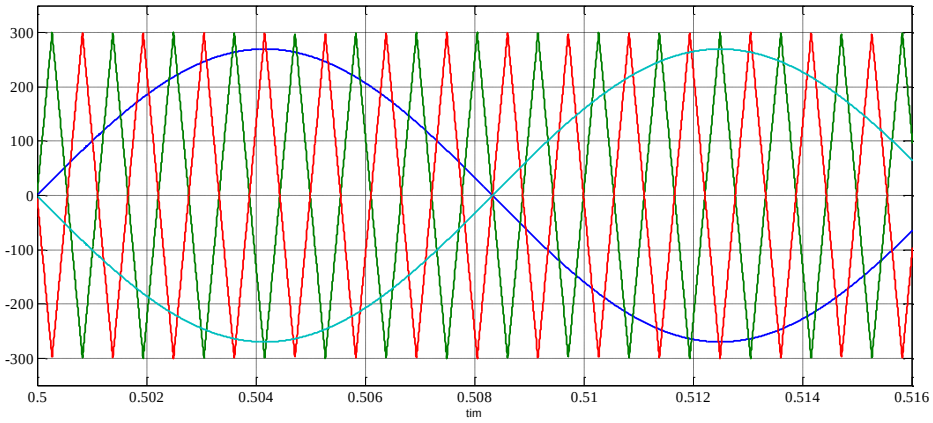


Fig. 4.7. Phase shifted sine triangle PWM for natural balancing technique

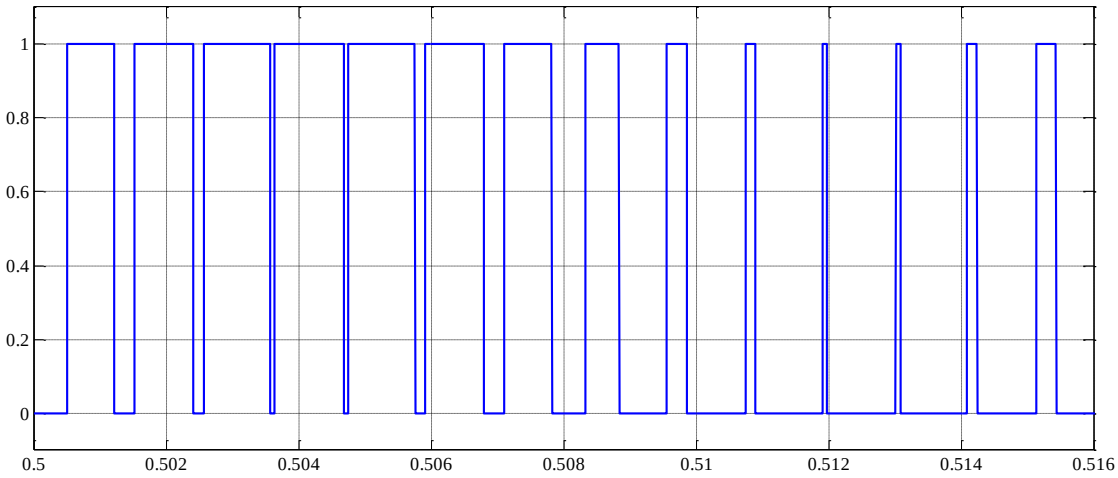


Fig. 4.8. Switching pulses for switch S_{a1}

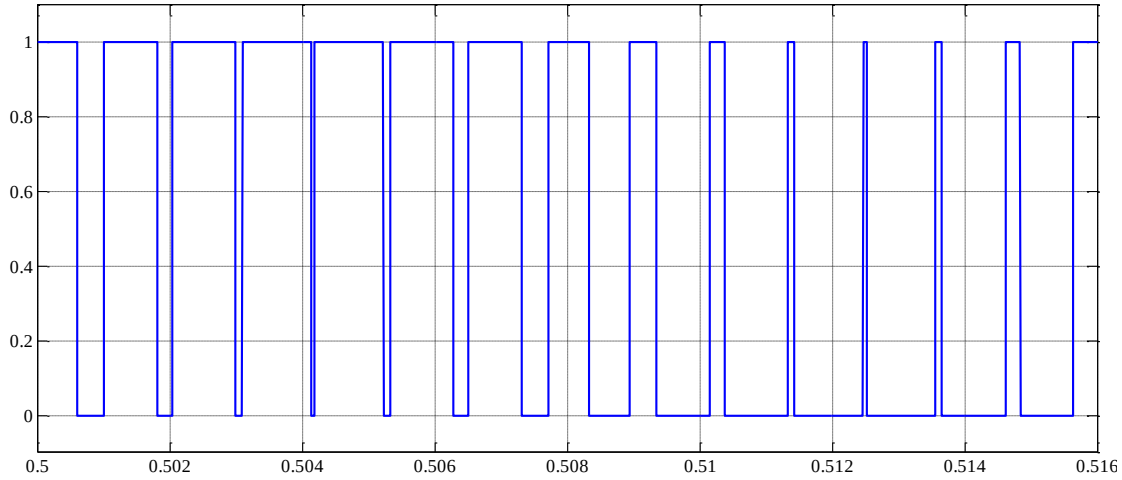


Fig. 4.9. Switching pulses for switch S_{a2}

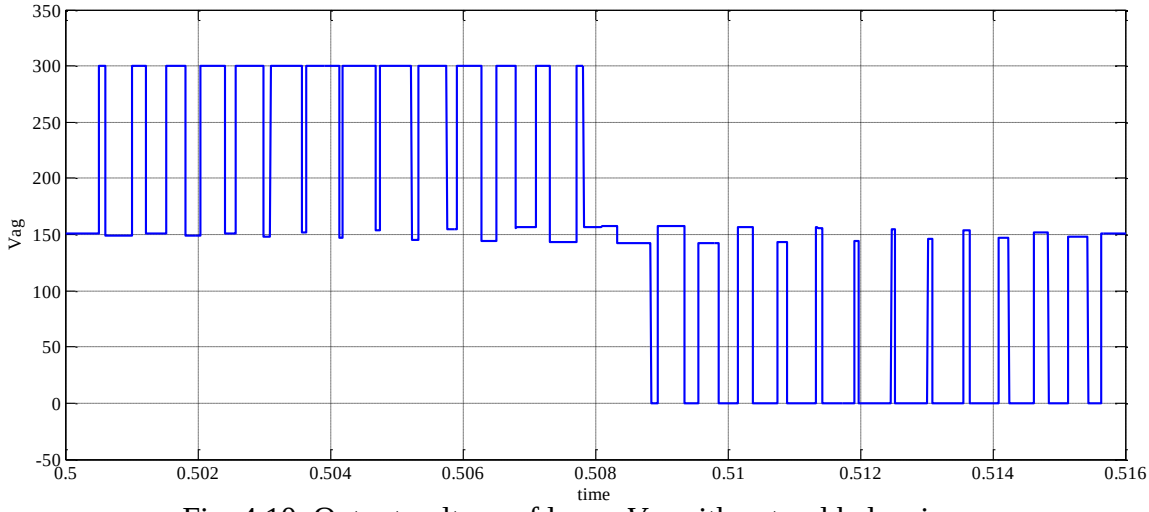


Fig. 4.10. Output voltage of leg *a*, V_{ag} with natural balancing

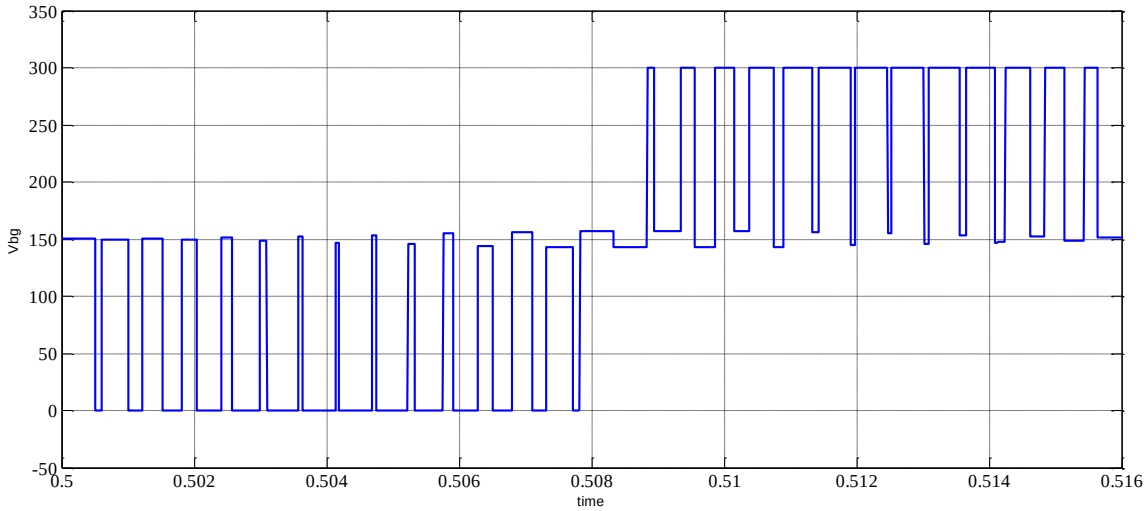


Fig. 4.11. Output voltage of leg *b*, V_{bg} with natural balancing

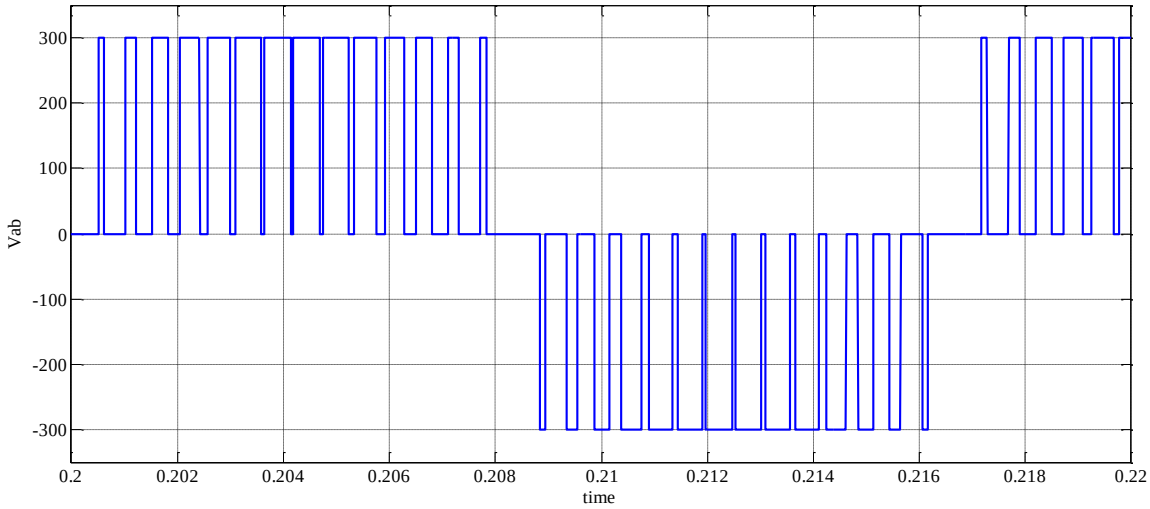


Fig. 4.12. Output voltage V_{ab} across load with natural balancing

The output voltage is expected to have levels at V_{dc}, $V_{dc}/2$, 0, $-V_{dc}/2$, and $-V_{dc}$. However, natural balancing method of capacitor voltage regulation does not generate all the required levels of the output voltage. For the considered topology, levels $V_{dc}/2$ and -$V_{dc}/2$ are missing in the output voltage waveform when this technique is used to regulate

the capacitor voltages. This could have been avoided if an even number of positive levels were initially selected. However, it might not be always desirable. In order to solve this problem, a new method called split natural balancing is proposed in the next section. This method is devised using the Unipolar PWM technique.

5. SPLIT NATURAL BALANCING TECHNIQUE FOR CAPACITOR VOLTAGE REGULATION

5.1. DISADVANTAGES OF NATURAL BALANCING

Natural balancing technique though, the simplest of all voltage regulating methods for an FCMLI, has a few disadvantages. As seen in the previous section, it is not very feasible for any number of voltage levels and moreover, is not very practical in implementation. Though it works well in a simulation where every condition is considered ideal, it doesn't produce the exact desired results when being implemented on real hardware using DSPs etc where the conditions might be different from ideal. This might cause few issues in practical implementation of natural balancing using PSPWM technique. To overcome these issues, split natural balancing technique is proposed by using which the capacitor voltages can either be charged or discharged according to the requirement to maintain a balance.

5.2. SPLIT NATURAL BALANCING TECHNIQUE

The split natural balancing technique for voltage regulation of capacitors in an FCMLI is similar to the conventional natural balancing technique which produces the switching pulses by comparing a sinusoidal reference signal with triangular carrier signals. In this proposed method, at any instant, only one of the legs of the single-phase inverter produces the output voltage while the other leg produces a zero voltage level. In other words, for one half of the fundamental cycle of the sinusoidal references, only leg *a* of the inverter operates and for the second half-cycle, leg *b* of the inverter operates. Figures 5.1 to 5.5 show the sinusoidal reference signal, (V_{ref}) and the triangular carrier

waveforms, switching pulses for the switches S_{a1} and S_{b1}, Output voltage V_{ag} on leg *a*, and output voltage V_{bg} on leg *b*, respectively. Leg *a* works during the period when V_{ref} is shown as solid wave and leg *b* is operating when V_{ref} is shown as a dashed line waveform.

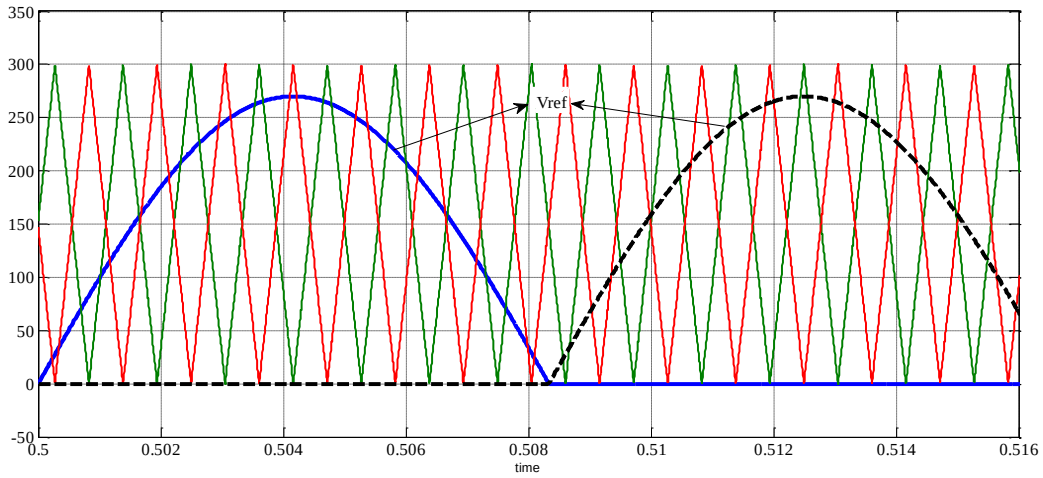


Fig. 5.1. Sine triangle PWM for split natural balancing

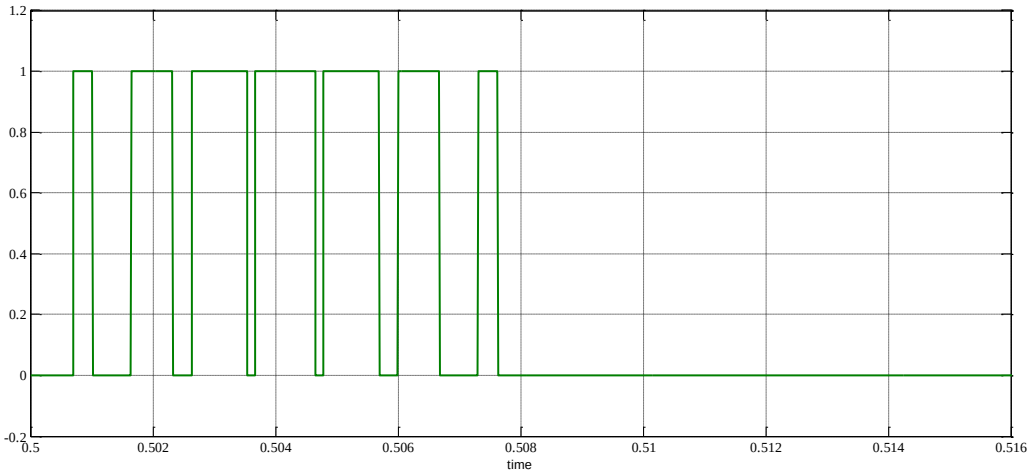


Fig. 5.2. Switching pulses for switch S_{a1}

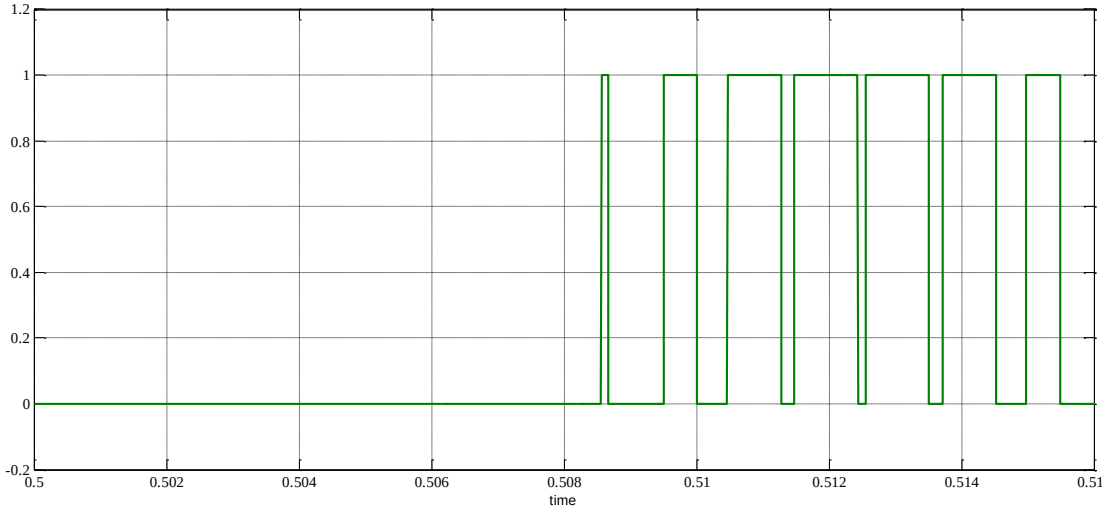


Fig. 5.3. Switching pulses for switch S_{b1}

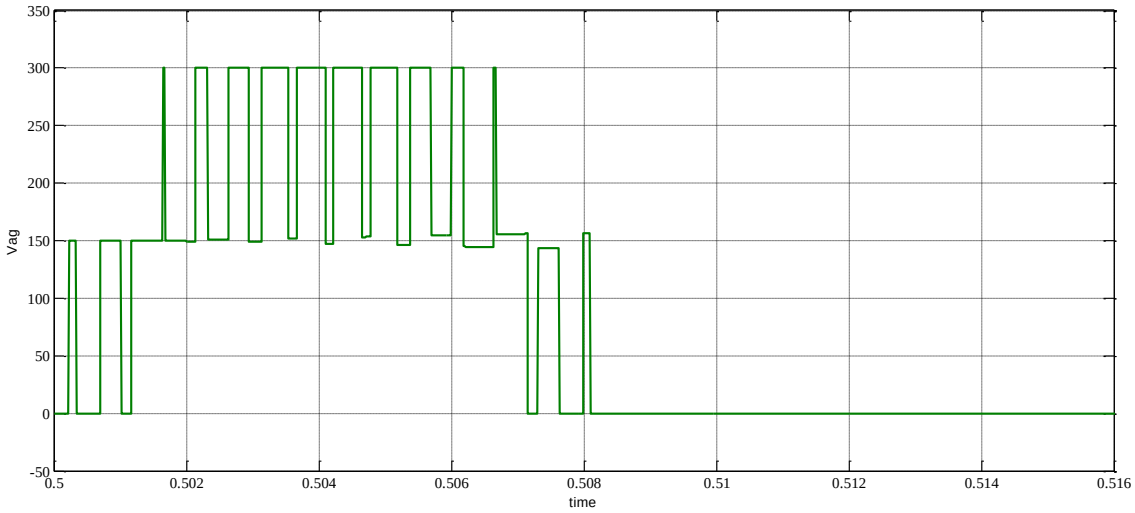


Fig. 5.4. Output voltage on leg *a*, V_{ag}

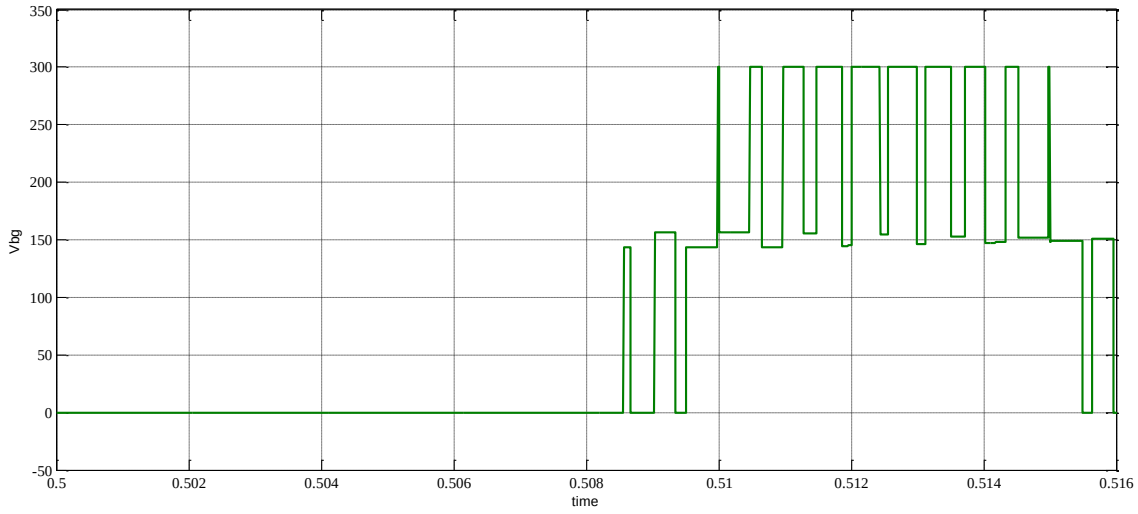


Fig. 5.5. Output voltage on leg *b*, V_{bg}

This method eliminates the problem of losing any of the levels in the output voltage. The output voltage V_{ab}, load current i_{Load}, and capacitor voltages V_{ca} and V_{cb} are shown in Figs. 5.6 to 5.9, respectively.

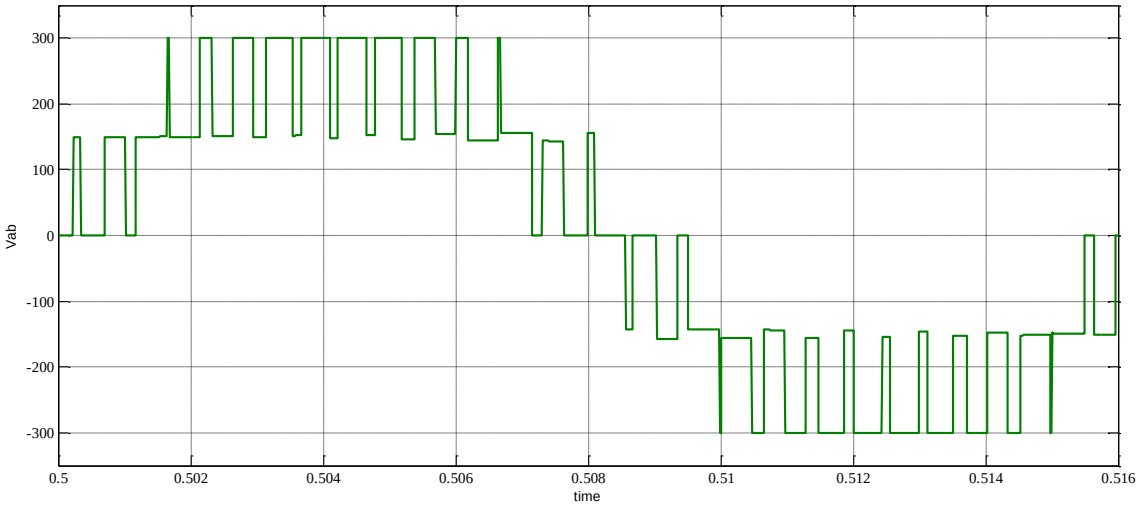


Fig. 5.6. Output voltage V_{ab} with split natural balancing

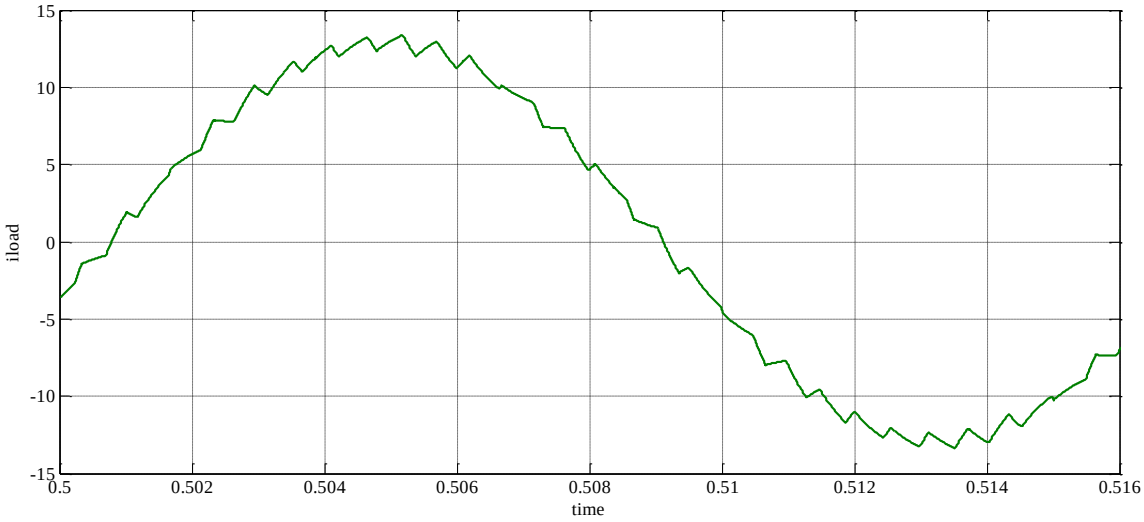


Fig. 5.7. Load current i_{Load} with split natural balancing

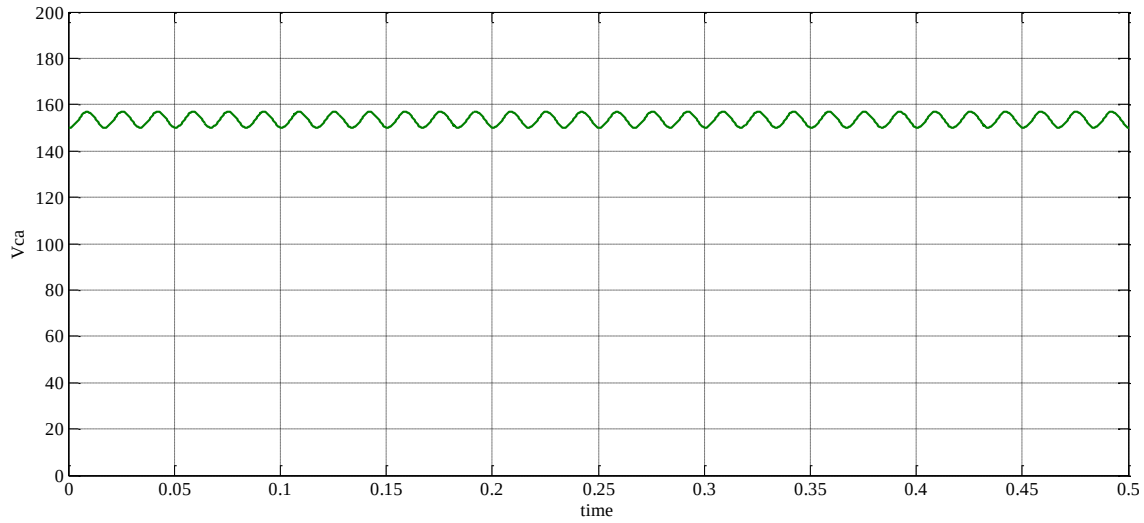


Fig. 5.8. Capacitor voltage V_{ca} with split natural balancing

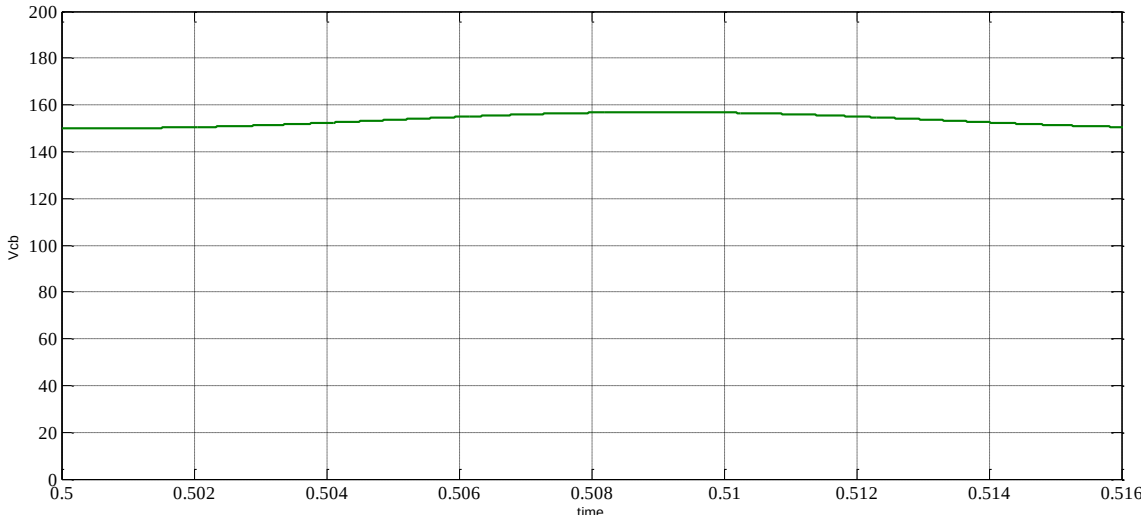


Fig. 5.9. Capacitor voltage V_{cb} with split natural balancing

It is one of the characteristics of any natural balancing technique that, the capacitor voltages are regulated around their initial values. Hence, if the initial voltage of capacitors is not at the desired value, then the required output may not be obtained. Figures 5.10 and 5.11 show the capacitor voltages on both the legs of the FCMLI topology considered, with different initial voltage levels. It can be observed that the capacitor voltages are regulated around the initial value of 120V on leg *a*, and that of 165V on leg *b* and never reach the desired value of 150V. Hence, the output voltage and current values change and are not at desired values either. Figures 5.12 and 5.13 depict the same.

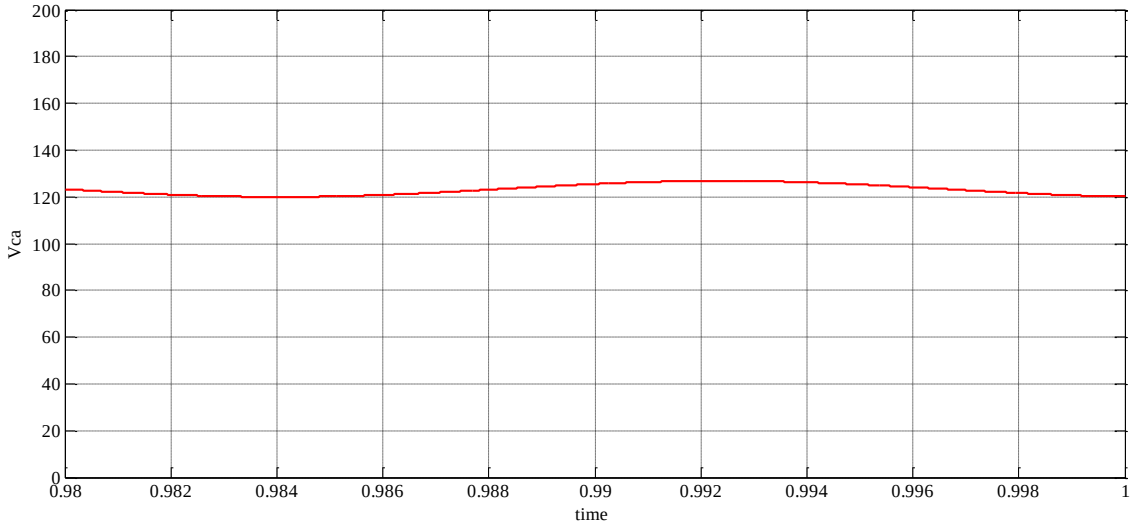


Fig. 5.10. Capacitor voltage V_{ca} when initial voltage value is 120V

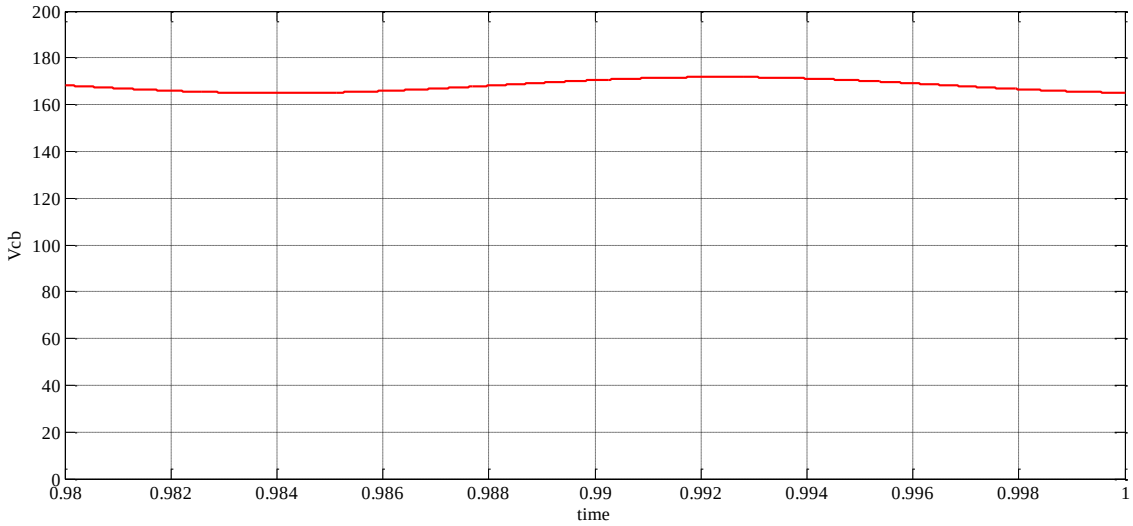


Fig. 5.11. Capacitor voltage V_{cb} when initial voltage value 160V

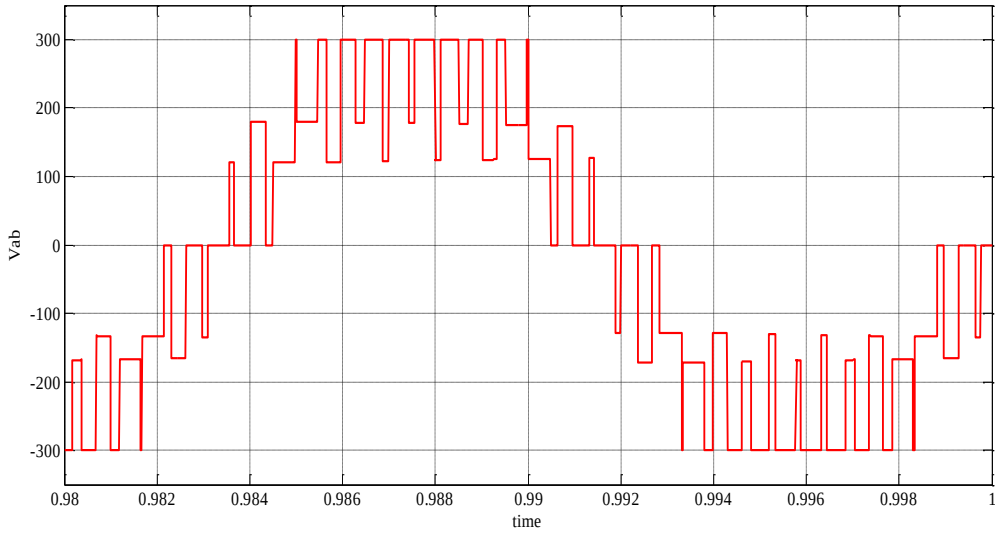


Fig. 5.12. Output voltage V_{ab} when initial capacitor voltage is not at desired level

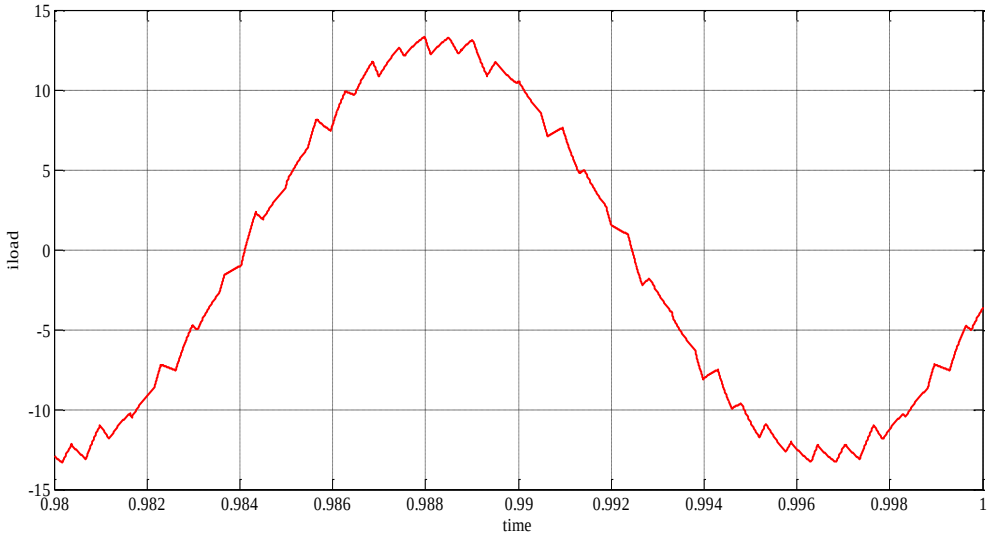


Fig. 5.13. Load current i_{load} when initial capacitor voltage is not at desired level

Thus, though split natural balancing eliminates the problem of losing states posed by conventional natural balancing, the capacitor voltages still depend on their initial voltage values. To overcome such issues in split natural balancing, a new method called

amplitude modulation adjustment (AMA) is devised to be used in a feedback loop along with split natural balancing. The next section discusses about this AMA method and the generalization of these methods to higher level FCMLI topologies.

6. AMPLITUDE MODULATION ADJUSTMENT (AMA) METHOD AND ITS GENERALIZATION TO HIGHER LEVEL TOPOLOGIES

6.1. AMPLITUDE MODULATION ADJUSTMENT (AMA) METHOD

In addition to the split natural balancing technique, capacitor voltages can be regulated by implementing a new method called amplitude modulation adjustment (AMA), which is done by changing the amplitude of carrier signal 2 by a factor *k*. It is given by the ratio of amplitude of carrier signal 2 to reference amplitude.

$$k = \frac{m_2}{m_{ref}}$$

where, m_{ref} is the reference amplitude and m_2 is the amplitude of carrier signal 2. It is observed that capacitor voltages were discharged for a value $k < 1$ and they were charged when $k > 1$. Figures 6.1 and 6.2 show the carrier signal waveforms for different values of *k*.

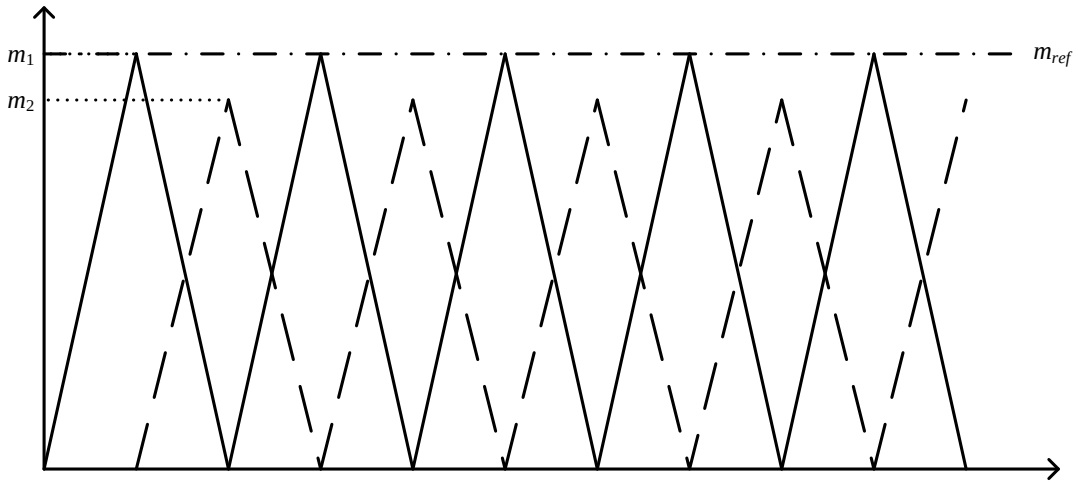


Fig. 6.1. Carrier signal waveforms for $k = (m_2/m_1) < 1$

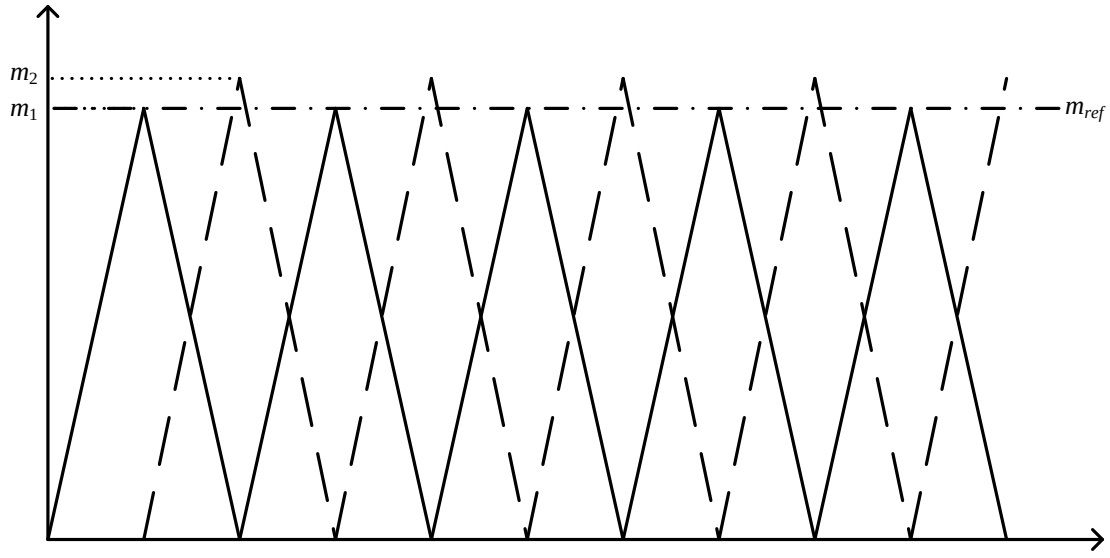


Fig. 6.2. Carrier signal waveforms for $k = (m_2/m_1) > 1$

6.2. SIMULATION RESULTS

Simulation results of the capacitor voltages on leg *a* of the considered single phase five-level FCMLI topology are shown for cases $k < 1$ and $k > 1$ in Figs. 6.3 and 6.4, respectively. It can be observed from the figures that capacitor voltage discharges when $k < 1$ and charges when $k > 1$. Since the capacitors on both the legs are identical in all aspects, a similar result of capacitor voltages can be obtained on leg *b*.

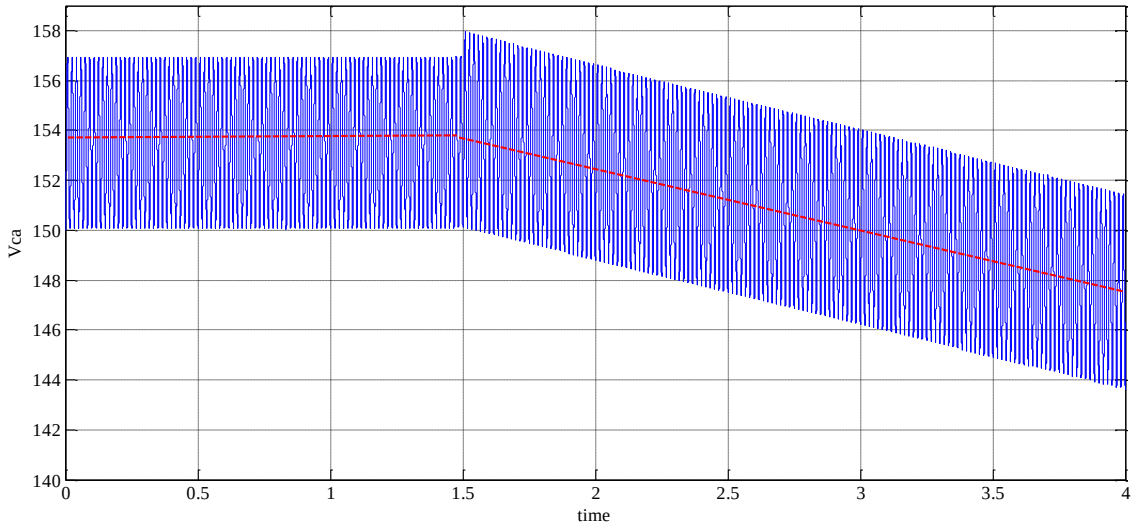


Fig. 6.3. Capacitor voltage V_{ca} for $k < 1$ at time = 1.5s

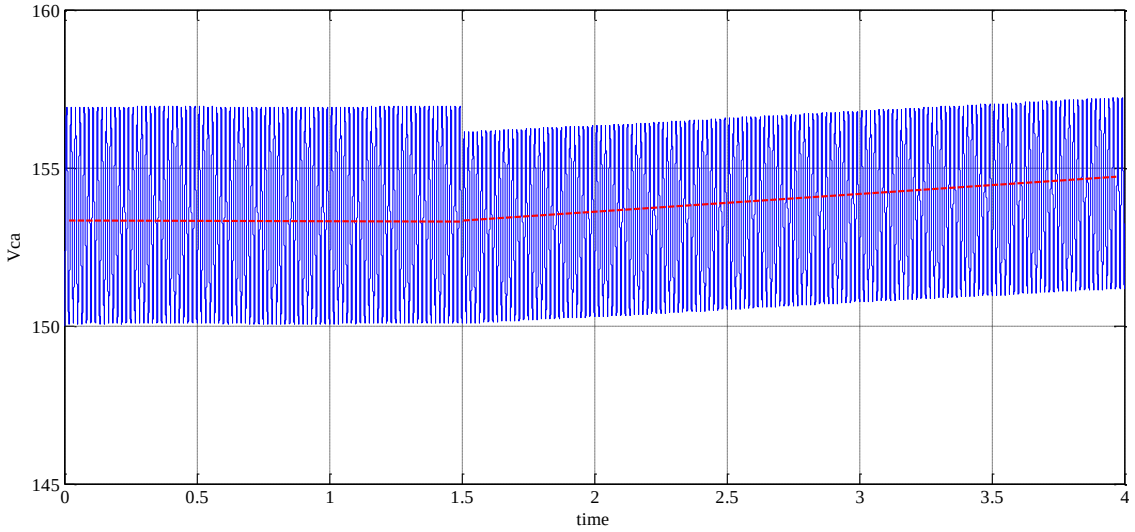


Fig. 6.4. Capacitor voltage V_{ca} for $k > 1$ at time = 1.5s

6.3. ANALYSIS

A sub interval of the output voltage on leg *a* is considered assuming a constant load current during that small period of time. Figure 6.5 shows the carrier signal waveforms for different values of *k* and reference sinusoidal waveform, switching pulses for switches Sa1 and Sa2, and output voltage V_{ag} on leg a. V_{dc} is the dc source voltage and V_{ca}, the capacitor voltage on leg *a*.

Sub-interval T1 is decided by carrier signal1. If load current i_{load} is positive, then the capacitor is charged. Sub-interval T2 is dependent on carrier signal 2. If load current iload is positive, then the capacitor will be discharged. For various conditions based on factor k which varies the width of T2, the capacitors are either balanced or charged or discharged. This can be explained as follows,

if k =1, T1 ≈ T2, capacitor voltages are balanced

k <1, T1 < T2, capacitor voltages are discharged

k >1, T1 > T2, capacitor voltages are charged

Similar results are obtained when width of T1 is changed because of the reference signal. Thus, capacitor voltages can be regulated as desired.

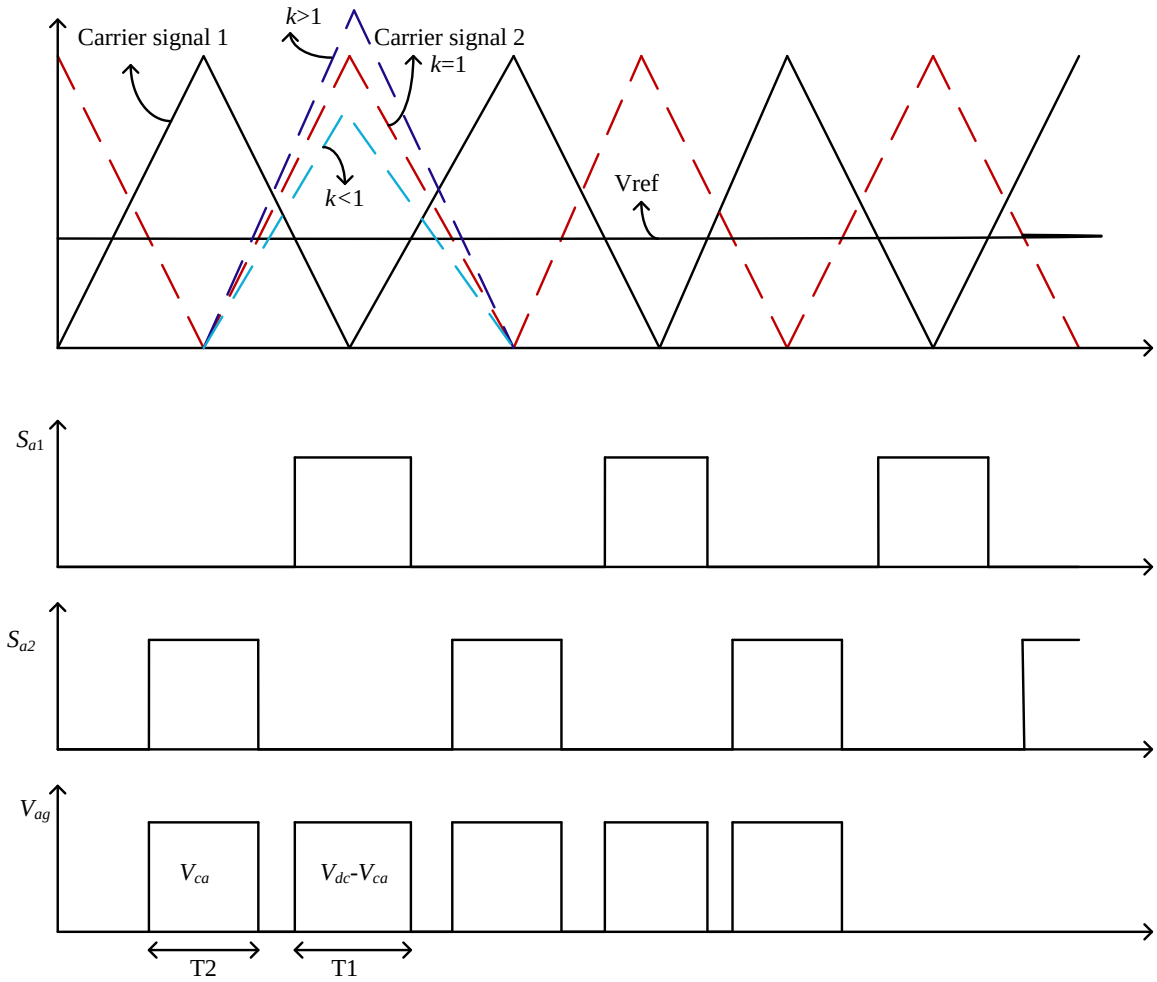


Fig. 6.5. Waveforms of carrier signals, reference, switching pulses for switches S_{a1} and S_{a2}, output voltage V_{ag} on leg a

6.4. FEEDBACK CONTROL FOR CAPACITOR VOLTAGE REGULATION

Combining the split natural balancing technique along with the AMA method for balancing the capacitor voltages in an FCMLI proves to be more advantageous in practical implementations. Therefore, a feedback control technique which uses these two methods is applied for voltage regulation. Figure 6.6 depicts this feedback control technique. The capacitor voltages are measured and compared with a constant reference value. The difference between these two values decides the value of k, the factor which in

turn is used to decide the amplitude of carrier signal 2. Thus, the capacitor voltages are either charged or discharged to maintain a constant value. A simple PI block with transfer function $T.F. = \frac{38}{S+38}$ is used in the feedback loop to control the factor 'k'. Bode plot for the same is shown in Fig. 6.7.

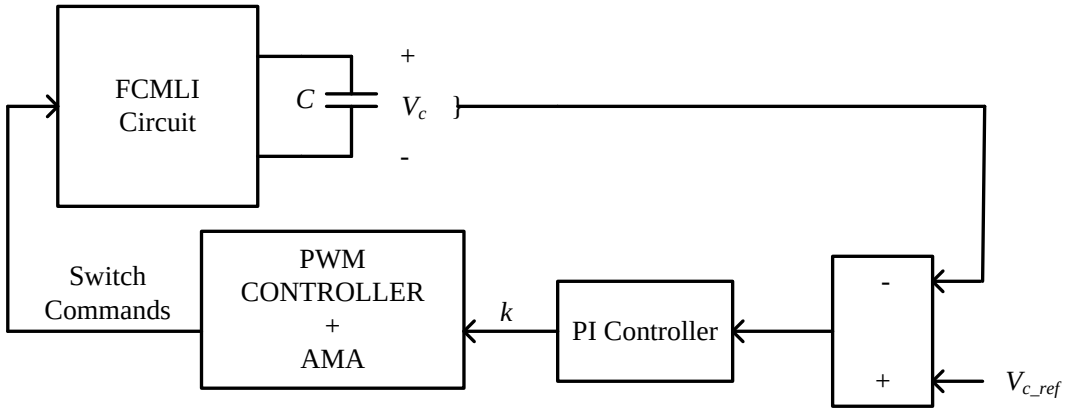


Fig. 6.6. Feedback control technique

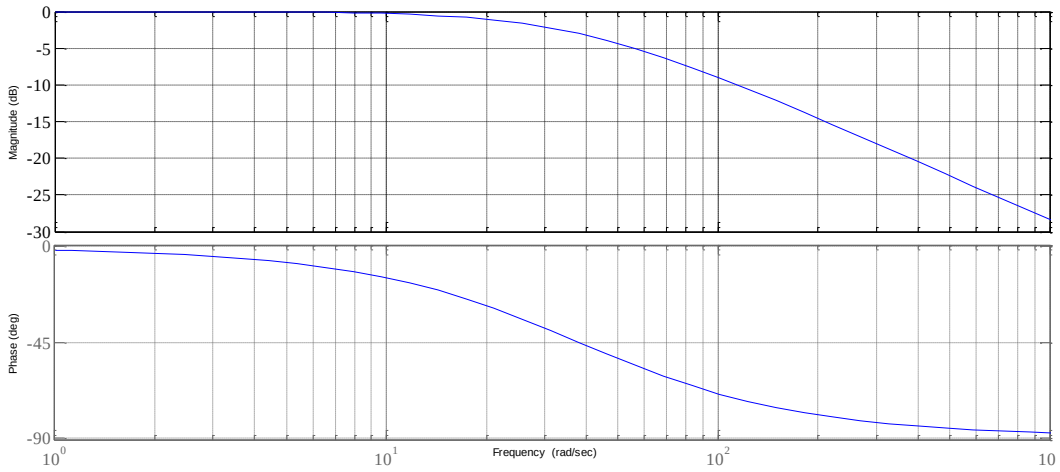


Fig. 6.7. Bode plot for the chosen PI controller

The next Figs. 6.8-6.11 show the output voltage V_{ab}, load current i_{load}, capacitor voltages V_{ca} and V_{cb} thus obtained when the initial capacitor voltages are not at the required levels. It can be observed that they however reach the desired value gradually and are settled around it when the feedback technique is used.

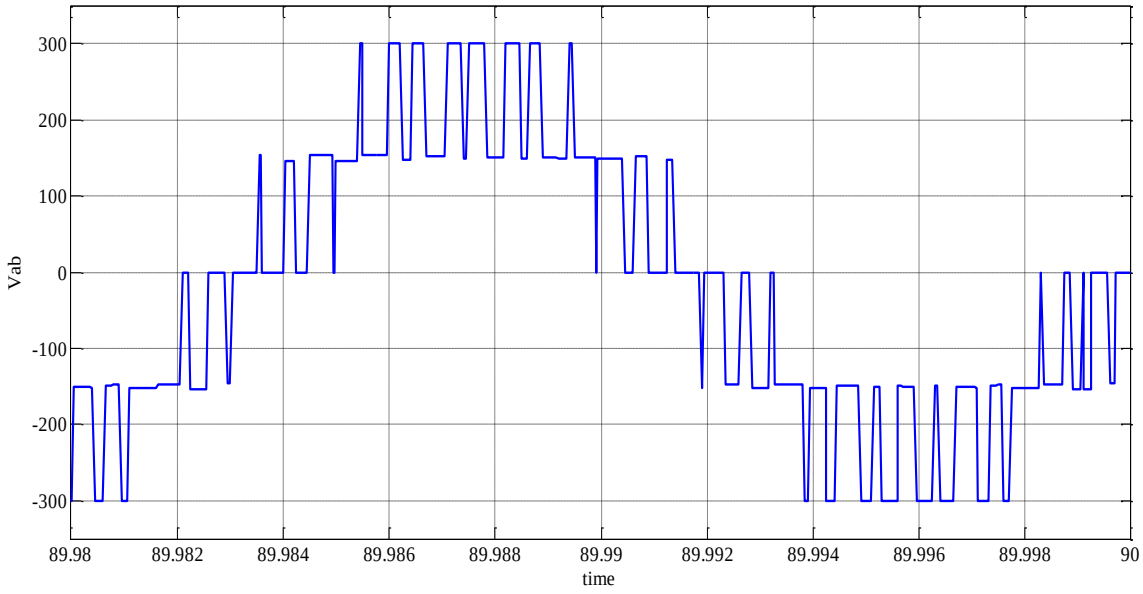


Fig. 6.8. Output voltage V_{ab}, with feedback technique

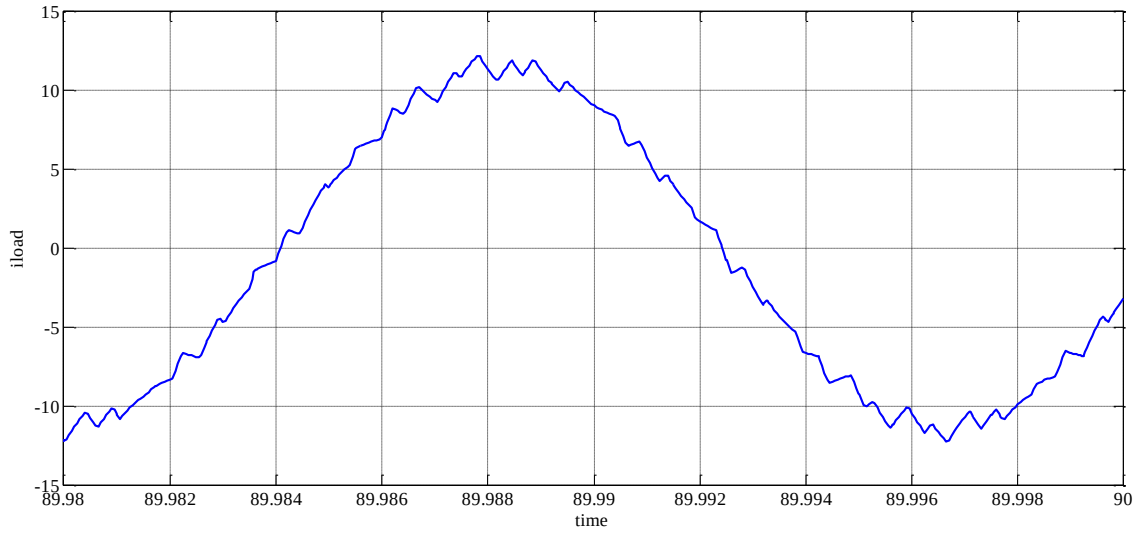


Fig. 6.9. Load current i_{load}, with feedback technique

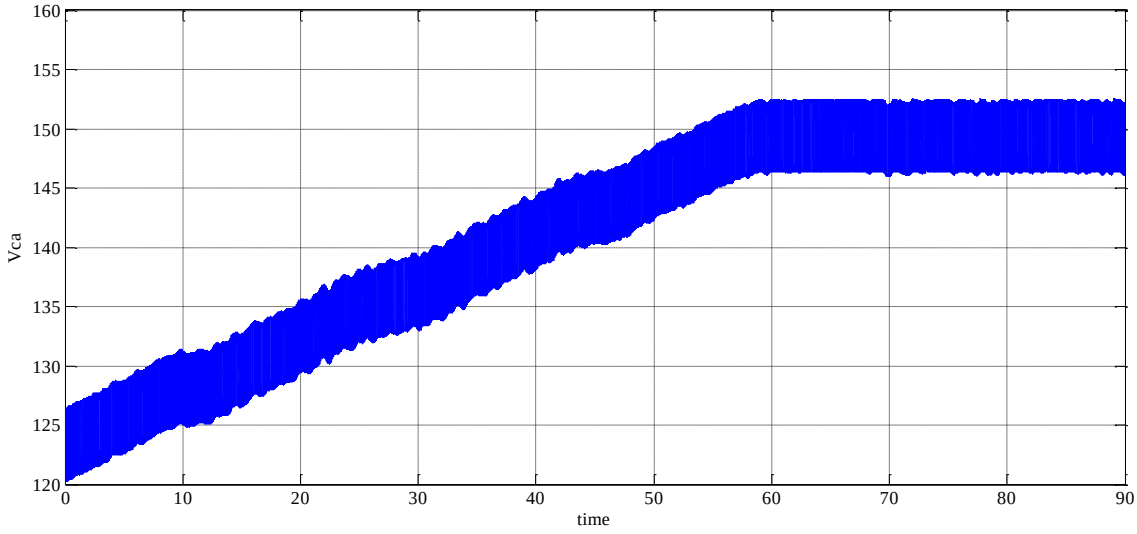


Fig. 6.10. Capacitor voltage on leg *a*, V_{ca}, with feedback technique

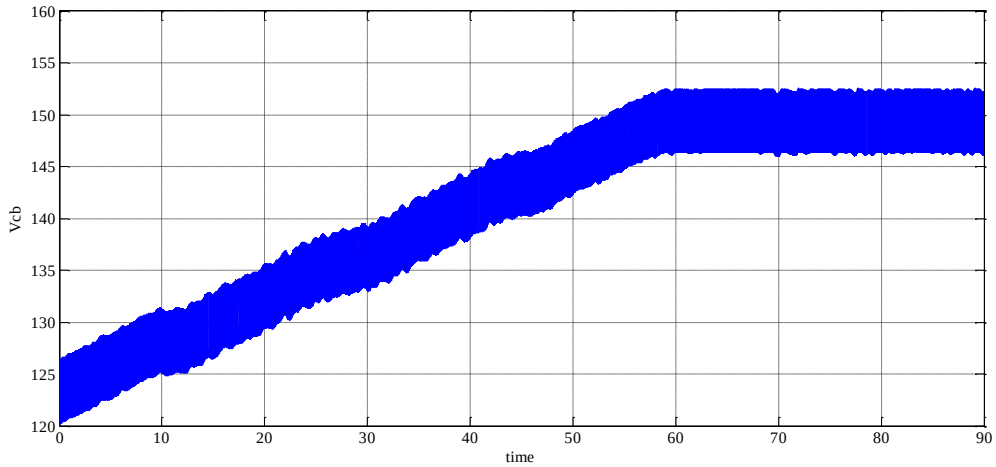


Fig. 6.11. Capacitor voltage on leg *b*, V_{cb}, with feedback technique

6.5. EFFECT OF LOAD CHANGE

The effect of sudden change in the load on capacitor voltages is shown in Figs. 6.12, and 6.13. The load has been decreased by five times at the instant of 1s. It is decreased from 20 Ω to nearly 4 Ω. A sudden change in the capacitor voltage can be observed at this instant. However, this is for a very short period of time, after which the capacitor voltages reach the desired value and are regulated around it. The increase in the load current because of the change in the load helps the capacitors to reach the desired value faster when compared to the longer time they take to recover in Figs. 6.10 and 6.11. This also is the reason for the increase in the peak-peak ripple of the capacitor voltages after the sudden change in load.

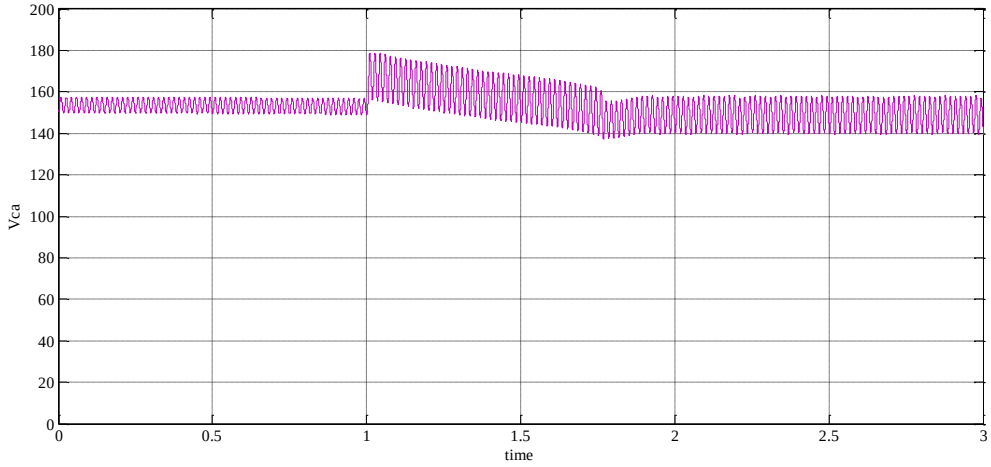


Fig. 6.12. Effect of sudden change in load on capacitor voltage V_{ca}

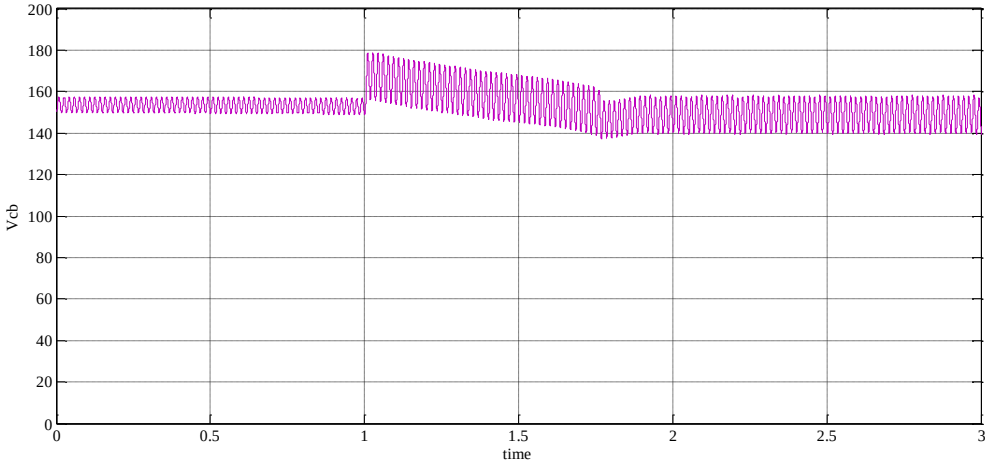


Fig. 6.13. Effect of sudden change in load on capacitor voltage V_{cb}

6.6. GENERALIZATION TO HIGHER LEVEL TOPOLOGIES

The concept of amplitude modulation adjustment (AMA) method can be extended to higher level flying capacitor multilevel inverter topologies. In a case where there are more than two carrier signal waveforms, the amplitude adjustment of more than one of them might be necessary. In such situations, a reference amplitude value which is equal

to the initial amplitude of the carrier signal waveforms is considered. Then, factor k_i by which the amplitude of the carrier signal has to be changed can be given by,

$$k_i = \frac{m_{csi}}{m_{ref}}$$

where, m_{csi} is the amplitude of the carrier signal i that has to be adjusted and m_{ref} is the reference amplitude as can be seen in Fig. 6.7.

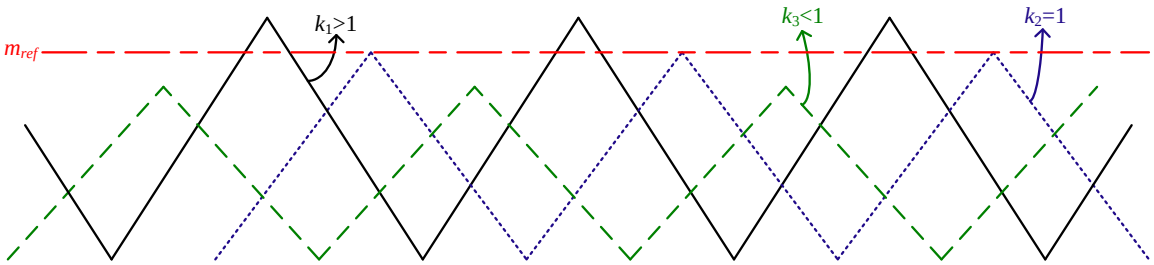


Fig. 6.14. Reference amplitude m_{ref} and carrier signal waveforms at different values of k_i

The same feedback technique described in the previous section which compares the capacitor voltages with a constant reference value and the error between which is used to decide upon the value of factor k, can be used for higher level FCMLI topologies as well. Figure 6.15 shows one leg of a seven-level flying capacitor multilevel inverter topology. It consists of three complementary switch pairs S_{a1} & S_{a1}', S_{a2} & S_{a2}', and S_{a3} & S_{a3}' and two clamping or flying capacitors C_{a1} and C_{a2}. The output voltage across terminals a and g, is a combination of algebraic sum of the dc link voltage V_{dc} and capacitor voltages V_{ca1} and V_{ca2}. The voltage arrangement is such that $V_{dc} = 2V_{ca1} = 4V_{ca2}$.

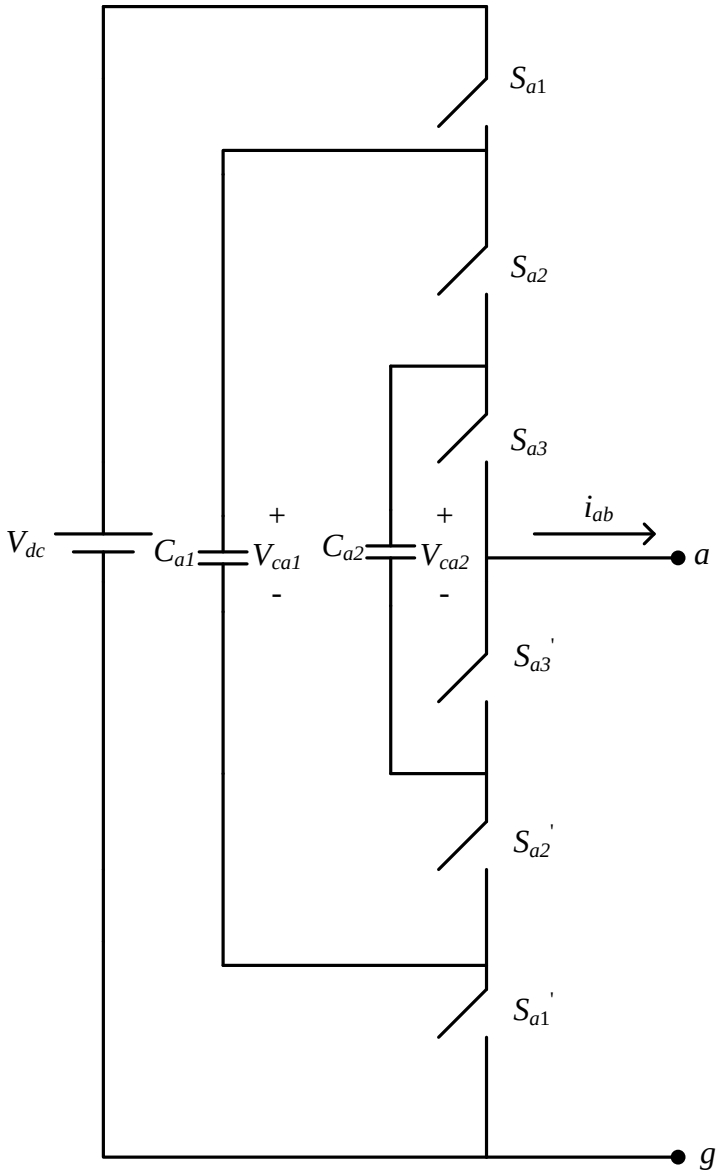


Fig. 6.15. Seven-level FCMLI topology

Figures 6.16, to 6.18 show the carrier signals, switching patterns and capacitor charging and discharging states for the considered topology with the reference signal at low, medium and high levels. Similar to the previous sections, a switch is ON when the reference signal is greater than its associated carrier signal. And, the current and voltage across the load are assumed to be in phase or the power factor is close to unity.

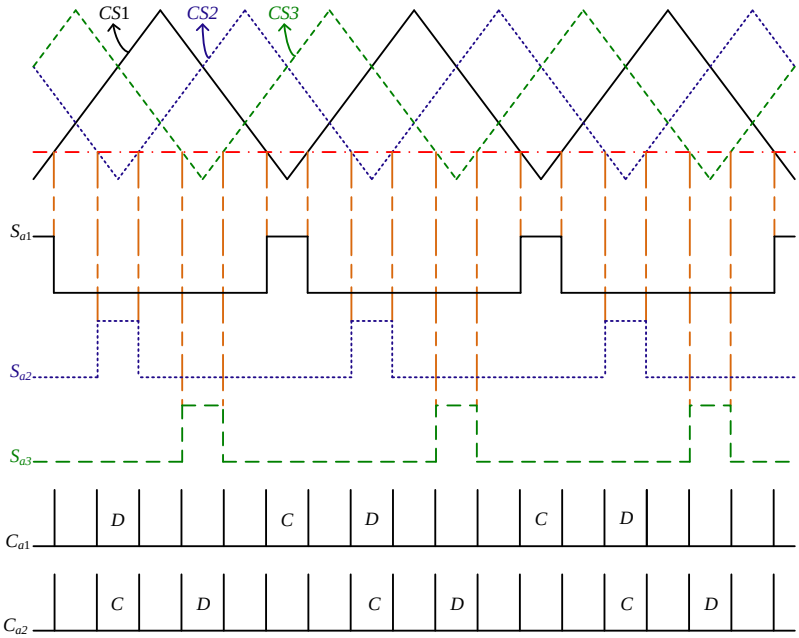


Fig. 6.16. Carrier signal waveforms, switching patterns and charging states of capacitors with reference signal at low level

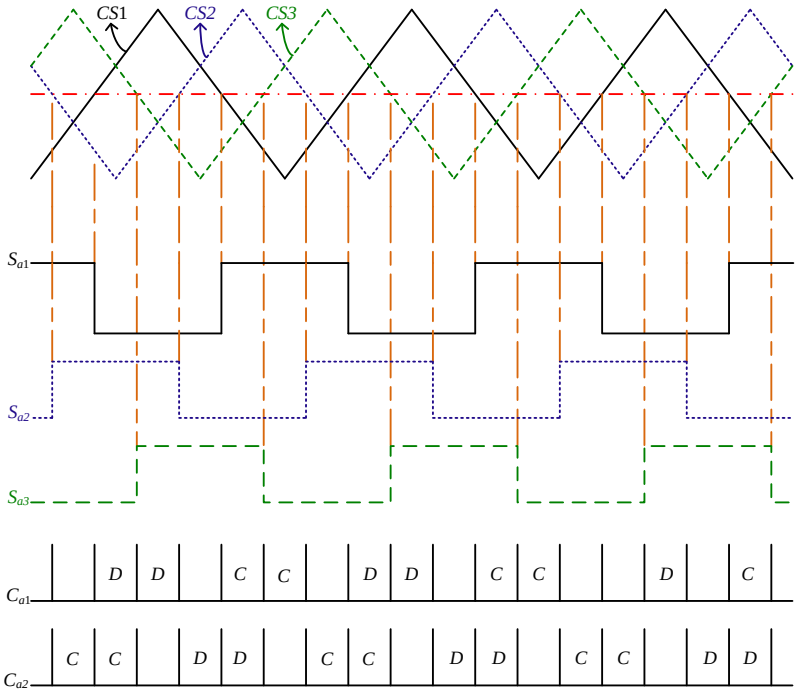
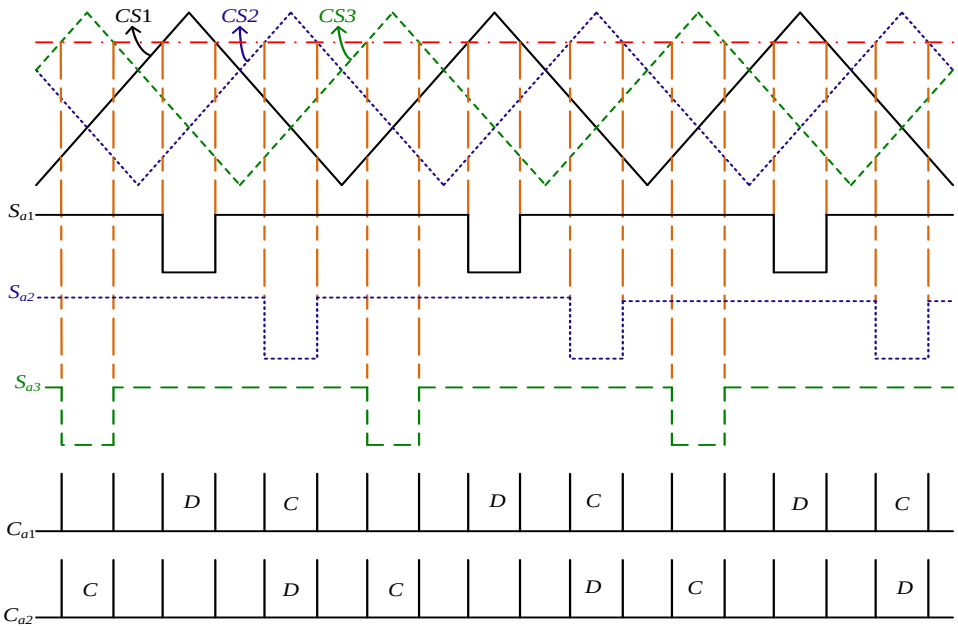


Fig. 6.17. Carrier signal waveforms, switching patterns and charging states of capacitors with reference signal at medium level



Figs. 6.18. Carrier signal waveforms, switching patterns and charging states of capacitors with reference signal at high level

It can be observed from the switching pattern that if the amplitude of first carrier signal *CS*1 is increased, capacitor C_{a1} is charged less and when the amplitude is decreased, the capacitor is charged more. Similarly, capacitor C_{a2} is charged more if the amplitude of carrier signal *CS*3 is increased. Therefore, the capacitor voltages can be well regulated by changing the amplitude of the corresponding carrier signals by using the amplitude modulation adjustment (AMA) technique.

In a similar fashion, the AMA method can be extended to an N-level flying capacitor multilevel inverter topology by considering reference amplitude and changing the amplitude of the corresponding carrier signals by a factor *k* which depends on the error between the desired and actual capacitor voltages.

7. HARMONIC ANALYSIS AND ADVANTAGES OF PROPOSED METHODS

A harmonic of a signal is defined as the component of that particular waveform with a frequency which is an integral multiple of the fundamental frequency. Total harmonic distortion (THD) is the measurement of the harmonic distortion present in the waveform and is defined as the ratio of the rms value of all non-fundamental frequency harmonic components to that of the fundamental frequency

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1}$$

where, V_n is the rms voltage at the n^{th} harmonic frequency, and V_1 is the rms voltage at the fundamental frequency.

For the considered FCMLI topology, the output voltage V_{ab}, across the load contains significant harmonics because of its various characteristics like not being purely sinusoidal, multilevel structure, and type of load. This leads to many complications when being used in industry applications like overheating of motors, undesired vibrations or mechanical resonance, etc. The use of filters to reduce or eliminate these harmonics is again a concern for design as it involves additional cost and size to the inverter topology. Therefore, it is required that the total harmonic distortion is relatively low and within a desired acceptable range. This section compares the harmonic analysis of the output voltage of the considered single-phase five-level FCMLI topology shown in Fig. 2.1, for different control techniques discussed earlier in this thesis.

7.1. HARMONIC ANALYSIS OF SINGLE-PHASE FIVE-LEVEL FCML INVERTER

Harmonic content present in the output voltage V_{ab} depends on the control technique used to obtain the switching pattern. Therefore, it varies with different kinds of techniques used for generating these switching pulses. Figures 7.1-7.28 show the voltage harmonic spectra for various control schemes like staircase modulation, phase disposition pulse width modulation (PDPWM), natural balancing using phase shifted pulse width modulation (PSPWM), etc, and the proposed techniques split natural balancing method, and feedback control using amplitude modulation adjustment technique. Harmonic spectra are obtained by performing FFT analysis using Matlab Simulink.

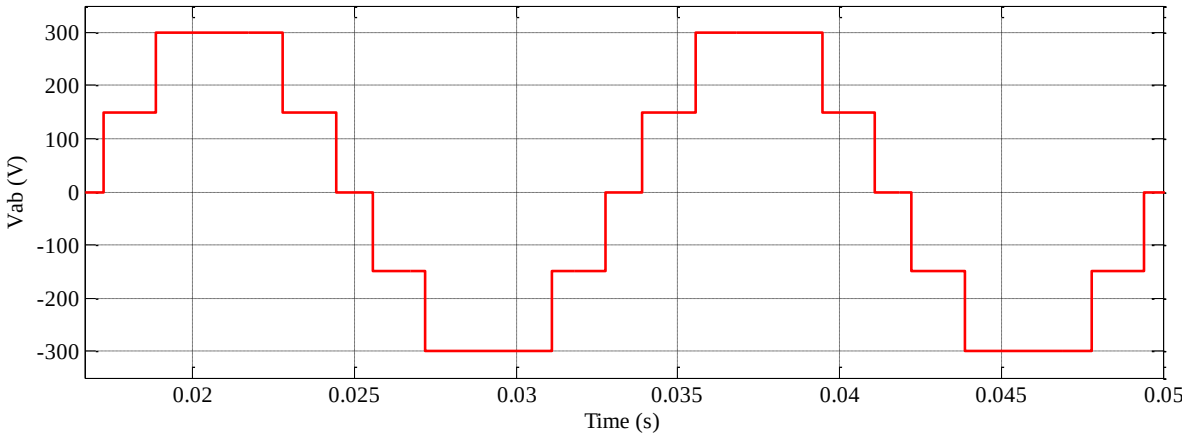


Fig. 7.1. Output voltage when staircase modulation technique is used for capacitor voltage regulation

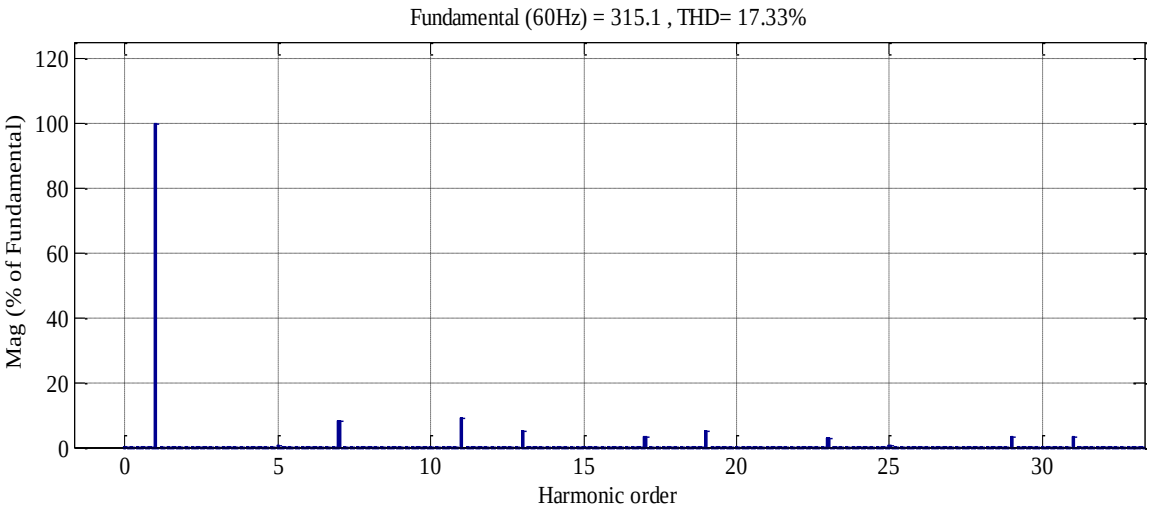


Fig. 7.2. Voltage harmonic spectrum when staircase modulation technique is used for capacitor voltage regulation

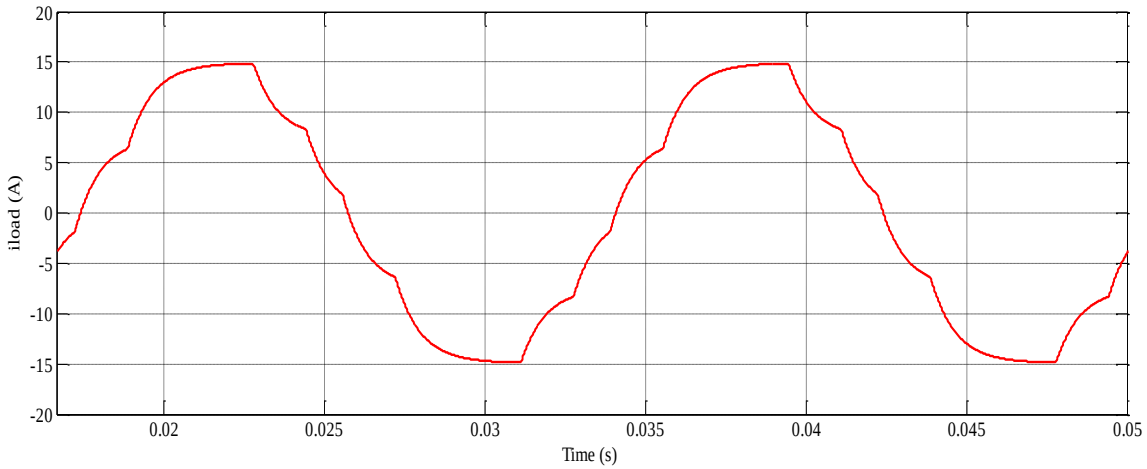


Fig. 7.3. Load current when staircase modulation technique is used for capacitor voltage regulation

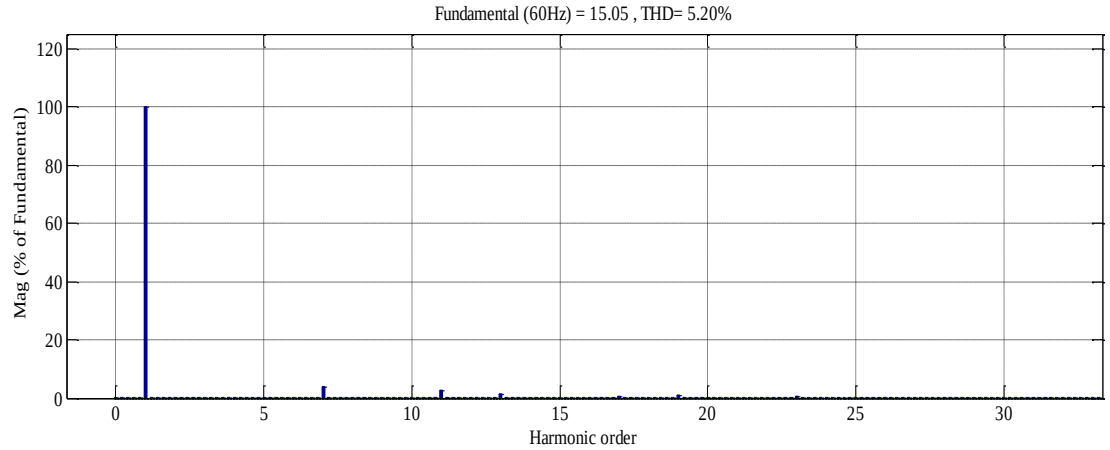


Fig. 7.4. Current harmonic spectrum when staircase modulation technique is used for capacitor voltage regulation

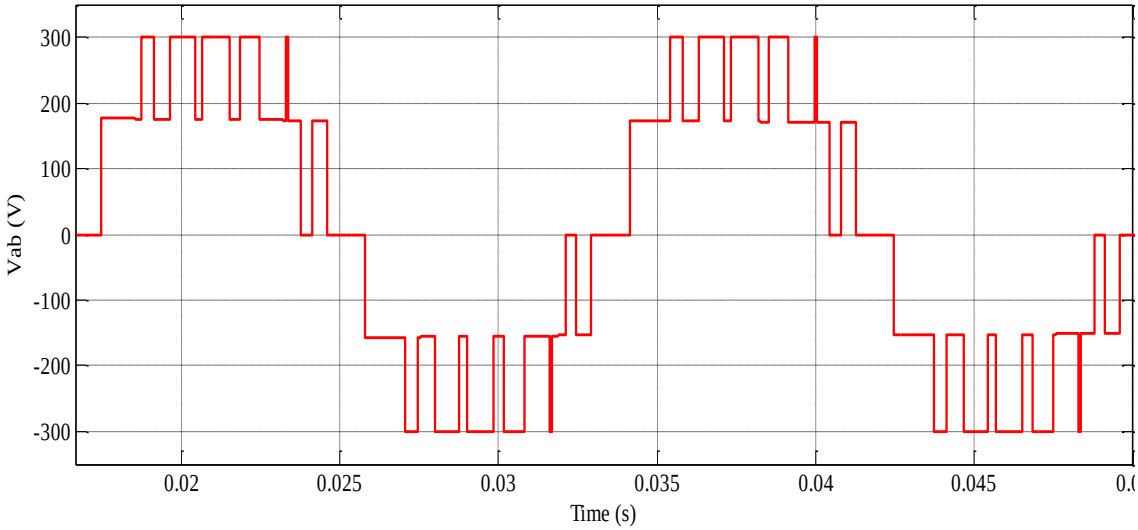


Fig. 7.5. Output voltage when PDPWM technique is used for capacitor voltage regulation

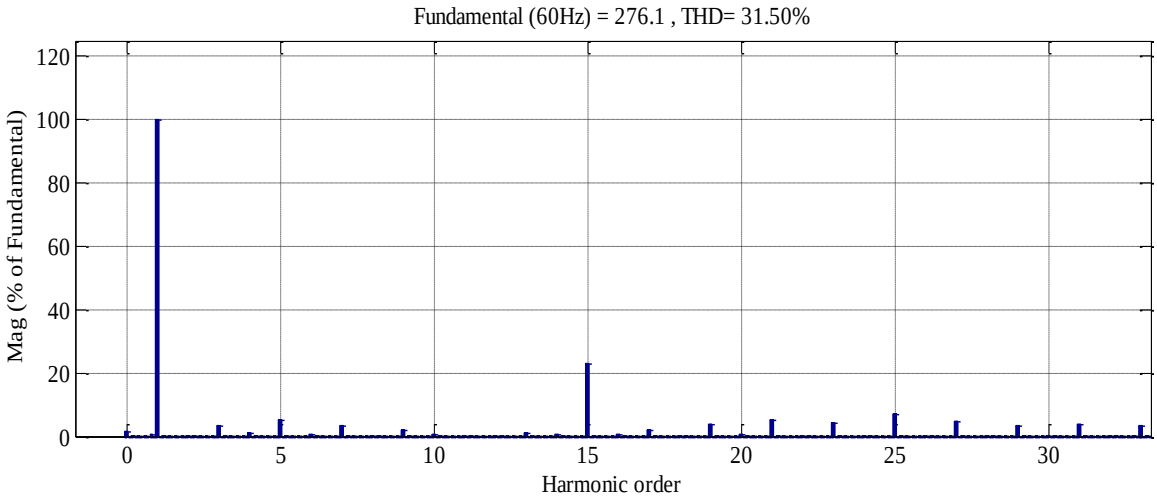


Fig. 7.6. Voltage harmonic spectrum when PDPWM technique is used for capacitor voltage regulation

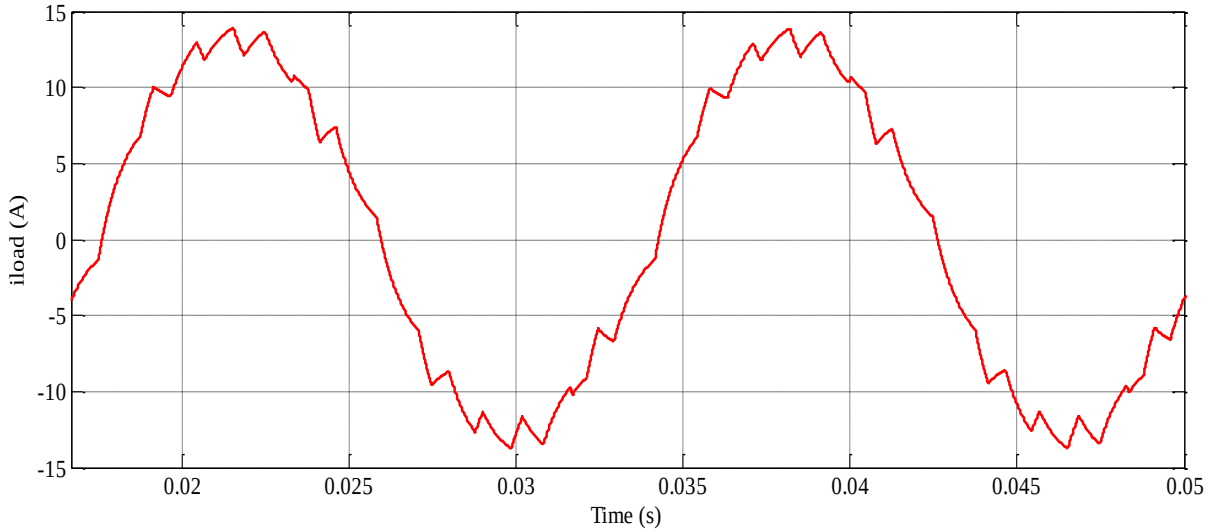


Fig. 7.7. Load current when PDPWM technique is used for capacitor voltage regulation

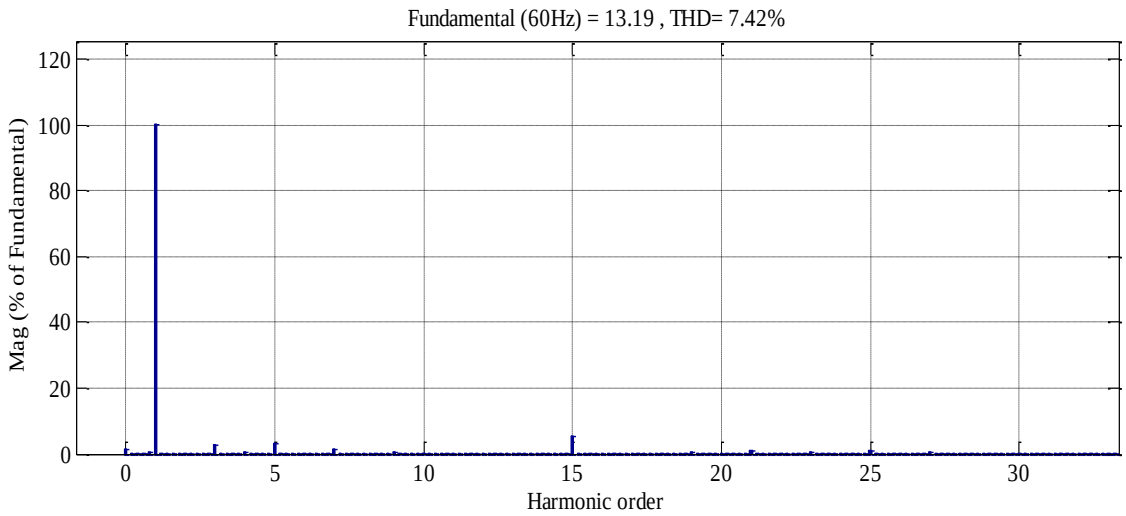


Fig. 7.8. Current harmonic spectrum when PDPWM technique is used for capacitor voltage regulation

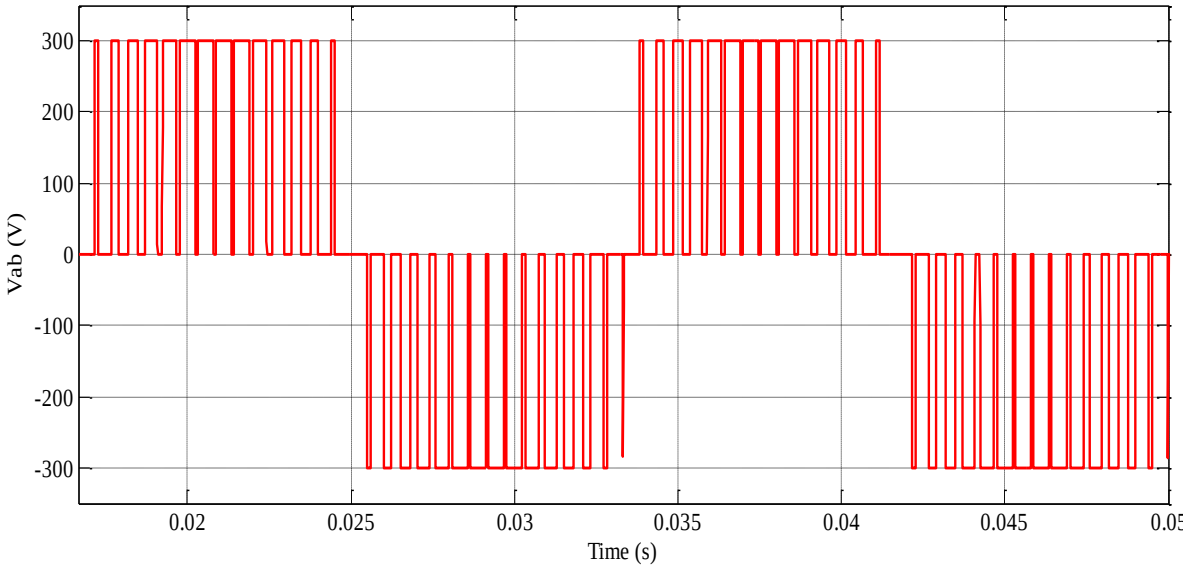


Fig. 7.9. Output voltage when PSPWM (natural balancing) technique is used for capacitor voltage regulation

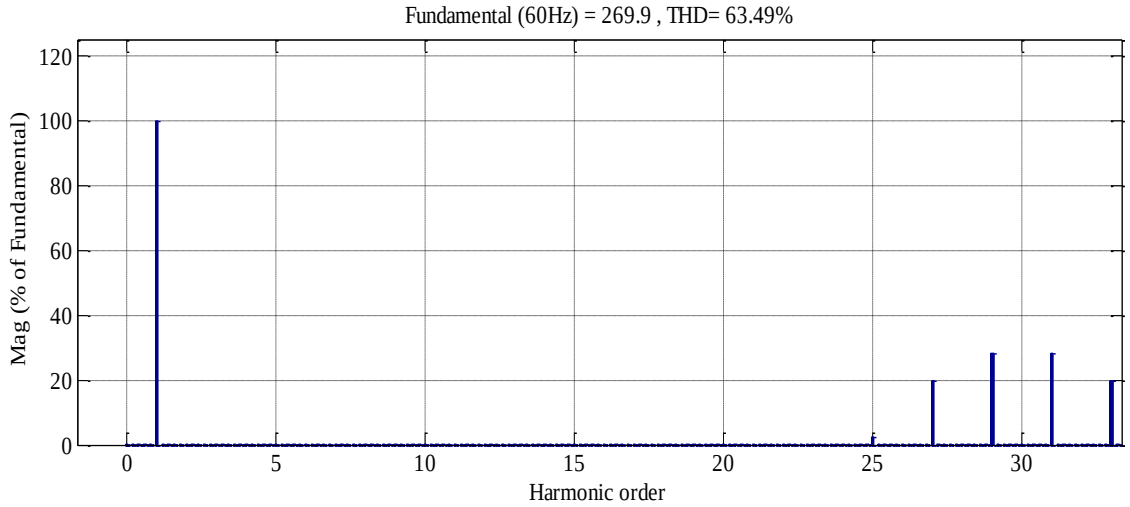


Fig. 7.10. Voltage harmonic spectrum when PSPWM (natural balancing) technique is used for capacitor voltage regulation

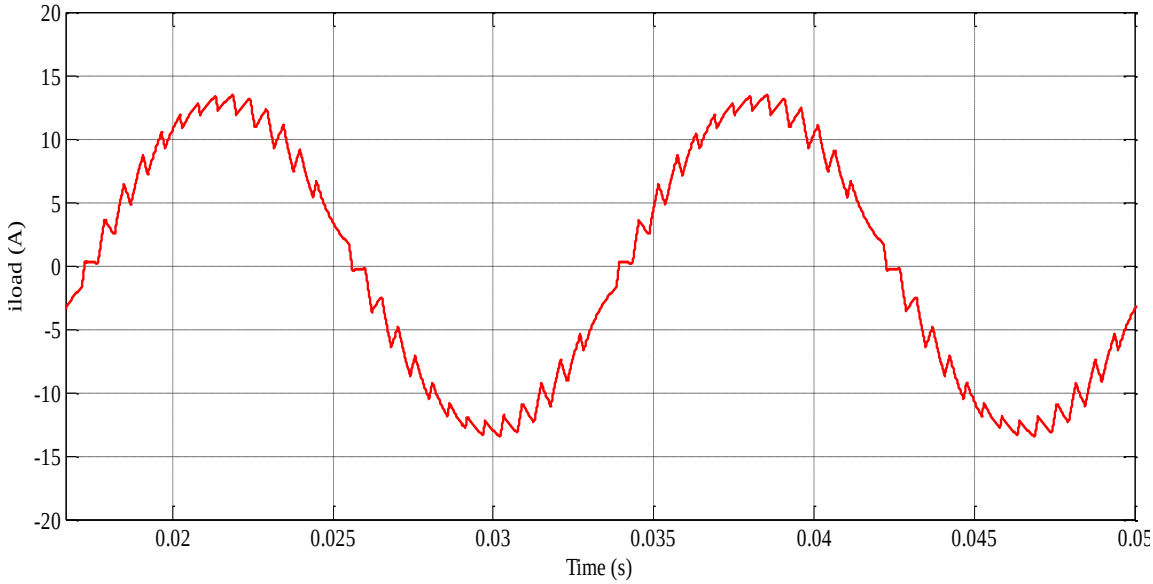


Fig. 7.11. Load current when PSPWM (natural balancing) technique is used for capacitor voltage regulation

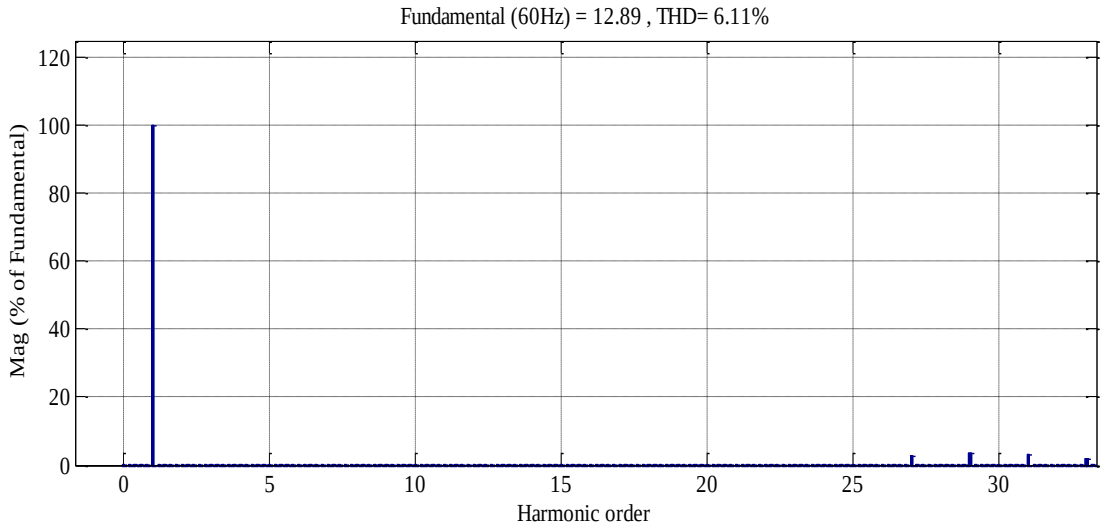


Fig. 7.12. Current harmonic spectrum when PSPWM (natural balancing) technique is used for capacitor voltage regulation

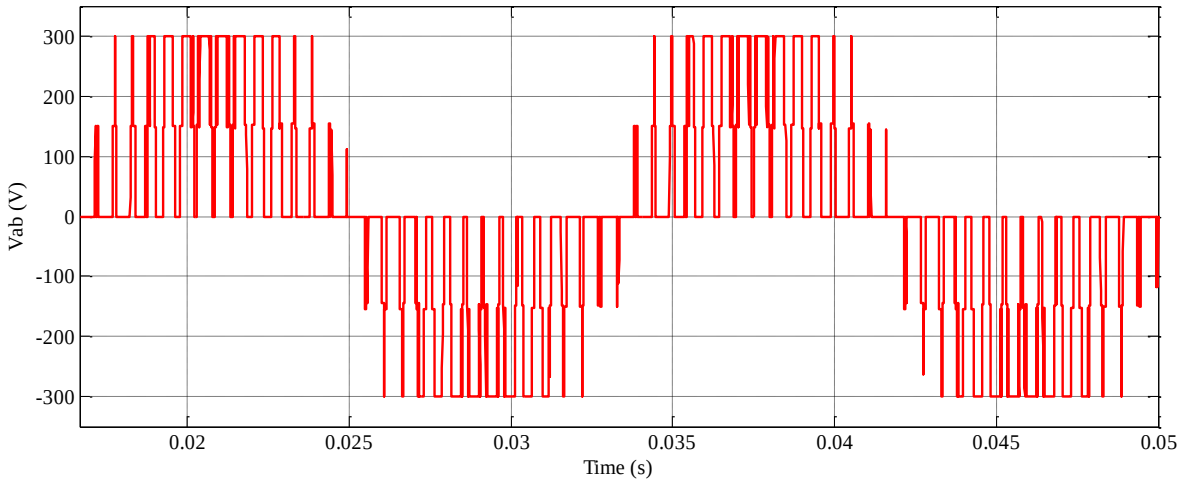


Fig. 7.13. Output voltage when PSPWM (natural balancing) technique is used for capacitor voltage regulation with modified carrier signal described in [75]

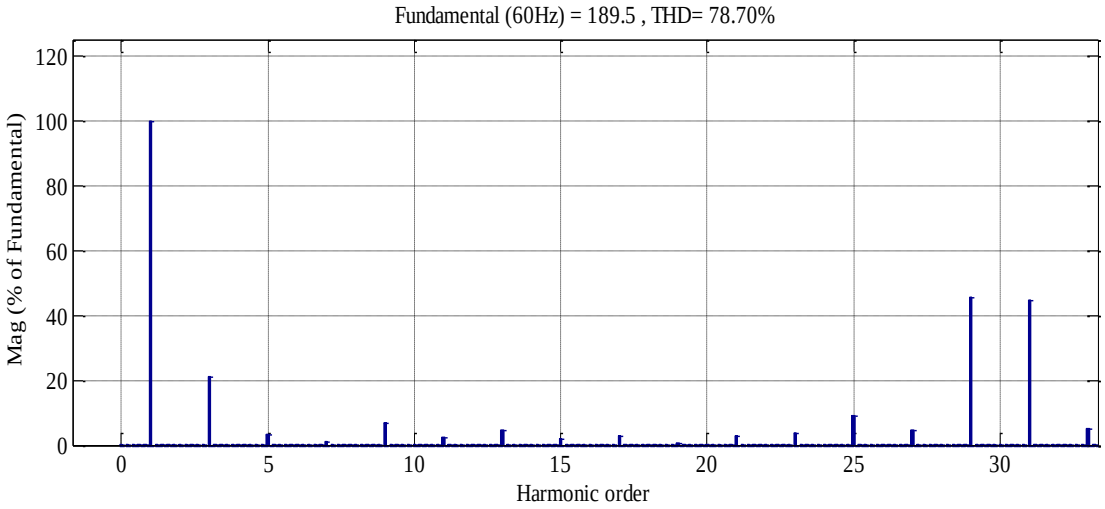


Fig. 7.14. Voltage harmonic spectrum when PSPWM (natural balancing) technique is used for capacitor voltage regulation with modified carrier signal described in [75]

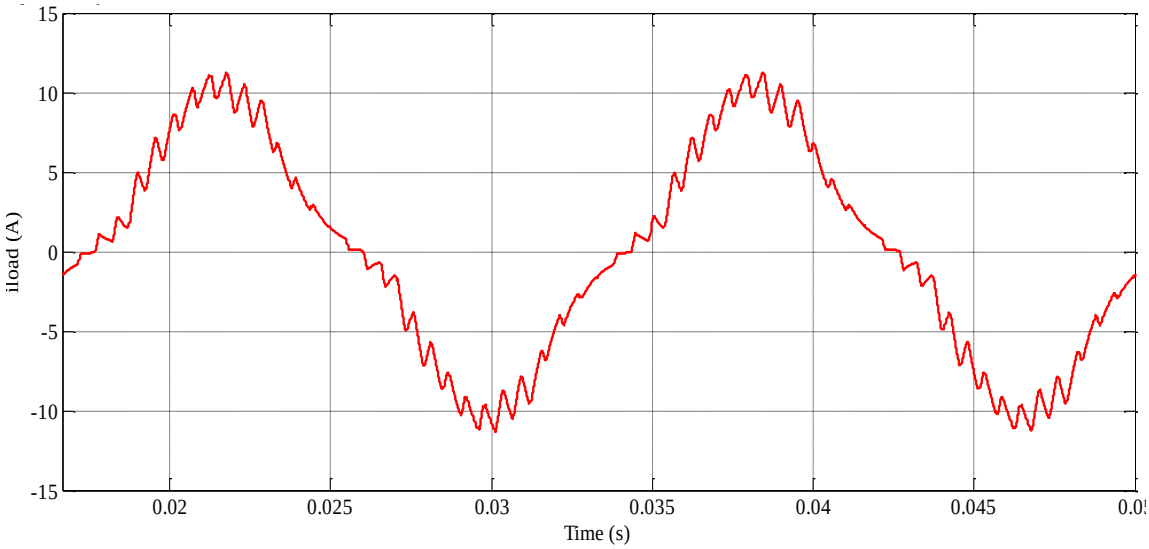


Fig. 7.15. Load current when PSPWM (natural balancing) technique is used for capacitor voltage regulation with modified carrier signal described in [75]

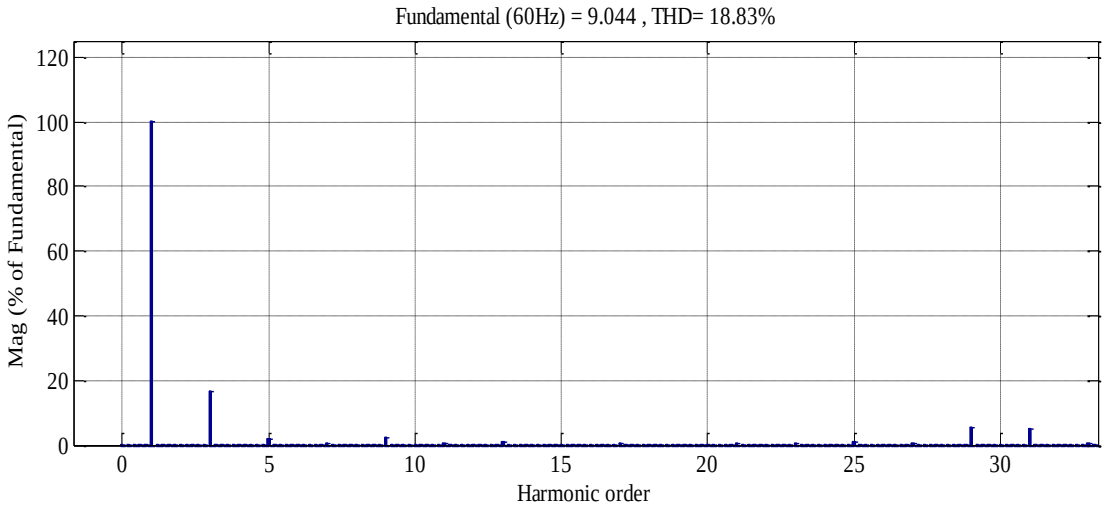


Fig. 7.16. Current harmonic spectrum when PSPWM (natural balancing) technique is used for capacitor voltage regulation with modified carrier signal described in [75]

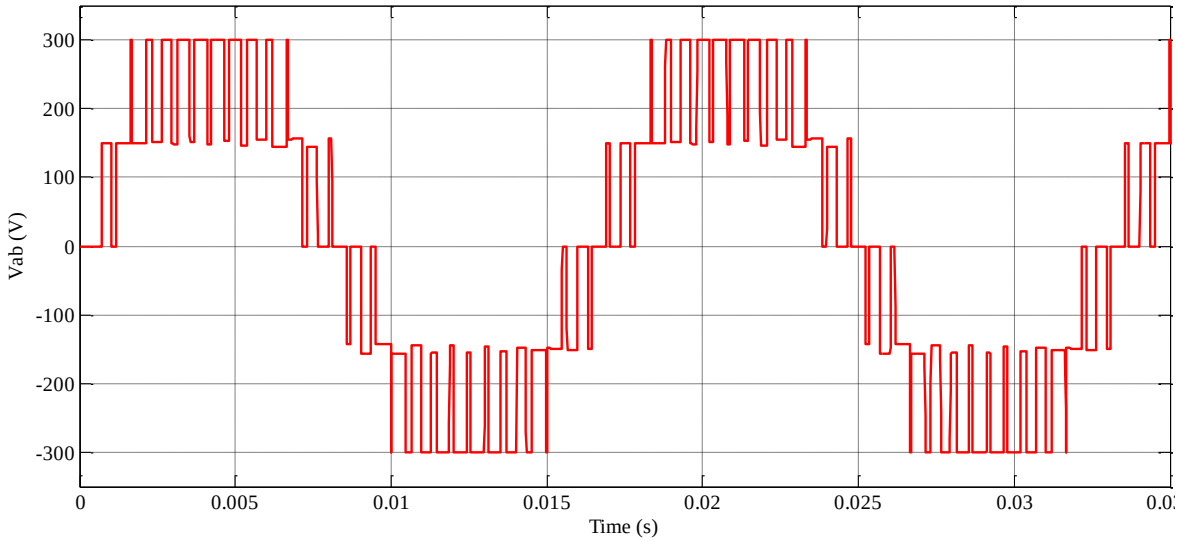


Fig. 7.17. Output voltage when split natural balancing technique is used for capacitor voltage regulation

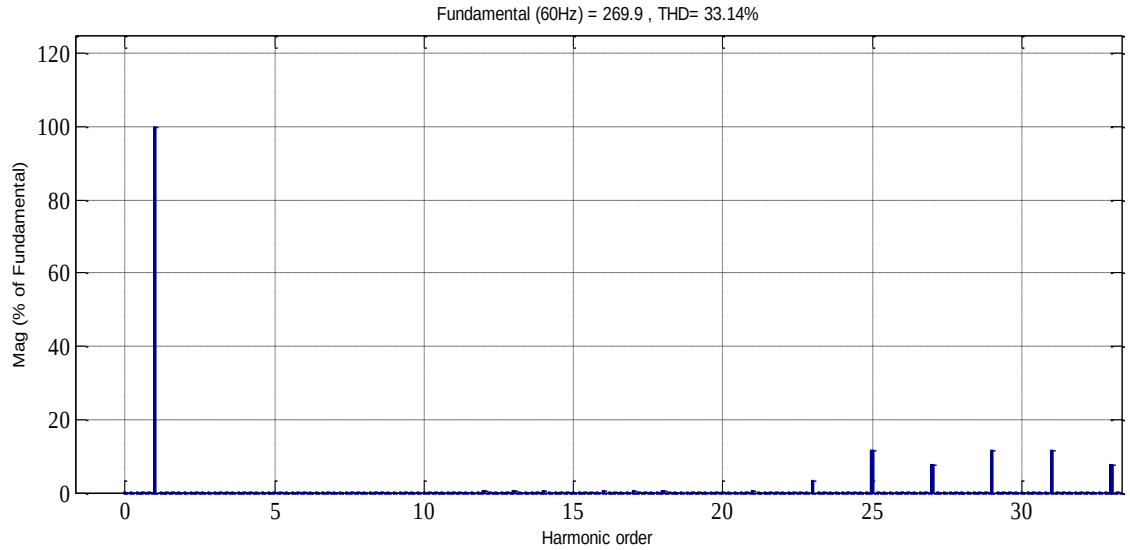


Fig. 7.18. Voltage harmonic spectrum when split natural balancing technique is used for capacitor voltage regulation

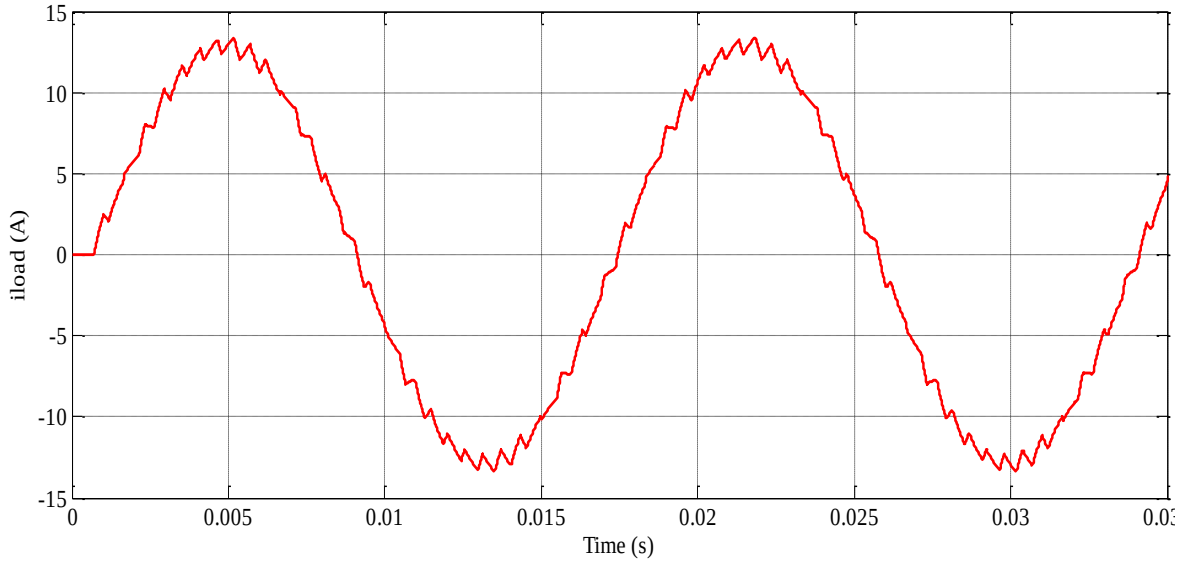


Fig. 7.19. Load current when split natural balancing technique is used for capacitor voltage regulation

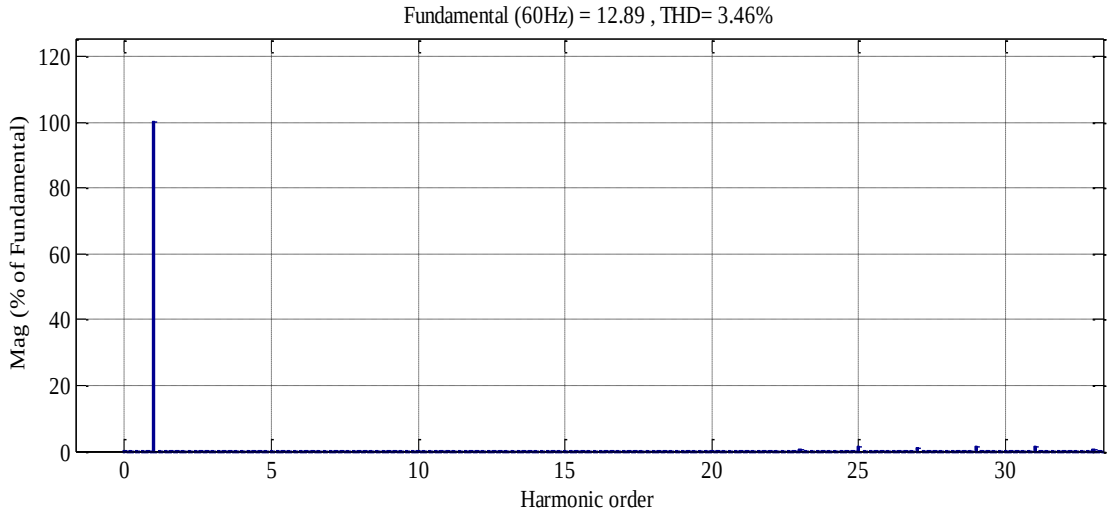


Fig. 7.20. Current harmonic spectrum when split natural balancing technique is used for capacitor voltage regulation

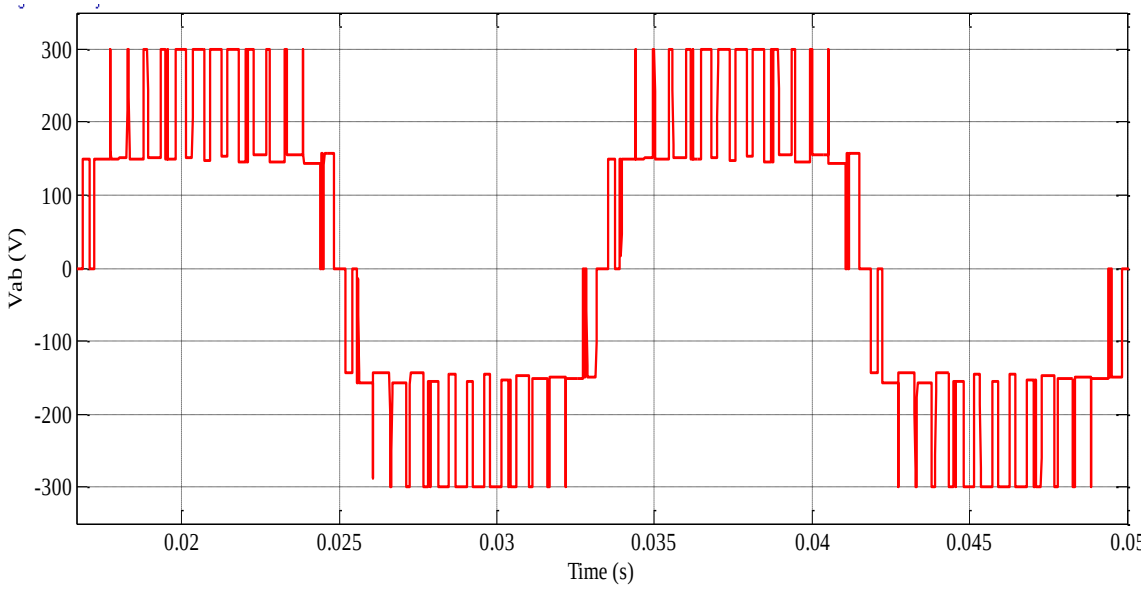


Fig. 7.21. Output voltage when split natural balancing technique is used for capacitor voltage regulation with modified carrier signal described in [75]

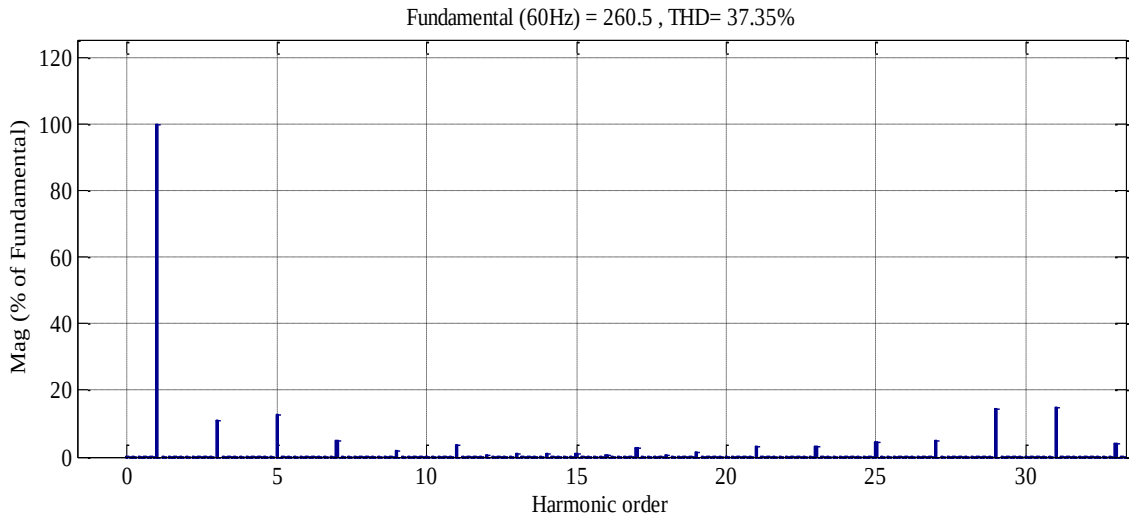


Fig. 7.22. Voltage harmonic spectrum when split natural balancing technique is used for capacitor voltage regulation with modified carrier signal described in [75]

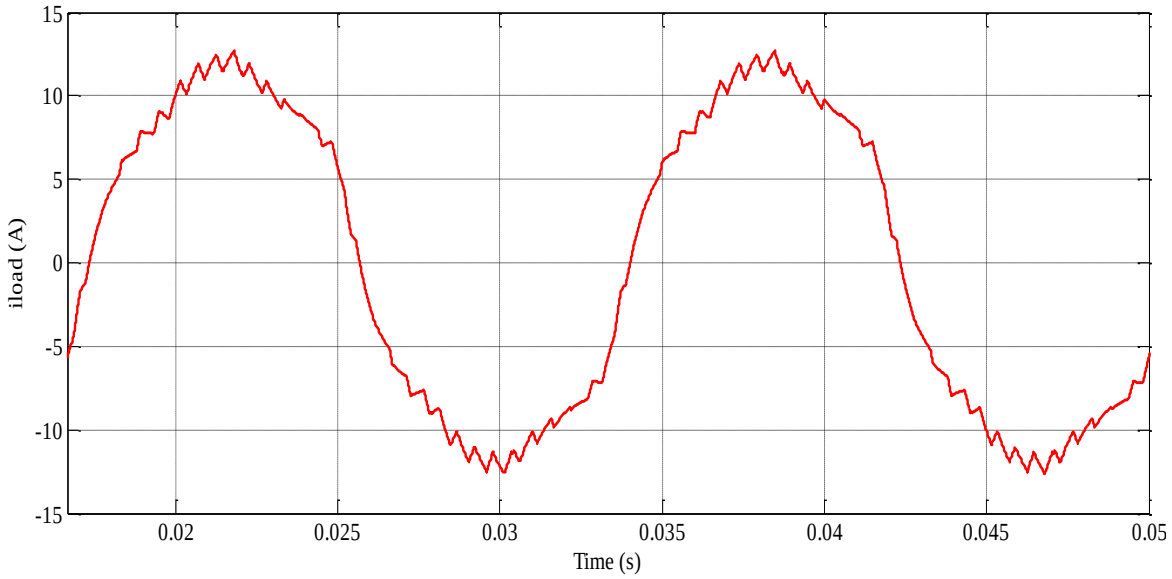


Fig. 7.23. Load current when split natural balancing technique is used for capacitor voltage regulation with modified carrier signal described in [75]

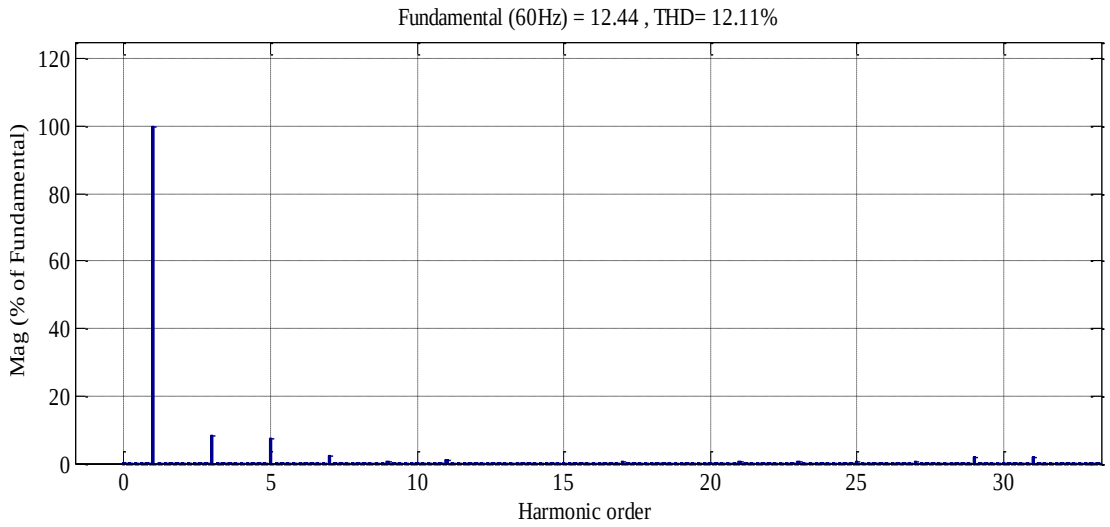


Fig. 7.24. Current harmonic spectrum when split natural balancing technique is used for capacitor voltage regulation with modified carrier signal described in [75]

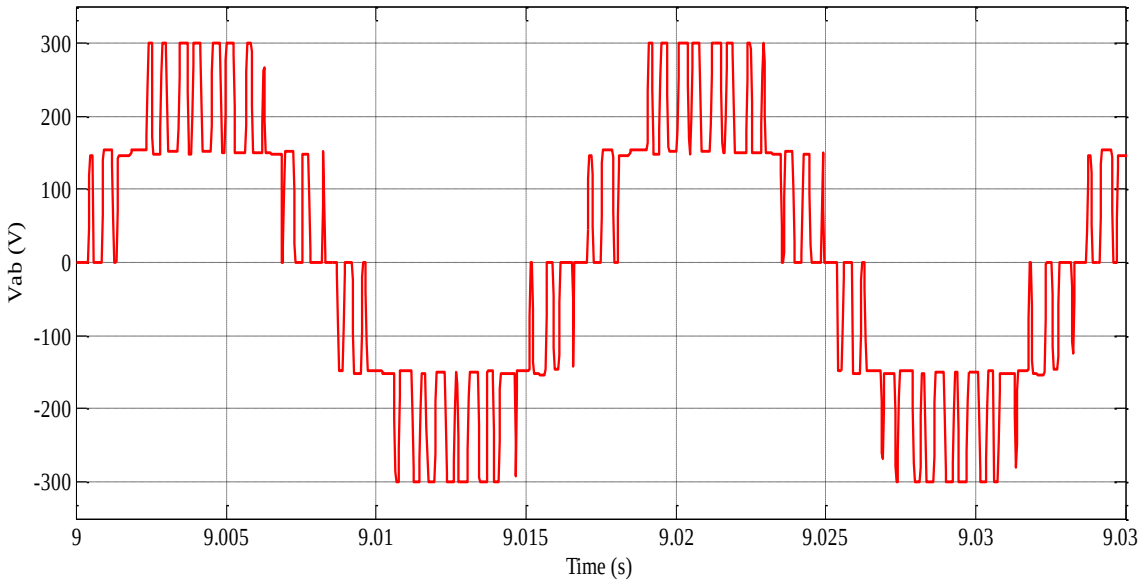


Fig. 7.25. Output voltage when feedback technique along with AMA method is used for capacitor voltage regulation

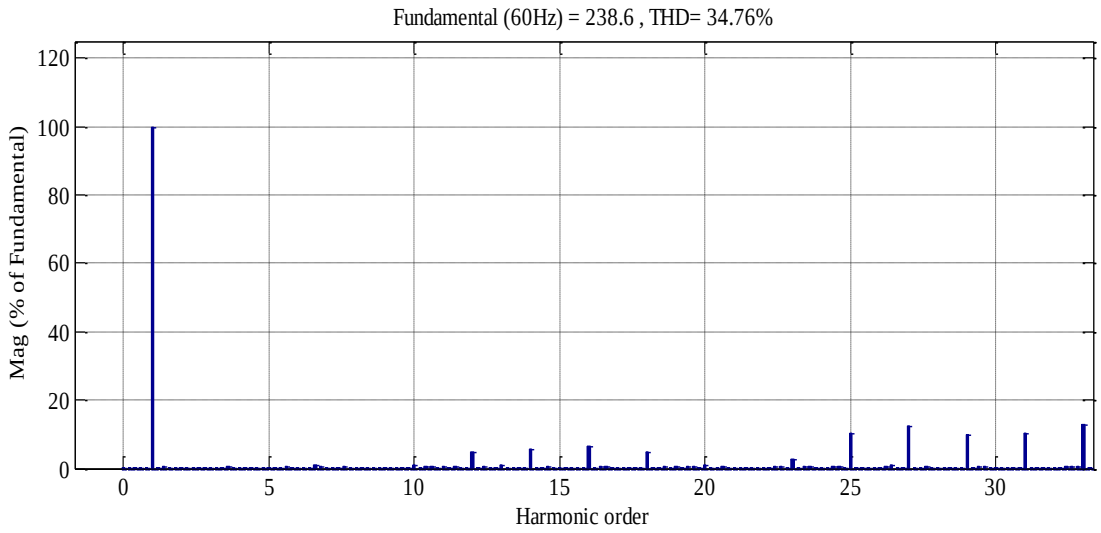


Fig. 7.26. Voltage harmonic spectrum when feedback technique along with AMA method is used for capacitor voltage regulation

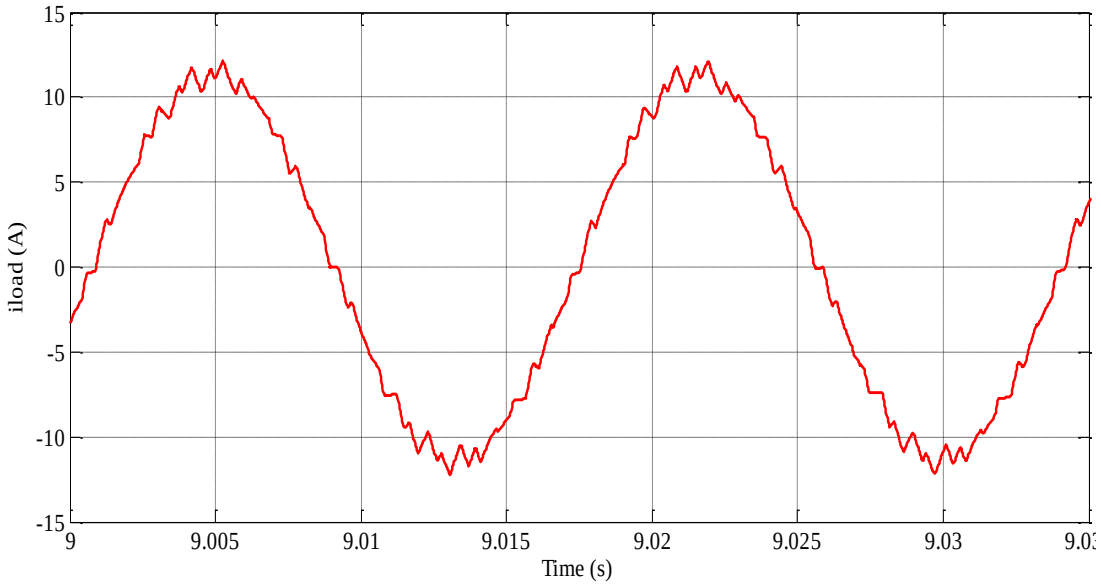


Fig. 7.27. Load current when feedback technique along with AMA method is used for capacitor voltage regulation

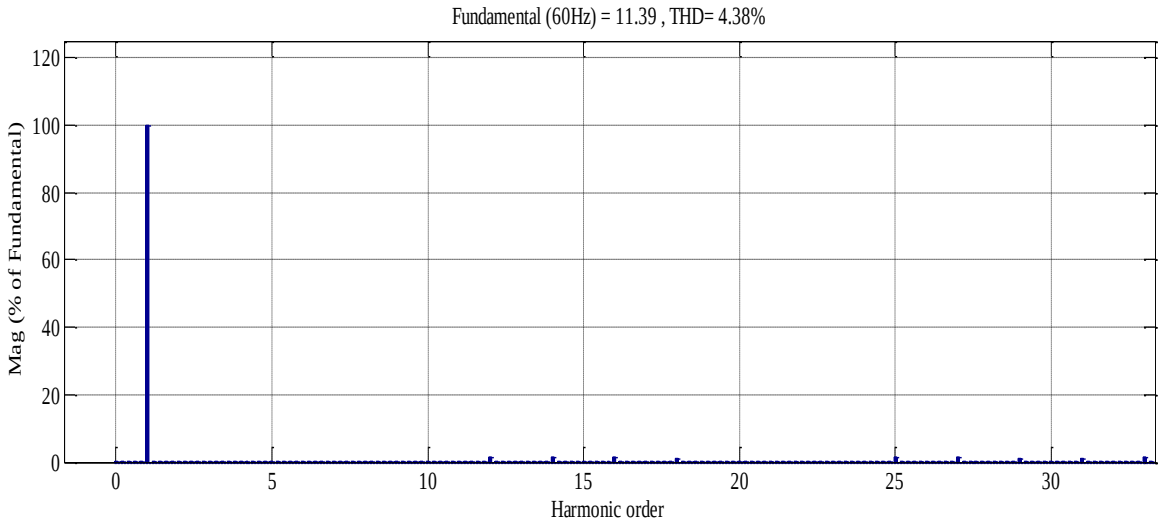


Fig. 7.28. Current harmonic spectrum when feedback technique along with AMA method is used for capacitor voltage regulation

The comparison of the harmonic analysis done on output voltage and load current with different control techniques are tabulated in Table 7.1, and Table 7.2, respectively. They show the amplitude of the fundamental component of load current i_{load} and output voltage V_{ab} and the percentage total harmonic distortion for the same.

Table 7.1
Comparison of various controlling techniques based on voltage harmonic analysis

Controlling Technique	Amplitude of Fundamental Component	%THD
Staircase Modulation	315.1	17.33
PDPWM	270	33.18
PSPWM	269.9	63.50
PSPWM with Modified Carrier Signal	189.5	78.69
Split Natural Balancing	270	33.31
Split Natural Balancing with Modified Carrier Signal	260.5	37.35
Feedback Technique using AMA method	239.4	34.58

Table 7.2
Comparison of various controlling techniques based on current harmonic analysis

Controlling Technique	Amplitude of Fundamental Component	%THD
Staircase Modulation	15.05	5.20
PDPWM	13.19	7.42
PSPWM	12.89	6.11
PSPWM with Modified Carrier Signal	9.044	18.83
Split Natural Balancing	12.89	3.46
Split Natural Balancing with Modified Carrier Signal	12.44	12.11
Feedback Technique using AMA method	11.39	4.38

The presence of high harmonics in the waveform is not desirable for many reasons mentioned in the above paragraphs. Therefore, the %THD has to be as low as possible. It can be observed from the tables that split natural balancing and phase disposition PWM techniques provide the lowest %THD when compared to other techniques. The amplitude of their fundamental component is also 90% of the highest amplitude of the output voltage waveform which is as desired. Though, the %THD obtained using staircase modulation or split natural balancing implemented using a modified carrier signal as explained in [75] is relatively close enough, it is not as low as the %THD obtained by using the proposed methods and the amplitude of fundamental component is better. Harmonic content in the output voltage can be reduced by implementing different methods such as mentioned in [76, 77], etc.

7.2. ADVANTAGES OF SPLIT NATURAL BALANCING AND AMA METHODS

Several methods have been developed for capacitor voltage regulation in flying capacitor multilevel inverters. Natural balancing technique which is implemented by using the phase shifted pulse width modulation is considered to be the simplest of all. However, it has some disadvantages as discussed in the previous sections and this calls for developing a relatively simpler technique for capacitor voltage regulation. There is a lot of research being done in this aspect and several papers have been published on methods similar to natural balancing with few modifications done.

Split natural balancing proposed in this thesis, which uses the Unipolar PWM method for generating the switching pulses is one such method. It is easy to implement with no modifications made to the carrier signals and the only difference from the

conventional natural balancing method is the usage of Unipolar PWM technique. It is clear from the figures and table above that it provides relatively lower level of harmonic content in the output voltage waveform. Though, PDPWM technique described in the thesis also gives desired results and acceptable harmonics, the requirement of four triangular carrier signal waveforms disposed in contiguous bands makes the method complicated to implement. And in addition, resolving the problem of capacitor voltages reaching the desired value instead of being regulated around their initial values can be difficult.

Split natural balancing technique eliminates this need for increased number of carrier signals disposed from each other, avoids the aspect of measuring capacitor voltages or polarity of load current as required in staircase modulation, and is simple in its implementation not requiring any change in the shape of the carrier signal waveforms as in [75]. Moreover, it provides feasibility to adjust the amplitude of the carrier signals waveforms which helps in regulating the capacitor voltages when their initial value is not at the desired level. Amplitude modulation adjustment method is used during this time when there is a requirement for making the capacitor voltages reach the desired value. It is easy to implement with simple control logic as described in Fig. 6.6. It also works in regulating capacitor voltages during sudden changes in load and can be applied to higher level topologies accordingly. All these aspects make split natural balancing and AMA methods very effective for balancing the capacitor voltages in an FCMLI circuit.

8. CONCLUSION

With the popularity they gained as easy alternatives for high power apparatus in industry, multilevel converters demand the development of more feasible topologies and control techniques. Few such topologies like diode-clamped, cascaded H-bridge cell, flying capacitor, and hybrid multilevel converters and their applications in industry are discussed. One of these topologies, the flying capacitor multilevel inverter is concentrated in this thesis. Existing techniques for the capacitor voltage regulation such as the natural balancing technique, phase-disposition sinusoidal PWM, of a single-phase, five-level flying capacitor multilevel inverter have been discussed. Though these methods regulate the capacitor voltages, there are several disadvantages associated with them. The staircase modulation technique requires measurement of the capacitor voltages and load current polarity, PDPWM has the drawback of requiring more number of carrier signal waveforms disposed in contiguous bands, natural balancing technique does not provide all the desired levels at the output voltage, etc. To overcome these, a new method called split natural balancing technique is proposed in this thesis which is similar to natural balancing in its implementation with the only difference being developed based on the Unipolar sinusoidal PWM. Moreover, with feedback which uses the amplitude modulation adjustment method devised, it helps to maintain the capacitor voltages at the desired value during times of undesired initial voltages, and sudden changes in the load. Generalization of the proposed methods to higher level flying capacitor multilevel inverters is explained. Harmonic analysis for the implemented methods is performed and compared, and the advantages of the proposed methods have been discussed.

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