An X-band MMIC Low Noise Amplifier Design with $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ pHEMT

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***Abstract*—A low noise amplifier (LNA) design operating at X-band frequency range of 8 – 12 GHz using 0.25 µm $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ pHEMT is presented. The target specifications of the MMIC LNA design are then addressed, the performance constraints and compromises that arise in the design of circuit topologies, biasing networks and matching configurations are also discussed. The design and analysis of the single input single-ended output, single and double stage LNAs are presented using all of the criteria. The simulations setup successfully showed an X-band LNAs are designed to match a 50 Ω input and output impedance. The proposed design is an MMIC LNA that combines high performance with low cost and avoids expensive external components.**

***Index Terms*—InGaAs/InAlAs pHEMT; Low Noise Amplifier; MMIC; X-band.**

I. Introduction

The low noise amplifier (LNA) is a crucial component in RF transceiver design which characterizes the whole performance of the RF receiver. It is the most important block in any receiving system because the receiving system sensitivity is generally determined by its gain and noise figure (NF). Most of the high-frequency LNAs, such as those used in L-band, X-band and Ku-band are designed with CMOS, JFET, pHEMT and MESFET technologies [1-3]. In general, the noise figure, available gain, and stability over a wide range of frequency are key elements in LNA designs. Low NF without adequate gain or poor return loss degrades system performance while high gain without adequate NF also compromises system performance [4-5]. Current development of InP based InAlAs/InGaAs High Electron Mobility Transistors (HEMTs) have demonstrated excellent high frequency and high-gain performance which dominates the microwave and millimetre wave (mm-wave) applications, i.e. in LNAs [6-8] and sensor/radar [9]. The superior performance of InP based InAlAs/InGaAs pseudormophic High Electron Mobility Transistors (pHEMTs) makes them the most preferred candidates for active devices selection and a significant aspect in the fabrication of Monolithic Millimeter Wave Integrated Circuit (MMIC) LNAs. The design of MMIC LNAs itself has emerged from the design for very low frequency, low noise figure, very high power, etc.

The main goal of this research is to design and test an LNA for the high-frequency microwave circuit, i.e., in the C- and X-band applications. This work is an extension of the previous development [10-12] of LNA design for Square Kilometre Array (SKA) radio telescope system operating over a frequency range of 0.4 - 1.4 GHz; which is based on a simple 1 µm gate pHEMT device. With the increasing demand for higher frequency and lower noise applications, the strained channel $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$/InP pHEMT with 0.25 µm gate length technology is chosen for this research. This is due to its superior physical properties, resulting in an increased in the cutoff frequency (f_T) and transconductance (g_m), which are the fundamental parameters for low noise characteristics. In this work, the optimized pHEMT model and proper biasing technique are considered to achieve the target specification of the single- and double-stage MMIC X-band LNA design.

II. Design Approach

An optimal LNA design must have low noise figure, high gain, wide bandwidth, low power dissipation, compact size and must be unconditionally stable over the desired frequency range. Proper selection of network topology and the frequency of interest are key to the LNA circuit design. For this project, the X-band frequency range of 8.0 - 12 GHz is selected. An accurate model, biasing technique and circuit topology are crucial to achieve very low noise; the minimum noise figure (NF_{min}) of the transistor [4]. Although HEMT technologies alone cannot meet all of these requirements simultaneously, the LNA can be designed to meet most of the system requirements. The DC bias points will depend on the circuit applications such as low noise, high gain or high power. Tradeoffs between noise figure, gain, bandwidth, linearity, supply voltage, and power consumption has to be considered carefully especially in high-frequency frequency LNA designs [2-3]. Since noise is the primary concern in this project, the biasing network and impedance matching is defined so that the designs' system impedances are optimized, the circuits are stable, and, of particular importance, give the lowest possible noise characteristics.

The noise figure is targeted to be better than 1 dB over a very wide range of frequencies in the band of interest. However, for higher frequency band i.e., X-band LNA design, higher noise figures are expected. The LNA must also provide stable gain and small signal loss over the entire operating bandwidth. The LNA circuit gain in this project is targeted to achieve a moderate gain range of around 25 dB to 35 dB.

The upper gain value is to prevent the circuit from oscillating, which commonly happens in very high gain circuits. Input and output return losses are specified to be better than -5 dB.

A. Active Device Selection

One of the most practical approaches for improving the overall performance of the LNA is accomplished by using the appropriate active device; which has an optimized epitaxial layer structure and biasing conditions. The most critical parameter; noise figure, depends on the correct selection of the active device. In this project, the active device is a novel high breakdown, low leakage current InP-based pHEMTs using advanced InGaAs/InAlAs material system. The pHEMT sample XMBE131 was developed and fabricated using conventional optical lithography at the University of Manchester [13]. According to Haus and Adler [14], the lowest possible NF that can be achieved for an LNA is not better than the NF_{min} of the transistor. The optimization of the pHEMT epitaxial layers as shown in Figure 1 improves the overall performance of the LNA. The performance enhancement of the device was achieved through the advanced bandgap engineering, resulting in low gate leakage and an improvement in the devices' thermal stability as can be observed in XMBE131 pHEMT device characteristics [13],[15]. The $In_{0.7}Ga_{0.3}As$ compressively strained channel is an excellent choice for fabricating high-frequency low-noise devices, due to its high mobility and high saturation velocity. Additionally, the development and fabrication of submicron devices improve circuit low noise performance by means of gate scaling.

XMBE131
(Cap) $In_{0.53}Ga_{0.47}As$ 50Å
(Barrier) $In_{0.52}Al_{0.48}As$ 150Å
δ-doped
(Spacer2) $In_{0.52}Al_{0.48}As$ 100Å
(Channel) $In_{0.70}Ga_{0.30}As$ 160Å
(Spacer1) $In_{0.52}Al_{0.48}As$ 100Å
δ-doped
(Buffer) $In_{0.52}Al_{0.48}As$ 4500Å
(Substrate) InP Fe doped

Figure 1: Epitaxial layer for XMBE131 pHEMT

B. LNA Topology

In the LNA design, the important goals are minimizing the noise figure of the amplifier [16], producing higher gain, low power consumption and producing stable 50 Ω input impedance. To achieve all these goals, different LNA architectures are available. Several circuit design techniques have demonstrated their robustness, such as the capacitive peaking technique, the inductive peaking technique, the common-gate (CG) input configuration, and the common-drain (CD) input configuration [17-18]. Figure 2 shows a few LNA topology available for LNA circuit design with a single transistor (Single stage LNA) or double stage LNA (cascaded single stage LNA) as in Figure 2 (a) - (d).

The Common Source (CS) amplifier is implemented in the LNA design which has a noise measure close to the NF_{min} measure of the transistor over a wide bandwidth. The disadvantage of the CS configuration is that it suffers from a lack of gain flatness as the gain is very high at low frequency and tends to be very low at high frequency [4]. Nevertheless, this can be encounter by using a proper matching network in the LNA designs and biasing on CS configurations on both stages to provide good RF survivability and good linearity.

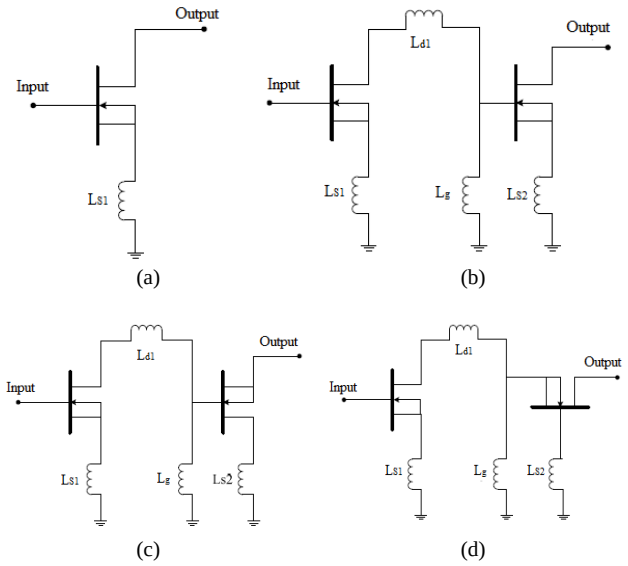


Figure 2: Schematic diagrams of basic LNA topologies. (a) single transistor, (b) common source, (c) common drain and (d) common gate [4]

C. Matching Network

Matching circuits are designed using Advanced Design System (ADS) [19] simulator and appropriate device model. An amplifier must be unconditionally stable which can be designed with a proper matching network and terminations [16]. The optimized scattering coefficients of pHEMT sample XMBE131 were determined to design the input/output matching network. The input circuit is designed to match the source and the output circuit should match the load in order to deliver maximum power to the load. Input/output matching circuit is essential to reduce the unwanted reflection of signal and to improve the efficiency of the transmission from source to load. The general input/output circuit for an LNA is shown in Figure 3 which illustrated a 2-port network.

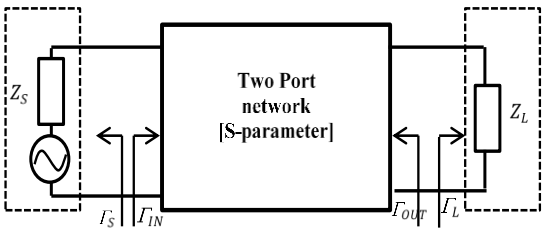


Figure 3: General input and output circuit of LNA

where Γ_{in} and Γ_{out} indicate reflection coefficient of the load at the input port and output port of 2-port network while Γ_S is reflection coefficient of power supplied to the input port and Γ_L. The first stage noise figure of the receiver overrules noise figure of the whole system. To get minimum noise figure using a transistor, power reflection coefficient should match with Γ_{opt} and load reflection coefficient should match with $*\Gamma_{out}$. The calculation of these coefficients can be found using Equation (1) – (4). A lossless matching network on both sides

of the transistor must be designed to transform the input and output impedance, Z_0 to the source and load impedance, Z_S and Z_L required in the design specifications.

$$\Gamma_{out} = \Gamma_L^{*} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (1)$$

$$\Gamma_{in} = \Gamma_S^{*} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (2)$$

$$\Gamma_S = \Gamma_{opt} \quad (3)$$

$$\Gamma_L = \Gamma_{out}^{*} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (4)$$

D. Biasing Network

The drain bias current affects the noise figure more as compared to the drain voltage. Additionally, drain bias also affects the amplifier gain. With insufficient current, the gain will be low. Typically, LNAs are biased at 15 to 20 percent of the drain saturation current (I_{DSS}) as a compromise between gain and noise [20]. The I_{DSS} scales with device size, so a larger device will consume more power than a smaller device. By reducing the device size while maintaining the I_{DSS} bias, DC power consumption can be reduced. As a result of improper network biasing, the LNA will oscillate or the noise will increase. A DC biasing network using an inductor as bias chokes is displayed in Figure 4.

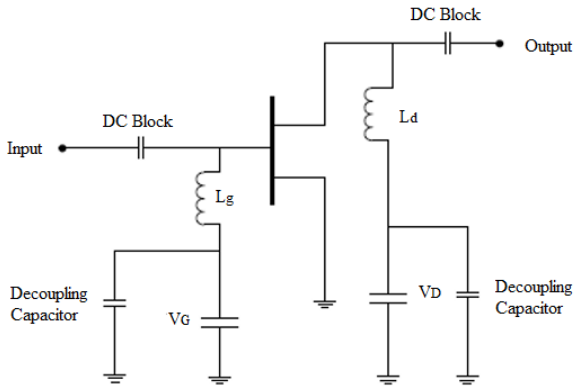


Figure 4: Circuit diagram for biasing circuit with inductor

The DC blocking capacitors are used at the input and the output bias circuit to isolate the bias. The decoupling capacitors are used to prevent the leakage of RF signals into the power supplies. These DC blocking and decoupling capacitors are crucial, especially with regard to the circuit layout, since leakage from either the power supplies or RF signal can cause the circuit to behave incorrectly. This bias network can be modified as a high resistor biasing circuit by substituting the chokes with a high-value resistor.

One of the most practical approaches for improving the overall performance of the LNA is by the selection of the appropriate active device; which has an optimized epitaxial layer structure and biasing conditions.

III. PROPOSED DESIGN SPECIFICATION

Circuit design method of the X-band LNA is similar to RF circuit design techniques where lumped elements are employed for matching networks. The noise figure is kept at a minimum since noise figure is an important metric for a satellite receiver. This amplifier normally used in the first stage of a receiver array for the X-band wireless communications service (WCS) and industrial, scientific, and medical (ISM) frequencies [20-22].

There are two circuits developed for the X-band LNA; single-stage LNA (SSLNA) and double stage LNA (DSLNA) respectively. Table 1 shows the comparison of device size, frequency range and the center frequency of the X-band design and literature. The X-band LNA design is shown in Table 2.

Table 1
Device Size and Frequency Specification

Device criteria	This work (SSLNA)	SSLNA [21]	This work (DSLNA)	DSLNA [22]
Gate length, Lg (nm)	250	100	250	< 200
Size, W (μm)	2x50	2x50	2x50	160
Frequency range (GHz)	8-12	7-11	8-12	7.8 - 9.4
Center frequency (GHz)	8.4	9.8	8.4	8.6

Table 2
Target Specification for X-band LNA Compared to Related Works

S-Parameter	This work (SSLNA)	SSLNA [21]	This work (DSLNA)	DSLNA [22]
S_{11} (dB)	-12.8	-11.3	> 10	-26
S_{12} (dB)	-20.2	Not mentioned	-20.2	Not mentioned
S_{21} (dB)	> 10	9 ±0.9	> 20	>30
S_{22} (dB)	<-10	-10.1	<-15	-27
Noise Figure, NF	< 1.5 at 8.4 GHz	1.48 at 9.8 GHz	< 2	< 0.6

In the X-band LNA, the design of a new input matching network is proposed that obviates the need for the gate inductance, L_g. The gate inductance is an important noise contributor due to its finite quality factor, a resistance appears in series with (R_S), adding directly to the noise of the system. The LNA circuit design for both single-stage and double-stage LNA are shown in Figure 5 and 6.

IV. SIMULATION RESULTS

The single stage single-ended MMIC LNA for the frequency range of 8 - 12 GHz, with center frequency set at 8.4 GHz is shown in Figure 5. The optimized s-parameter is obtained from the 2 x 50 μm XMBE131 pHEMT sample [23]. The active device was also biased at V_{GS}=-0.52 V, 13 mA I_{DS} (90% g_m or 10% I_{DSS}) and the source-drain voltage, V_{DS} of 3 V. The NF_{min} calculated for the XMBE131 pHEMT at the frequency of 8 GHz is approximately 0.5 dB [23].

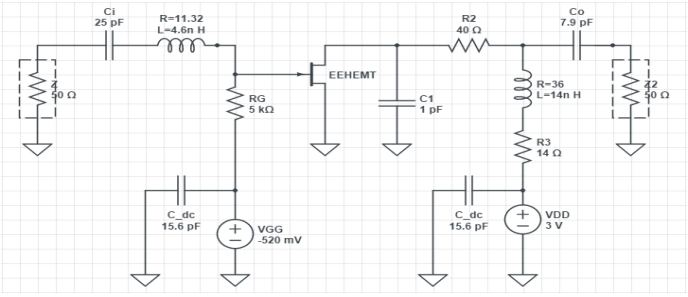


Figure 5: Circuit diagram of single stage LNA (SSLNA)

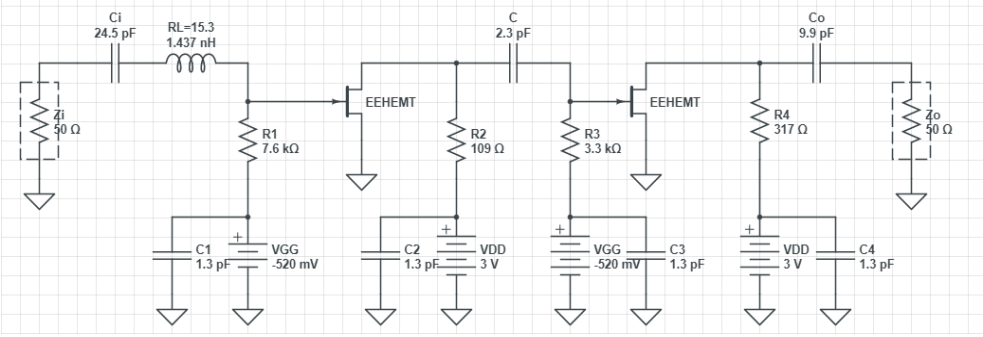
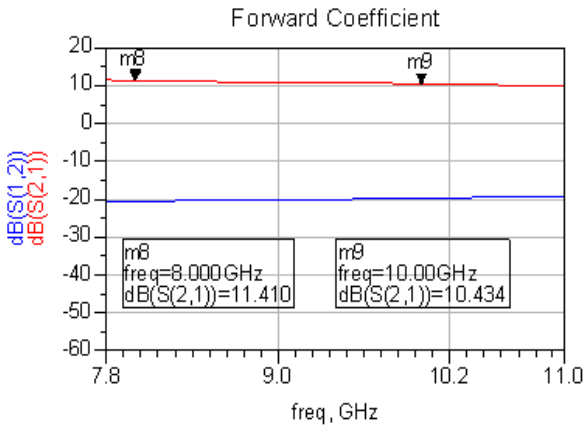
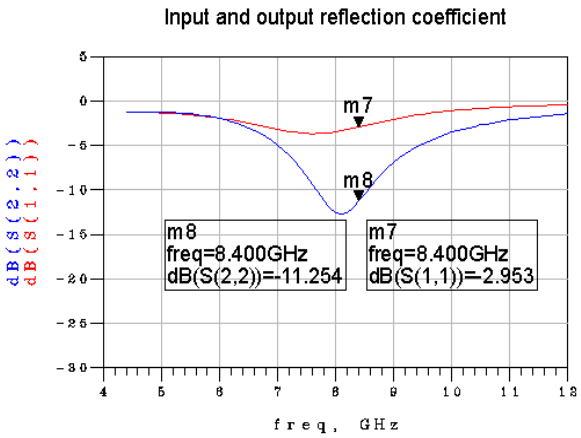


Figure 6: Circuit diagram of double stage LNA (DSLNA) for 8-12 GHz

The simulation results recorded that the amplifier gain, S_{21} is 11.4 dB and flat gain is maintained over the frequency range. The input insertion loss, S_{11} is 2.9 dB, overall noise figure is 1.9 dB at 8.4 GHz and the output insertion loss, S_{22} is -11.25dB. The reflection loss, S_{12} is 20 dB. These values were within the design specification, except for very low input insertion loss. The output s-parameter and noise figure result are shown in Figure 7.

To improve the output gain and noise performance, a double staged single-ended X-band MMIC LNA is designed. This LNA circuit is using the same biasing configuration as employed in the SSLNA X-band design where V_{GS} = -0.52V and I_{DS} = 13.2 mA. The DSLNA circuit diagram for X-band LNA is presented in Figure 6. For both designs, the first stage amplifier is designed with minimum noise figure and a low-pass network at the output in order to reduce the spurious and higher harmonic content. The band-pass networks configuration at the input and inter-stages will provide good broadband matching and gain forming to increase the stability [24]. The second stage is designed to provide high gain.





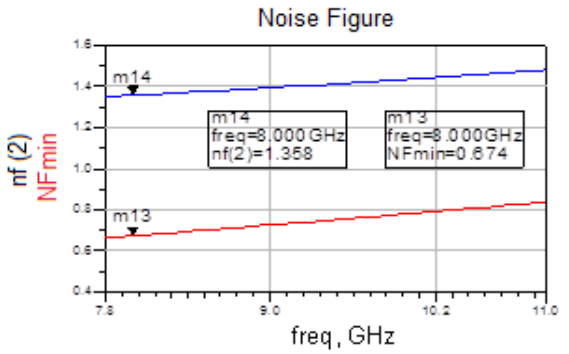


Figure 7: Gain, Noise figure and Input/output reflection results for SSLNA at 8-12 GHz

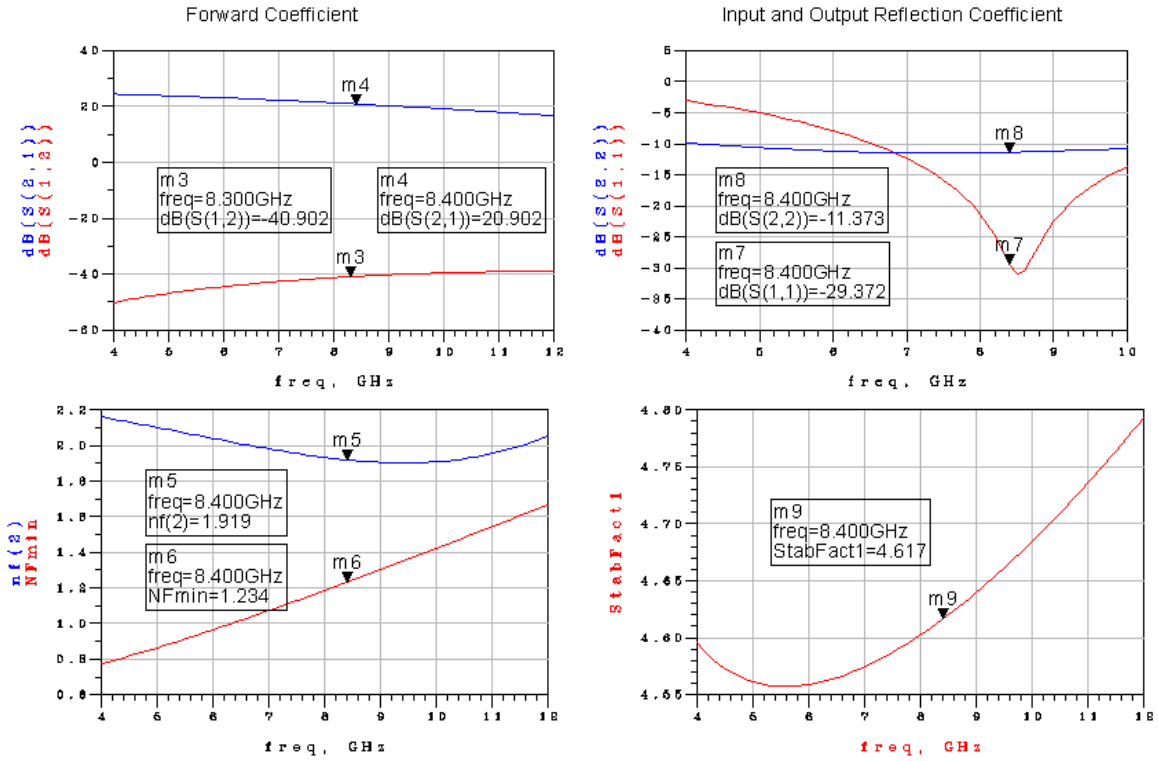


Figure 8: Gain, noise figure, input and output reflection results for DSLNA operating at 8-12 GHz

The DSLNA circuit design results in an overall gain, S21 of 20 dB. The input insertion loss, S11 is 29 dB, the overall noise figure, NF of 1.9 dB at 8.4 GHz, the output insertion loss, S22 of -11.3 dB and reflection loss, S12 is about 41 dB. The circuit stability factor is 4.6. Overall, these values met the design specification tabulated in Table 2. Figure 8 demonstrates the s-parameter results for the DSLNA circuit design.

V. CONCLUSION

The single- and double-stage low noise amplifier designed to operate at X-band frequency is reported. The simplest topology for the MMIC InGaAs/InAlAs pHEMT LNA development operating in the frequency range of 8-12 GHz is described. The designed LNA shows excellent performance to meet the specification of high gain, unconditional stability, low power dissipation, and low noise figure. The MMIC LNA design is optimized for operation at the drain voltage of 3V and biased at VGS = -0.52 V and IDS =13.2 mA. The simulation results show excellent performances including input and output return loss of-41dB and -11.3dB respectively, an overall gain, S21 of 20 dB, and NF of 1.9 dB at 8.4 GHz which distinguishes it from other LNAs in the literature.

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