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Prediction of soft error response of integrated circuits to electrostatic discharge injection via simulation field; Package interaction for electrostatic discharge soft error prediction; Full wave model for simulating noise ken electrostatic discharge generator

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Department:

PREDICTION OF SOFT ERROR RESPONSE OF INTEGRATED CIRCUITS TO ELECTROSTATIC DISCHARGE INJECTION VIA SIMULATION

FIELD PACKAGE INTERACTION FOR ELECTROSTATIC DISCHARGE SOFT ERROR PREDICTION

FULL WAVE MODEL FOR SIMULATING NOISEKEN ELECTROSTATIC DISCHARGE GENERATOR

by

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Approved by

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ABSTRACT

In the first section, a concept for analyzing soft error response in ICs to ESD via coupling through flex cable structures is presented. Its novelty lies in accounting for the transient electromagnetic fields radiated by the ESD generator that couples to the flex cable PCB thereby causing disturbance on the IC under test. This is accomplished in three stages; first by developing a full wave model of the DUT which includes modeling the PCB and flex cable geometry and validating it in frequency domain with regard to the transfer impedance. This followed by combining the ESD generator with the DUT model to simulate the voltage at the IC input in time domain. Finally the time domain results from full wave simulation are combined with an equivalent IC response model in SPICE to predict soft error failures due ESD.

In the second section, a more detailed modeling of the IC including the lead frame geometry, bond wires and IBIS/ICEM models are incorporated to investigate coupling of fields from three different injection techniques- H field loop probes, TEM cell and ESD generator. For the first time a complete simulation model which includes the ESD generator, passive elements of the DUT structure (PCB) and a detailed model of the IC has been developed to predict interaction of radiated field from the generator to the IC.

The third section shows a CST MWS model was generated to simulate the discharge current and the transient field of an ESD generator. Individual components of the Noise Ken ESD generator (ESS-2000) were modeled, validated and combined. The complete full wave model was verified by comparing the simulated discharge current waveforms and induced loop voltages with the measured results.

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1. INTRODUCTION

Electrostatic discharge (ESD) can damage or disrupt a system by injecting currents or by their associated transient fields. Getting an understanding of the underlying reason, such as the coupling paths can not only help resolve ESD issues, but can also be used to estimate ESD performance. Study of system level ESD disturbances has been approached from mainly two different directions, circuit modeling [1], [2], [3] or full wave numerical simulation of currents and fields from an ESD generator [4], [5], [6], [7], [8], [11]. Transient fields from ESD events can either couple directly to the lead frame and bond wires in ICs or indirectly through strong coupling structures such as flex cable PCBs therby causing soft errors in ICs. Soft errors are typically defined as logical errors which cause failures in operation of the IC and can be cured at least by resetting the system.

The adopted approach is to develop a complete simulation model which includes the ESD generator model, the passive DUT structure and IC response models to predict ESD related soft errors in ICs caused due ot coupling via electromagnetic fields.

This thesis describes two distinct co-simulation strategies whereby a full wave model of the generator is combined with a simple model of an IC represented as a low pass filter to predict voltages and currents via coupling through a passive structure such as a flex cable PCB. The investigation further moves on to modeling the IC in greater detail with the lead frame structure, bond wires and the use of IBIS models to simulate induced noise voltages and currents on the IC pin. The development covers definition of the test platforms; modeling and verification of the of the flex cable and PCB geometry in frequency domain and subsequent combination with the ESD generator model in time

domain; combining full wave simulation result with simple IC model in SPICE to predict soft errors; detailed modeling of the IC including geometry and equivalent IBIS models of various pins; correlation of measured and simulated voltages at the IC pins for three different field injection techniques, loop probes, TEM cell and the ESD generator.

The last section of the thesis gives a detailed full wave model of a commercially available ESD generator in CST MWS and verification of the model with regard to discharge current and induced loop voltage waveform.

2. EXPERIMENTAL INVESTIGATION OF ESD COUPLING TO IC VIA FLEX CABLE PCB

Real world commercial products often consists of a system of flex cable connected PCBs. The victim IC is maybe mounted on one PCB and is connected via a signal trace on another PCB by a flex cable. The flex cable is a very strong coupling region to ESD. An ESD discharge on the first PCB is not only accompanied by the spread of the discharge current throughout the system but also by the fast changing transient electromagnetic fields. These field components can couple onto the flex cable and drive a common mode current through it thereby leading to a soft error in the IC mounted on the other PCB. The objective of this research concentrates on proposing a simulation strategy to model the flex cable with the interconnected PCBs via a full wave simulation tool and simulate the voltage at the IC input in response to ESD discharge onto the board. This section details the test platform used for our purpose and the soft error failure levels of the IC in response to ESD coupling via the flex cable structure.

2.1 DEFINITION OF TEST PLATFORM

The test platform includes an IC mounted on one PCB (Board 2) which is connected to another PCB (Board 1) via a flex cable structure. Two distinct PCB geometries with separate circuit schematics are used for testing two different types of ICs. The test PCB is a 4 layer board. The stack up configuration of the boards are as follows,

- **Layer 1:** Signal, Power traces and Ground fill
- **Layer 2:** Solid Ground

- **Layer 3:** Empty
- **Layer 4 :** Solid Ground

The boards are equipped with SMA connectors and current measurement loops embedded underneath the trace connecting to the CLK pin of the IC to measure the voltages and currents at the IC input. The IC's used for our purpose are D-type flip flops from Potatosemi and ON Semiconductor, thus, they detect noise events that surpass their input low-high transition definition on the CLK pin. They are available in two different speed classes: 600 MHz CMOS and 8 GHz SiGe. The two classes of ICs are classified as slow and fast ICs for identification purpose. The circuit diagram of the slow IC mounted on the board is shown in Figure 2.1.

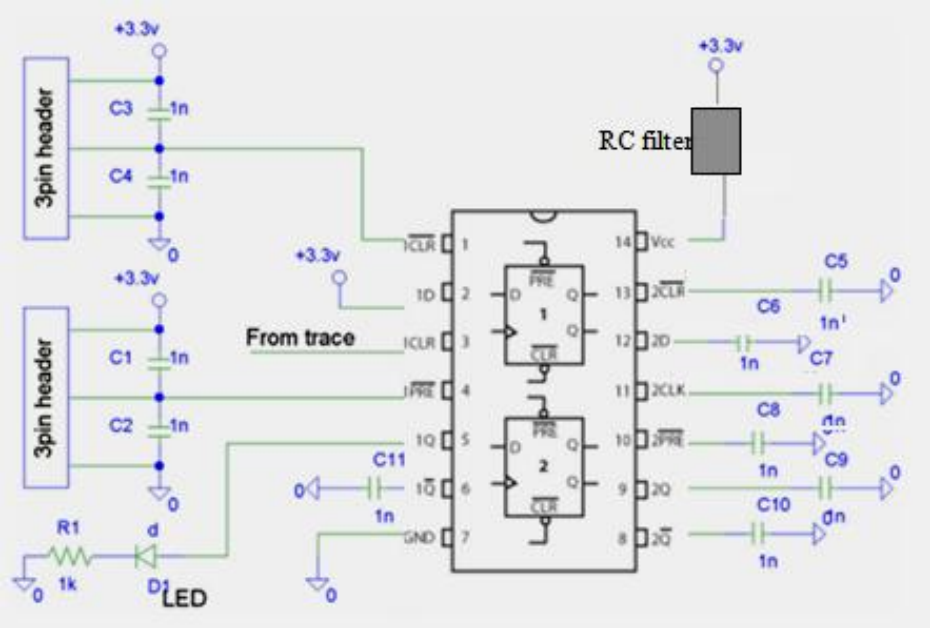

Figure 2.1. Circuit diagram of the slow IC mounted on the PCB

Some of the specifications of the slow IC are as follows,

- Operating frequency is faster than 600MHz
- VCC Operates from 1.65V to 3.6V
- Propagation delay < 2ns max with 15pf load
- Input capacitance: 4pF
- Voltage at input pin for logic high level: 2-5 V

The various operating states of the IC are shown in Table 2.1.

Table 2.1. Truth table for operation of the IC

Pin Description

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

The IC is operated in the state marked by the blue box. The layout of the IC on the board is shown in Figure 2.2.

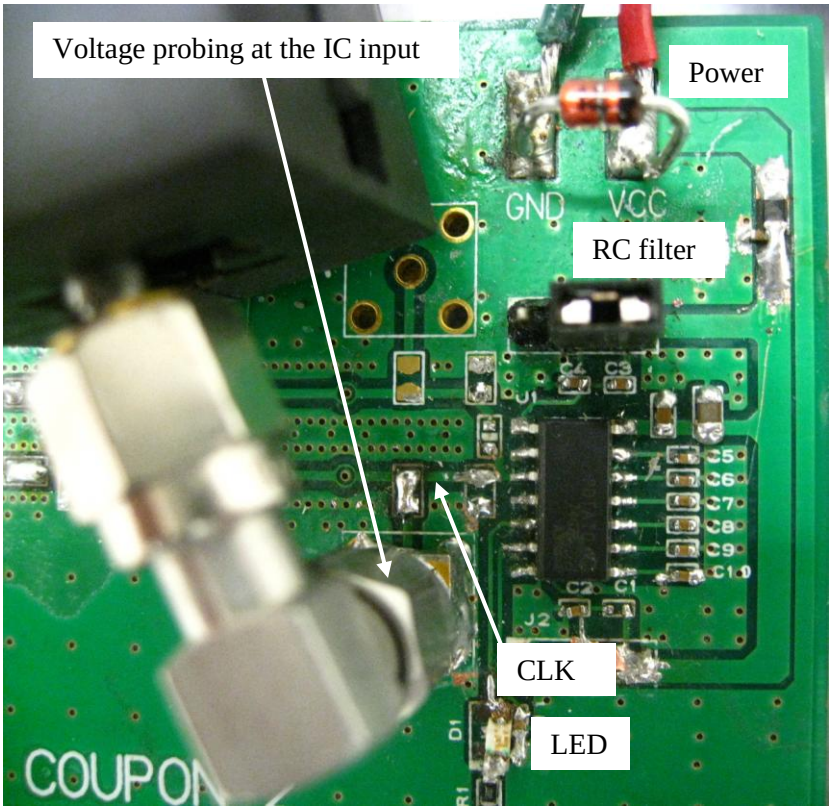

Figure 2.2. Photo of the IC and various components on the PCB

The IC is powered from a DC power supply at 3.3 V. A 3.3 V Zener diode is placed across the power supply to protect the IC against over voltage. An RC filter is also mounted on the power trace to block RF signals propagating into the power pin of the IC. Voltage at the IC CLK input is measured from an SMA connector mounted close to the IC. An SMT LED is mounted to observe state of the output pin in response to voltage pulses on the CLK pin. The circuit diagram of the fast IC mounted on the board is shown in Figure 2.3.

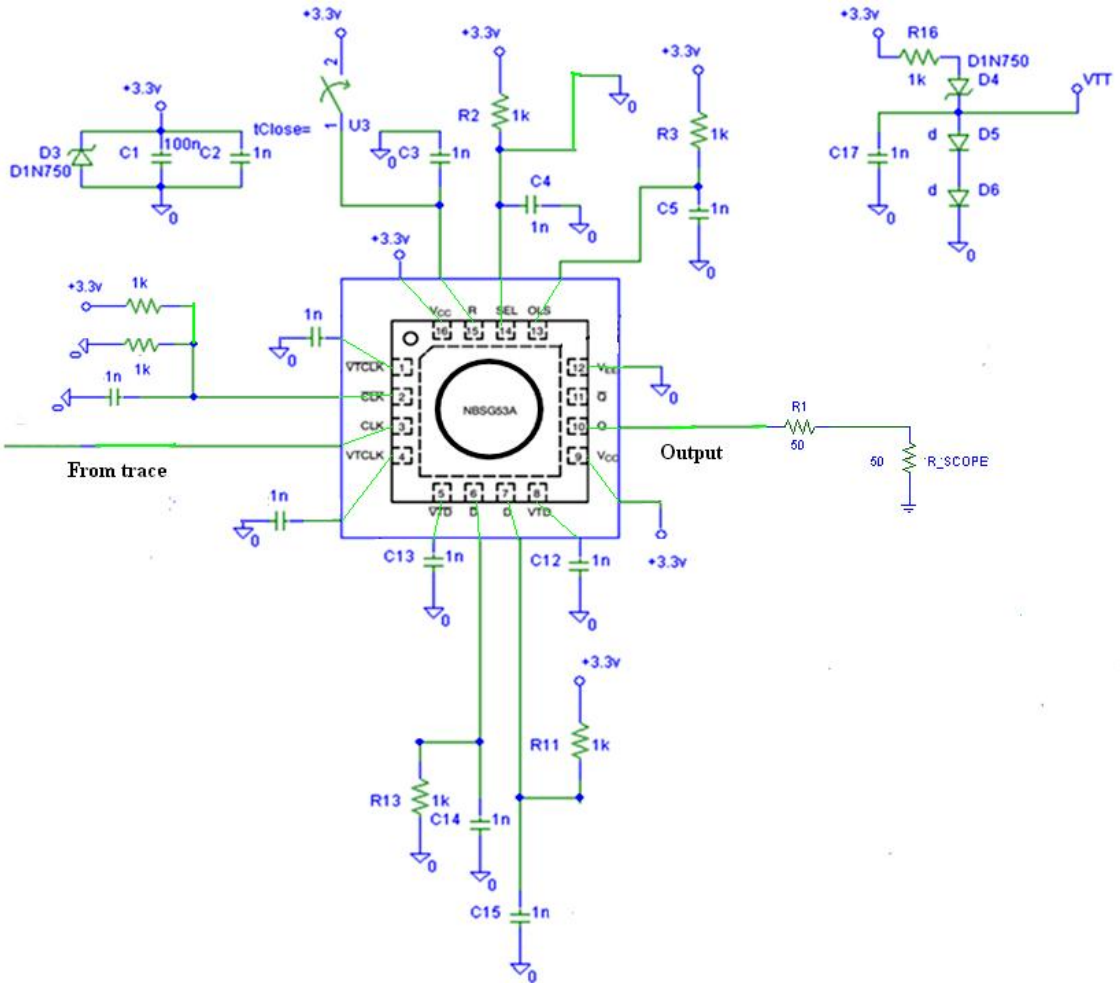

Figure 2.3. Circuit diagram of the IC mounted on the PCB

Some of the specifications of the IC are as follows,

- Operating frequency is faster than 8GHz
- VCC Operates from 2.375V to 3.465V
- D Flip-flop mode, DFF (Active with Select High)
- 50 Internal Input Termination Resistors on all Differential Inputs
- Selectable Output Level, OLS = VCC (800 mV Peak-to-Peak Output)

The various operating states of the IC are shown in Table 2.2.

Table 2.2. Truth table for operation of the IC

R	SEL	D	CLK	Q	Function
H	x	x	x	L	Reset
L	H	L	Z	L	DFF
L	H	H	Z	H	DFF
L	L	x	Z	$\overline{Q}$	DIV/2

Z = LOW to HIGH Transition

The IC is operated in the state marked by the blue box. The layout of the IC on the board is shown in Figure 2.4.

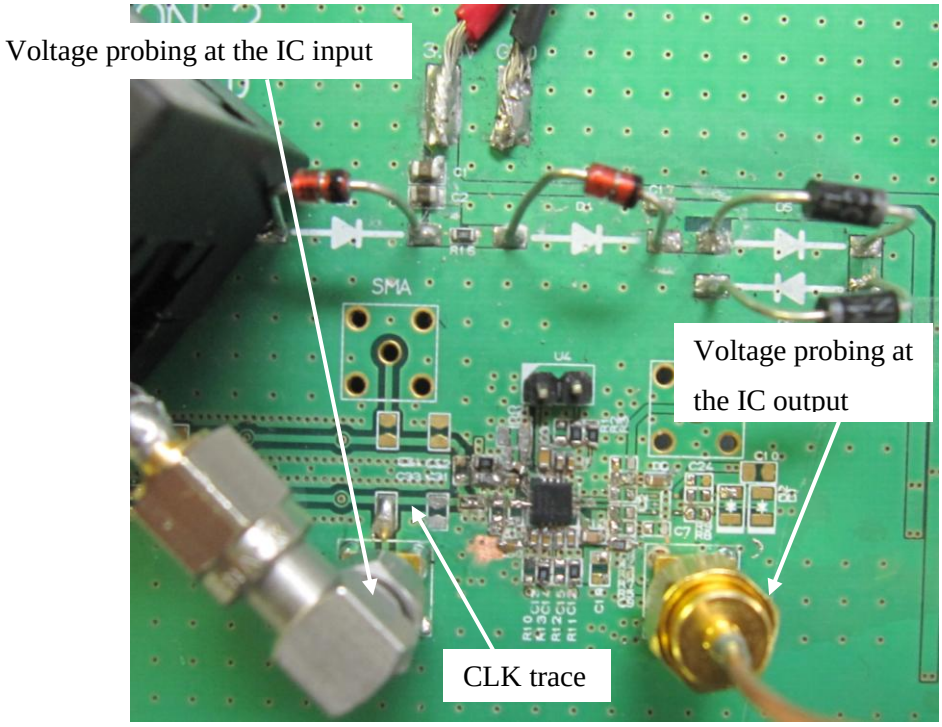

Figure 2.4. Photo of the IC and various components on the PCB

2.2 CHARACTERIZATION OF IC

Characterization of both the ICs is performed with respect to voltage at the IC input vs pulse width. The objective of this test is to determine the speed of response at the IC input. The IC input can then be represented as an equivalent low pass filter followed by a threshold detector in circuit simulation for subsequent co-simulation with full wave simulation results. Both the ICs are mounted on individual PCB test boards and Transmission line pulses (TLP) of varying magnitude and pulse widths are injected into the CLK trace of the IC while observing the response at the output (Q). At the time of failure, the voltage at the IC is measured to obtain the desired curve. The failure threshold curve for the ICs obtained from the above information shows the input response to different pulse widths.

2.2.1 Measurement setup. The measurement setup is shown in Figure 2.5.

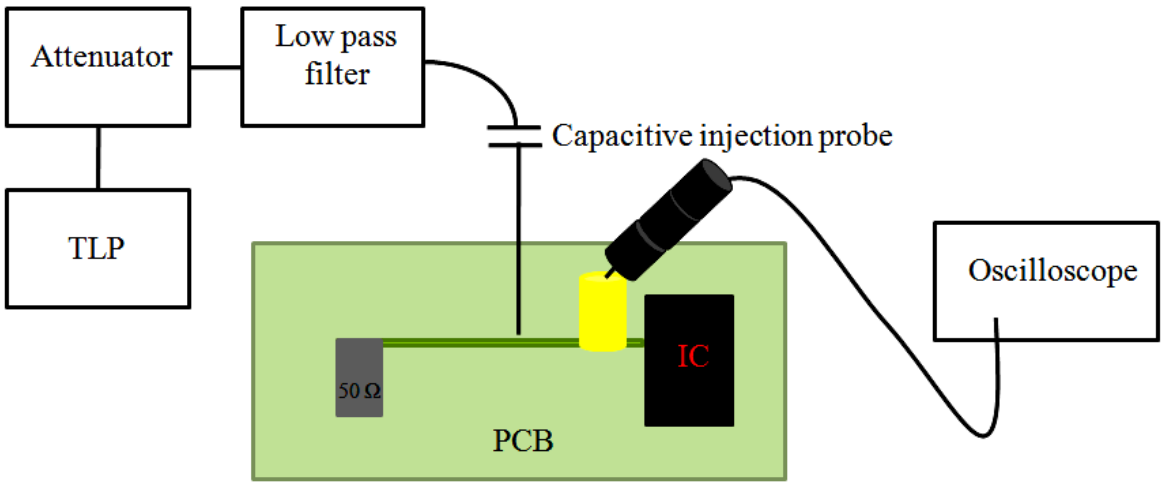

Figure 2.5. Measurement setup for characterization of the IC

The signal trace on the PCB is terminated with 50 Ω resistor on one end and the CLK pin of the IC on the other end. The low pass filter following the TLP generator modulates the original TLP pulse and generates pulses of varying magnitude and pulse widths which is injected via a capacitive probe (C = 1pF) onto the CLK signal trace at the input of the IC. At the instant when the IC triggers, voltage pulses at the IC input are recorded on an oscilloscope. A high voltage attenuator of 22 dB is used depending upon the charge voltage of the TLP generator.

2.2.2 Measurement results. Figure 2.6 shows the different voltage waveforms measured at the input of the slow IC (PO74G74A). The failure threshold curve for the slow IC is obtained from Figure 2.6 and is shown in Figure 2.7.

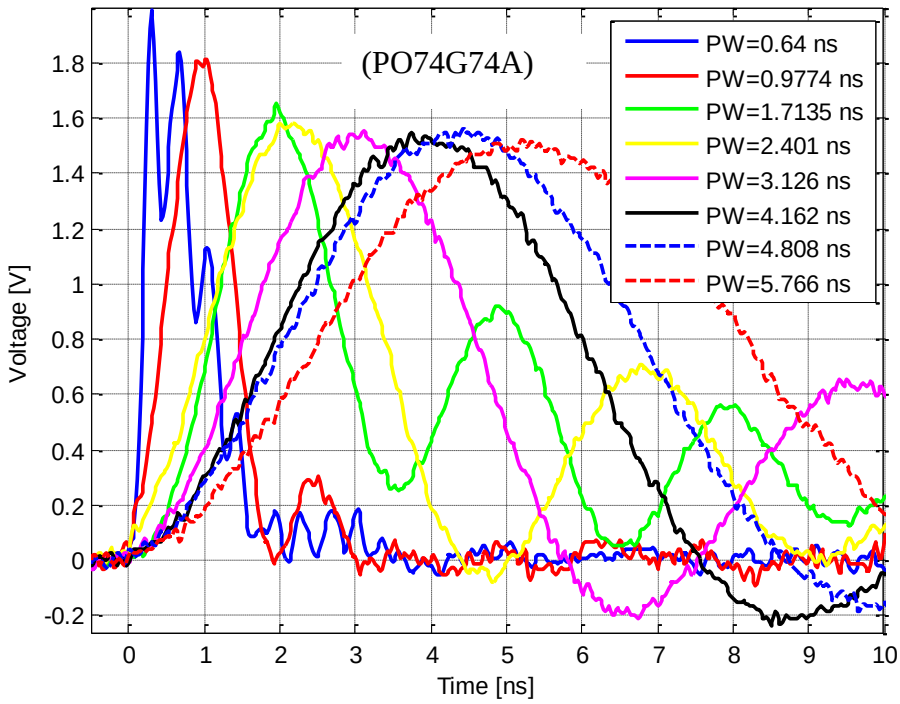

Figure 2.6. Pulses of varying magnitude and pulse width at the slow IC input

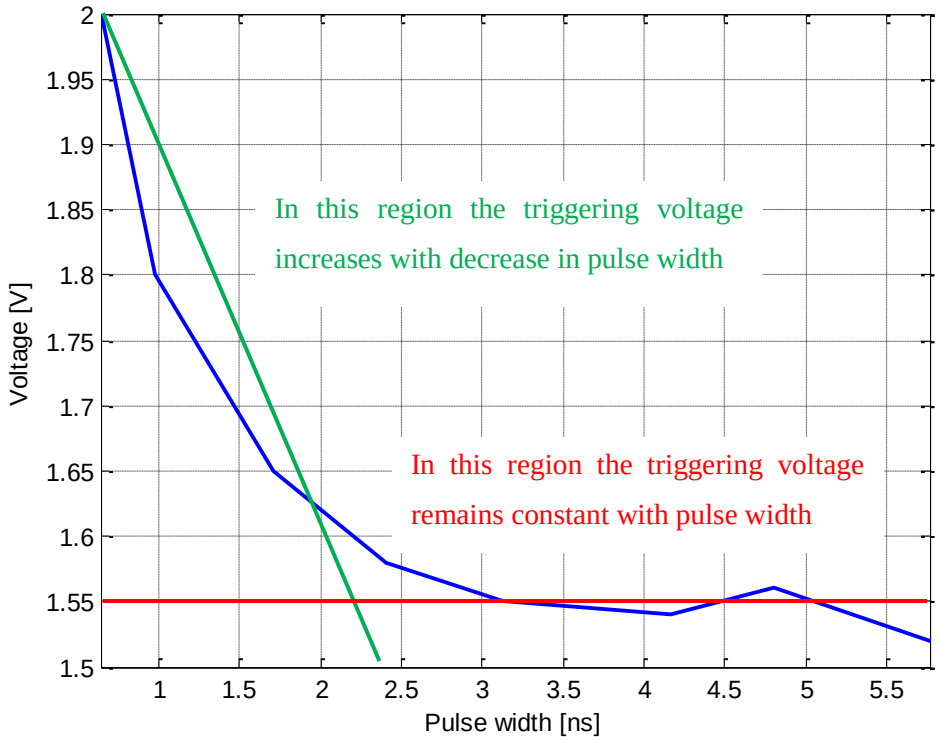

Figure 2.7. Voltage at the slow IC input vs Pulse width

The failure threshold curve is used to model the input structure of the IC in SPICE. From Figure 2.6 and Figure 2.8 one observes that different low pass filters gives rise to different rise times and pulse widths of the injected TLP pulse. The pulse width is defined at 50 % of the magnitude of the pulse. In the region marked by the red line the triggering voltage remains fairly constant with increase in pulse width. However as the pulse width becomes narrow the voltage required to trigger the IC goes up. The same characterization procedure is performed on the fast IC (NBSG53A) as well. Figure 2.8 shows the different voltage waveforms measured at the input of the fast IC. The failure threshold curve is shown in Figure 2.9.

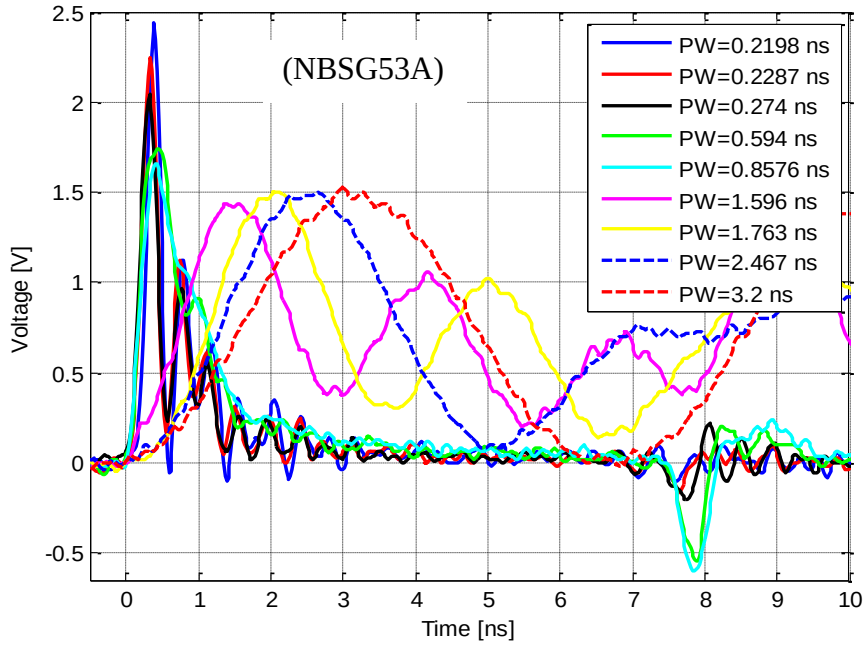

Figure 2.8. Pulses of varying magnitude and pulse width at the fast IC input

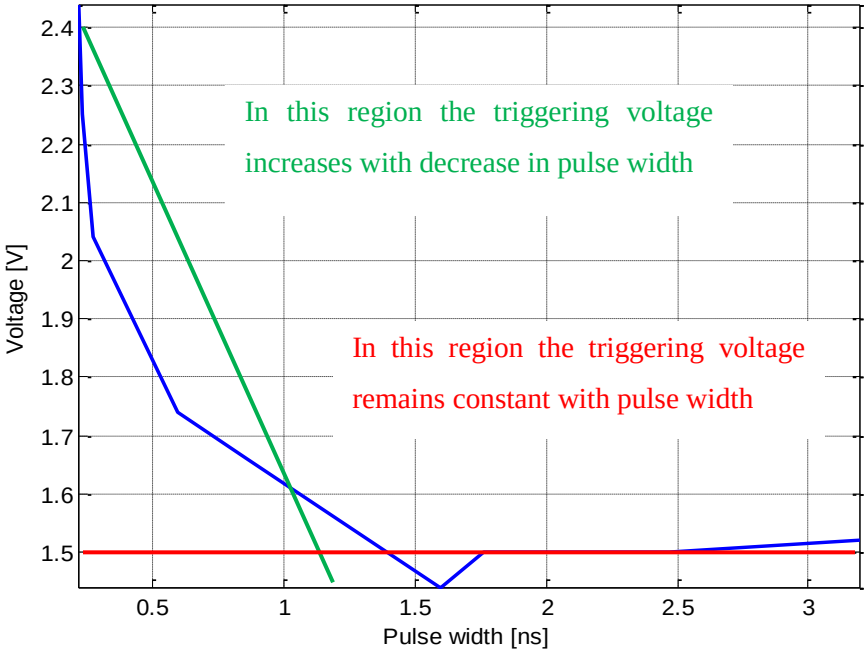

Figure 2.9. Voltage at the fast IC input vs Pulse width

Comparing Figure 2.7 and Figure 2.9, the curve for the fast IC starts rising at a much lower pulse width (<1 ns) in comparison to the slow IC (<2 ns). This agrees with the expectation that the faster IC (NBSG53A) is in fact faster than the slower IC (PO74G74A). One would expect to see the speed of response of both the ICs to be in the ratio of ~ 1:10. However it is not reflected exactly from the threshold curves of the ICs. One of the reasons for that could be because of the fact that the speed of response of the ICs may not necessarily correlate to with the speed of the IC due to different technologies associated with both of them.

2.3 ESD IMMUNITY OF ICs

The objective of this experiment is to document the crash levels of both the ICs for different ESD charge voltages. The test case is an IC mounted on one PCB (Board 2) which is connected to another PCB (Board 1) via a flex cable. The crash levels of the IC attached to the CLK trace in flex cable setup is determined experimentally by injecting ESD pulses on PCB Board 1. Simultaneously the voltage at the IC input is recorded at the instant of failure.

2.3.1. Measurement setup. The immunity of the ICs has been determined for two different ESD generator models: EM TEST DITO & NOISEKEN. The ESD generators are discharge on the edge of PCB1. The reason to choose the edge is because in commercial products the chances of an ESD discharge at the edge of PCB structures is relatively more than to the center. The IC is mounted on PCB 2 which is grounded to the large ground plane and PCB 1 is floating above the ground plane. Both the ESD generators are discharged on PCB 1 at a fixed position (2 mm x 2 mm from the edge of

the board, PCB1). On discharge the triggering voltage at the IC input is recorded in an oscilloscope. A 20 dB attenuator and a power limiter is used in front of the oscilloscope as an over voltage protection device. The signal trace on PCB 1 connecting to the CLK trace on PCB2 via the flex cable is terminated with 50 Ω. The three traces on the flex cable are in SIGNAL-GROUND-FLOATING configuration. Figure 2.10 shows the measurement setup of ESD discharge on to the boards.

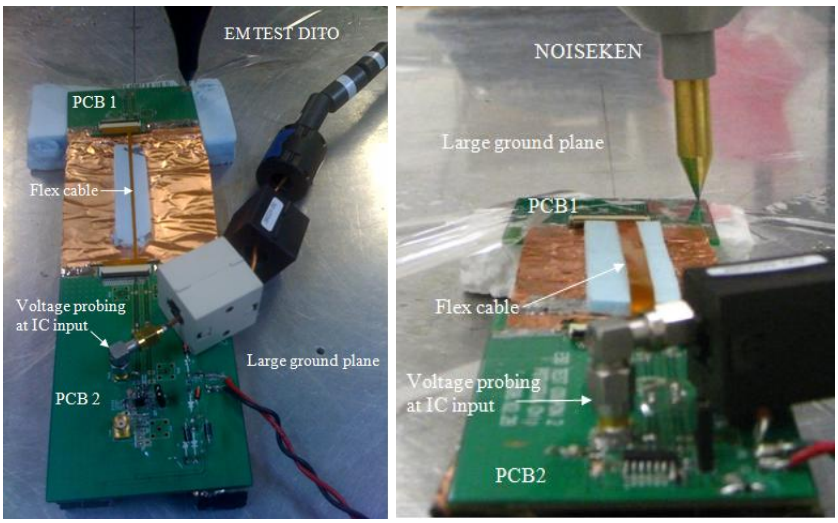

Figure 2.10. Measurement setup with ESD discharge on board

The flex cable is mounted on the boards via connectors. The flex cable is a single layer type with 40 traces on it. Only three traces are included in the measurement setup to reduce the complexity of modeling all the traces in the flex cable structure. The whole setup is mounted on an ESD table. The oscilloscope is housed inside a metal chamber to prevent direct coupling of the ESD generator to the ports of the instrument. To further

improve shielding from the ESD generator, a semi rigid cable loaded with ferrites is used to measure the voltage at the IC input at the time of discharge.

2.3.2. Measurement results. It is a known fact that with ESD measurements there is always an issue with repeatability of results. Hence it is very important to establish the repeatability of test results before moving on further.

Table 2.3. Repeatability of ESD test on discharge to board for slow IC

EM-TEST DITO	**0.7 kV**	**0.8 kV**	**1 kV**
NOISEKEN	**0.7 kV**	**0.8 kV**	**0.9 kV**
0^0	Does not trigger	Triggers, Repeatable	Triggers, Repeatable
	Does not trigger	Does not trigger	Triggers, Repeatable
90^0	Does not trigger	Triggers, Not Repeatable	Triggers, Repeatable
	Does not trigger	Triggers, Repeatable	Triggers, Repeatable
180^0	Does not trigger	Triggers, Repeatable	Triggers, Repeatable
	Does not trigger	Triggers, Repeatable	Triggers, Repeatable
270^0	Does not trigger	Triggers, Repeatable	Triggers, Repeatable
	Does not trigger	Does not trigger	Triggers, Repeatable

From the above table, the crash level for the slow IC is in between 0.8 kV and 1 kV. An interesting observation is the sensitivity of the IC to the orientation of the ESD generator. At lower ESD charge voltage levels the IC triggers for some orientations of the generator and in others not. This suggests that the orientation of the pulse forming

network inside the ESD generator is such that there is more coupling of fields from the generator to the flex cable structure for some orientations making the IC more sensitive with regard to ESD discharge. Hence for reproducibility of results the voltage waveforms at the IC input were measured at 1 kV for both the ESD generators.

Figure 2.11 shows the voltage waveforms measured at the slow IC input for the two different ESD generators (at 0^{o} orientation) when the IC triggers at 1kV.

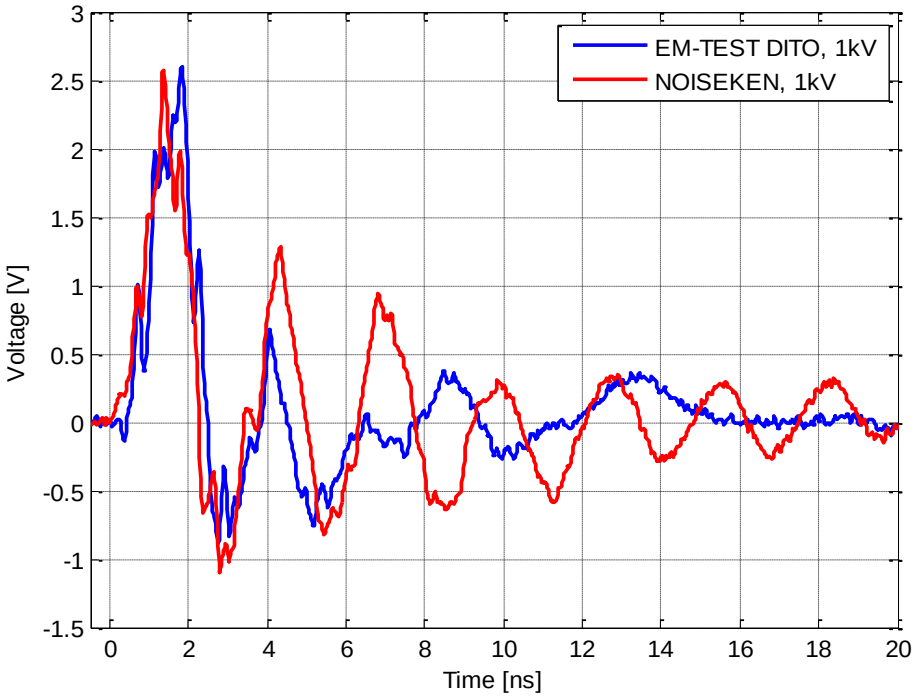

Figure 2.11. Comparison of voltage at the IC input for discharge onto the board

The data is measured on the oscilloscope with a sampling frequency of 20 GS/s. One notices a ringing a frequency of ~0.4 GHz (2.5 ns) in the voltage waveform at the IC

input for the NOISEKEN generator. A spectrum analysis of the above voltage waveform shown in Figure 2.12 also validates that fact.

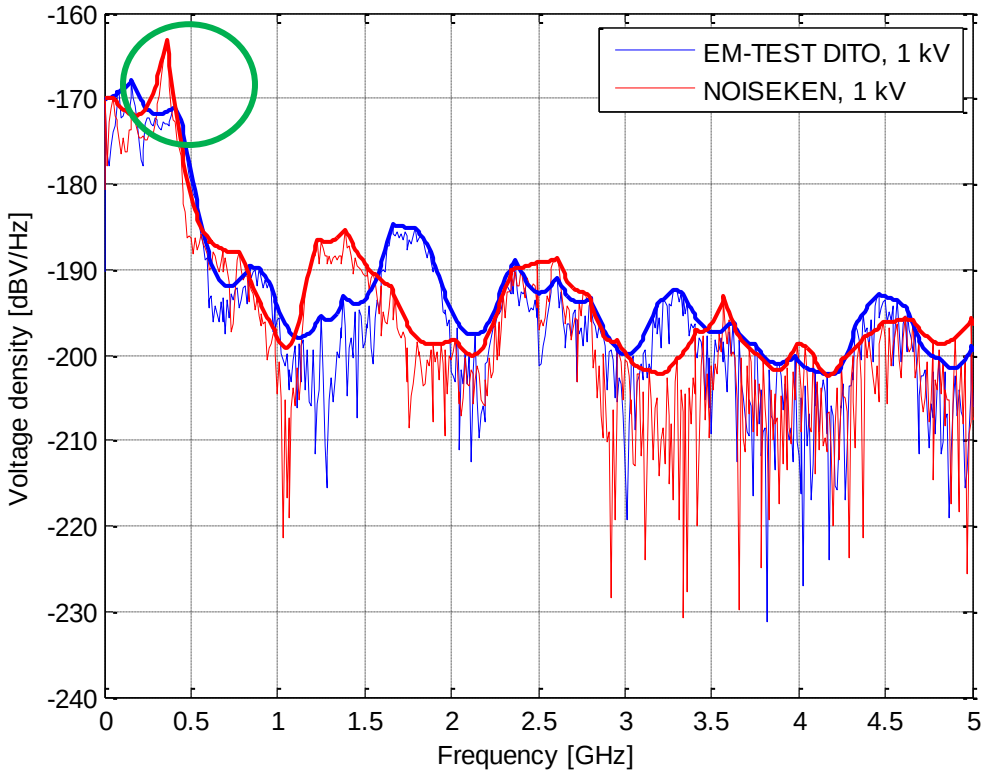

Figure 2.12. Comparison of frequency spectrum of voltage at IC input

The above figure shows the frequency domain comparison of the voltage waveforms at the IC input from two different ESD generators. The resonance peak at 0.4 GHz (indicated by the green circle) corresponds to the ringing noticed in the time domain voltage waveform. This peak is caused due to the coupling from the flex cable. Above 3 GHz the spectrum does not make any sense and is just noise. The reason one does not see

the resonance peak for the EM TEST DITO generator could be because of the fact that there is a null in the frequency spectrum of the generator which cancels out the resonance from the flex cable coupling.

Table 2.4 shows the repeatability of the ESD test during discharge with both the ESD generator for the fast IC.

Table 2.4. Repeatability of ESD test on discharge to board for fast IC

EM-TEST DITO	**0.6 kV**	**0.7 kV**	**0.8 kV**
NOISEKEN	**0.8 kV**	**0.9 kV**	**1 kV**
0^0	Does not trigger	Triggers, Not Repeatable	Triggers, Repeatable
	Triggers, Not Repeatable	Triggers, Not Repeatable	Triggers, Repeatable
90^0	Does not trigger	Triggers, Not Repeatable	Triggers, Repeatable
	Does not trigger	Triggers, Not Repeatable	Triggers, Repeatable
180^0	Does not trigger	Triggers, Repeatable	Triggers, Repeatable
	Does not trigger	Triggers, Not Repeatable	Triggers, Repeatable
270^0	Triggers, Repeatable	Triggers, Repeatable	Triggers, Repeatable
	Triggers, Repeatable	Triggers, Repeatable	Triggers, Repeatable

At intermediate voltages between 0.6 kV and 0.7 kV (for EM-TEST DITO) and 0.8 kV and 0.9 kV (for NOISEKEN), the IC triggers for some orientations of the

generator and in others not. Especially it triggers for the 270 degree orientation, which suggest that the orientation of the pulse generator (inside the ESD generator) at 270 degree is such that there is more coupling of the fields from the generator to the flex cable structure making the IC more sensitive with regard to ESD discharge. So for discharge to board one can say that the ESD failure level of the IC is between 0.7 kV and 0.8 kV when the EM TEST DITO generator is used and 0.9 kV to 1 kV when the NOISEKEN generator is used.

Figure 2.13 shows the voltage waveforms measured at the fast IC input for the two different ESD generators (at 0^{o} orientation).

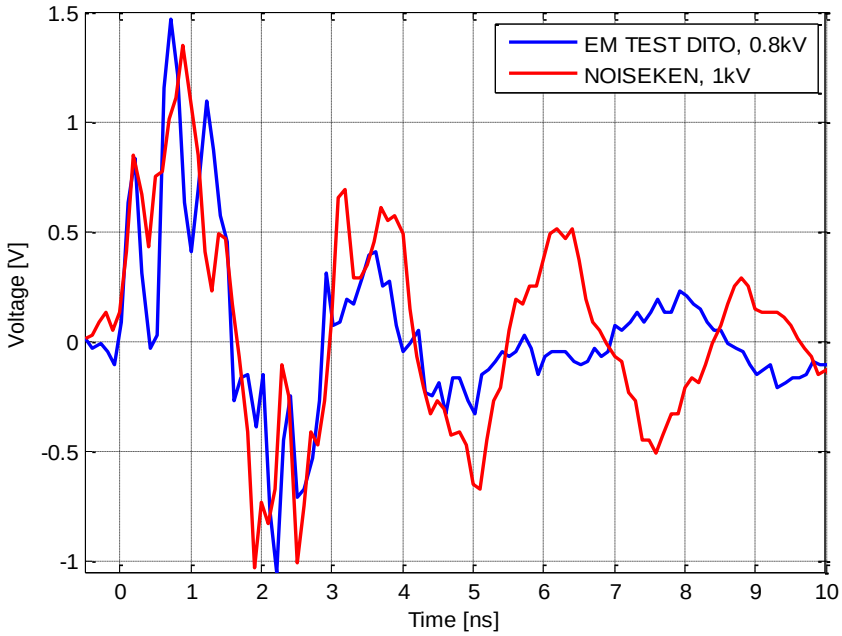

Figure 2.13. Comparison of voltage at the IC input for discharge onto the board

The data is measured on the oscilloscope with a sampling frequency of 10 GS/s. Ideally it is always recommended to take measurements with the sampling frequency set to 20 GS/s or more if available to capture the high frequency components accompanying a discharge. One notices a ringing a frequency of ~0.4 GHz (2.5 ns) in the voltage waveform at the IC input for the NOISEKEN generator. A spectrum analysis of the above voltage waveform validates that fact. The original spectrum of the voltage waveform is processed using a function called "Connect_extremes". The function is basically a square running average filter which either finds an average of the maximas or minimas of a curve. Figure 2.14 shows the plot of the average of the maximas in the frequency spectrum of the voltage waveform.

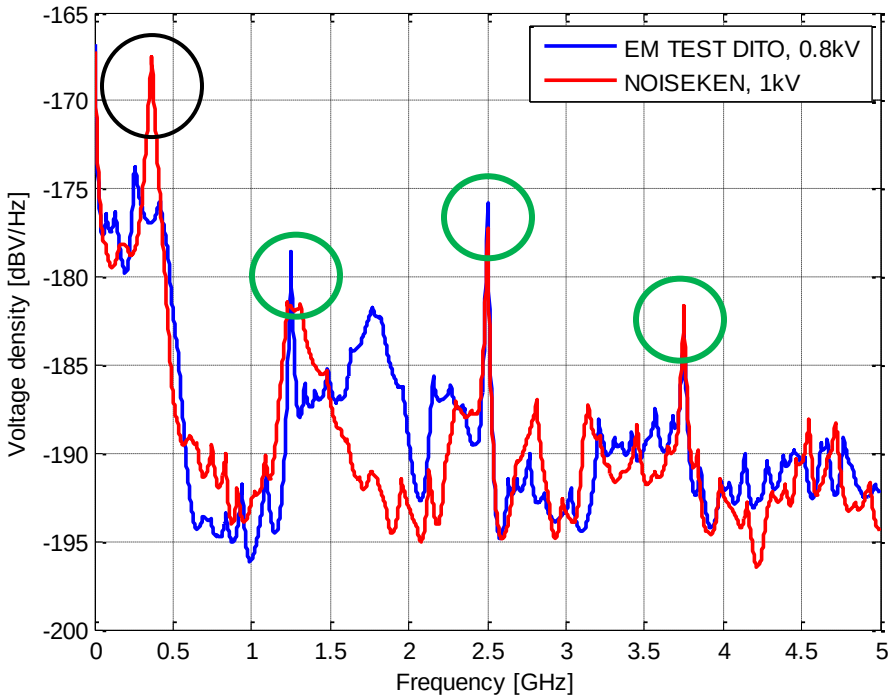

Figure 2.14. Comparison of frequency spectrum of voltage at IC input

The above figure shows the frequency domain comparison of the voltage waveforms at the IC input from two different ESD generators. We notice resonance peaks at 1.25, 2.5 and 3.75 GHz. These are not actually resonances but artifacts of the AD convertor in the oscilloscope. The artifacts appear in the voltage spectrum for both the ESD generators. The resonance at 0.4 GHz for the NOISEKEN generator is caused due to the coupling from the flex cable. A comparison of the discharge current when the generator is discharged on to the board is measured using an F2000 current clamp and is shown in Figure 2.15. A comparison of the spectrum of the discharge current for the two ESD generators is shown in Figure 2.16.

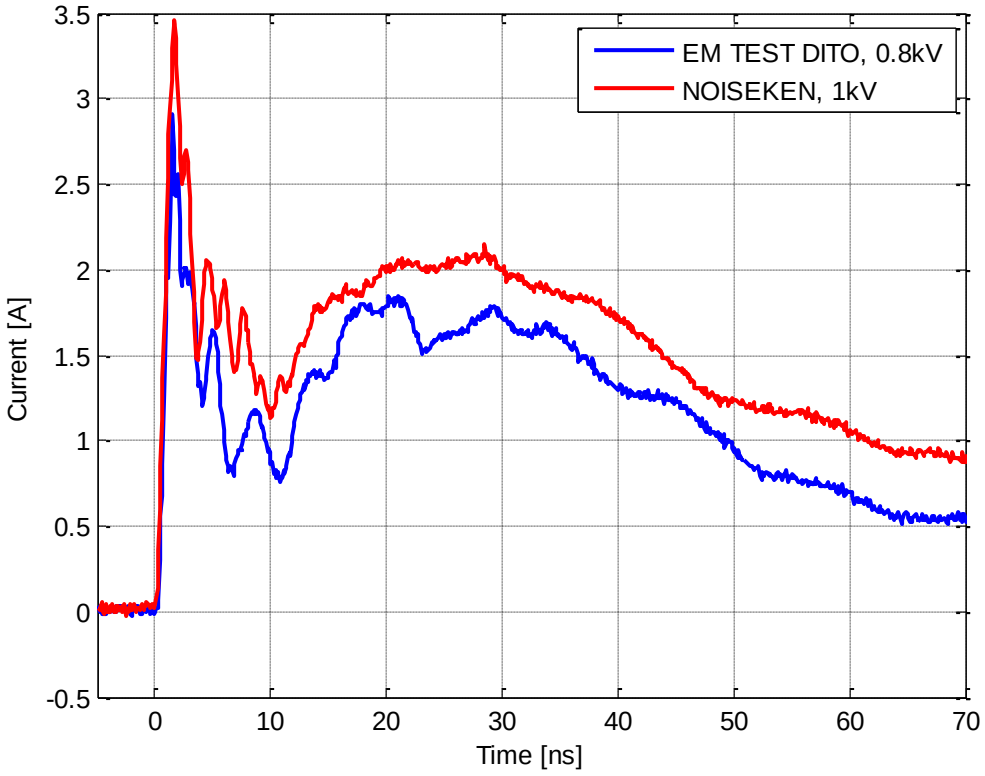

Figure 2.15. Comparison of discharge current onto board

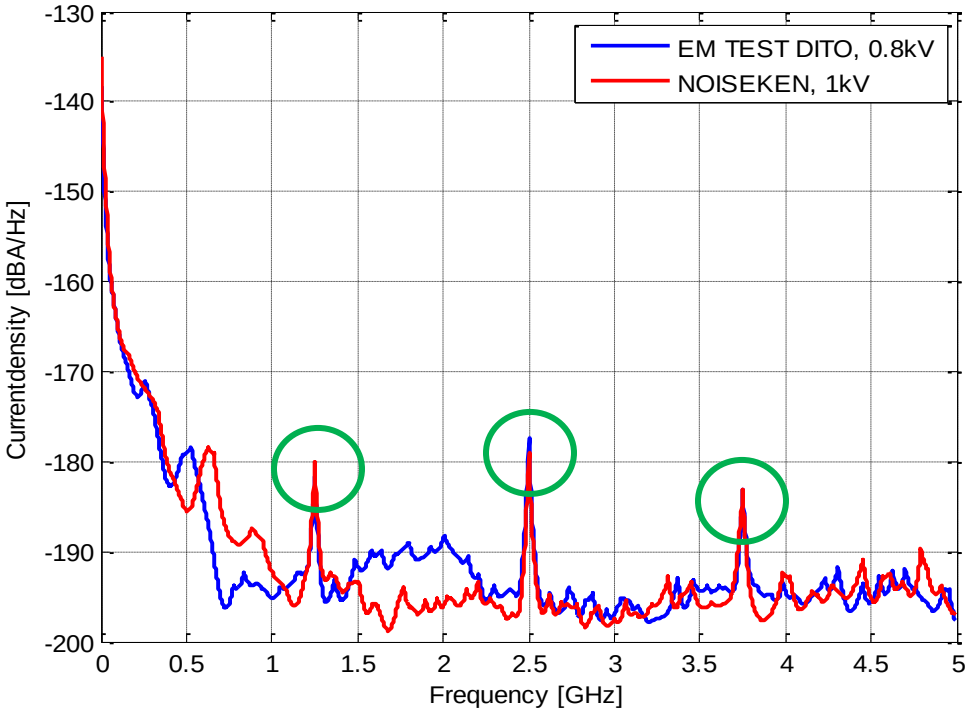

Figure 2.16. Comparison of spectrum of the discharge current onto board

The artifacts at 1.25, 2.5 and 3.75 GHz appear in the discharge current spectrum for both the ESD generators as well. To formulate an expectation of the peak voltage at the IC input for the frequency of interest one can look at the transfer impedance between the discharge point and the IC input. The transfer impedance (Z_T) gives the information on how much of spectral content of the discharge current is transferred to the IC input. It is defined as the voltage at the IC input divided by the discharge current from the ESD generator i.e.

Z_{T_Linear} (Ω/Hz) = Voltage at IC input (V/Hz)/Discharge current (A/Hz)

Or,

Z_{T_Log} (dBΩ/Hz) = Voltage at IC input (dBV/Hz) - Discharge current (dBA/Hz)

Figure 2.17 shows the comparison of the transfer impedance for both the ESD generators when discharged on the board (PCB1). The thing to consider however is, the transfer impedance makes sense only in those regions where both the current density and voltage density spectrum makes sense.

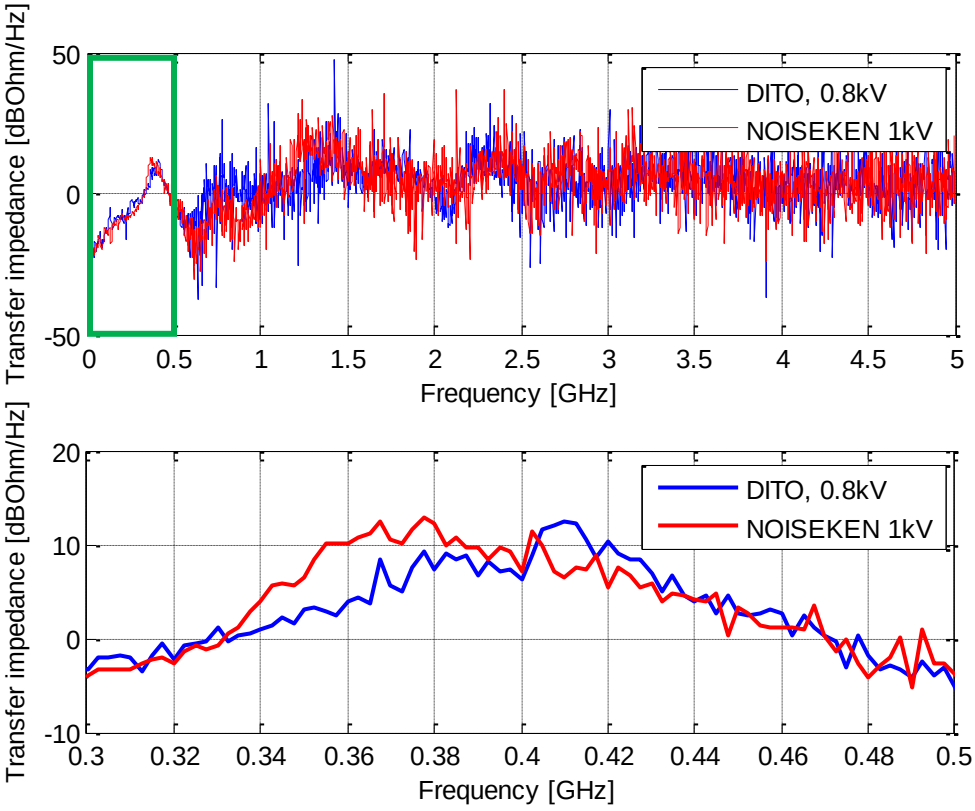

Figure 2.17. Transfer impedance for discharge on to the board

One of the frequencies of interest is the resonance peak at 0.4 GHz caused due to the coupling of the flex cable. In case of the EM-TEST DITO at 0.4 GHz the transfer impedance is 6 dBΩ which implies that for 1A of ESD current one would expect approximately 2V at the IC input.

3. NUMERICAL PREDICTION OF SOFT ERROR ESD UPSET LEVEL

Investigation of ESD related failures with regard to discharge current and voltages using circuit simulators has been performed with fair degree of success [1], [2], [3]. Circuit simulators have been able to predict the failure levels of ICs to ESD. However they suffer from the major drawback that circuit simulators cannot simulate the fast changing electromagnetic fields accompanying ESD discharge. The transient EM fields are in GHz ranges and can cause soft errors in ICs which is difficult to model in SPICE like simulators. Numerous authors have applied numerical methods for calculating coupling of transient fields from ESD [4], [5], [6], [7], [8]. This is one of the main reasons to include the full wave model of the ESD generator, passive DUT structures and input response models of the ICs to accurately simulate the coupling of the fast changing EM fields to the test structure. This section describes the detailed full wave modelling of the interconnected PCB structure with the flex cable and the ESD generator model to simulate the voltage at the IC input in response to coupling of fields via the flex cable PCB. The results from the full wave simulation are subsequently combined with simple IC response models to predict the occurrence of soft error failures in ICs.

3.1 FREQUENCY DOMAIN MODEL OF FLEX CABLE PCB

The objective is to model the flex cable board with the IC and the ESD generator in CST MWS and simulate the voltage at the IC input. The IC input is modeled as passive lumped elements in the CST model. To simulate the voltage accurately two distinct models were developed,

- Frequency domain model of the flex cable board where an injection is made from PORT1 of the network analyzer into PCB1 with reference to the large ground plane while S21 is measured on PORT2 at the IC input.
- After verification of the model in frequency domain, the ESD generator model is included with the DUT model in time domain to simulate the voltage at the IC input.

Previous work on modeling of flex cable PCBs have been performed using both full wave simulation tools [9] and analytical methods [10]. In the present test case the flex cable has 40 traces embedded in a dielectric medium. These 40 traces form highly coupled resonators. Accuracy of the simulation is strongly dependent on modeling the resonances correctly. Moreover it is difficult to model the entire flex cable with so many traces because of the small dimension of the traces. To overcome this, the complexity of the problem was reduced to just three traces on the flex cable.

3.1.1. Measurement setup. The measurement setup of the flex cable board is shown in Figure 3.1.

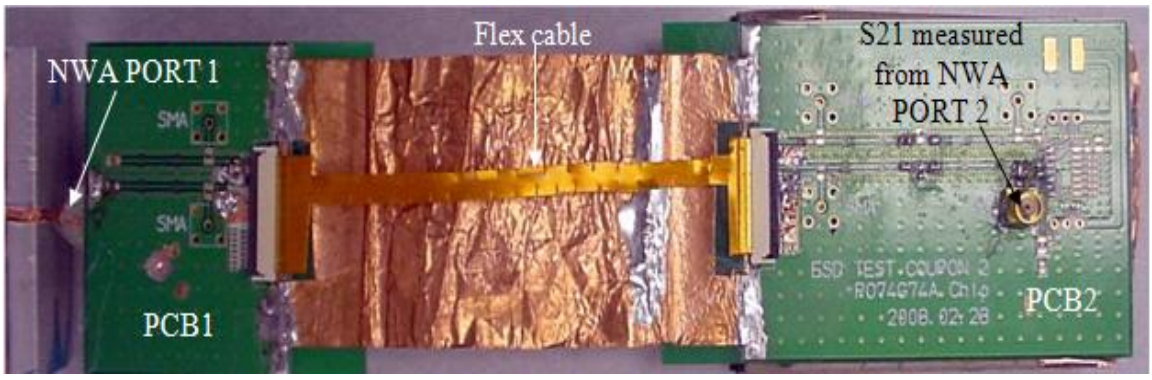

Figure 3.1. Measurement setup for transfer impedance measurement

The two PCB boards interconnected via the flex cable PCB is mounted on a metal table top with good electrical connection to earth ground. PCB1 is kept floating above the table top while PCB2 is connected to the system ground plane through gaskets. An injection is made to the ground plane of PCB1 from PORT1 of the network analyzer. S21 is measured from the SMA connector at PORT2. The SMA connector is mounted at the input to the IC. The three traces on the flex cable are in SIGNAL-GROUND-FLOATING configuration. The copper tape connects the ground plane of the both the PCBs. The flex cable is embedded between two Plexiglass plates. The purpose is to change the wave propagation along the flex cable, which would enable us to see which resonances or which behavior is strongly influenced by the flex cable waves. The signal traces on both the PCBs are terminated with 50 Ω resistors. The transfer impedance measurement is sensitive to the measurement setup and depends on the following factors,

- Height of the flex cable PCB from the copper tape connecting the ground plane of both the boards.
- Orientation of the flex cable meaning whether it is perfectly horizontal or curved to some extent.
- Height of both the boards from the ground plane of the table.
- Reliable connection between the ground planes of the boards through the copper tape.
- Stability at the injection point from PORT1 of the network analyzer to PCB1.

The measured S21 between the injection point and the input to the IC is shown in Figure 3.2.

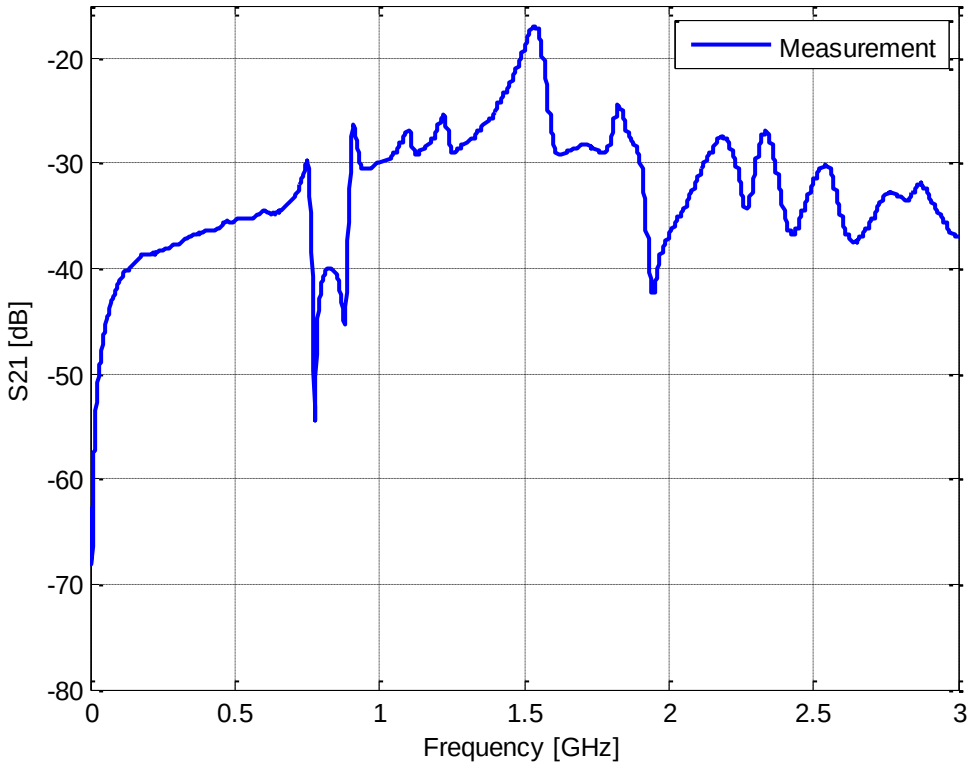

Figure 3.2. Measured S21 of flex cable board

3.1.2. Full wave simulation model. An equivalent full wave CST model of the DUT was created and the simulation results were verified with measurement. The CST model is run in frequency domain solver to compute the transfer impedance (S21) and also the input impedance (Z11) looking into the test DUT from PORT1 of the network analyzer. Only three traces are included in the model. The frequency range of simulation is set from 50 MHz to 3 GHz. Figure 3.3 shows the CST model of the flex cable board.

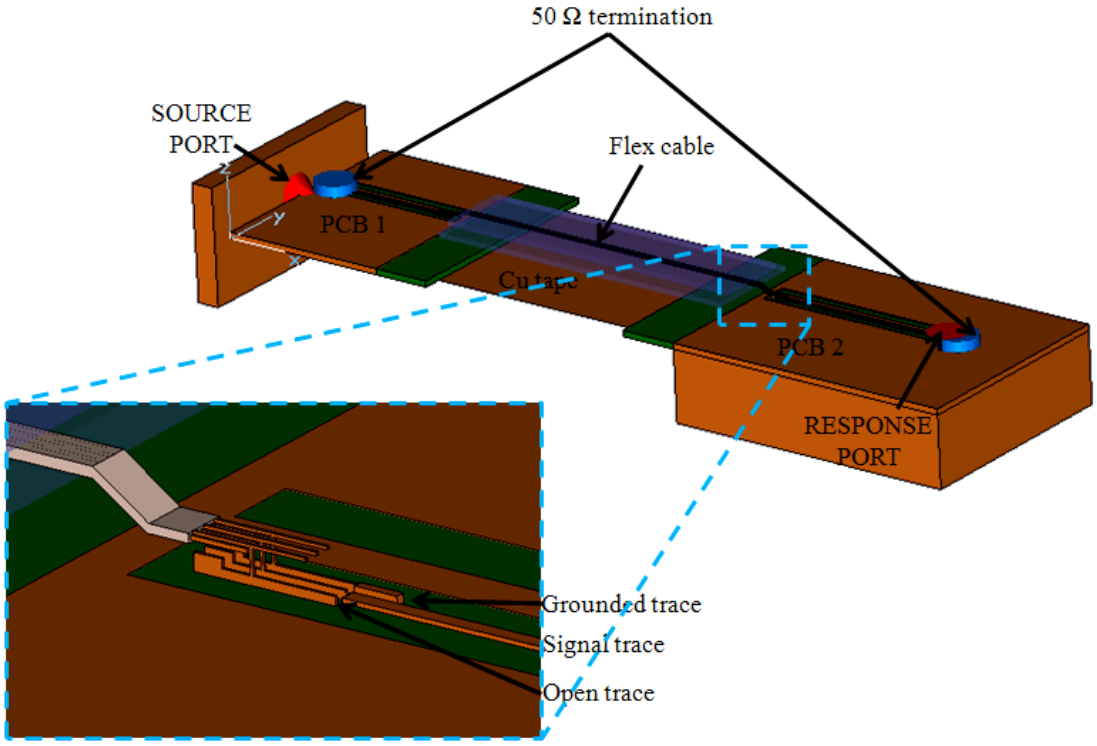

Figure 3.3. CST model of flex cable board

The SOURCE PORT and the RESPONSE PORT are modeled as discrete S parameter ports with 50 Ω reference impedances to represent the network analyzer ports. A magnified view of the flex cable connector is also shown in the above figure. The flex cable connectors are modeled to scale with the actual geometry. In accordance with the measurement setup the traces on the flex PCB are in SIGNAL-GROUND-FLOATING configuration. The terminations on the signal trace are modeled as 50 Ω lumped resistor elements to PCB GND. Table 3.1 shows how each element is modeled and the consequences of those modeling strategies.

Table 3.1: Equivalent modeling of individual components

Real structure	**Model**	**Consequences**
Wall	Modeled as Copper	It is part of the excitation structure and is a metal block.
PCB1 & PCB2 Ground layer	Modeled as copper blocks. The ground layer of the boards are connected by large number of vias, hence this assumption.	From previous modeling experience one can safely assume this simplification.
PCB1 & PCB2 dielectric	Modeled as FR-4 blocks embedded into the ground layer of the boards.	Acceptable solution.
Flex cable traces	Modeled as thin sheet of Copper.	The traces are modeled as 0.15 mm thick with 0.08 mm of dielectric layer above and below.
Signal traces on PCB	Modeled as copper blocks with finite thickness.	Acceptable solution.
Copper connect	Modeled as infinitely thin sheet of PEC to reduce number of mesh cells.	It is not known how the results would change if modeled with some finite thickness.
Extra dielectric	Modeled as FR-4 blocks.	Acceptable solution.
Gaskets	Modeled as copper block.	Acceptable solution.
Cut traces on the flex cable	They are ignored in the model.	Can be safely ignored.

A comparison of the measured and simulated Z11 looking into PCB1 is shown in Figure 3.4. The resonance at 400 MHz matches pretty well. The impedance looking into PCB1 matches quite well over the whole frequency range. A comparison of the measured and simulated S21 is shown in Figure 3.5.

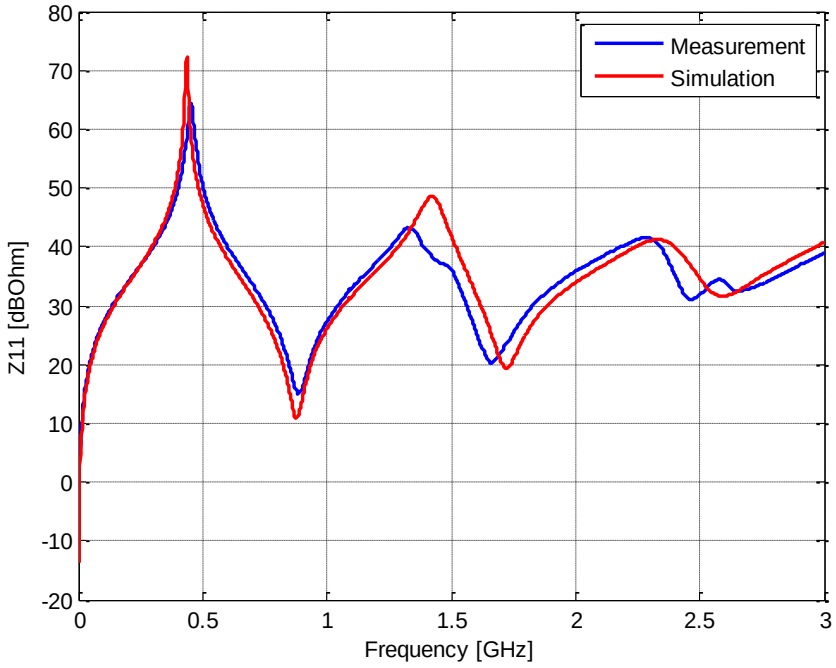

Figure 3.4. Comparison of measured and simulated Z11

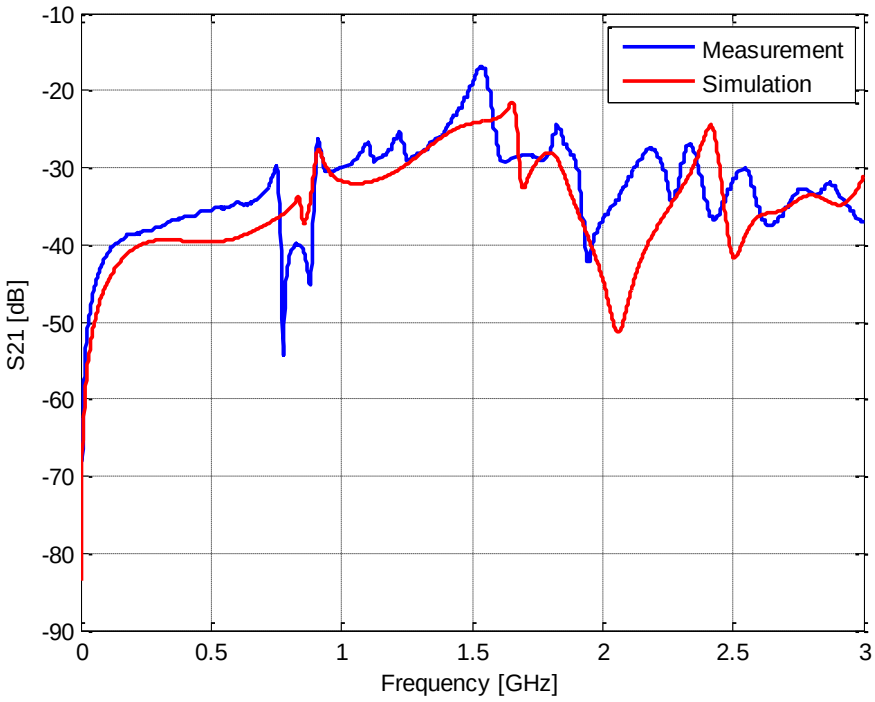

Figure 3.5. Comparison of measured and simulated S21

The measured and simulated S21 matches quite well across the whole frequency range up to 3 GHz. There are certain deviations which are minor and have been accepted.

3.1.3. Challenges in modeling of flex cable structure. Modeling the flex cable structure in full wave simulation tool proved to be quite a challenge. The main reason for that being the individual traces on the flex cable are so close to each other that they form strongly coupled resonators. So any deviation in the shape or orientation of the flex cable would change the resonances in the S21 curve quite appreciably. Also initially certain assumptions were made with regard to modeling the flex cable PCB which turned out to be wrong. To highlight a few of them,

- Initially the flex cable connector was ignored as it was thought to be not critical to the overall setup since it was very small in comparison to the dimension of the flex cable. However it turned out to be a very crucial element for the simulation model.
- The length of the ground connection was not modeled accurately which added extra inductance to the ground trace thereby leading to mismatch between the measurement and simulation results.
- The air volume between the traces of the flex cable and the copper tape was not modeled accurately which again led to differences between measured and simulated results.
- It was assumed that the thin dimension of the traces on the flex cable could be represented as infinitely thin sheets. Also no attention was paid to modeling the dielectric of the flex cable. These two factors also turned out to be very crucial in getting an accurate model of the flex cable.

Figure 3.6 shows an initial comparison of the measured and simulated result taking into account the above mentioned assumptions.

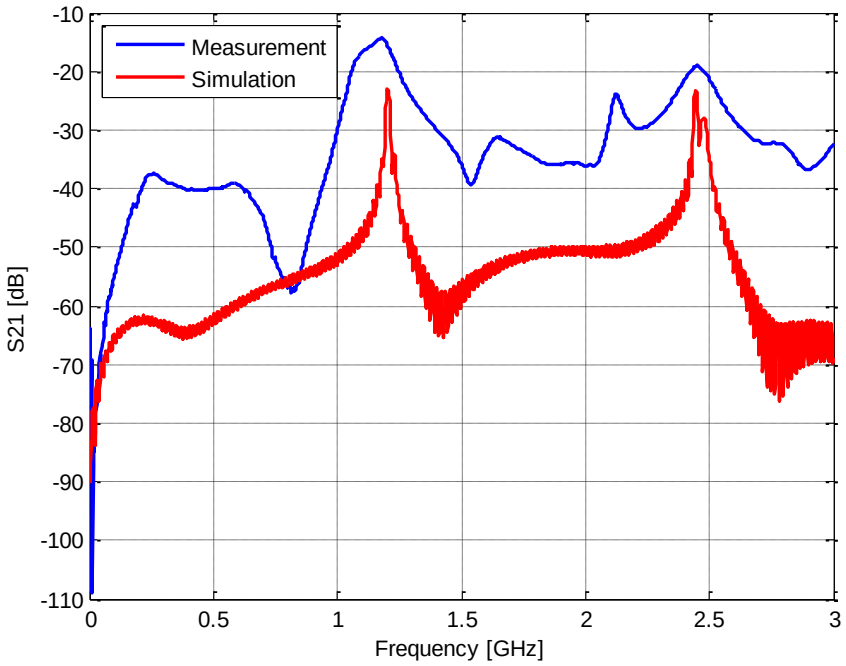

Figure 3.6. Comparison of measured and simulated S21

Comparing the curves in the figure above one can see that there are big deviations between the measured and simulated results. This suggests that the assumptions made initially were wrong to begin with. Taking that into consideration some of the important factors during modeling of the flex cable are listed as follows,

- Modeling of the dielectric in the flex cable is crucial for resonance frequency match. The important parameters are dielectric constant and thickness of the traces in the flex cable PCB.
- Distance between the flex cable and the copper tape is critical. It is important to model the air volume between the flex traces and the copper ground accurately.
- Accurate modeling of the connector pins such as width, length, height and pitch is critical.
- Shape and length of the ground trace is important. Modeling the length of the ground connection inaccurately adds extra inductance to the ground trace which can also cause difference between the measurement and simulation results.

3.2 TIME DOMAIN MODEL OF FLEX CABLE PCB WITH ESD GENERATOR

In the previous section the model of the flex cable board was verified in frequency domain. As the next step a complete model of the flex cable board and the IC input with the ESD generator is combined in time domain to simulate the voltage at the IC input at the instance when it crashes. The model of the ESD generator with regard to discharge current and transient electromagnetic fields had been previously verified in [11]. The full wave simulation is carried out in the time domain solver in CST MWS. Figure 3.7 shows the CST model of the flex cable board with the slow IC and the EM TEST DITO generator.

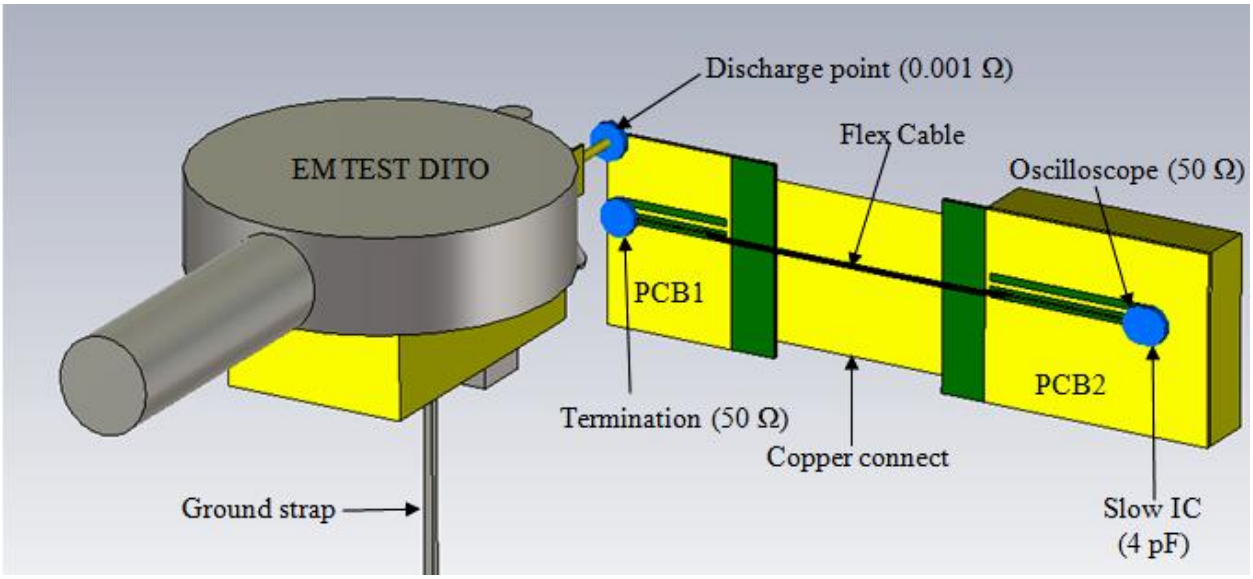

Figure 3.7. CST model of slow IC with flex cable board and EM TEST DITO

From experimental observations it was found that the slow IC triggered at 1 kV when the ESD generator was discharged on the board (PCB1). Hence ESD discharge is simulated at 1 kV. The discharge point is selected 2mm x 2mm from the edge of the board as in the measurement setup. The IC input is modeled as capacitive load of 4 pF obtained from the data sheet. The ground strap of the ESD generator is modeled as a short strap to reduce the size of the computational domain. Length of the ground strap does not affect the initial peak of the discharge current or the peak magnitude of the voltage at the IC input. Discharge tip is modeled as 0.001 Ω lumped resistive element. Voltage at the IC input is simulated as measured on the oscilloscope which is modeled as a 50 Ω lumped element to ground of PCB 2. The signal trace on PCB1 is terminated with 50 Ω in accordance with the measurement setup.

A comparison of the measured and simulated voltage at the slow IC input is shown in Figure 3.8.

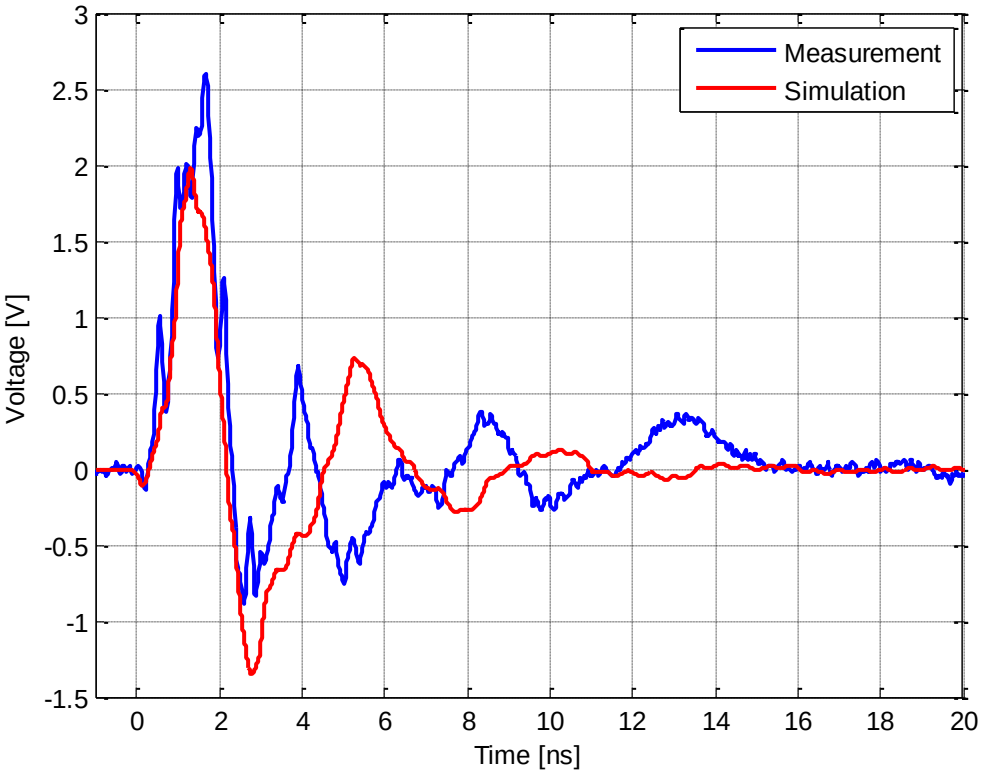

Figure 3.8. Comparison of measured and simulated voltage at the slow IC input

The peak value of the simulated voltage deviates around 0.5 V from the measured data. This small difference has been accepted based on measurement uncertainties. A comparison of the spectrum of the voltage waveforms is shown in Figure 3.9.

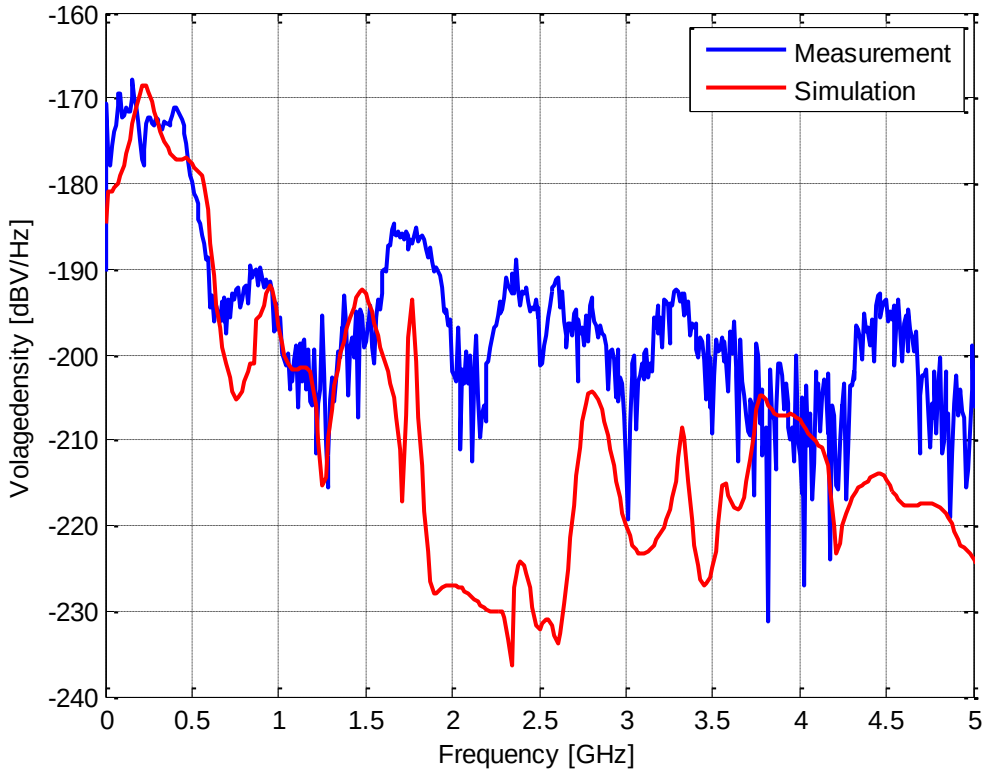

Figure 3.9. Comparison of spectra of voltage at slow IC input

The spectra of the voltage waveform at the IC input matches fairly well up to about 1.5 GHz. The reason for this could be due to limitations of the ESD generator model to simulate the high frequency content of the measured voltage waveform accurately enough. Also the differences between the measured and simulated S21 for the flex cable boards are not exactly matching which adds to the deviation in the frequency spectrum of the voltage at the IC input. Figure 3.10 shows the comparison of the measured and simulated discharge current onto the board at 1 kV ESD charge voltage.

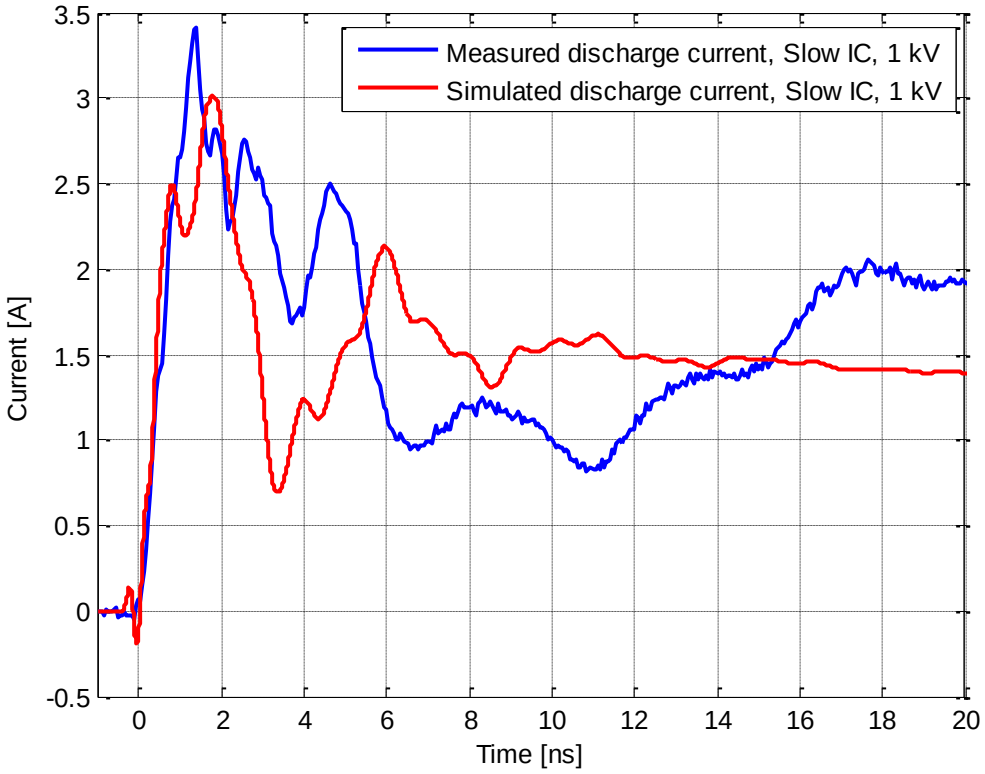

Figure 3.10. Comparison of measured and simulated discharge current

There is a deviation in the peak value of the measured and simulated discharge current. The position of the second peak of the discharge current depends on the length of the ground strap. The longer the ground strap, the farther the second peak is from the first peak. The ground strap length in the simulation model is short which justifies the second peak at 6 ns.

3.3 FULL WAVE MODEL + ESD SOFT ERROR MODEL OF IC

To predict system level ESD failure scenarios the complete simulation model would ideally require the ESD generator model, passive model of the DUT and some form of IC response model. Previous research [11] combines the full wave model of the ESD generator along with passive DUT structure, but no form of IC models. Full wave simulation by itself is not enough to accurately predict the noise voltages at the IC pins in the event of an ESD disturbance. So the ultimate objective is to simulate the time domain voltage waveform in a full wave simulator tool and then combine the simulated result with a soft error upset model of the IC in SPICE to predict the crash levels of the ICs. The next section combines the full wave simulation model (linear) with an equivalent model (non-linear) of the IC to simulate ESD related soft error failure levels.

The CST simulation for the slow IC has been successful with regard to the voltage at the IC input. The SPICE model to predict the crash level of the slow IC is shown in Figure 3.11. V_IC_INPUT is the voltage at the IC input simulated in CST.

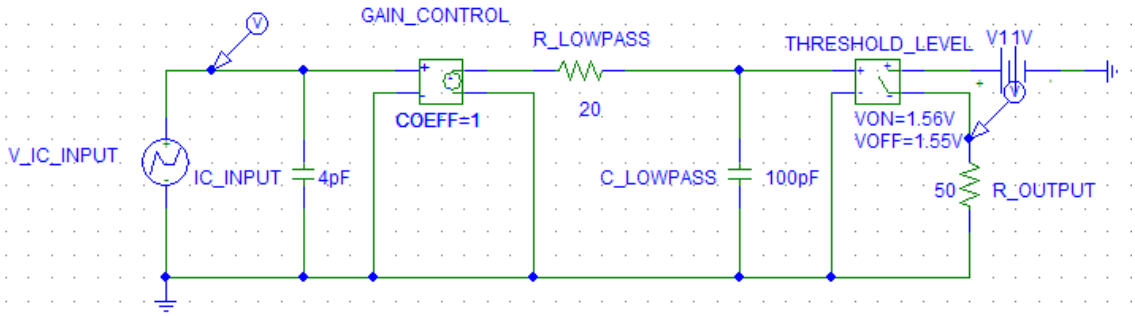

Figure 3.11. SPICE model to predict crash level of Slow IC in response to ESD

Figure 3.12 shows the simulated voltage, V_IC_INPUT.

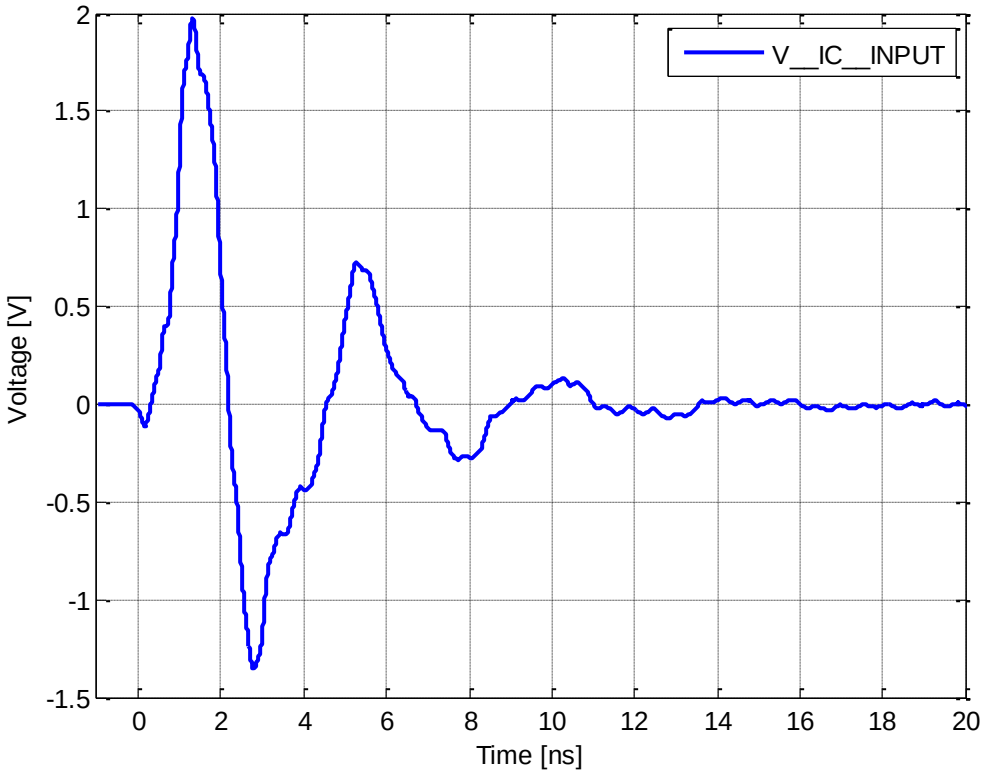

Figure 3.12. Simulated voltage at the Slow IC input in CST MWS

The IC_INPUT is modeled as a 4 pF capacitor to ground. R_LOWPASS and C_LOWPASS form a filter to model the speed of response of the IC. Figure 3.13 shows the speed of response of the slow IC with respect to the peak value of voltage at its input.

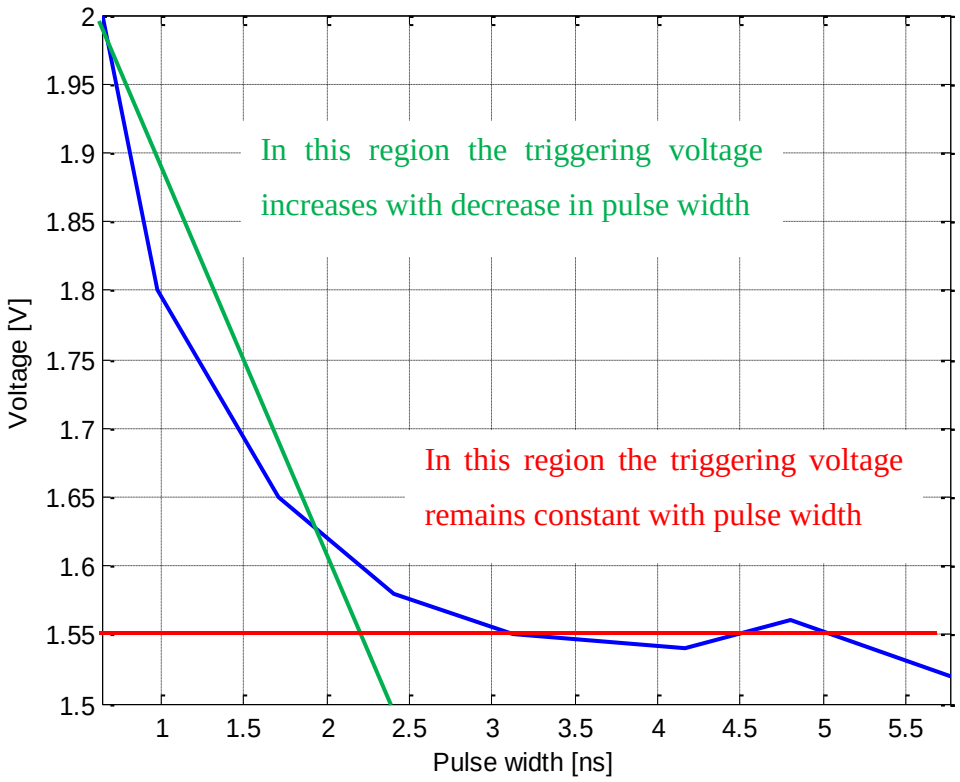

Figure 3.13. Voltage at the IC input vs Pulse width

The threshold curve for the slow IC starts to rise at around 2ns. The R_LOWPASS and C_LOWPASS components model the 2ns (R*C = 20*100 pF = 2*10-9). The threshold level is 1.55 V and is modeled as a switch. If the peak value of the noise pulse at the input to the switch is greater than the threshold level, a square pulse of magnitude 1 is expected at R_OUTPUT, which signifies that the IC has triggered. The voltage at the input to the switch (THESHOLD_LEVEL) is shown in Figure 3.14. Voltage waveform observed at R_OUTPUT is shown in Figure 3.15.

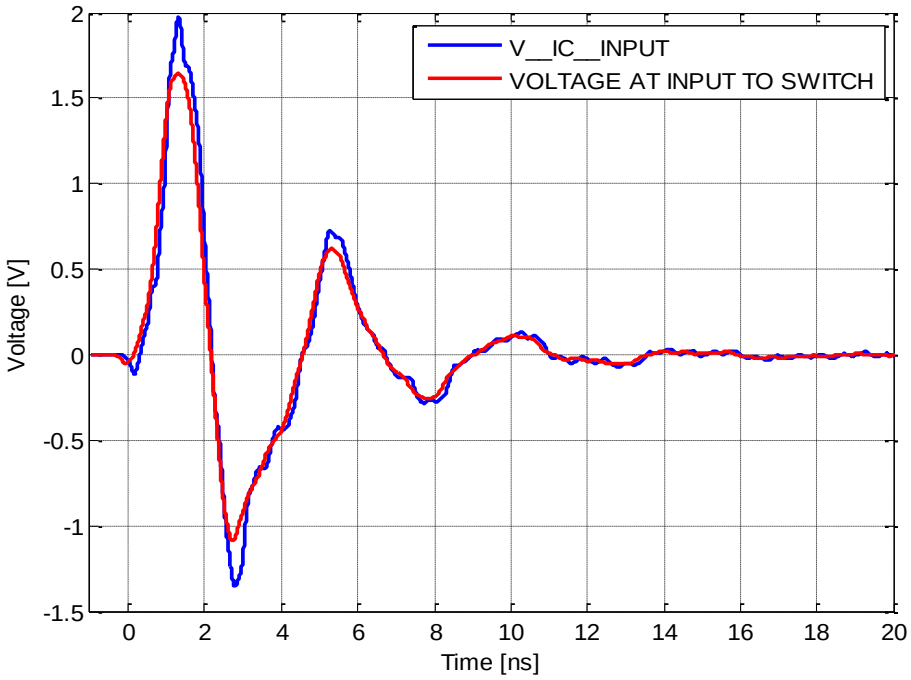

Figure 3.14. Comparison of voltage at the IC input and at the input to the switch

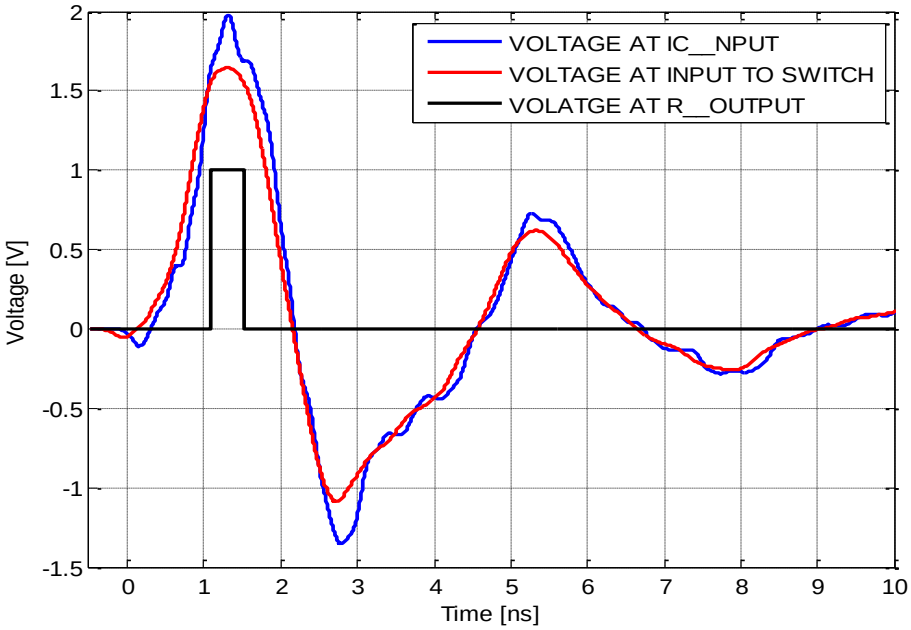

Figure 3.15. Voltage at R_OUPUT indicating that the IC has triggered

When the “VOLTAGE AT INPUT TO SWITCH” is greater than the threshold level i.e. 1.55 V, the voltage across “R_OUPUT” goes to a high (1) indicating that the IC has triggered. This correlates well with the occurrence of soft error in the IC in the event of ESD discharge to the board at a charge voltage of 1 kV.

3.4 CONCLUSION

Touch screen features are increasingly being incorporated into small hand held devices such as mobile phones and PDAs. This would likely lead to increased disturbance from ESD related events. An occurrence of ESD either from a human hand or from any metal object on to the LCD might couple through the flex cable and cause soft error failures in an IC mounted on another board inside the product. Moreover with improved IC technology, the threshold levels in ICs are decreasing as well making them more susceptible to different transient phenomena. Hence it is very important for EMC engineers to get an understanding of the coupling mechanism through the flex cable structure and be able to predict system level ESD disturbances occurring in such devices.

The proposed co-simulation strategy models this specific situation and is able to predict ESD related soft errors in ICs via coupling through flex cable PCBs fairly accurately. The simulation method shows a way to build 3D model of flex cable geometries and also points out the important parameters for consideration during modeling. Also for the first time a full wave model of the ESD generator has been combined with an IC response model and the DUT structure to predict system level soft errors.

4. FIELD PACKAGE INTERACTION FOR IC SOFT ERROR PREDICTION

ESD events on commercial products are accompanied by transient electromagnetic fields which can couple onto ICs leading to soft errors. The lead frame structure of ICs along with bond wire connections often form effective loops which couples to the high frequency fields causing induced noise signals on individual pins of the IC. Estimation of the field strengths, derivatives of the field strengths and noise voltages would help understand the coupling mechanism to the IC in much better way.

This section introduces an efficient co-simulation method to predict soft error response in ICs caused by ESD through a combination of full wave modelling and SPICE simulation. The new strategy is able to quantify field strengths and induced noise voltages on pins of the IC for three different field injection techniques – H-field loop probes, field injection via TEM cell and ESD injection. An electromagnetic coupling model for the lead frame structure of the IC is combined with two types of IC models: an IBIS based model and a lumped element model to simulate noise voltages at the IC inputs. The method is verified by comparing simulated and measured noise signals.

4.1 ESD FAILURE PARAMETERS

The failure levels of the IC can be expressed in different ways based on our requirements,

1) One of the ways to define the failure level is by the TLP charge voltage. However the TLP charge voltage is not a correct representation of the failure levels of the IC. Quantification of the failure levels in terms of the induced currents and voltages would give a much better understanding of the crash levels.

2) A better representation of the failure levels is the field strengths on the lead frame of the IC. Estimation of the field from the loop probes must take into account the ratio of the dimension of the loop to the trace on the lead frame, the height of the loop probe above the lead frame, location of the probe with respect to the trace (offset or no offset), variation of the field underneath the probe and how it wraps around the lead frame. All these considerations have to be taken carefully into account since unrealistic assumptions might lead to deviation of the expected results from actual values.

3) The derivative of the field or current helps to estimate the induced voltages on the lead frame of the IC. The induced voltage gives qualitative information on the maximum noise voltages the IC can tolerate before it crashes.

4) The induced voltages computed from analytical solutions are always a rough estimation of the values. To get accurate results one would need to perform full wave simulation of the lead frame of the IC to determine the field strengths.

4.2 DEFINITION OF TEST PLATFORM

The test bench includes two distinct PCB boards,

1) **Normal board:** This PCB board has a dimension of 15x15 cm. It is a 4 layer board. The stack up configuration of the board is as follows,

   - **Layer 1 (TOP):** SIGNAL (Cu)
   - **Layer 2:** GROUND (Cu)

- **Layer 3:** POWER (Cu)
- **Layer 4 (BOTTOM):** SIGNAL TRACE & GROUND (Cu)

This board is primarily used for field scanning, direct injection and system level ESD tests.

2) **TEM Cell board:** This PCB board has a dimension of 10x10 cm. It is a 4 layer board. The stack up configuration of this board is as follows,

   - **Layer 1 (TOP):** SIGNAL (Cu)
   - **Layer 2:** POWER (Cu)
   - **Layer 3:** GROUND (Cu)
   - **Layer 4 (BOTTOM):** IC PAD WITH VIAS & GROUND (Cu)

   This board is primarily used for TEM cell measurements and also system level ESD tests. On this board the test IC (DDR SDRAM) is mounted on the Layer 4 instead of Layer 1.

The test platform primarily includes three main ICs,

1) **ALTERA EP3C5E144C7N (FPGA IC):** The EP3C5E144C7N is a Cyclone III FPGA from ALTERA. It is mounted in a 144 pin Enhanced Quad Flat (EQFP) package. It operates at three voltage levels 1.2V, 2.5V, 3.3V which is supplied to

the IC by a combination of three voltage regulators. The IC pins are housed in 8 different banks.

2) **MICRON MT46V64M8 (DDR-SDRAM MEMORY IC):** The **MT46V64M8** is a Dual Data rate synchronous high data rate Dynamic RAM organized as 8 x 64 MB, fabricated with MICRON′s high performance CMOS technology. The **MT46V64M8** uses 8 data lines and 13 address lines. It has 66 pins housed in a TSOP (II) package. The interface for the DDR-SDRAM is SSTL2 and the maximum frequency of operation is 133 MHz. The device requires a supply voltage of typically 2.5 V for its operation.

3) **ALTERA EPSC16 (FLASH MEMORY IC):** The EPSC16 is a 16-Mbit flash memory device that serially configures the FPGA IC. It is housed in an 8 pin SOIC package. It has a serial interface that can store configuration data for FPGA devices that support active serial configuration and reload the data to the device upon power-up or reconfiguration.

Figure 4.1 shows the top view of both the test boards. The PCB board primarily includes an FPGA (Cyclone III, EP3C5E144C7N), the flash memory IC (EPSC16) and the test IC (DDR SDRAM memory). A simple READ/WRITE operation is performed where the FPGA generates address and random data bits and writes to DDR SDRAM. It concurrently fetches data from the DDR memory and compares the READ and WRITE data.

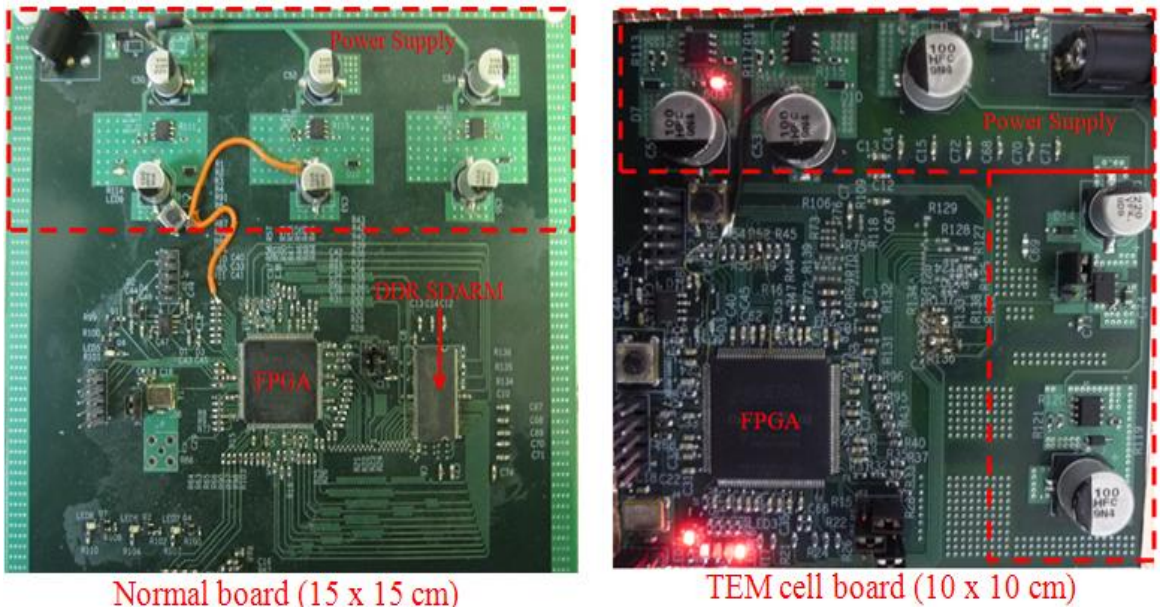

Figure 4.1. TOP view of the test platform

All read & write operations are in burst mode and interleaved with each other. The flash memory is used to program the FPGA so that it can operate in untethered mode. A group of LEDs indicate the status of operation and the failure of the DDR SDRAM memory as shown in Figure 4.2. Table 4.1 gives the functionality of the LEDs.

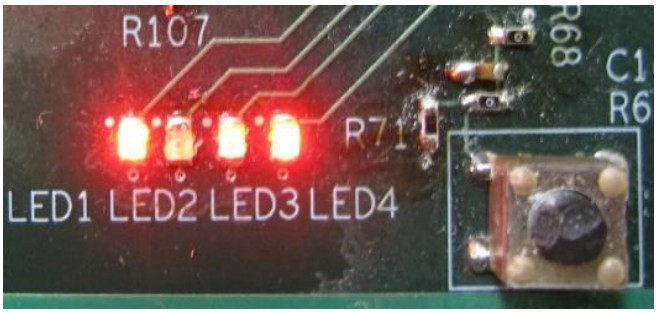

Figure 4.2. Status of the DDR SDRAM memory

Table 4.1. Functionality of the LEDs

LED	STATE	FUNCTION
1	ON	DDR data error
	OFF	No DDR error
3	BLINKING	System is running
	ON/OFF	System stopped
4	ON	FPGA is comparing data
	OFF	FPGA is not comparing data

5. FULL WAVE MODEL OF MEMORY IC (DDR SDRAM)

In order to accurately estimate the field strengths and induced noise voltages in response to field excitations a full wave model of the lead frame of the IC is required [12]. The following sections show the modeling of the individual components of the memory IC. The primary structural components are as follows:

1) Lead frame geometry of the IC
2) Model of die and package of the IC
3) Model of the bond wires in the IC
4) Modeling the Capacitance to the die for VDD, VDDQ and Input pins of the IC
5) Modeling the resistance to the die for bidirectional Data pins of the IC

Full wave model of the DDR SDRAM memory includes the lead frame geometry along with the distributed lumped elements obtained from a combination of IBIS and ICEM models.

5.1 MODEL OF PHYSICAL GEOMETRY OF IC

5.1.1. Lead frame model of IC. The lead frame of the IC was constructed in CST. The lead frame model replicates the exact lead frame structure of the IC. Figure 5.1 and Figure 5.2 shows the lead frame model of the IC. The material property chosen for the lead traces is Alloy42. The reason being for lead frame package, the typical material for the lead frame is Alloy42 (42% Nickel, 58% Iron). The conductivity of alloy42 is σ = 1.64 S/m.

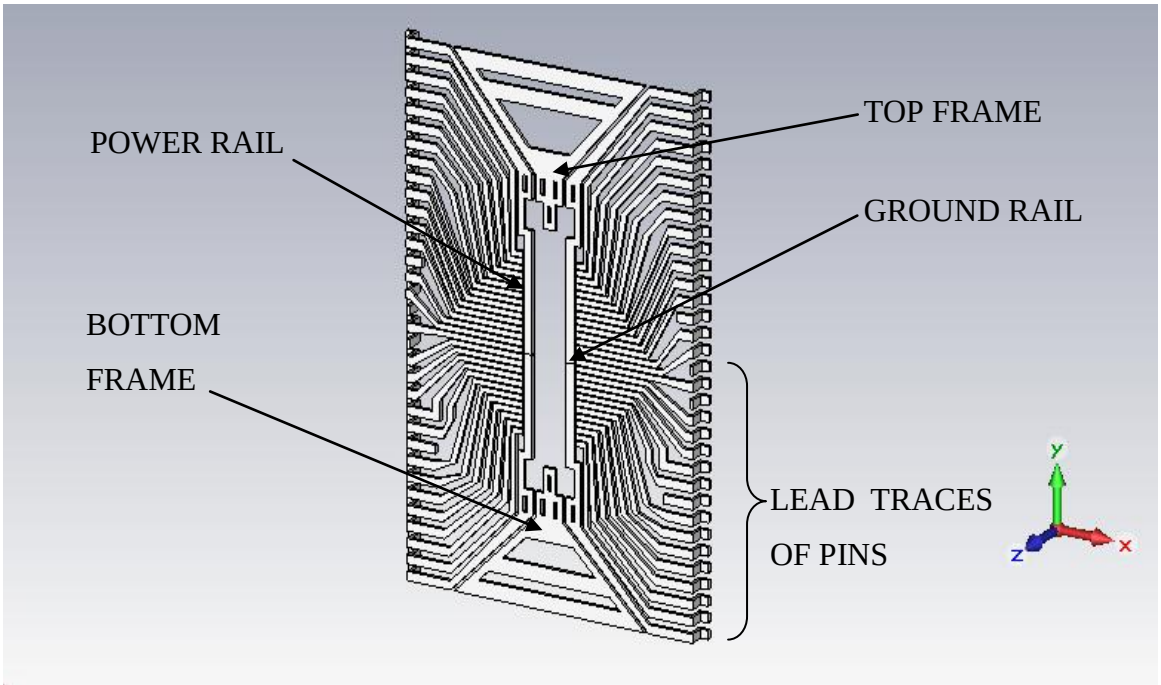

Figure 5.1. Lead frame model of the IC

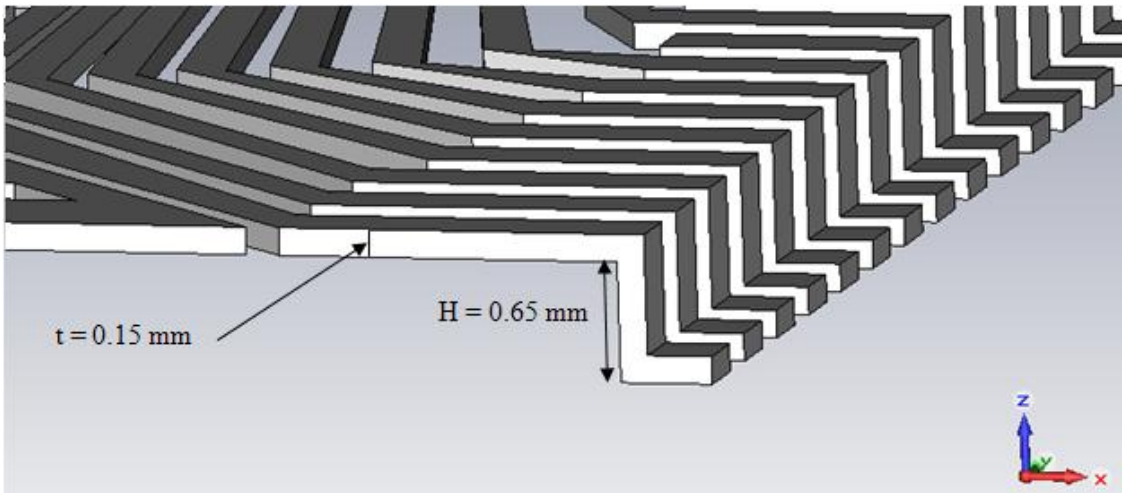

Figure 5.2. Dimension of lead traces

Thickness of the lead traces is 0.15 mm and the height of the lead frame structure is 0.65 mm.

5.1.2. Die and package model of IC. The die inside the IC has been modeled as a solid rectangular block as shown in Figure 5.3. Figure 5.4 shows the cross sectional model of the lead frame of the IC along with the die.

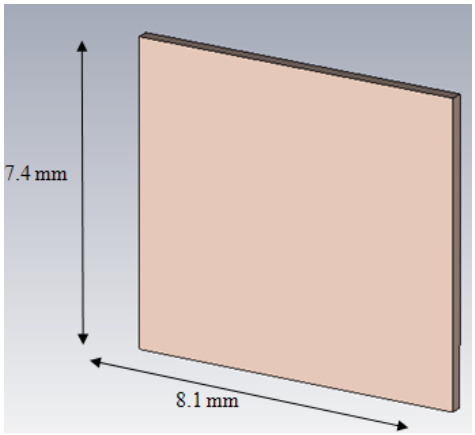

Figure 5.3. Die model of the IC

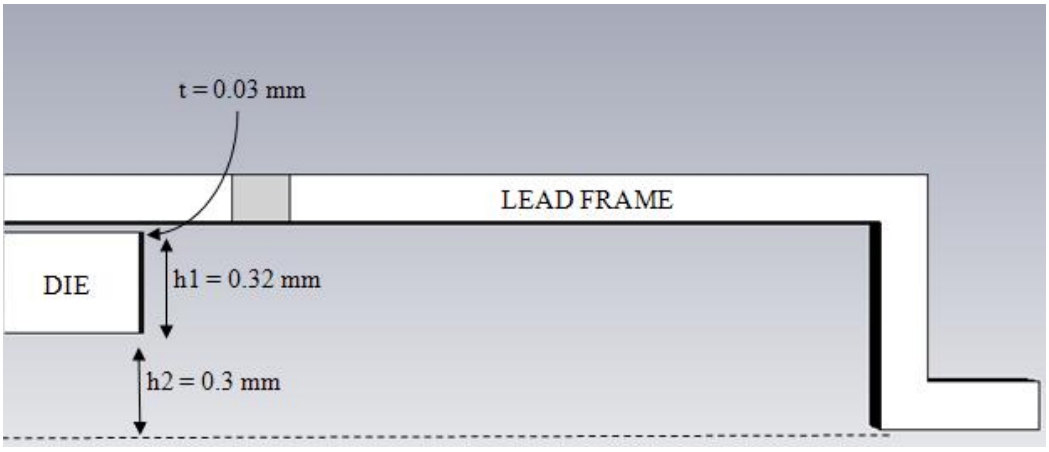

Figure 5.4. Cross sectional view of the die with the lead frame

The distance between the die and the lead frame of the IC is 0.03 mm. In reality the material property of the die is Silicon with varying degree of doping concentrations leading to highly non linear behavior. Hence modeling the die with silicon is improbable in a full wave simulation tool. As a consequence, the die is modeled as a PEC block so that it could be modeled linearly in CST MWS. All the geometries and dimensions have been measured with high degree accuracy. The package for the IC is also modeled as a solid rectangular block as shown in Figure 5.5.

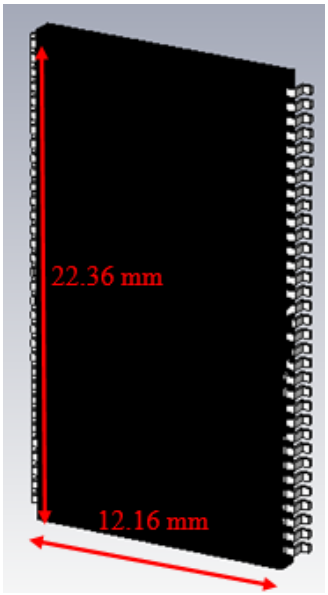

Figure 5.5. Package model of the IC

The material property chosen for the package Epoxy with $\epsilon_r = 4$ according to the default value in CST. The height of the package above and below the lead frame has been measured and modeled accordingly.

5.1.3. Bond wire model of IC. Modeling of the bond wire is very crucial to accurate estimation of the field strength coupling to the IC. The reason being, coupling of transient EM fields to the bond wires is highly dependent on the dimensions, orientation and loop area. Hence inaccurate modeling of the bond wires would lead to over estimation or under estimation of the field components coupling to it. It was difficult to determine the exact diameter and height of the bond wire from the X-ray pictures of the IC. As an alternative typical values (available from commercial ICs) for the height and the diameter were used for our purpose. Typically A-14 type bond wires are used for TSOP type packages. The bond wires are made of gold and have a diameter of 25 µm and a height of 160 µm. Figure 5.6 shows the bond wire model of the IC.

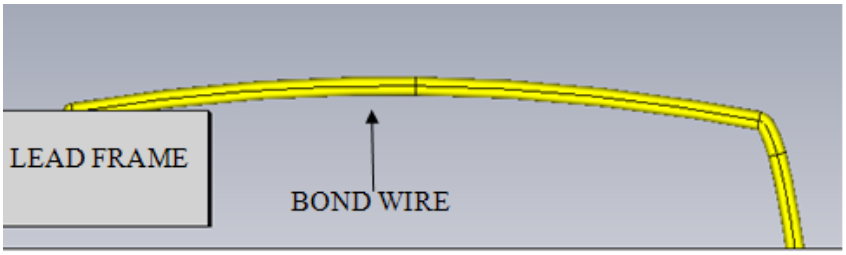

Figure 5.6. Bond wire model of the IC

The diameter of the wire is 25 µm and the height is 160 µm. The material property chosen for the bond wire is gold with a conductivity of $\sigma = 4.09*10^7$ S/m according to the default value in CST.

5.2 EXTRACTION OF LUMPED PARAMETERS FROM IBIS/ICEM MODELS

5.2.1. Capacitance from VDD to VSS. The ICEM model provides the capacitance value between the power rails. However the IC manufacturer usually does not provide the ICEM models. So in order to get the capacitance value a measurement setup is made to measure this value. The measurement setup is in accordance with the ICEM standard [22]. Figure 5.7 shows the experimental setup.

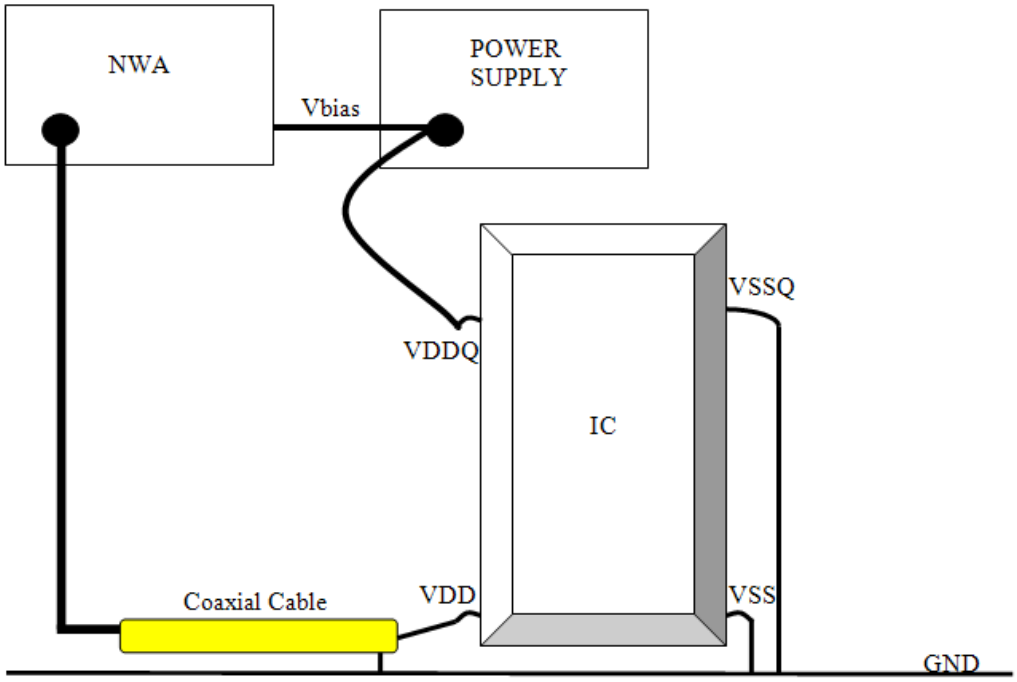

Figure 5.7. Experimental setup to measure capacitance

The figure above shows the experimental setup to measure the capacitance value. The VDD pin of the IC is connected via a coaxial cable to PORT 1 of the NWA. Outer

conductor of the coaxial cable is connected to GND and the inner conductor is connected to the VDD pin. VSS pin is connected to GND. The VDD pin of the IC is biased to different voltage levels via a power supply which biases PORT 1 of the NWA through the back panel. VDDQ pin is also biased to the same voltage as VDD during the measurement. All the remaining pins of the IC are kept floating. The capacitance value between VDD and VSS is obtained by measuring the input impedance looking into the VDD pin while the IC is biased to VDD/2. The input impedance looking into the VDD pin, for three different bias voltages are shown in Figure 5.8.

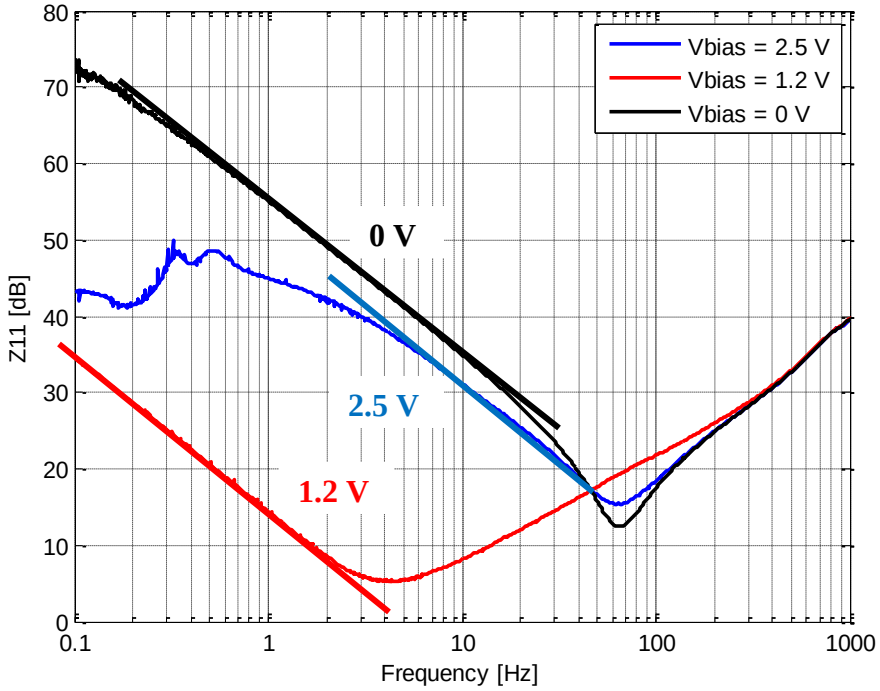

Figure 5.8. Measured Impedance looking into VDD pin

From the above figure, when the bias voltage is 1.2 V i.e. half of the VDD (2.5 V), we observe the capacitance between VDD and VSS. The capacitance value is approximately 30 nF. This capacitance is total capacitance between the VDD and VSS rails in the IC. At 2.5 V bias voltage, non liner switching circuits turn on inside the die which causes the resistive region at lower frequencies. The switching behavior of the non linear circuit is also visible at low frequencies. The rising part of the curve is caused due to the inductance of the path between the VDD and VSS pins.

We select the capacitance value corresponding to 1.2 V bias voltage. The capacitance value obtained is 30 nF. From the X-ray model of the memory we see that there are four bond wire connections between VDD power rail and VSS ground rail through the die (the die is modeled as PEC). So this capacitance is modeled as distributed capacitance between the bond wires and the die in the CST model. Figure 5.9 shows the CST model of the IC in accordance to the measurement setup.

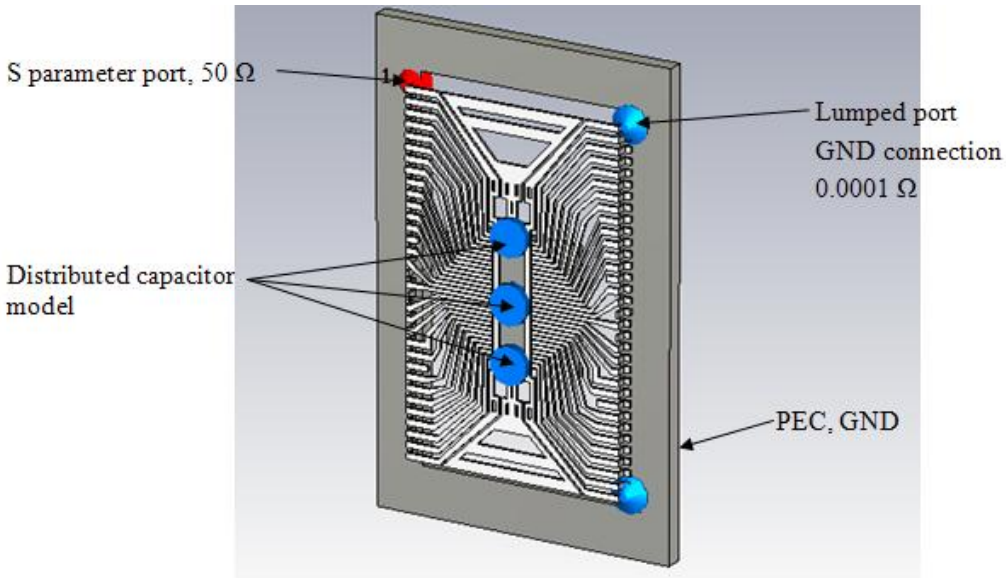

Figure 5.9. CST model to simulate Z11 into VDD pin

The above figure shows the CST model to simulate the impedance looking into the VDD pin of the IC. Going along with the measurement setup, all other pins of the IC model are kept floating. Figure 5.10 shows a magnified view of the distributed lumped capacitor added to the model.

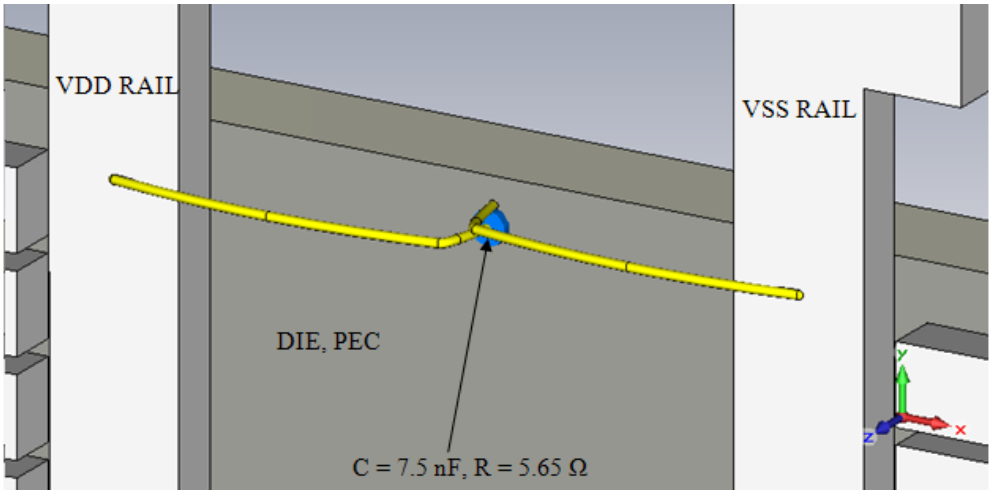

Figure 5.10. Distributed lumped modeling of capacitance between VDD and DIE

The figure above shows the magnified view of one of the four bond wire connections. For modeling purpose the total capacitance value (30 nF) is divided in parallel between four bond wire connections to the die. In reality all the VDD pins are connected to each other and the on die capacitance is the equivalent capacitance of the all the VDD pins to the die. A lumped element is connected between the VDD bond wire and the die to simulate the capacitance between VDD and VSS. The parasitic resistance is added to match the measured impedance curve. Figure 5.11 shows the comparison of the measured and simulated results.

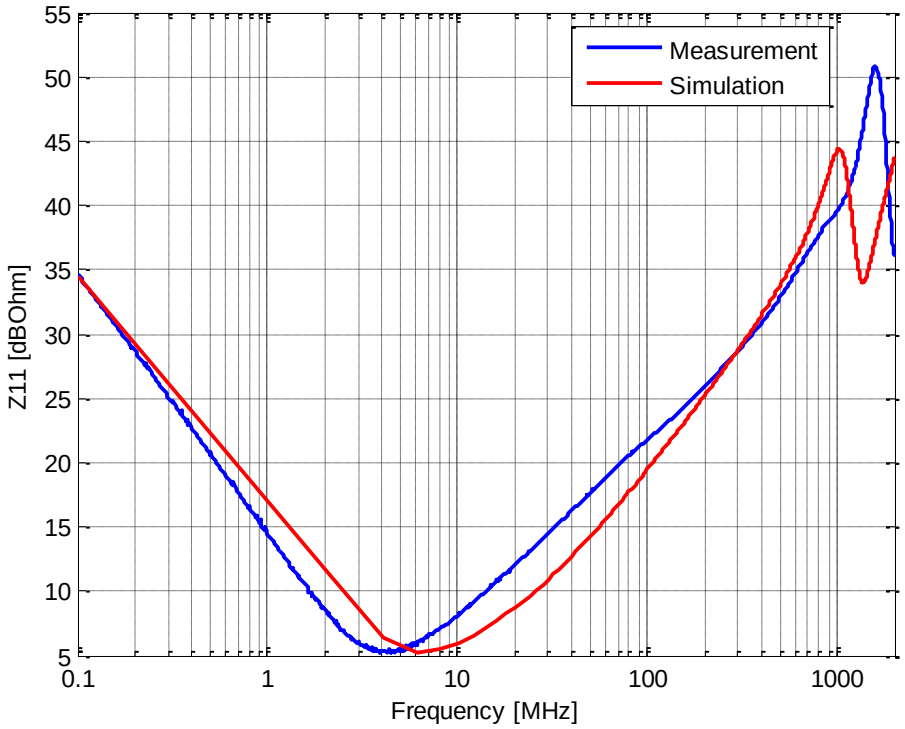

Figure 5.11. Comparison of measured and simulated Z11 into VDD pin

From the above figure we see that the results match quite well except the difference in resonance frequency. Fine tuning of the CST model would give us a more accurate match.

5.2.2. Capacitance from VDDQ to VSSQ. The same procedure was adopted to measure the capacitance between the VDDQ pin and the VSSQ pin. The only difference in the measurement setup was that this time around the IC was probed on the VDDQ pin and VSSQ pin was grounded. At the same time the VDD pin of the IC was biased at the same voltage as VDDQ. All other pins of the IC were kept floating as before. Figure 5.12 shows the impedance measured looking into the VDDQ pin for different bias voltages.

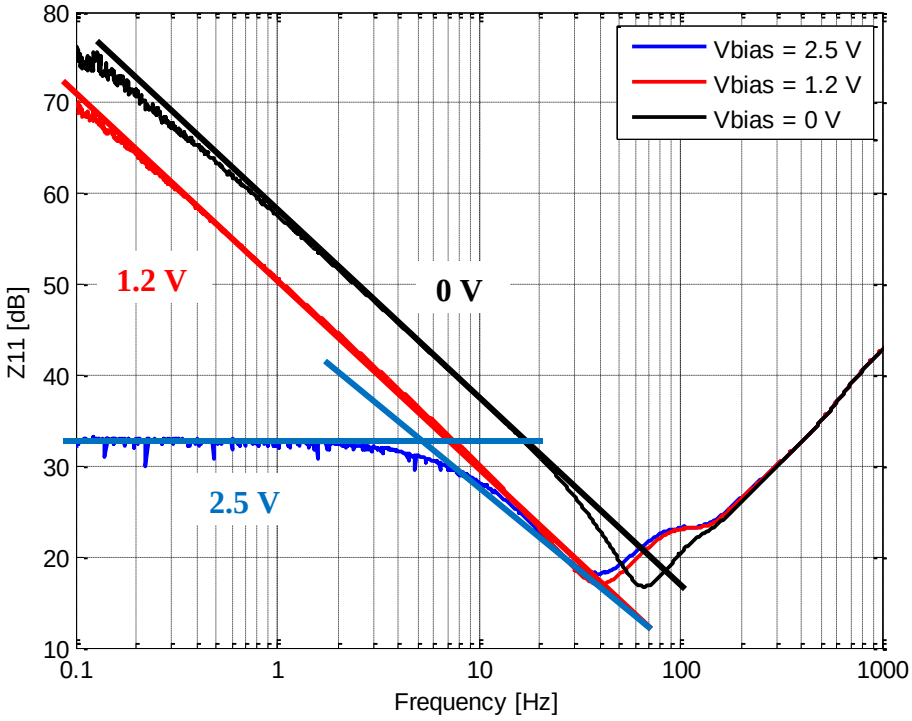

Figure 5.12. Measured Impedance looking into VDDQ pin

From the above figure, when the bias voltage is 1.2 V i.e. half of the VDD (2.5 V), we observe the capacitance between VDDQ and VSSQ. The capacitance value is approximately 464 pF. This capacitance is total capacitance between the VDDQ and VSSQ pins in the IC. At 2.5 V bias voltage, we again see that resistive region in low frequency range. For our simulation model we model the capacitance between the VDDQ and VSSQ pins at 1.2 V bias voltage. The capacitance value obtained is 464 pF. From the X-ray model of the memory we see that there are five bond wire connections between VDDQ and VSSQ through the die (the die is modeled as PEC). So this capacitance is modeled as distributed capacitance (92.8 pF) between the bond wires and the die in the CST model.

5.2.3. Capacitance from Input to VSSQ. The capacitance from the Input classes of pins to the VSSQ is obtained from the IBIS model provided by the IC manufacturer. The input pins are divided into two classes of pins. All the command pins and the address pins are categorized as INPUT1 class of pins. This capacitance value is modeled a lumped 1.25 pF capacitor. The address pin A12 is categorized as INPUT2 class of pin whose capacitance value is 1.4 pF. Both the capacitances are modeled as a lumped capacitor element between the bond wire and the die. For the CLK pins the capacitance value is obtained as 1.4 pF.

5.2.4. Model of I/O pins (DQ, DQS, DM). The I/O pins could be in three different states. They are listed below as,

- **Input:** When data is written to the memory IC, the DQ/DQM pins acts as input pins. In this state we model the connection between the bond wire and the die as a capacitive lumped element derived from the IBIS model of the IC. The capacitance value for the lumped element is 3 pF for DQ0-DQ7, 3.3 pF for DQS pin and 3.85 pF for DM pin.
- **Output High:** When data is read from the memory IC, the DQ/DQM pins acts as output pins. The lumped resistance value added to the CST model is obtained from region shown in the V-I curve of the IBIS model in Figure 5.13. The resistance value is obtained from the region shown by the green curve. The differential resistance obtained is 12 Ω.
- **Output Low:** In the ouput-low state the resistance value is obtained from the V-I curve of the IBIS model from the region marked in red in Figure 5.14.

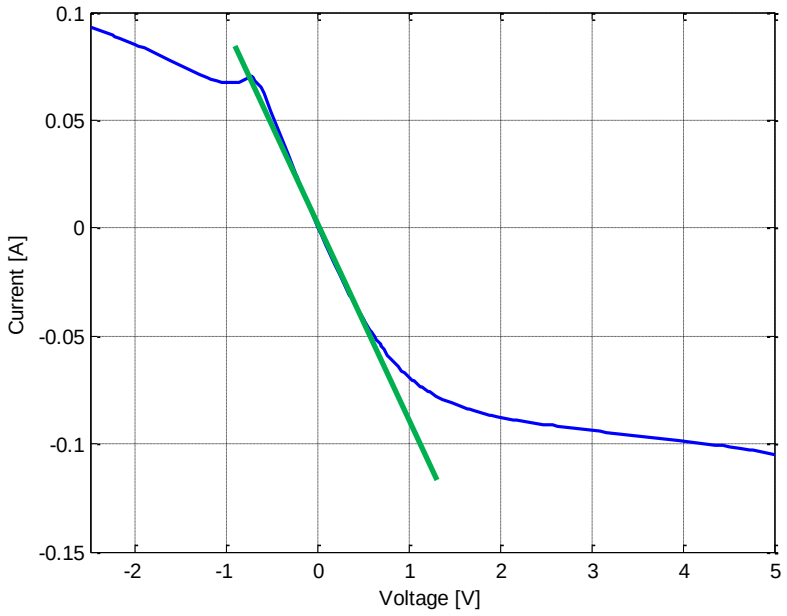

Figure 5.13. Pullup V-I curve for DQ pins obtained from IBIS model

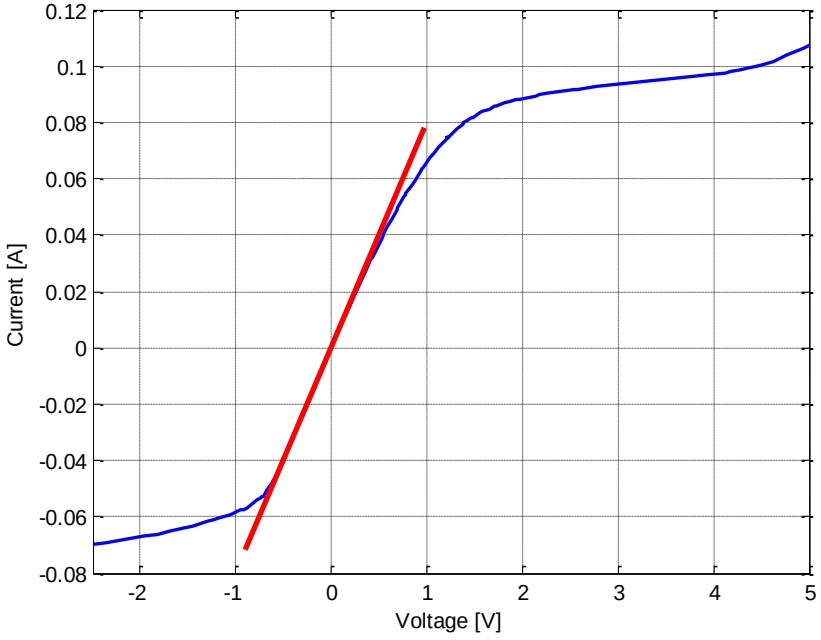

Figure 5.14. Pulldown V-I curve for DQ pins obtained from IBIS model

The resistance value is obtained from the region shown by the green curve. The differential resistance obtained between 0V and 0.5V is 12.5 Ω.

5.3 CONCLUSION

Full wave modeling of the lead frame of the IC along with accurate modeling of the bond wires and distributed lumped elements obtained from a combination of IBIS and ICEM models can help to predict the field strengths and induced noise voltages when subjected to field excitations. Simulation of the induced noise voltages can be performed either in frequency domain or time domain. In frequency domain the S-parameter block of the geometry is obtained and then combined with the IBIS model of the particular pin to obtain the voltages at the interconnect level. On the other hand in time domain simulation an equivalent lumped model of the memory IC is used to obtain the voltages at interconnects directly.

To obtain the capacitance of the VDD and VDDQ pins to the die, measurements have been performed in accordance with the standard [2222]. The capacitance for the VDD pins comes out to be in the range of 30 nF and for the VDDQ pins it is around 460 pF. These capacitances can be modeled as distributed lumped elements in our full wave model. The capacitances of the Input class of pins (Address pins/Control pins) have been obtained from the IBIS model. The capacitance value is typically 1.4 pF. These capacitances have also been modeled as lumped capacitive elements.

For the I/O class of pins (Data pins), the connection between the bond wire and the die could be either a capacitive element when it is acting as an Input pin (when data is written to the memory IC) or a resistive element (when data is read from the memory IC).

The capacitance value is again obtained from the IBIS model and the resistive values are obtained from the pull up and pull down curve in the IBIS model. The capacitance value is 3 pF and the resistance value is typically low at around 12 Ω.

6. FIELD SCANNING OF DDR MEMORY IC

The objective of this test was to do a preliminary manual scanning of the test IC (DDR SDRAM memory) to obtain an initial idea of the crash level expressed in terms of the field strength, derivative of the field strength and induced voltages at the lead frame of the IC. A number of different E/H field probes were selected for this purpose.

6.1 MEASUREMENT SETUP

Manual field scanning is performed on the larger board (Normal board, 15 cm x 15 cm). Once the system is functioning normally, E/H field probes are moved manually over the memory in an attempt to cause failure. In the test case a failure is defined as a mismatch between the READ and WRITE data. While performing the test, LED1 is monitored which shows a comparison of the READ and WRITE data. Figure 6.1 shows the experimental setup for the test.

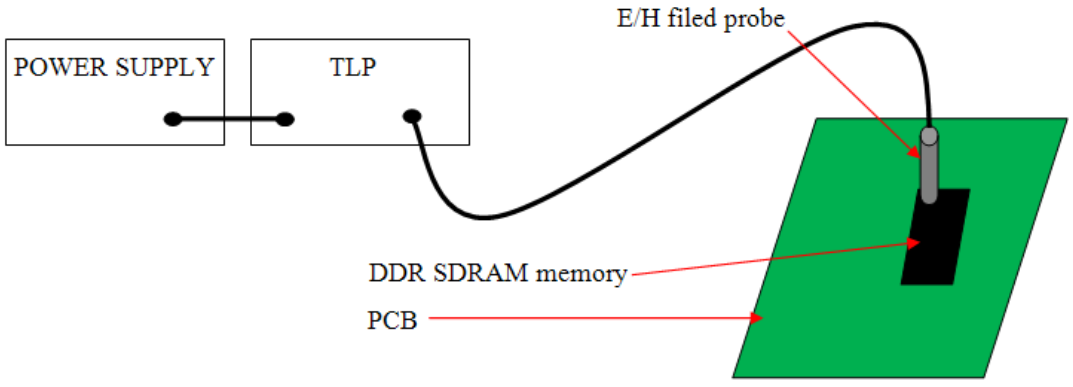

Figure 6.1. Experimental setup for the test

The experimental setup includes a high voltage power supply, a transmission line pulser (TLP) and number of E/H field probes. The H field probes used for excitation is shown in Figure 6.2,

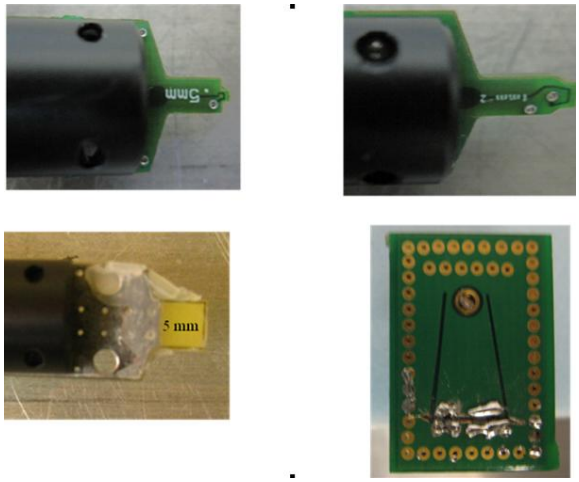

Figure 6.2. H field probes used for manual scanning

Manual scanning is performed by exciting the probes with the TLP and moving them manually over the memory in an attempt to cause failure. When LED1 glows it indicates that there is an error and the TLP voltage is recorded. For the H field probe the scanning is performed in both the polarization as shown in Figure 6.3. The current research draws from the previous work on susceptibility of ICs in response to near field aggression [13], [14], [15], [16].

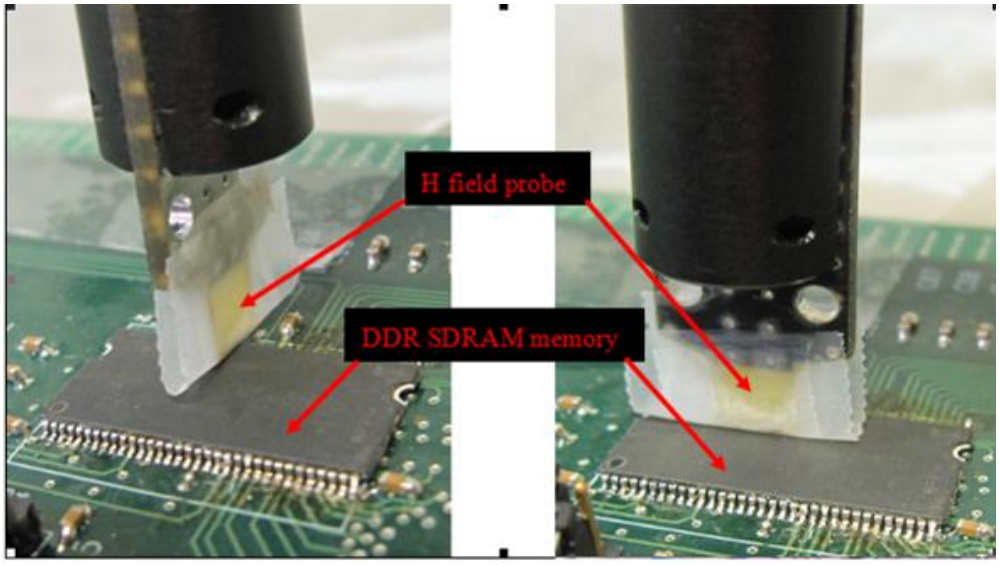

Figure 6.3. Manual scanning of DDR memory with H field probe in dual polarization

6.2 ANALYTICAL ESTIMATION OF MAGNETIC FIELD STRENGTH

As the first step one needs to formulate an expectation of the failure levels of the test IC by analytically determining the field strengths at the height of the lead frame of the IC. Figure 6.4 illustrates computation of the H field strength at the height of the GND plane.

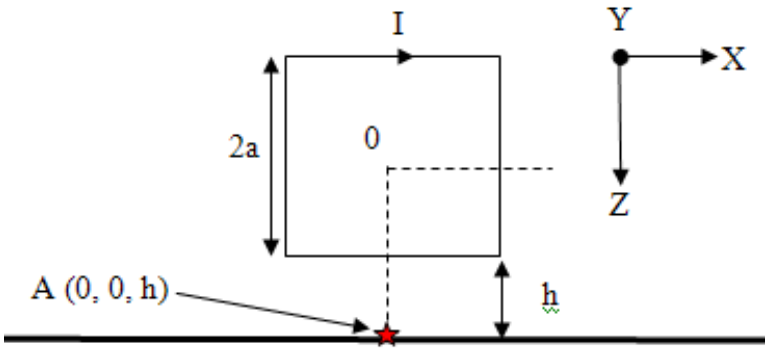

Figure 6.4. Orientation of the magnetic field loop probe above the GND plane

The figure above shows a vertical square loop with edge length '2a' above the ground plane. The height of the loop above the ground plane is 'h'. There is no other metal in between the loop probe and the GND pane. Using image theory the magnitude of the field can be determined right beneath the loop probe at a point on the GND plane [23]. The vector potential of the field can be determined by,

$$\vec{A}(\vec{r}) = \hat{a}\frac{\mu I}{4\pi}\int_{I_1}\frac{dl'}{\sqrt{(x-x')^2+(z-z')^2+(y-y')^2}}$$

and the magnetic field, H, can be obtained by,

$$\vec{H}(\vec{r}) = \frac{1}{\mu}\nabla\times\vec{A} = \hat{a}_x\frac{\partial A_z}{\partial y} + \hat{a}_y\left(\frac{\partial A_x}{\partial z} - \frac{\partial A_z}{\partial x}\right) - \hat{a}_z\frac{\partial A_x}{\partial y}$$

The field strength is calculated at the point **A (0, 0, h)**. At that point $\frac{\partial A_x}{\partial y} = 0$, $\frac{\partial A_z}{\partial y} = 0$. Therefore the only remaining component of the field is the 'Y' direction. The PCB loop probe is excited by TLP pulses of varying magnitude. Figure 6.5 shows the TLP pulse at 500 V charge voltage measured on an oscilloscope. The oscilloscope loads the TLP with 50 Ω. The peak value of current (I), is ~ 500/50, 10 Amps. The magnetic field strength (H) is proportional to the TLP voltage. The magnitude of field strength also increases with increase in loop size for the same TLP charge voltage.

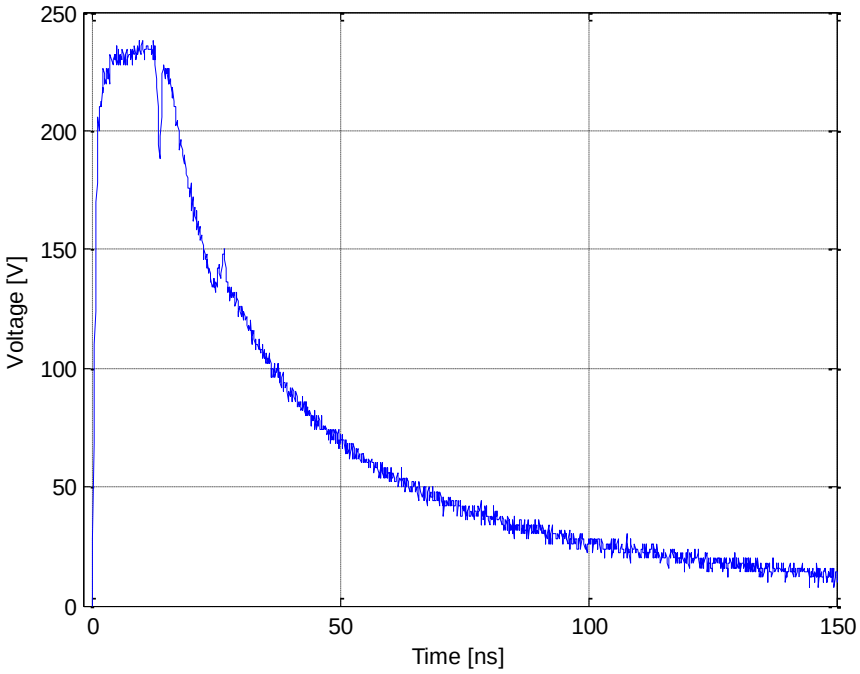

Figure 6.5. TLP voltage waveform at 500 V charge voltage

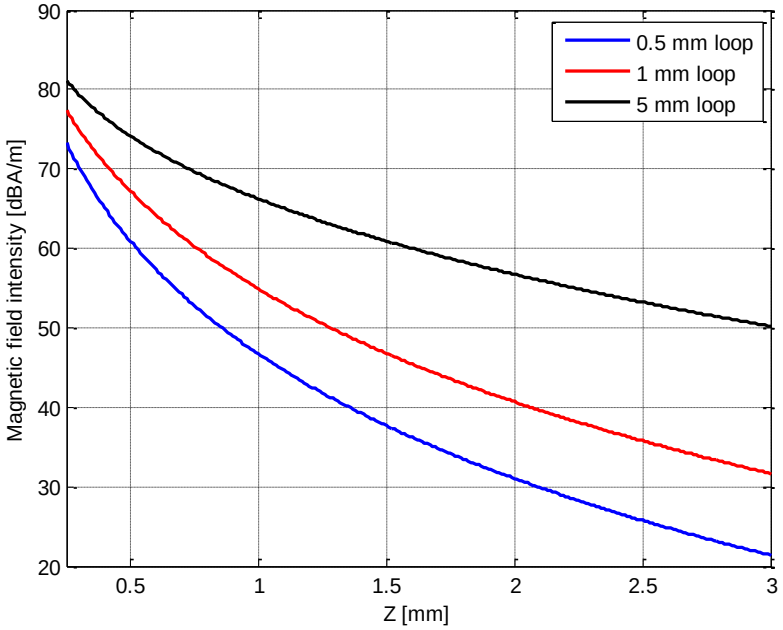

Figure 6.6. H field strength vs Height above GND plane at TLP voltage of 0.5 kV

Figure 6.6 shows the variation of the magnetic field strength with respect to the height of the probe above the GND plane. From Ampere's law, at small distances the magnetic field varies as 1/h and as the distance increases the magnetic field varies as $1/h^2$. As the next step the field strength at the height of the lead frame of the IC is computed [23]. Figure 6.7 illustrates an example for the 1 mm H field loop probe.

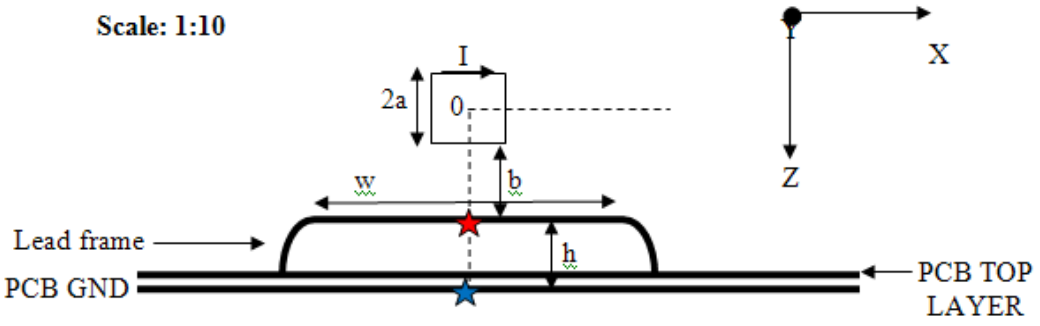

Figure 6.7. Orientation of the magnetic field loop probe above the lead frame (1 mm)

The figure above shows the orientation of the loop above the lead frame of the IC. The figure has been drawn to a scale of 1:10. The parameters are explained below,

2a = Loop size (**1 mm**)

b = Height of lower part of the loop probe from the lead frame of the IC

= Extension of the dielectric of the PCB probe below the loop (**0.6 mm**)

+ Distance between package on top of the IC to the lead frame (**0.4 mm**)

= **1 mm**

h = Height of lead frame from GND plane of PCB

= Distance from the lead frame to the TOP layer of the PCB (**0.8 mm**)

+ Distance from the TOP layer of the PCB to the GND layer (**0.16 mm**)

= 0.96 mm

w = Length of the trace on the lead frame of the IC (**5 mm**)

The 'Y' component of the magnetic field strength is calculated at a point (**blue star, B(0,0,a+b+h))** on the GND plane using the concept of image theory and Equation (2), since at this point X & Z components of the fields are zero. Then the field is computed at the height of the lead frame (**red star, A(0,0,a+b)**). Estimation of the field strength takes into consideration the following assumptions,

1) There is no current flowing on the lead frame of the IC which would also contribute to the field strength. As a consequence of the assumptions one underestimates the field strength at the ground plane and at the lead frame.

Figure 6.8 shows the magnetic field strength at the lead frame of the IC for two different loop sizes. With increase in loop size the failure level of the IC goes down since the magnitude of field coupled to the lead frame or the bond wires increases. This fact is illustrated in Figure 6.9. The field strength is calculated right below the loop at the location of the red star, **A (0, 0, a+b)**. However increase in field strength is not linear with loop size.

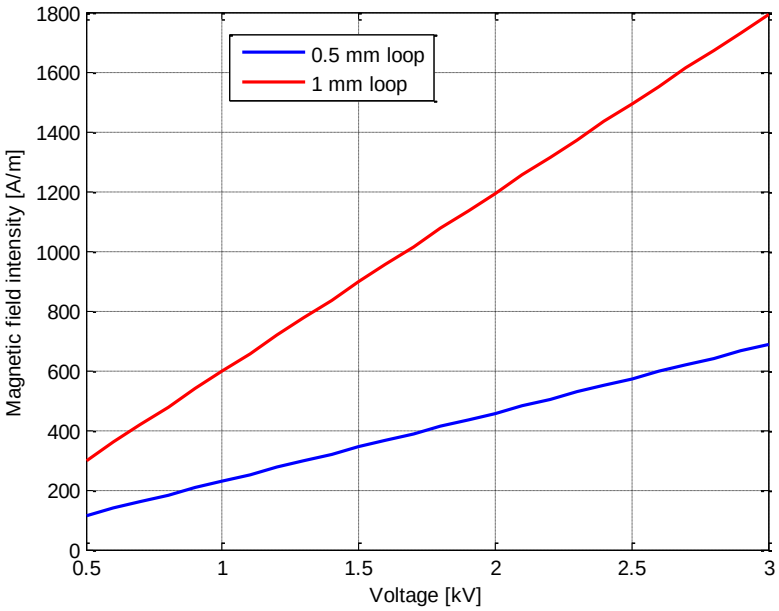

Figure 6.8. H field strength vs TLP charge voltage at a height of the lead frame

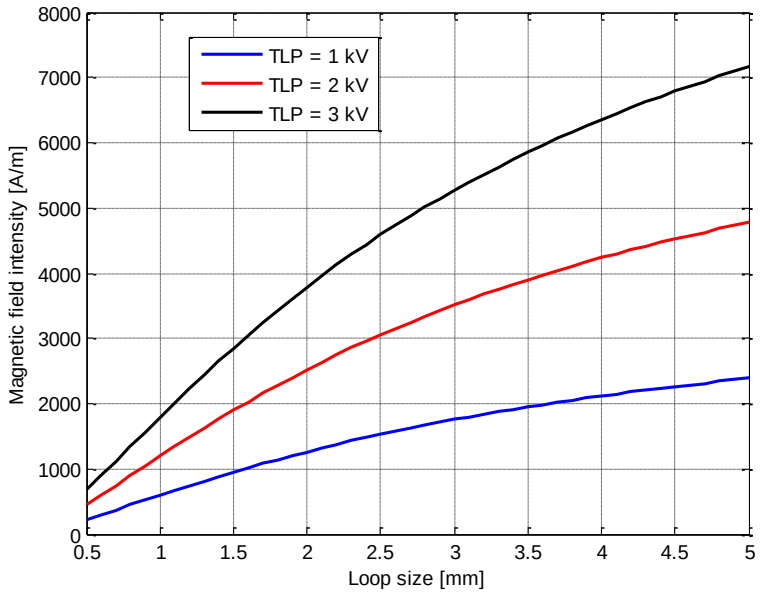

Figure 6.9. Variation of field strength vs loop size for different TLP voltages

6.3 ANALYTICAL ESTIMATION OF INDUCED NOISE VOLTAGE

According to Faraday's law of induction the peak value of the induced voltage is given by,

$$V_{induce} = -\frac{\mu}{dt}\int_{0}^{h}\int_{-L_t}^{L_t} H_y \cdot dz \cdot dx$$

Where,

It is assumed that the lead frame is in X direction and the magnetic field is in Y direction.

B = Magnetic flux density = μH

dx = Length of the trace on the lead frame = $2L_t$

dz = Height of the lead frame above the GND plane

dt = Rise time of TLP pulse = 0.7 ns

In calculation of the induced voltage [23], the following assumptions have been made at this stage,

1) From previous study it has been shown that, when the trace length is larger than twice the probe width, the induced voltage converges to a final value [23]. This is a consequence of decrease in field strength away from the field probe as the trace length increases. Therefore, the parts of the trace that are in a region of weak field do not contribute to the induced voltage. Taking this assumption into consideration the cross sectional area over which the integration operation is performed to obtain the induced loop voltage would be different for three different loop sizes. The following figures show schematic for computation of the induced voltage for three different loop sizes.

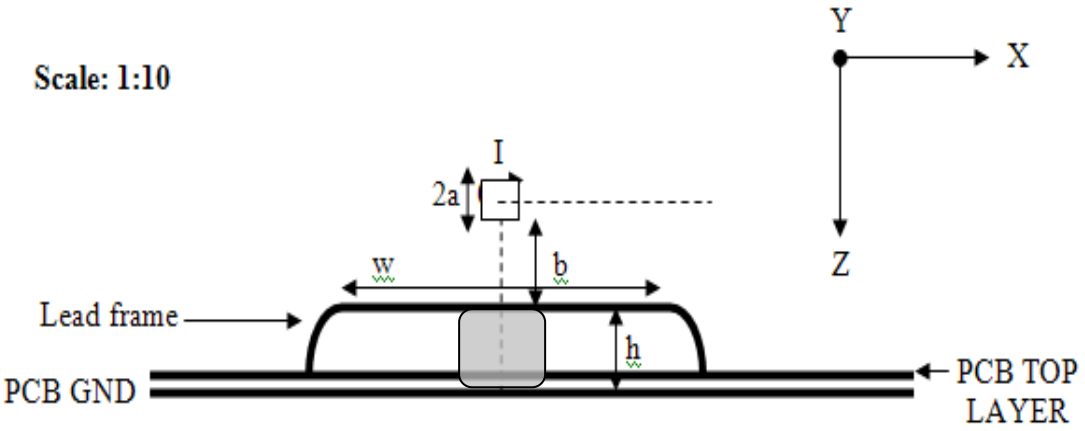

Figure 6.10. Computation of induced voltage on the lead frame for 0.5 mm loop

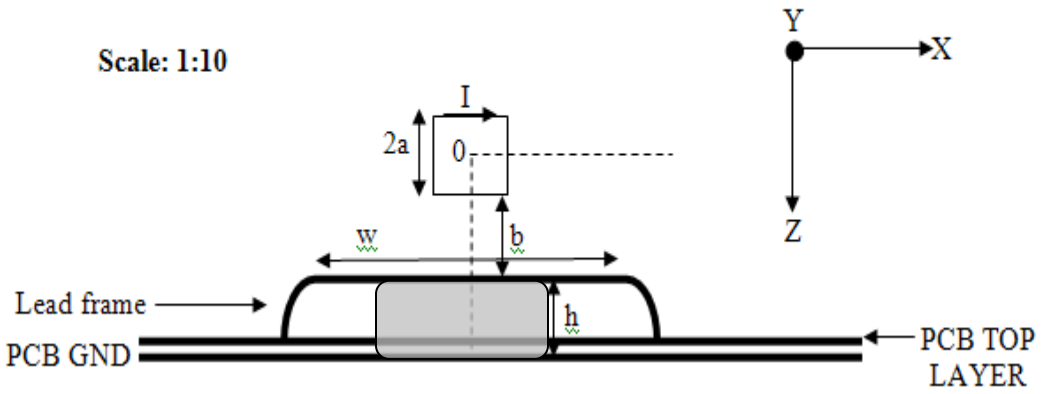

Figure 6.11. Computation of induced voltage on the lead frame for 1 mm loop

Figure 6.12 shows the induced noise voltage estimation for the 5 mm H field loop probe. Again only the shaded region enclosing the loop of the lead frame is used to calculate the induced voltage.

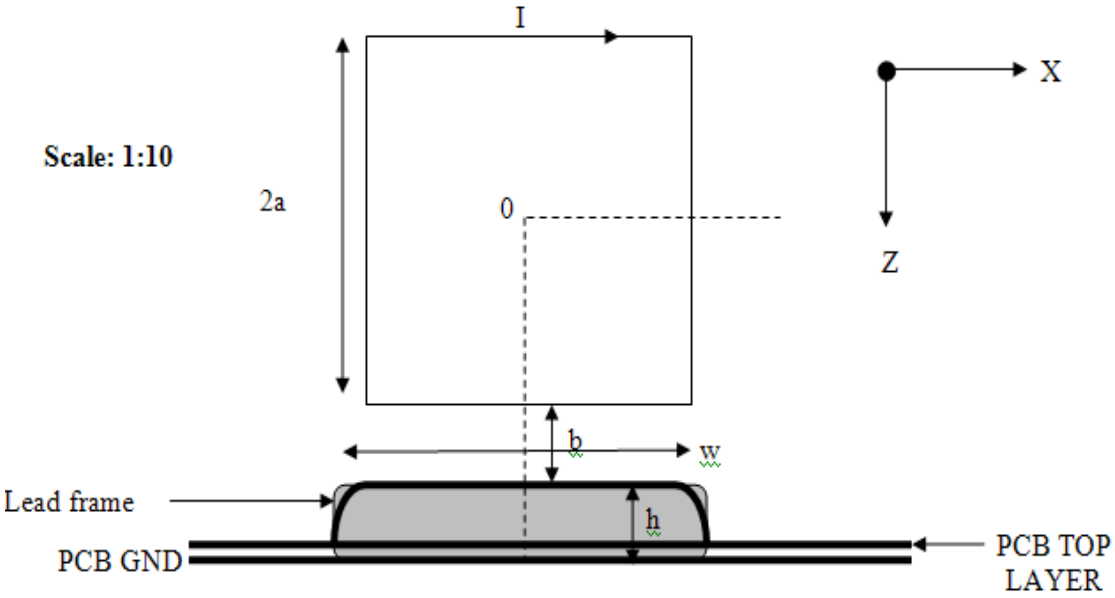

Figure 6.12. Computation of induced voltage on the lead frame for 5 mm loop

The parameters for computation of the induced voltage are explained below,

2a = Loop size (**0.5/1/5 mm**)

b = Height of lower part of the loop probe from the lead frame of the IC

= Extension of the dielectric of the PCB probe below the loop (**0.6 mm**)

+ Distance between the package on top of the IC to the lead frame (**0.4 mm**)

= **1 mm**

h = Height of lead frame from GND plane of PCB

= Distance from the lead frame to the TOP layer of the PCB (**0.8 mm**)

+ Distance from the TOP layer of the PCB to the GND layer (**0.16 mm**)

= 0.96 mm

w = Length of the trace on the lead frame of the IC. = $2L_t$ = (**5 mm**)

The integration operation in the analytical equation is performed by computing the magnetic field in discrete steps along the line X=0 between the points A (0, 0, a + b) and B (0, 0, a + b +h). The shaded region in the figure is the area through which the magnetic flux wraps around the trace thereby causing an induced voltage on the lead frame. This shaded region is divided into discrete strips of cross sectional areas along the 'Z' direction by the number of components of the field calculated as above. Then Faraday's equation is employed by multiplying the magnetic field strength with discrete areas and added all together to obtain the total induced voltage.

2) At present the time step (dt) used to compute the induced voltage has been assumed to be equal to the rise time of the TLP pulse. However this is not exactly correct since the TLP pulse rises very fast initially and then slows down. So the time derivative of the current would also be a continuously changing component rather than a constant value.
3) In the computation of induced voltages, adjacent traces of the lead frame have been ignored. Full wave simulation of the whole structure would show the effect of adjacent traces on field strength and induced noise voltages.

Taking the 1 mm loop probe as an example, Figure 6.13 shows the variation of induced voltage on the lead frame of the IC with respect to the TLP voltage. The induced voltage at the lead frame at 0.5 kV TLP voltage is comparatively low (600 mV) and hence does not cause a failure of the IC.

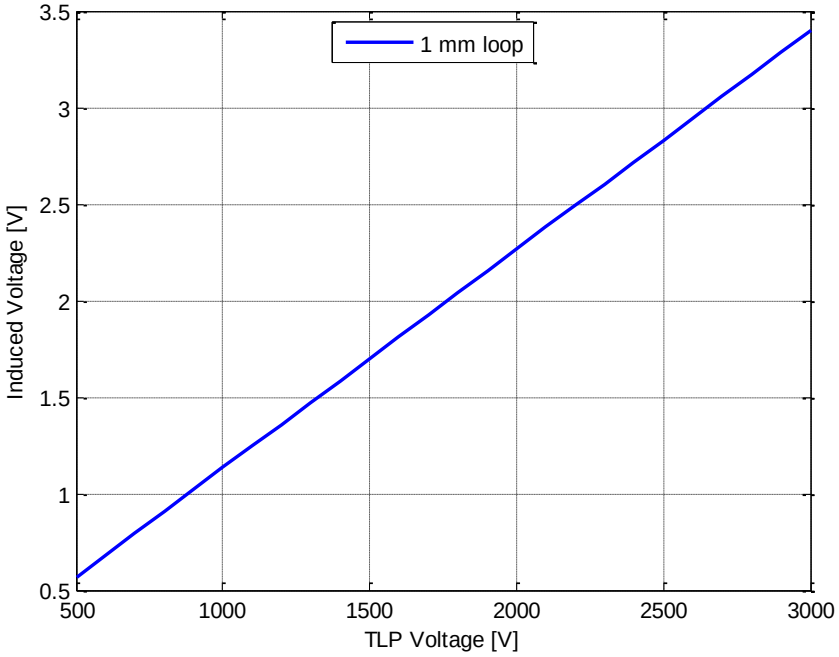

Figure 6.13. Induced voltage vs TLP voltage for 1 mm loop size

As the TLP voltage increases to say 1.5 kV TLP voltage one would expect the IC to fail since the induced noise voltage is around 1.7 V which is large enough to cause a failure.

6.4 MAGNETIC FIELD INJECTION

The following section gives the experimental results obtained from H-field injection onto the memory IC.

6.4.1. H-field test (5 mm loop). The manual scan was performed for both the polarization of the probes. The two orientations of the probes are shown in Figure 6.14.

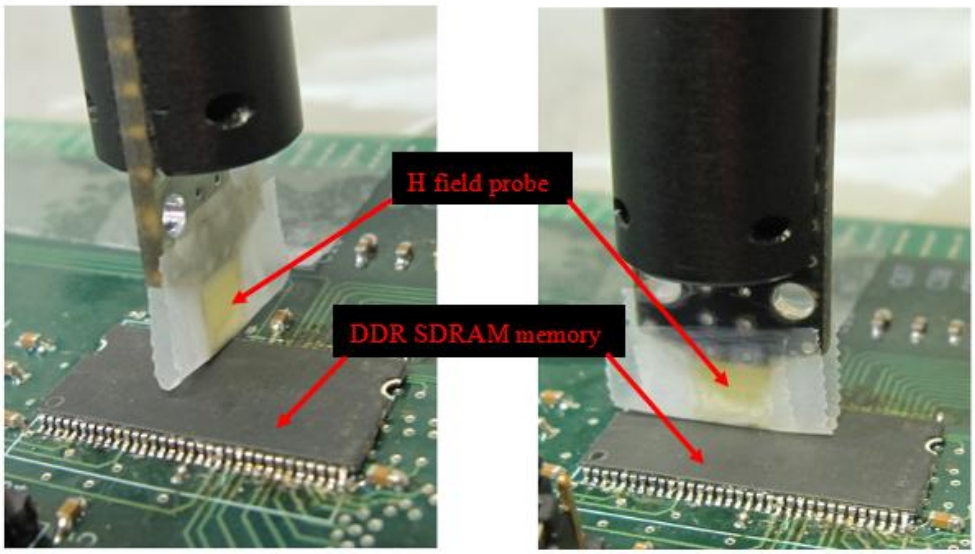

Figure 6.14. Manual scanning of DDR memory with H field probe in dual polarization

Table 6.1. Manual scanning results for 5 mm H field loop probe

TEST VOLTAGE (kV)	ESTIMATED FIELD STRENGTH (kA/m)	ESTIMATED INDUCED VOLATGE (V)	DUT STATUS	REMARK
0.5	1.2	7.35	LED 1 glows (error)	DQS, DM & nWE pins are the only sensitive pins.
1	2.4	14.7	LED 1 glows (error)	Disturbance on DQ pins (DQ2 & DQ3) and some address pins (A4 - A12) causes errors.
2-3	4.8-7.17	29.5-44	LED 1 glows (error)	The memory fails almost on all locations where the probe is held.

The results were a combination of scanning in both the polarizations. It is assumed that the IC's fastest response time is faster than the rise time of the TLP pulse. Hence only the peak magnitude of the induced voltages is considered. The DQS/DQ pins are more sensitive to excitation by H field at lower voltages followed by other control pins such as nWE/nCAS/nRAS followed by the address pins ($A_0 - A_{12}$).

6.4.2. H-field test (1 mm loop). Table 6.2 shows the manual scan results for the particular probe.

Table 6.2. Manual scanning results for 1 mm H field loop probe

TEST VOLTAGE (kV)	ESTIMATED FIELD STRENGTH (kA/m)	ESTIMATED INDUCED VOLATGE (V)	DUT STATUS	REMARK
1	600	1.14	LED 1 does not glow (NO error)	
1.5	900	1.7	LED 1 glows (error)	Disturbance on DQ pins DQS, DM & nWE pins causes errors.
2	1200	2.26	LED 1 glows (error)	Disturbance on some of the address pins causes failure.
3	1800	3.4	LED 1 glows (error)	The memory fails in almost all locations where the probe is held.

It is understandable that with decrease in loop size the failure level of the IC goes up since the noise voltage induced on the lead frame decreases in magnitude. The address pins of the IC more robust and can withstand higher field excitations.

6.4.3. H-field test (0.5 mm loop). Table 6.3 shows the manual scan results for the particular probe.

Table 6.3. Manual scanning results for 0.5 mm H field loop probe

TEST VOLTAGE (kV)	ESTIMATED FIELD STRENGTH (kA/m)	ESTIMATED INDUCED VOLATGE (V)	DUT STATUS	REMARK
2	450	0.4	LED 1 does not glow (NO error)	
3	700	0.6	LED 1 glows (error)	Disturbance on DQ pins DQS, DM & nWE pins causes errors.

The estimated voltage induced on the lead frame of the IC with this particular H field probe is too small (in the range of several hundred mV) at lower TLP voltages to cause any failure of the IC. However there are some failures at 3 kV TLP charge voltage**.** To get a more accurate estimation of the field and the induced loop voltages one would need a full wave simulation of the lead frame of the IC with the probe model. The analytical method can only give an approximate value of the field strengths and voltage levels. As expected, for the smallest loop size the minimum failure level of the IC goes up further to 3 kV.

6.5 MEASUREMENT OF INDUCED NOISE VOLTAGE

While performing manual field scanning with the H-field probes the induced noise voltage on the DQ3 pin of the memory IC is measured. The purpose of this measurement is to correlate the measured and simulated induced noise voltage waveform. The detailed description of the full wave simulation and the comparison of results are shown later in the report. Figure 6.15 shows the induced noise voltage riding on the signal waveform of the DQ3 pin when excited by the 1 mm H field loop probe at a TLP charge voltage of 3 kV.

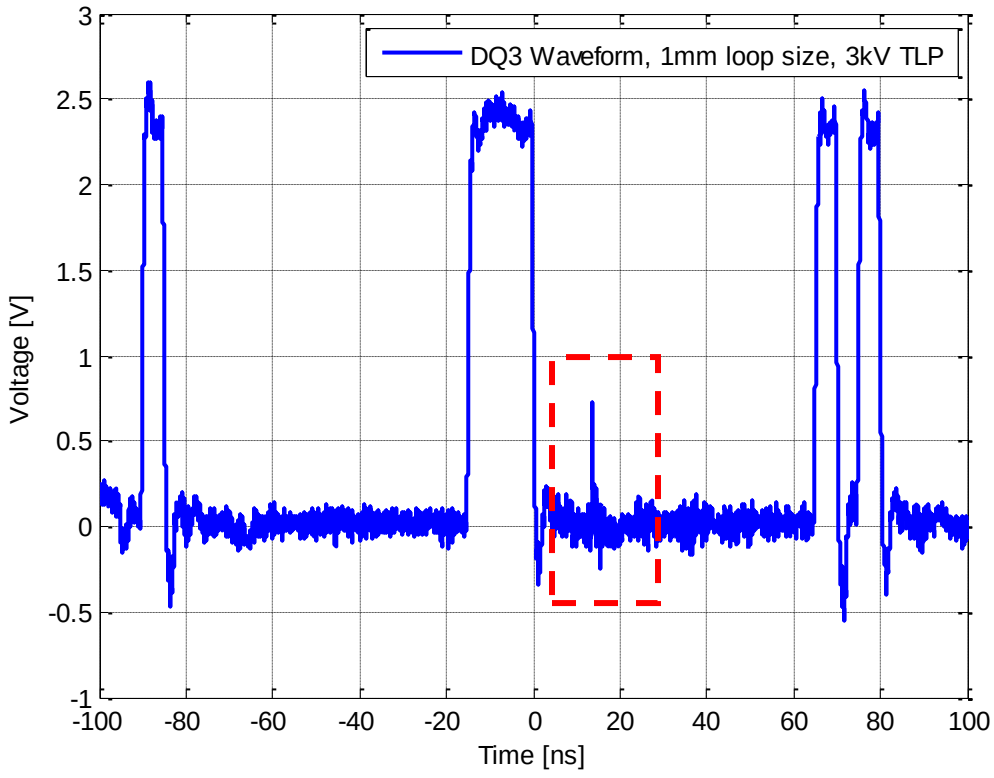

Figure 6.15. Noise Voltage waveform on DQ3 pin for positive TLP pulse (3 kV)

The figure above shows the measured voltage waveform on the DQ3 pin at 3 kV TLP charge voltage (with 1 mm H- field loop probe). The region highlighted by the red box shows the fast rising pulse caused due to the excitation by the loop probe. Peak magnitude of the disturbance pulse is around 0.8-1 V (0.7 V). The peak magnitude of the noise signal is greater than the threshold level of the IC leading to a bit error. Figure 6.16 shows the induced noise voltage riding on the DQ3 pin of the memory IC when excited by the 5 mm H field loop probe at a TLP charge voltage of 1 kV.

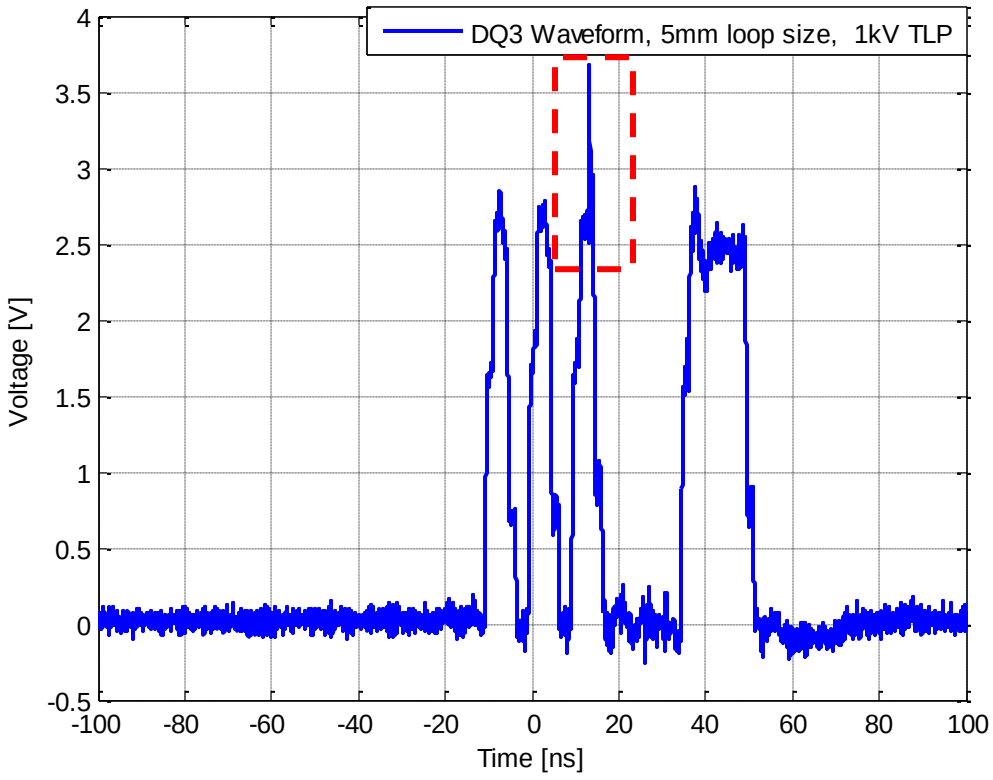

Figure 6.16. Noise Voltage waveform on DQ3 pin for positive TLP pulse (1 kV)

The region highlighted by the red box shows the fast rising pulse caused due to the excitation by the loop probe. The error is in probably caused due to latch up of the IC. Peak magnitude of the disturbance pulse is around 0.8-1.2 V (1.1 V).

6.6 SIMULATION OF INDUCED NOISE VOLTAGE

Full wave simulation of the DDR SDRAM memory model has been performed in frequency domain to determine the induced noise voltages in response to field excitation. The excitation source is an H field loop probe (1 mm) fed by a TLP pulse of varying magnitude 1 kV. Some minor modifications are made to the original model to simulate the induced noise voltages. Figure 6.17 shows the simulation model.

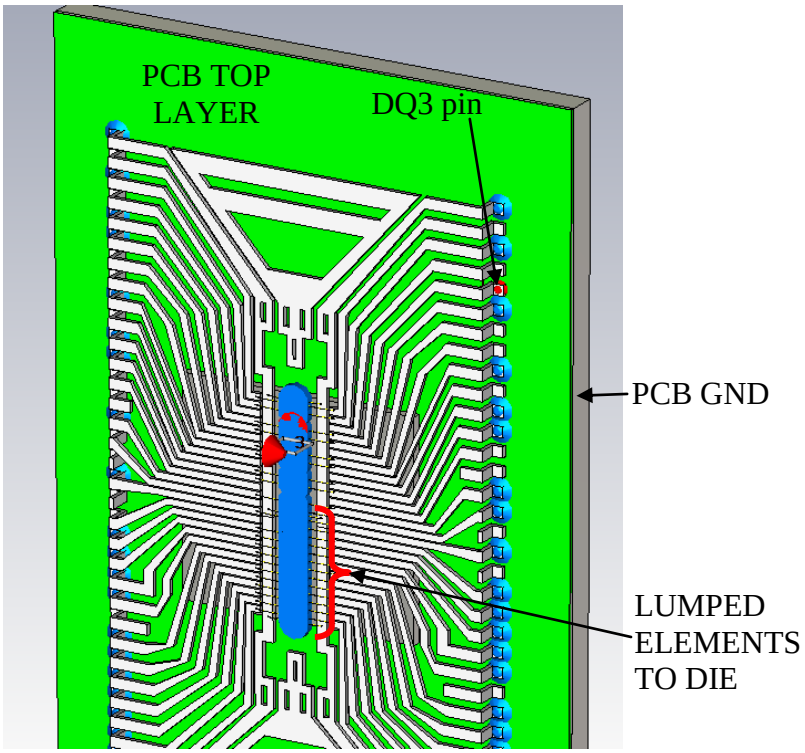

Figure 6.17. Complete 3D model of the memory IC

All the lumped elements are included in the full wave model of the memory IC. The only change that has been made is for the DQ1 & DQ3 pin shown in Figure 6.18. Instead of adding lumped elements derived from the IBIS model for the DQ pin, two S parameter ports have been defined. PORT 1 connects the lead trace of DQ3 to PCB GND whereas PORT 2 connects the bond wire of DQ3 to the die. Similarly PORT 5 connects the lead trace of DQ1 to PCB GND whereas PORT 4 connects the bond wire of DQ1 to the die. Figure 6.18 shows the magnified view of the ports and bond wire for DQ3 and DQ1 pin of the memory IC respectively.

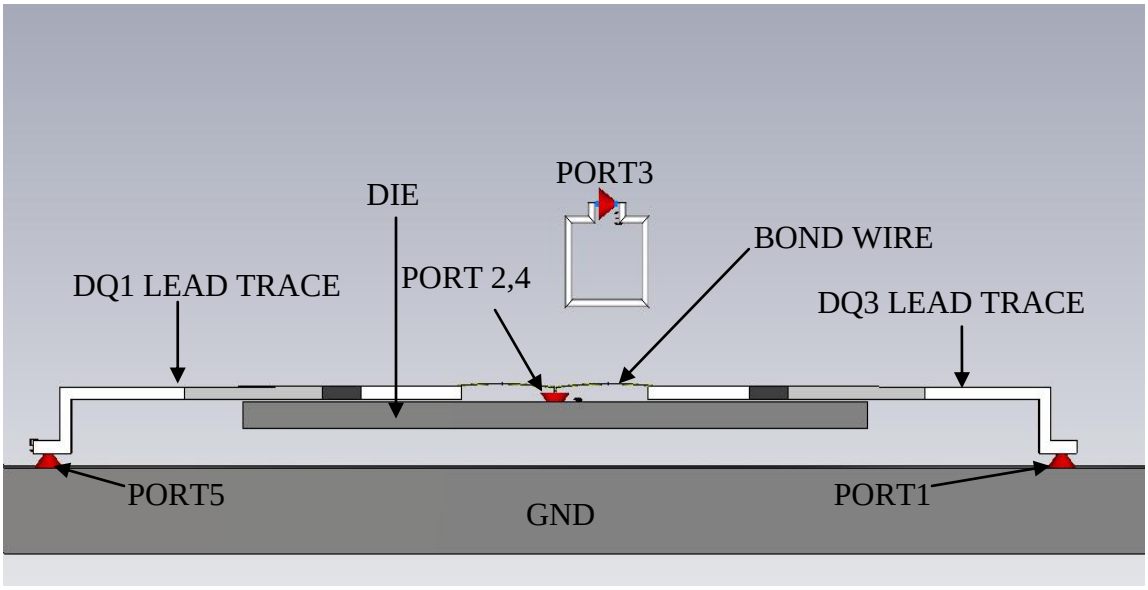

Figure 6.18. Definition of ports and loop probe

PORT 1 is connected to GND plane whereas PORT 2 and PORT 4 are connected to the die. The H field loop probe has been modeled as a square loop of dimension 1mm

x 1mm. The material chosen for the loop is PEC and the radius of the wire has been chosen to be 0.05 mm. PORT 3 is the excitation port at the loop and has been defined as an S parameter port with 50 Ω reference impedance. PORT 1, PORT 2, PORT 4 and PORT 5 are also defined as S parameter ports with 50 Ω reference impedance. PORT 4 and PORT 5 have been included in the model to determine the induced cross talk noise voltage on the adjacent pin of the memory IC when subjected to H field excitation. All the other geometries of the lead frame with the package, bond wires and top later of the PCB along with the other lumped elements connecting to the die has been included in the model. The frequency range of simulation is from 0 to 6 GHz.

The equivalent circuit in CST DS is shown in Figure 6.19. The simulation is performed when the DQ pin is acting as an Output pin in low state. The figure shows the combined full wave model of the memory IC with the IBIS model of the DQ3 & DQ1 pin and the input pins of the FPGA. The excitation source is defined as the TLP pulse with a 50 Ω source resistance. The transmission lines connecting the DQ1 & DQ3 pin of the memory IC to the respective pins of the FPGA have also been included in the simulation model. They are modeled as microstrip lines as in the actual geometry and their impedance is 50 Ω. The voltage waveform simulated at Probe 1 is the induced noise voltage at the DQ3 pin (with reference to PCB GND) whereas the voltage simulated at Probe 5 is the induced coupled noise voltage (Cross talk) on the DQ1 pin (with reference to PCB GND) of the memory IC. Different magnitudes of TLP pulses are applied to the excitation source to determine the relative magnitude of the induced noise voltages at the DQ pin.

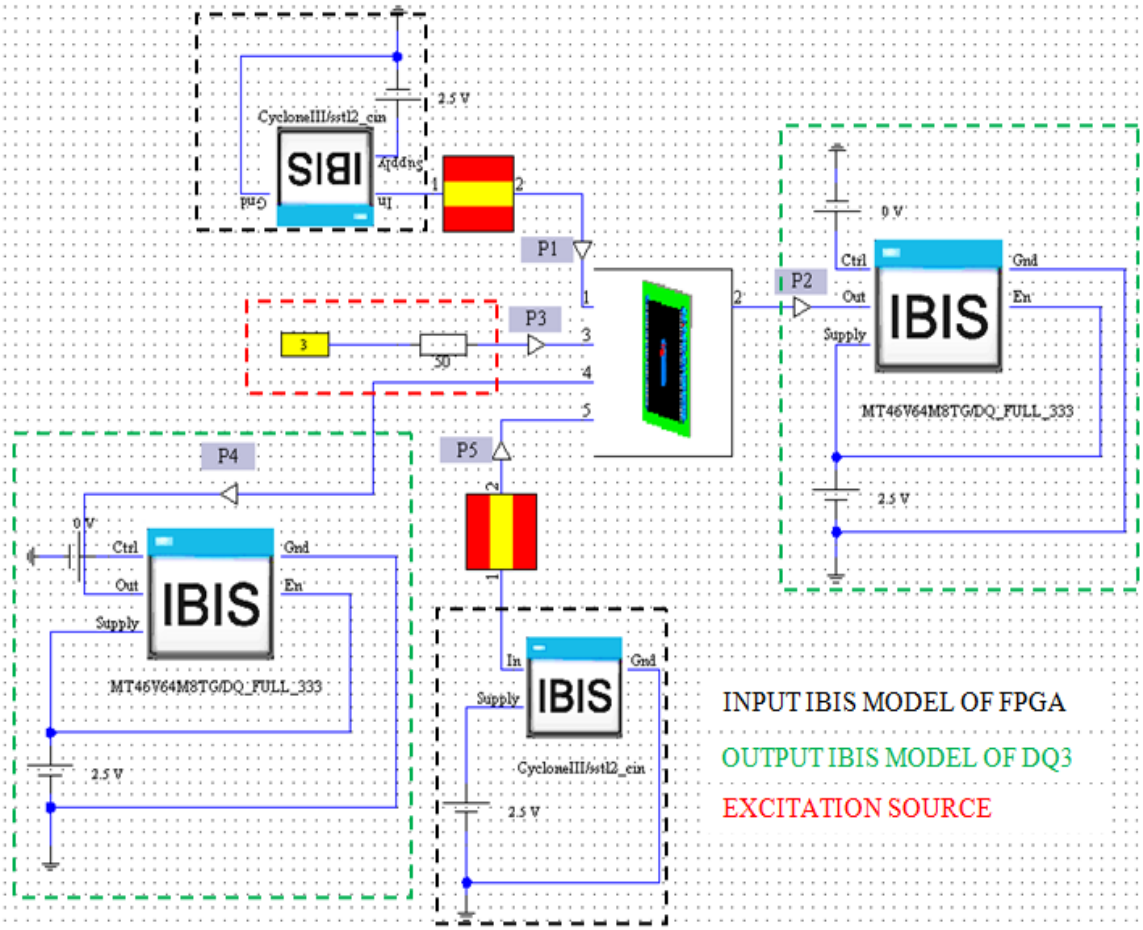

Figure 6.19. Equivalent circuit in CST DS

A comparison of the induced noise voltage at Probe 1 (DQ3 pin) for two different TLP voltages is shown in Figure 6.20. The figure shows the comparison of the induced noise voltage at the DQ3 (with reference to PCB GND) pin of the memory at two different TLP voltage levels. At 1 kV TLP charge voltage the peak magnitude of the induced voltage is ~ 0.28 V which is not large enough to cross the threshold level and cause failure in operation of the IC. This fact is also supported from observation results while performing manual field scanning of the IC.

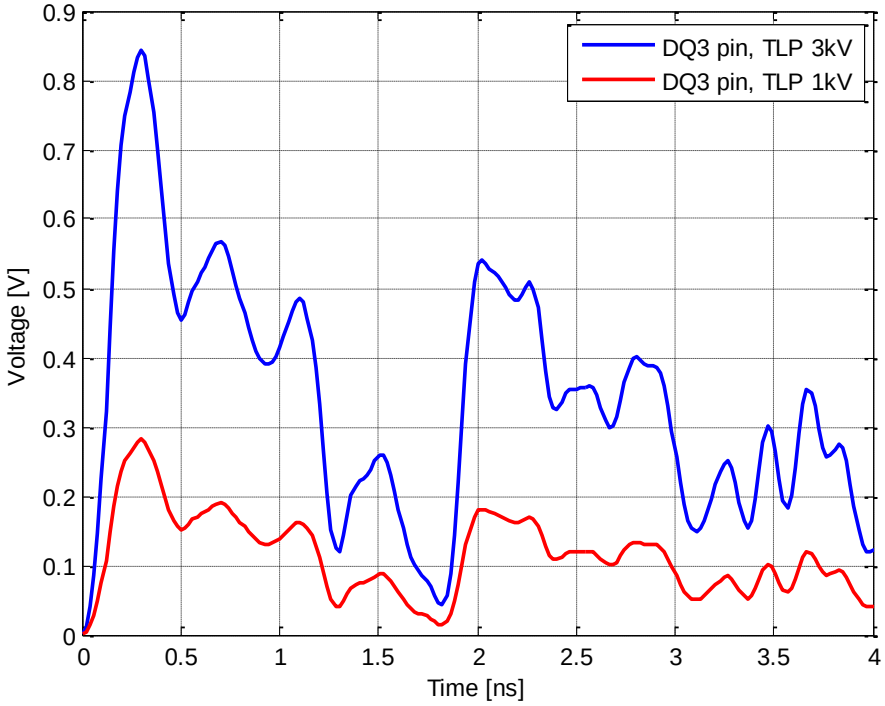

Figure 6.20. Induced noise voltage at Probe 1 (DQ3 pin) of the memory IC

At 3 kV TLP voltage the peak magnitude of the induced noise voltage is ~ 0.85 V, which is large enough to cause misinterpretation of a data bit by the FPGA leading to a bit error. A comparison of the induced noise voltage at Probe 5 (DQ1 pin) for two different TLP voltages is shown in Figure 6.21. The peak value of the induced voltage on DQ1 pin at 3 kV is ~ 0.48 V. It could be possible that the coupled voltage to the DQ1 pin is large enough to cause an error by itself. At 1 kV (~ 0.15 V) the peak magnitude of the voltage waveform is not large enough to cause any error.

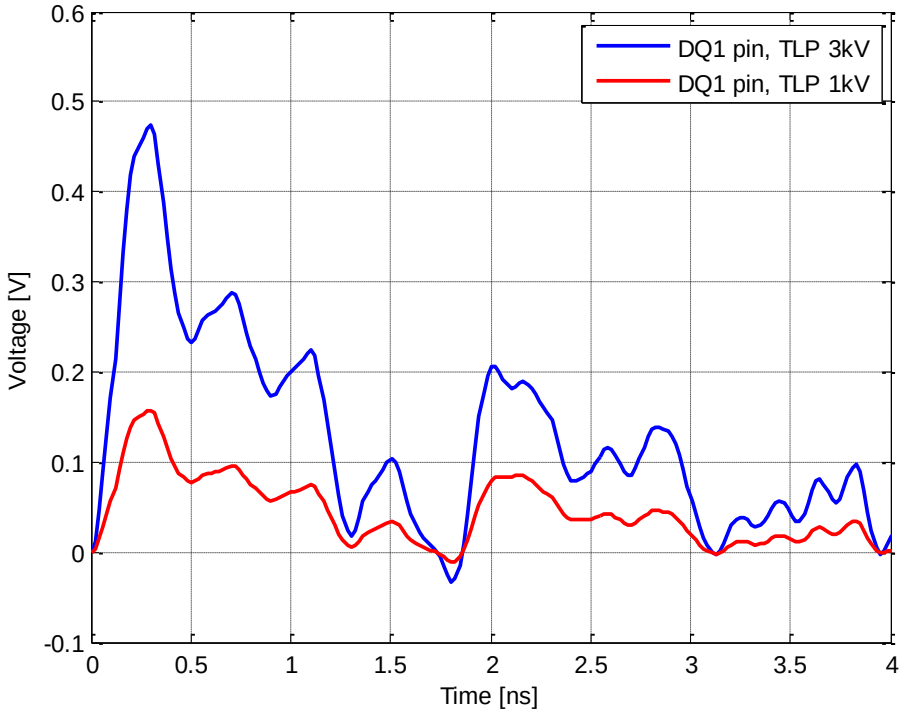

Figure 6.21. Induced noise voltage at Probe 5 (DQ1 pin) of the memory IC

An identical simulation was performed with a 5 mm H-field loop probe. A comparison of the induced noise voltage at 1kV TLP voltage for two different loop sizes at Probe 1 (DQ3 pin) of the memory IC is shown in Figure 6.22. From the figure we see that the peak magnitude of the induced noise voltage at the DQ3 pin of the memory IC is much larger in magnitude for the 5 mm loop at a TLP charge voltage of 1 kV (< 1 V). This also explains the fact as to why the memory IC shows no failure when excited by the 1 mm loop probe whereas it shows failure when excited by the 5 mm loop probe at the same TLP voltage.

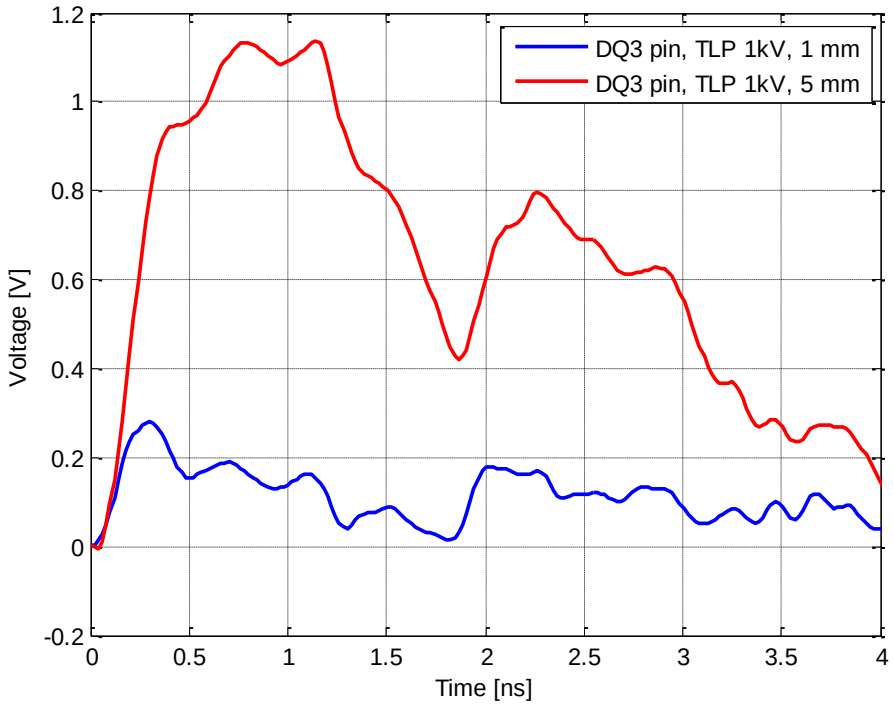

Figure 6.22. Comparison of induced voltage at Probe 1 (DQ3 pin) for two loop sizes

6.7 COMPARISON OF RESULTS

This section shows the comparison of measured induced noise signal on the DQ3 signal and simulated result. Figure 6.23 and Figure 6.24 shows the comparison of measured and simulated induced noise signal on the DQ3 pin when excited by the 1 mm H field loop probe at a TLP charge voltage of 3 kV. At the time of measurement the H field loop probe was held on top of the test pin of the memory IC while con currently measuring the induced noise signal via a coaxial probe on the oscilloscope.

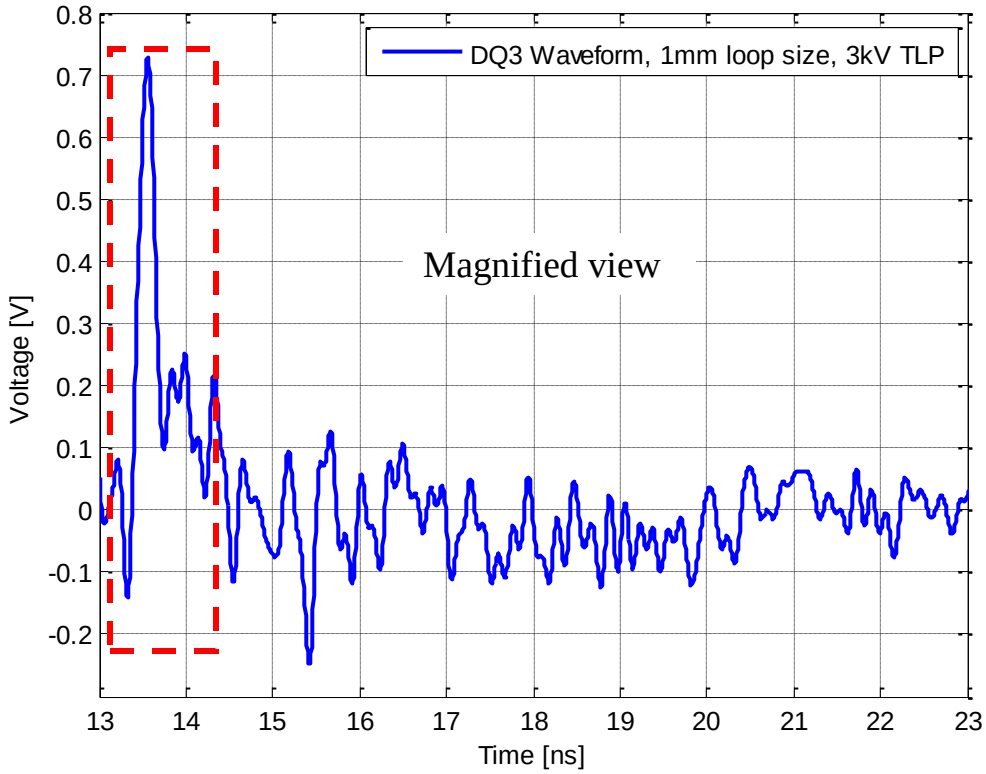

Figure 6.23. Noise voltage waveform on DQ3 pin for positive TLP pulse (3 kV)

The figure above shows a magnified view of the measured noise voltage waveform on the DQ3 pin at 3 kV TLP charge voltage (with 1 mm H- field loop probe). The region highlighted by the red box shows the fast rising pulse caused due to the excitation by the loop probe. Peak magnitude of the disturbance pulse is around 0.8-1 V (0.7 V). The peak magnitude of the pulse is greater than the threshold level of the IC leading to a bit error. Figure 6.24 shows the simulated induced noise signal on the DQ3 pin of the IC with reference to PCB GND.

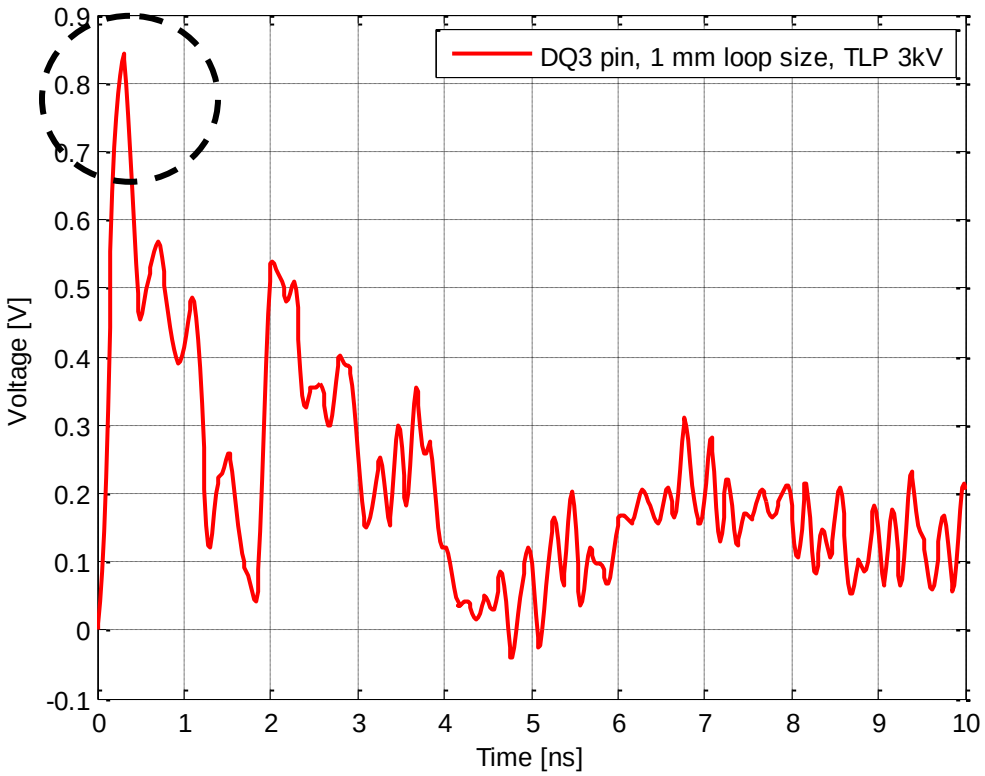

Figure 6.24. Simulated noise signal on the DQ3 pin with 1 mm loop probe

The figure above shows the simulated noise signal on the DQ3 pin of the IC. On comparing Figure 6.23 and Figure 6.24, the peak value of the measured and simulated noise voltage waveform show good correlation with each other.

Figure 6.25 and Figure 6.26 shows the comparison of measured and simulated induced noise signal on the DQ3 pin when excited by the 5 mm H field loop probe at a TLP charge voltage of 3 kV.

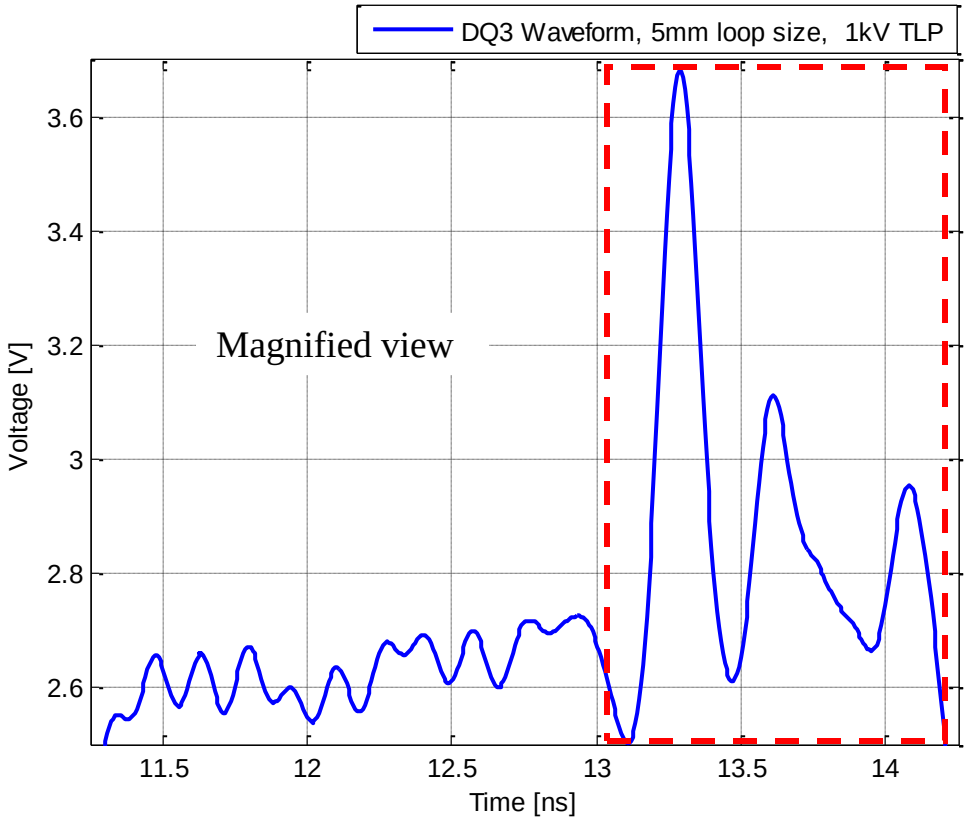

Figure 6.25. Noise voltage waveform on DQ3 pin for positive TLP pulse (1 kV)

The figure above shows the magnified view of measured induced noise signal on the DQ3 pin of the IC when disturbed using the 5 mm H field loop probe. The region enclosed in the red box is the noise pulse riding on the bit stream when it is in the high state (2.5 V). The peak magnitude of the noise pulse is ~ 1.1 V. Figure 6.26 shows the simulated noise signal on the DQ3 pin. The peak value of the simulated noise signal is also approximately 1.1 V which correlates quite well with the measured data.

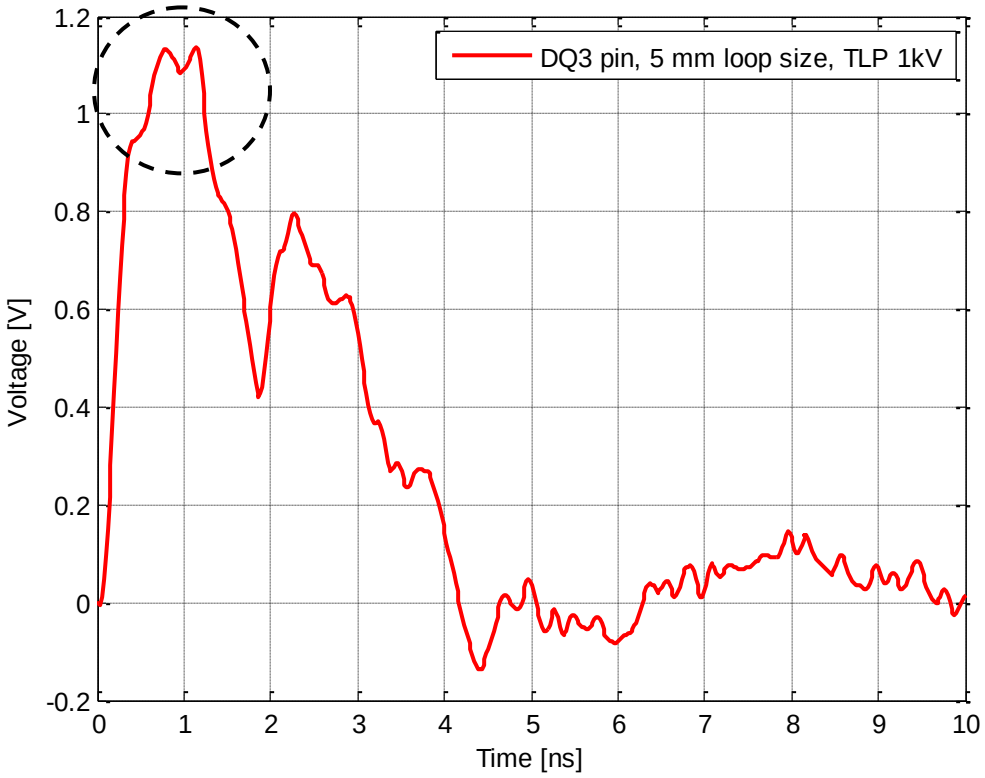

Figure 6.26. Simulated noise signal on the DQ3 pin with 5 mm loop probe

The good correlation of results suggests that the simulation strategy works in predicting the induced noise signal.

6.8 CONCLUSION

The preliminary objective of the initial manual scanning testing was to acquire knowledge as to what degree the DDR memory could with stand E/H field excitation without having errors. A common trend noticed during the testing was that the data and control pins of the memory IC were more sensitive to excitation. The address pins of the IC were more robust and could withstand higher field excitations. Based upon

measurements and simulation of induced voltages on the lead frame of the IC, one could say that noise voltages in the range of 0.1~0.2 V would definitely not cause a soft error. However noise signal between 0.6 to 0.8 V would in all probability cause an error. Magnetic field strengths of the order of 400A/m have been shown to cause failure of the memory IC. The failure mechanism of the IC has not been determined as of now. However one could make a fairly good assumption that an error occurs due to either improper recognition of a bit leading to a bit error.

Good correlation between the measured and simulated results suggests that the methodology of combining full wave simulation with co-simulation in CST DS works quite well in predicting the induced noise signal. The simulation model does not tell us exactly which pin of the memory IC gets disturbed leading to an error but it does give us a statistic of the noise signals on other pins of the IC, to get an idea of the likelihood of a failure due disturbance on a particular pin.

7. FIELD INJECTION VIA TEM CELL

7.1 INTRODUCTION

Field injection is also performed by a specially designed TEM cell with reduced septum height. The height of the septum from the top wall is 1 cm. Fast rising transient pulses were applied to the TEM cell and the crash level of the memory IC was documented. The objective is to characterize the immunity of the test IC and show the correlation between measured and simulated results.

7.2 MEASUREMENT SETUP

Figure 7.1 shows the measurement setup for field injection via the TEM cell.

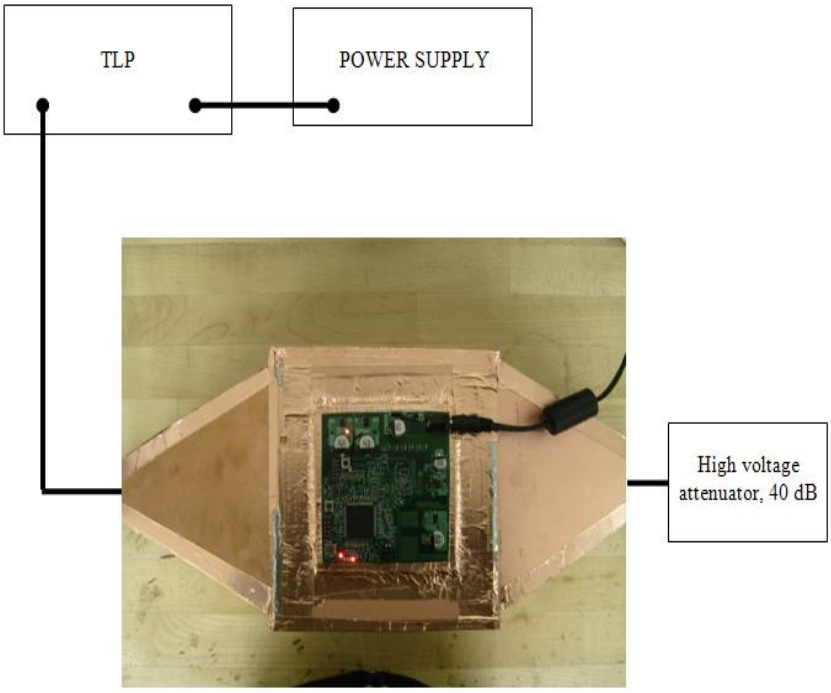

Figure 7.1. Measurement setup for field injection via TEM cell

The specially designed TEM cell has a reduced septum height from the top wall of the TEM cell. This enables excitation with higher field strengths to cause failure of the DUT. The TEM cell board with the memory IC is mounted on the TEM cell in two orientations. The injected waveform into the TEM cell is a TLP pulse of varying magnitude. The crash level of the memory is recorded on injection of the pulse to the TEM cell. The memory IC failed repeatedly at 2.0 kV. For negative polarity the IC failed repeat -1.7 kV. At 90 degree orientation the IC showed failure levels at 2.25 kV and -2.1 kV respectively.

7.3 MEASUREMENT RESULT

Figure 7.2 shows the measured induced noise voltage waveform on the CKE pin of the memory IC. The induced noise voltage was measured at the CKE (Clock Enable) pin of the memory IC. It is an active high signal at 2.5 V. The noise signal is measured on an oscilloscope with a sampling rate of 10 Gs/sec. It is always better to record data on the oscilloscope with a sampling rate of 20 Gs/sec or even higher if available. The high frequency components of the data waveform are not visible if the sampling rate is low. The peak value of the induced voltage is 1 V. During the TEM cell measurement it is difficult to determine which pin of the IC is getting affected leading to soft errors. Hence this pin of the IC was selected to get an idea of the induced voltage levels at one of the pins. A full wave model of the TEM cell along with the lead frame of the IC would give a better idea of the induced noise and the affected pins of the memory IC.

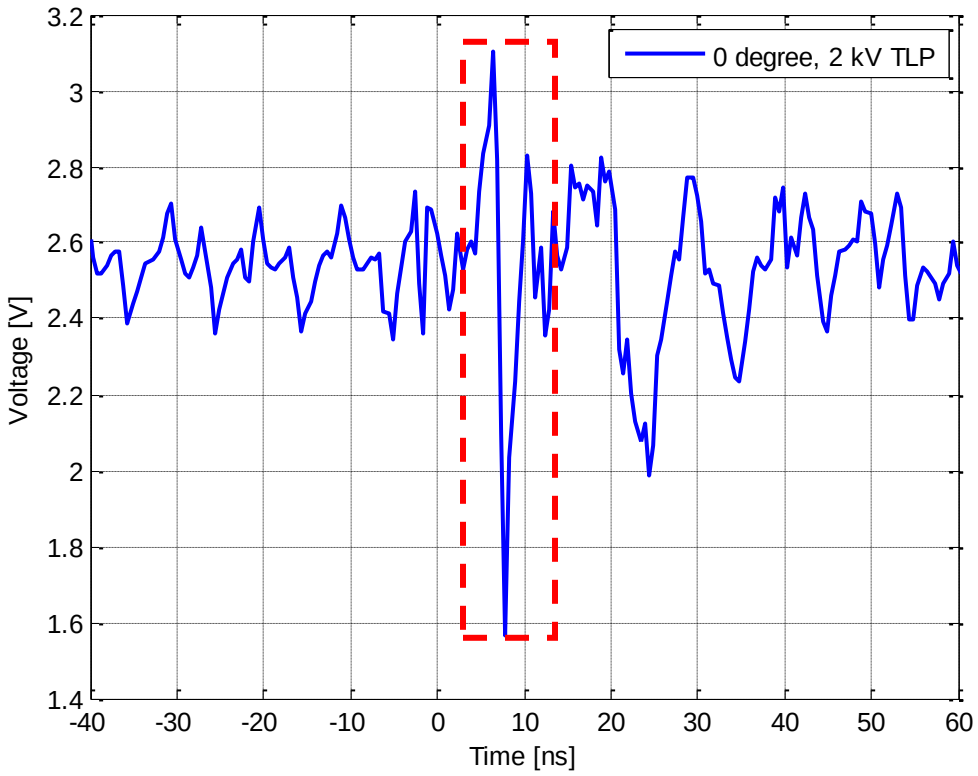

Figure 7.2. Measured voltage waveform on CKE pin

7.4 SIMULATION OF INDUCED NOISE VOLTAGE

Figure 7.3 shows the full wave simulation model of the lead frame of the IC with the PCB board and the septum region of the TEM cell. The four sides of the septum are bounded by PEC walls. The PCB geometry also includes the lead frame structure of the memory IC along with the associated lumped elements. A time domain simulation is performed for the first 10 ns to determine the noise signal voltage at the CKE pin of the memory IC. Figure 7.4 shows the simulated induced noise voltage waveform on the CKE pin of the memory IC.

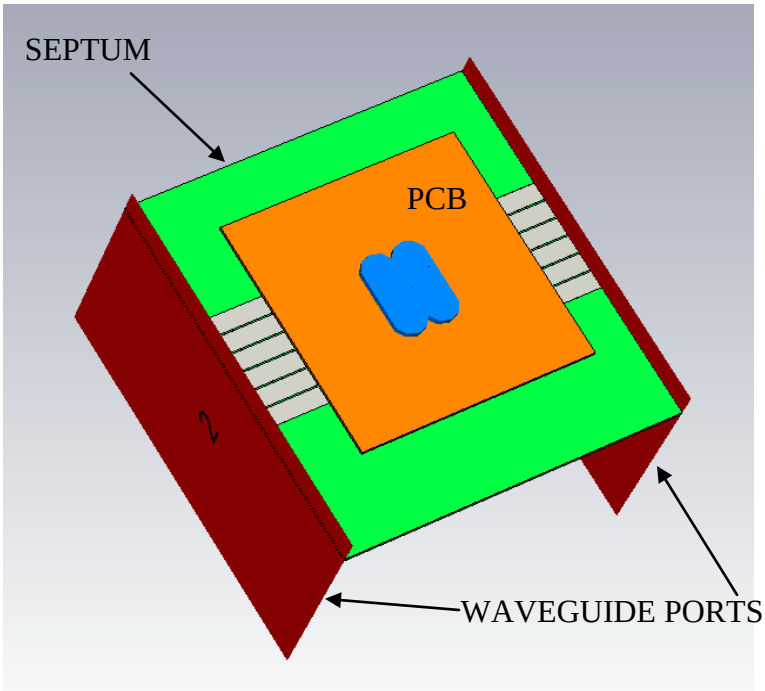

Figure 7.3. Full-wave simulation model of TEM cell + IC

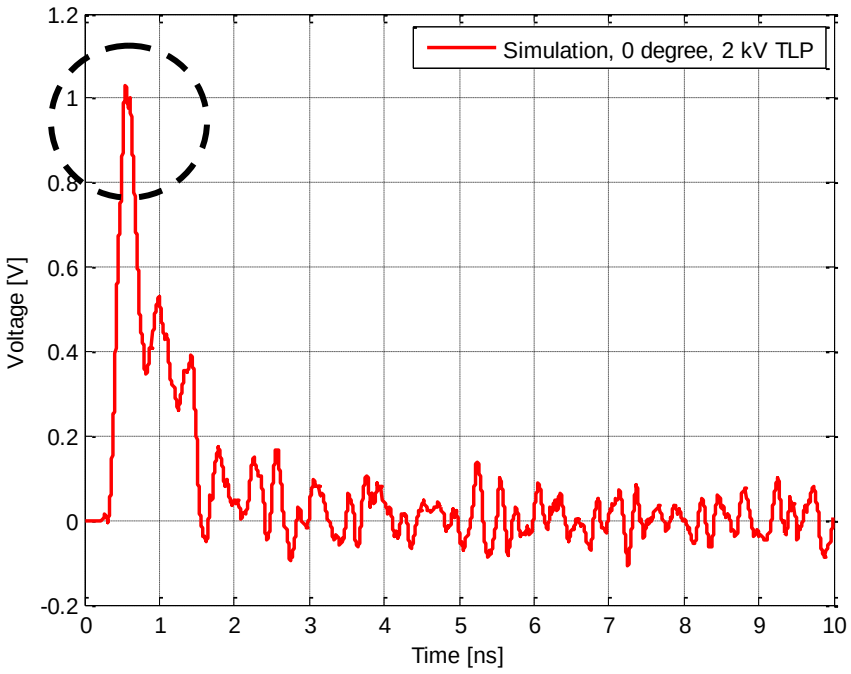

Figure 7.4. Simulated induced noise voltage signal on CKE pin

Comparing Figure 7.2 and Figure 7.4 we see that the peak value of the simulated induced noise signal is ~1 V which matches quite well with measurement results. While performing the measurement it is difficult to identify which pins of the memory IC are affected leading to error. Also it is unrealistic to measure the induced noise signal on all the pins of the IC. The time domain simulation model overcomes this limitation by providing us with the induced noise signals simulated on all the pins of the memory IC. From this data one can formulate an expectation of the IC pins which could get disturbed due to field excitation. Figure 7.5 shows the plot of peak voltage magnitudes of address, data and control pins of the IC at the time of excitation.

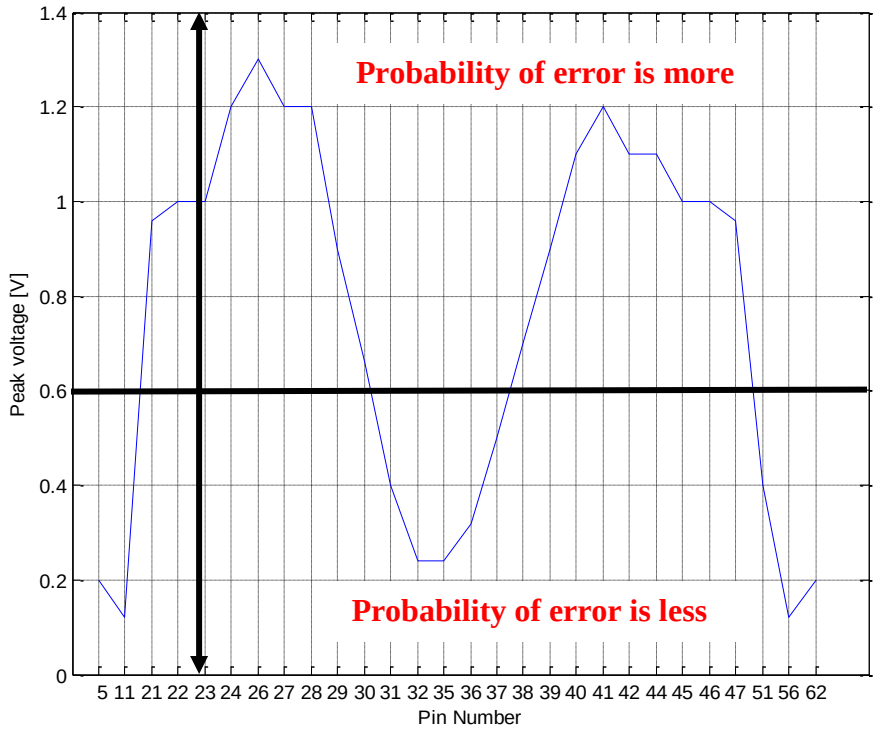

Figure 7.5. Simulated pin voltage distribution on excitation by TEM cell

The figure above shows the simulated pin voltage distribution of the memory IC on excitation by the TEM cell. The threshold level of the memory IC is ~ 0.6 V. So all the pins of the IC with peak induced noise greater than 0.6 V has a greater probability of a failure at the time of excitation. This information is useful since it gives the relative sensitivities of different pins of the memory IC and likelihood of a failure.

7.5 CONCLUSION

The height of the septum from the top wall of the TEM cell is 1 cm (which is four times less than the standard Fischer TEM cell). Consequently one would expect to obtain four times the standard field strengths leading to failure of the DUT. This is also supported by observations while performing the immunity test. The memory IC shows no error even up to 5 kV TLP charge voltage when mounted on the Fischer TEM cell.

With the specially designed TEM cell, at a TLP charge voltage of 2 kV, field strengths in the order of 100 kV/m and 250 A/m have been shown to cause failures in operation of the memory IC.

It is difficult to identify which pins of the memory IC are getting disturbed leading to an error. A full wave 3D model of the TEM cell (only the septum region) along with the lead frame of the IC gives a statistic of the induced noise voltage for all the pins of the memory IC. This information helps to give a better idea of the memory pins which could get disturbed due to field excitation.

The present modeling strategy deviates from the previous work in the respect that the complete physical geometry of the test IC has been included into the simulation model instead of analytical calculations to determine the immunity of the IC [17], [18].

8. SYSTEM LEVEL ESD GENERATOR TEST

8.1 INTRODUCTION

The objective of this test was to document the immunity of the memory IC to the ESD generator. A full-wave simulation model of the ESD generator with the lead frame geometry of the memory IC on the PCB board is also presented along with the simulation results to compare against the measurement results.

8.2 MEASUREMENT SETUP

Figure 8.1 shows the measurement setup of the ESD generator being discharged on the TEM cell board with the memory IC mounted on it.

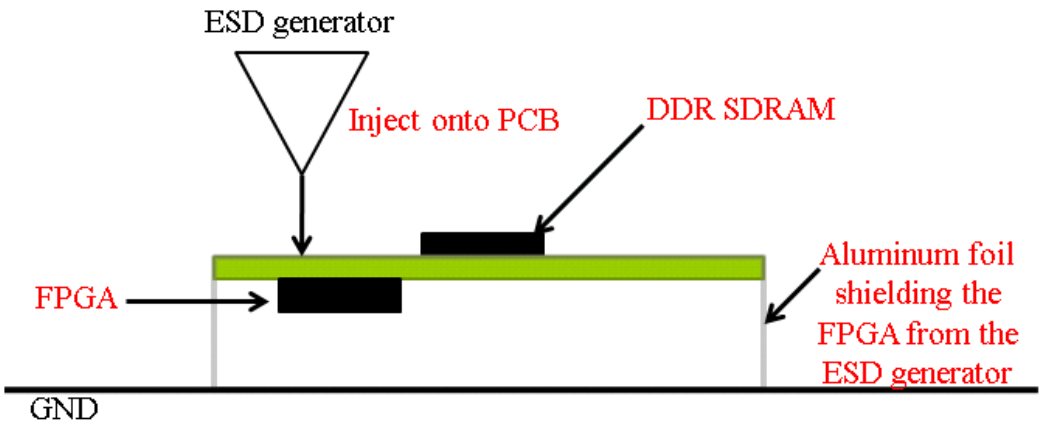

Figure 8.1. ESD Discharge on the TEM cell board

The TEM cell board is wrapped around in aluminum foil to shield the FPGA from the ESD generator. The ESD generator is discharged on the bottom layer of the board

with the memory IC mounted on it. Three different locations were selected as discharge points to measure the induced noise voltage on the DQ3, A4 & CLK pin of the memory IC at the time of malfunction of the IC. The whole setup is mounted on a large ground plane. Figure 8.2 shows the experimental setup to measure the induced noise voltage on DQ3 pin of the memory IC with reference to the PCB ground at the time of ESD discharge to the board.

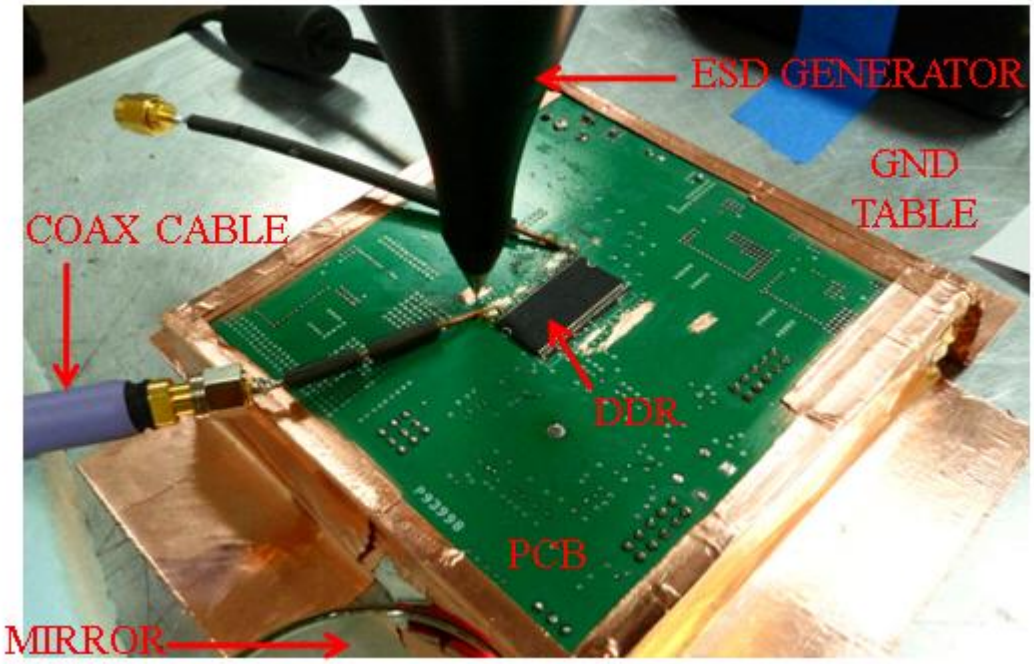

Figure 8.2. Measurement of Induced noise voltage on DQ3 pin

The TEM cell board wrapped around in aluminum foil is mounted on the ESD table. A coaxial cable is attached to the DQ3 pin of the memory IC to measure the induced noise voltage. The noise voltage is measured on an oscilloscope housed inside

the chamber to prevent direct coupling of the ESD generator to the scope. A small glass mirror is used to detect the failure of the memory IC in response to ESD injection onto the board.

8.3 MEASUREMENT RESULTS

The following figures show the measured induced noise voltage on the DQ3, A4 & CLK pin of the memory IC at the time of ESD discharge.

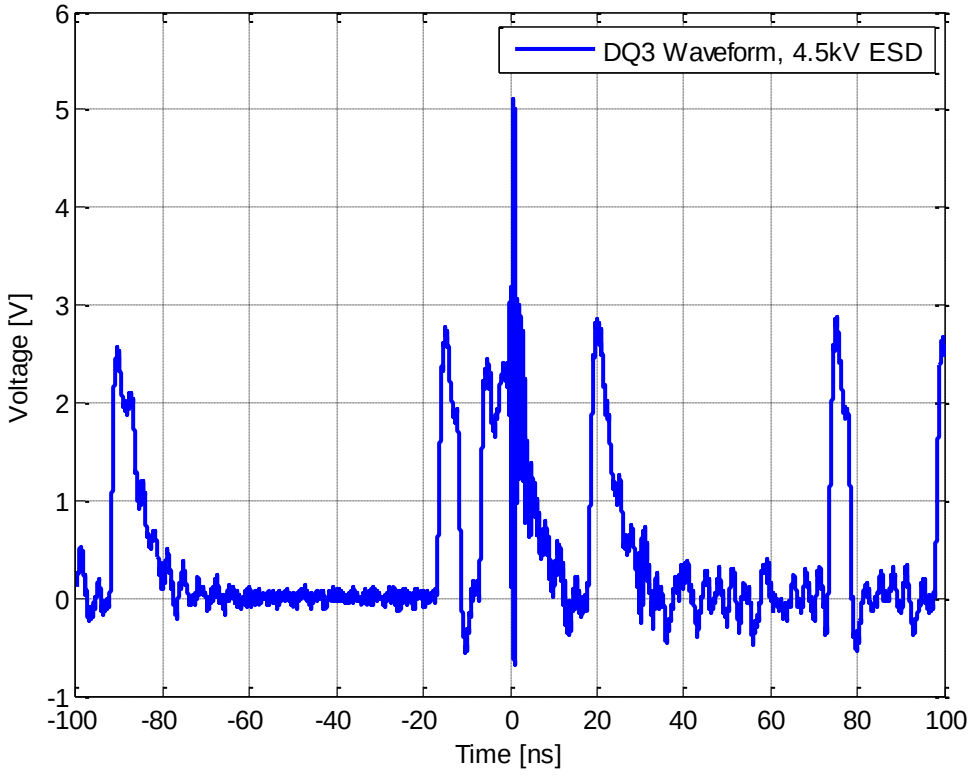

Figure 8.3. Induced noise voltage on DQ3 pin at positive ESD charge voltage

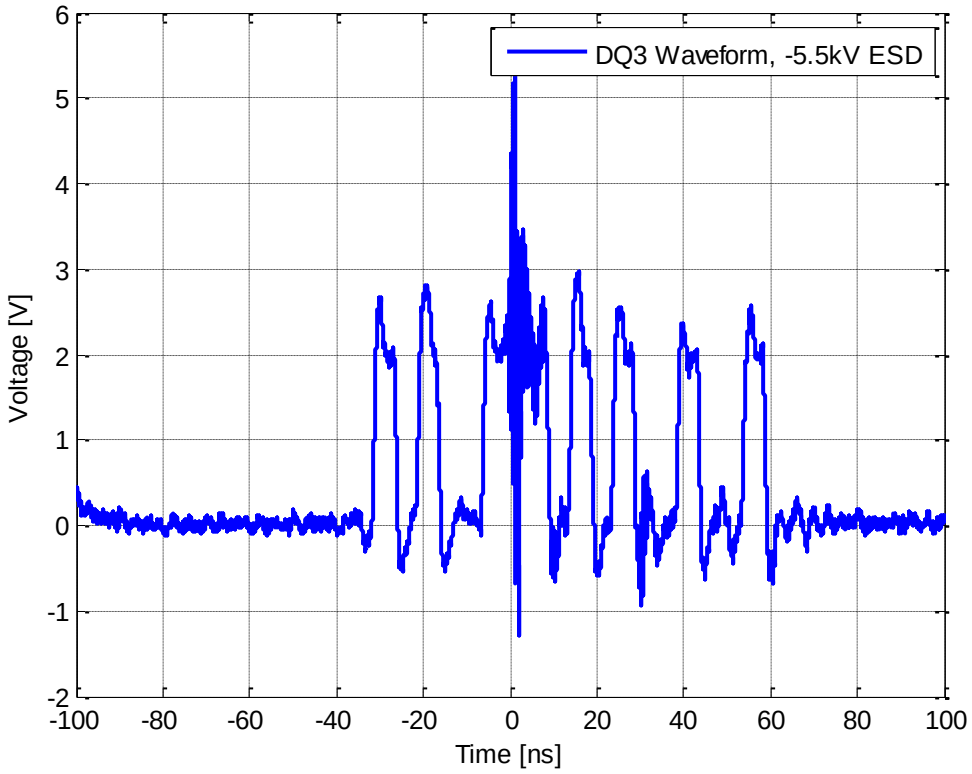

Figure 8.4. Induced noise voltage on DQ3 pin at negative ESD charge voltage

The figures above shows the induced noise voltage measured at the DQ3 pin at the time of discharge to the board. The ESD generator is discharged close to the DQ3 pin of the memory IC at a fixed distance. The voltage waveform on the DQ3 pin is measured for both the polarities. The sharp rising pulse due to the ESD discharge causes a latch up or a bit error in the normal operation of the memory IC. The peak value of the noise voltage is ~ 2.5 V. The noise voltage is also measured on the A4 pin at the time of discharge and is shown in Figure 8.5 & Figure 8.6.

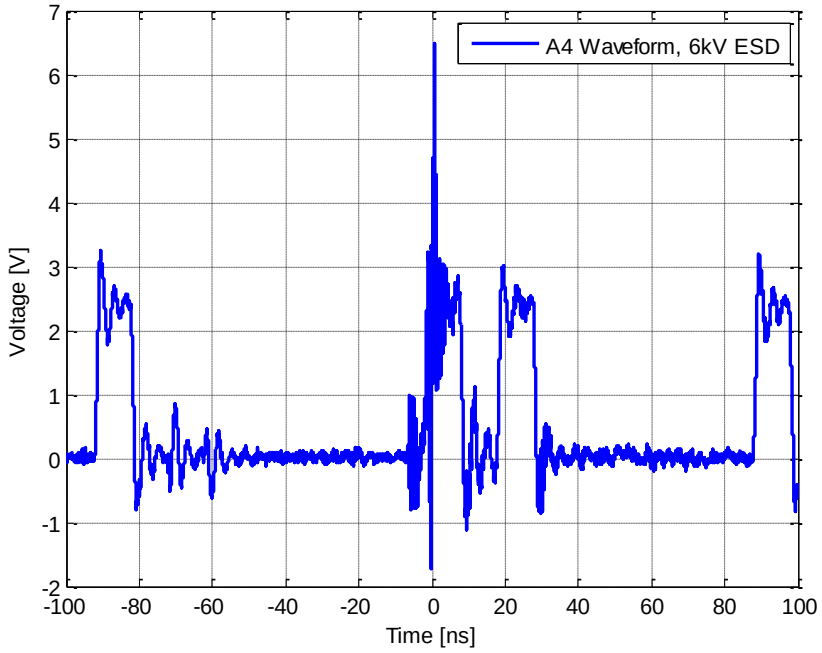

Figure 8.5. Induced noise voltage on A4 pin at positive ESD charge voltage

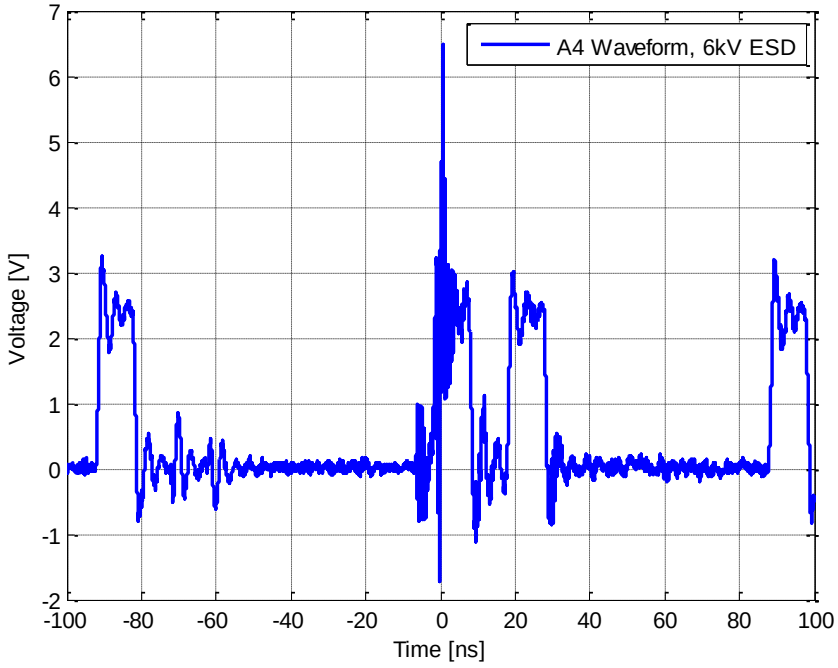

Figure 8.6. Induced noise voltage on A4 pin at negative ESD charge voltage

As with the DQ3 pin, ESD discharge on to the board at a fixed point close to the A4 pin causes failure in normal operation of the IC. ESD discharge causes a sharp rising pulse in the address bit of the memory IC causing a malfunction.

Finally the measured induced noise voltage on the CLK pin of the memory IC for both the polarities is shown in Figure 8.7 & Figure 8.8 respectively.

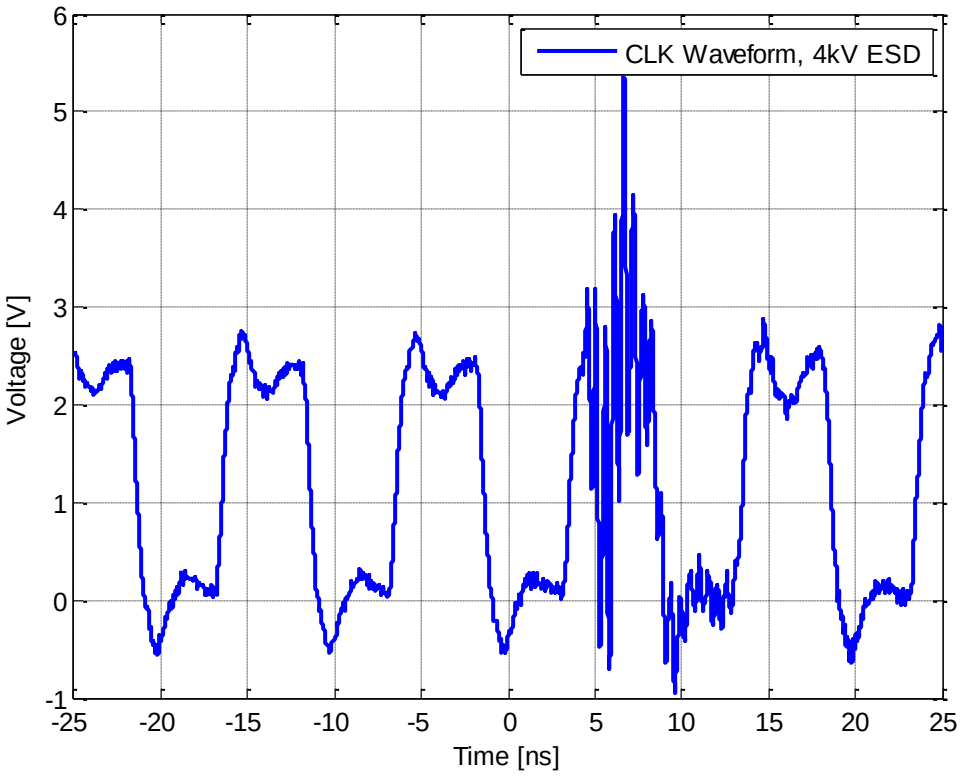

Figure 8.7. Induced noise voltage on CLK pin at positive ESD charge voltage

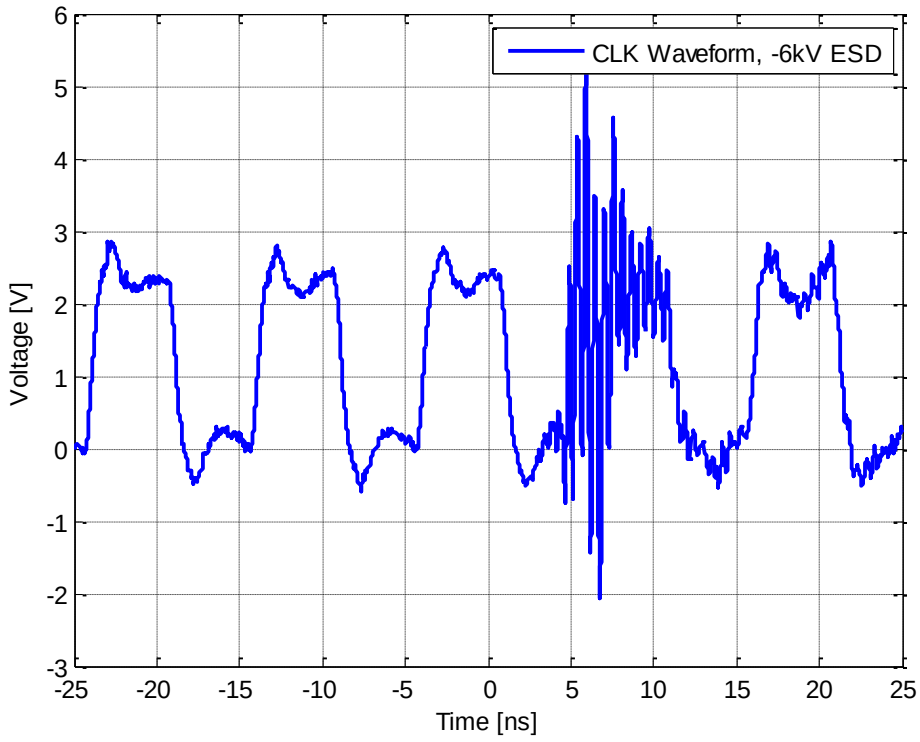

Figure 8.8. Induced noise voltage on CLK pin at negative ESD charge voltage

The next objective is to simulate the noise voltage waveform on the corresponding pins. To achieve that, a full wave model of the ESD generator along with the lead frame geometry of the IC and the PCB board is constructed in CST MWS.

8.4 SIMULATION OF INDUCED NOISE VOLTAGE

Time domain simulation is performed in CST MWS to obtain the induced noise voltage on DQ3 pin of the IC with reference to PCB GND. Figure 8.9 shows the full wave model of the complete structure with the ESD generator model and memory model.

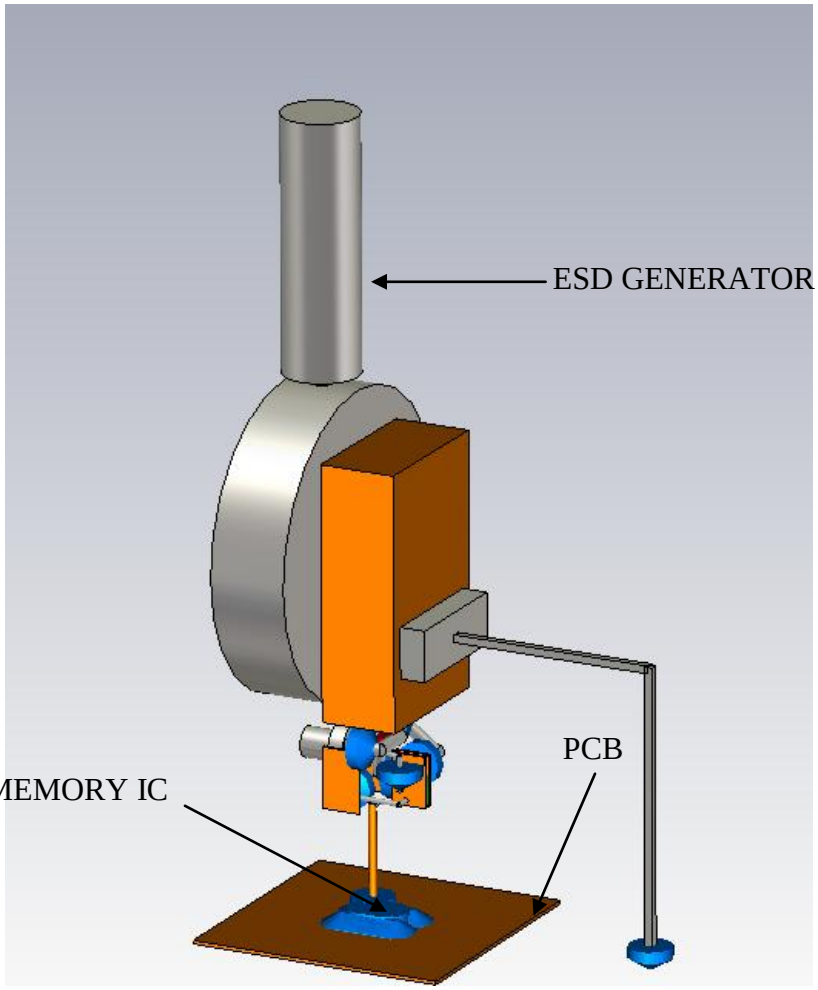

Figure 8.9. Complete 3D model of the memory IC with the ESD generator

All the lumped elements are included in the full wave model of the memory IC. Two lumped element ports have been defined on either end of the DQ3 pin connecting to the die and the PCB GND. PORT 1 connects the lead trace of DQ3 to PCB GND whereas PORT 2 connects the bond wire of DQ3 to the die. Figure 8.10 shows the magnified view of the ports and bond wire for DQ3 and DQ1 pin of the memory IC respectively.

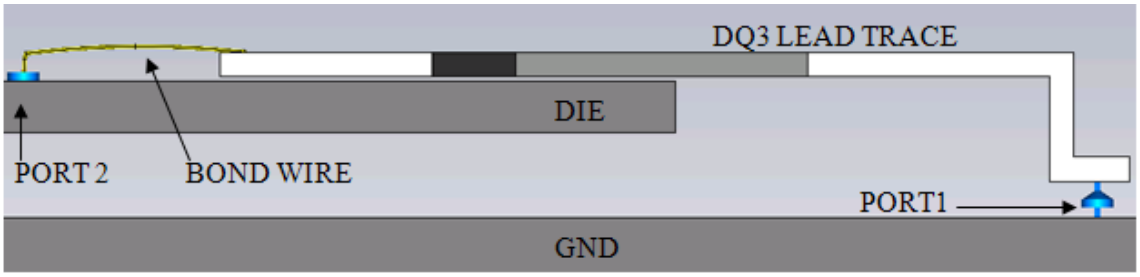

Figure 8.10. Definition of Ports on DQ3 lead trace

PORT 1 is connected to GND plane whereas PORT 2 is connected to the die. PORT 1 has been defined as a lumped element port with capacitance of C =10 pF. The capacitance models the high input impedance of the corresponding FPGA pin connected to the DQ3 pin via a trace on the actual board geometry. PORT 2 is defined as a lumped element port with resistance of R = 12.5 Ω to model the output high and low state resistance at the die. All the other geometries of the lead frame with the package, bond wires and top layer of the PCB along with the other lumped elements connecting to the die have been included in the model.

Figure 8.11 shows the comparison of the measured and simulated discharge current. The peak value of the discharge current matches quite well. The mismatch in the second peak is due to the short ground strap in the 3D model to reduce the computational domain.

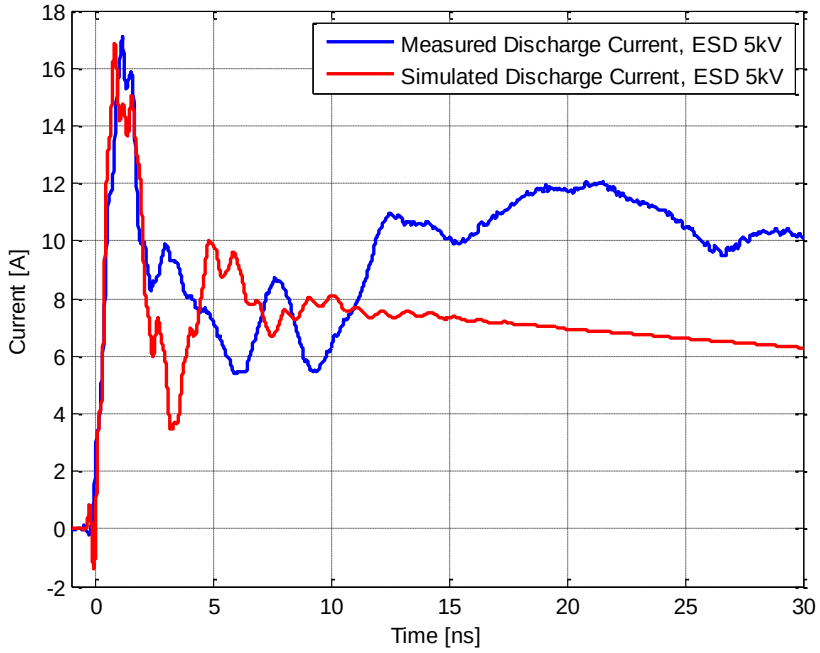

Figure 8.11. Comparison of ESD discharge current at 5kV

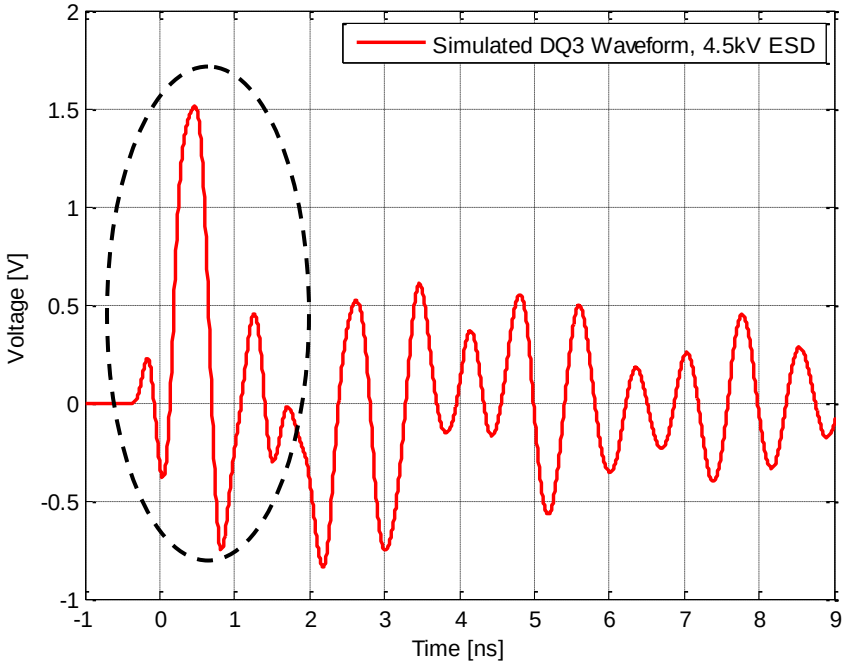

Figure 8.12. Simulated induced noise signal on DQ3 pin

Figure 8.12 shows the simulated induced noise signal on the DQ3 pin of the IC. The peak value of the measured induced voltage is ~ 2.5 V. The peak value of the simulated induced noise signal is 1.5 V. The reason in mismatch could be because of the limit of the ESD generator model. The ESD generator model is not able to model the transient electromagnetic fields greater than 3 GHz [11]. The pulse width of the measured nose signal is ~ 200 ps (at 50%) which is equivalent to 5 GHz. However the pulse width of the simulated noise signal is ~ 400 ps which is equivalent to 2.5 GHz. This could explain the deviation of the simulated noise signal from the measured value. Another reason could be due to direct coupling into the coaxial cable leading to higher magnitude of induced noise voltage waveform.

While performing the measurement it is difficult to identify which pins of the memory IC are affected leading to error. Also it is unrealistic to measure the induced noise signal on all the pins of the IC. The time domain simulation model overcomes this limitation by providing us with the induced noise signals simulated on all the pins of the memory IC. From this data one can formulate an expectation of the IC pins which could get disturbed due to field excitation. Figure 8.13 shows the plot of peak voltage magnitudes of address, data and control pins of the IC at the time of excitation. The figure below shows the simulated pin voltage distribution of the memory IC on excitation by the ESD generator. The threshold level of the memory IC is ~ 0.6 V. So all the pins of the IC with peak induced noise greater than 0.6 V has a greater probability of a failure at the time of excitation. This information is useful since it gives the relative sensitivities of different pins of the memory IC and likelihood of a failure.

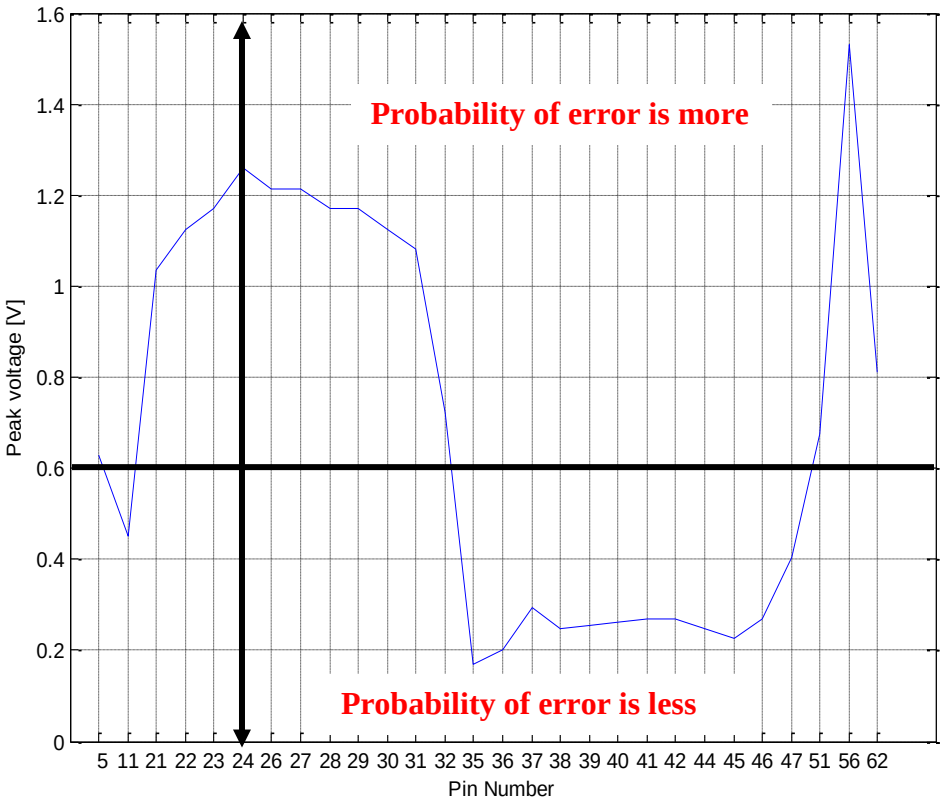

Figure 8.13. Simulated pin voltage distribution on excitation by ESD generator

8.5 CONCLUSION

Immunity of the memory IC in response to ESD discharge to the test board was documented for three different pins of the memory IC. The discharge point was selected close to the pins so as to increase the probability of an error due to disturbance on the selected pin. However ESD discharge could also affect adjacent pins leading to soft errors. It is not trivial to identify the exact pin of the memory IC that is getting disturbed. The full-wave simulation model of the ESD generator along with the lead frame geometry of the memory IC overcomes the problem of identifying the affected pins somewhat by giving the induced noise voltage for all the pins of the memory IC.

Field strengths of the order of 300A/m and 120kV/m are observed a few mm from the ESD test point at, e.g., 5kV contact mode, causing ESD related soft errors in the memory IC. Continuous improvements would be made to the full wave model to get a better a correlation between the measured and simulated waveform. Integrating the IBIS models of the memory and corresponding FPGA pins into the simulation model might improve the accuracy of the results.

8.6 COMPARISON OF FIELD INJECTION TECHNIQUES

One of the objectives in the investigation of field package interaction was to quantify the accuracy of the simulation results with measured sensitivities for the three types of field injection techniques: by the magnetic field loop probe, the TEM cell and the ESD generator. A qualitative comparison of the results for three different field injection techniques would help to establish the accuracy of the simulation results and also quantify the field strengths and induced noise voltages that lead to soft error failures in the test IC.

Table 8.1. Comparison of results for H field loop probe

Size (mm)	**Analytical estimation of noise voltage (V)**	**Measured induced noise voltage (V)**	**Full wave simulation of noise voltage (V)**
1	3.4	0.72	0.85
5	7.35	1.15	1.1

From the table above one can see that the measured induced noise signal on the DQ3 pin of the memory IC matches quite well with full wave simulation results.

However there is a deviation between the analytical estimation of the noise signal with the measured and simulated results. The reason for that is, during estimation of the induced noise voltage, the lead frame of the IC was approximated as a trace with the loop probe aligned on top of it. The analytical calculations do not take into account the intricate geometry of the multiple traces on the lead frame of the IC and the interaction between them. Full wave simulation of the whole structure would show the effect of adjacent traces on field strength and induced noise voltages. Also the time step (dt) used to compute the induced voltage has been assumed to be equal to the rise time of the TLP pulse. However this is not exactly correct since the TLP pulse rises very fast initially and then slows down. So the time derivative of the current would also be a continuously changing component rather than a constant value.

A comparison of the estimated field strength for the three different field injection techniques would also give a better idea of the levels which leads to soft error crash in the IC. Table 8.2 shows the comparison of the field strengths for field excitation by the magnetic field loop probe, TEM cell and the ESD generator respectively.

Table 8.2. Comparison of field strength for three field injection techniques

Type of field injection	**Magnetic field strength (A/m)**	**Electric field strength (V/m)**
H field loop probe	400	150
TEM cell	250	100
ESD generator	300	120

The field strength levels which lead to soft error failures in the memory IC are roughly close to each other for the three methods of field excitation. Getting an estimate would help to characterize the crash levels in a much better way with regard to magnetic and electric field strength.

9. FULL WAVE MODEL TO SIMULATE THE NOISEKEN ESD GENERATOR

An electrostatic discharge (ESD) event may cause severe failure on the product not only because of the discharge current but also the transient electromagnetic (EM) field that has broadband frequency spectra. An ESD immunity testing is specified by the IEC 61000-4-2 [19], in which the detailed waveform of the discharge current injected by an ESD generator is described. Several circuit approaching models of ESD generator can well describe the discharge current waveform [1], [2], [3]. However, only the full wave models are able to predict the field coupling [11]. Modeling the field coupling is essential, especially for soft-error prediction, as they are often caused by the frequency components of ESD transient fields greater than 1 GHz.

The objective is to create a full wave simulation model of the commercially available Noise Ken ESD generator in CST Microwave Studio and validate the model with measurement results. In the modeling process, individual components of the generator were modeled separately and verified by comparing measured and simulated Z_{11} parameter. After combining individual components, the whole model was generated and validated with respect to the discharge current and induced loop voltage. The individual model parameters were determined from both calculation and measurement.

9.1 INTRODUCTION TO ESD GENERATOR

An ESD generator is used to simulate the discharge current from a charged human body. The IEC 61000-4-2 specifies the discharge current waveform for commercial ESD generator. Different ESD generator may cause different current waveform. However, to match the IEC standard, most ESD generators consist of a capacitor of 150 pF and a

series resistor of 330 Ohm. In ESD immunity test, the discharge current waveform is calibrated by injecting the current into a current target, which is also described by the IEC 61000-4-2. Figure 9.1 shows an example of the Noise Ken ESD generator model developed in CST MWS.

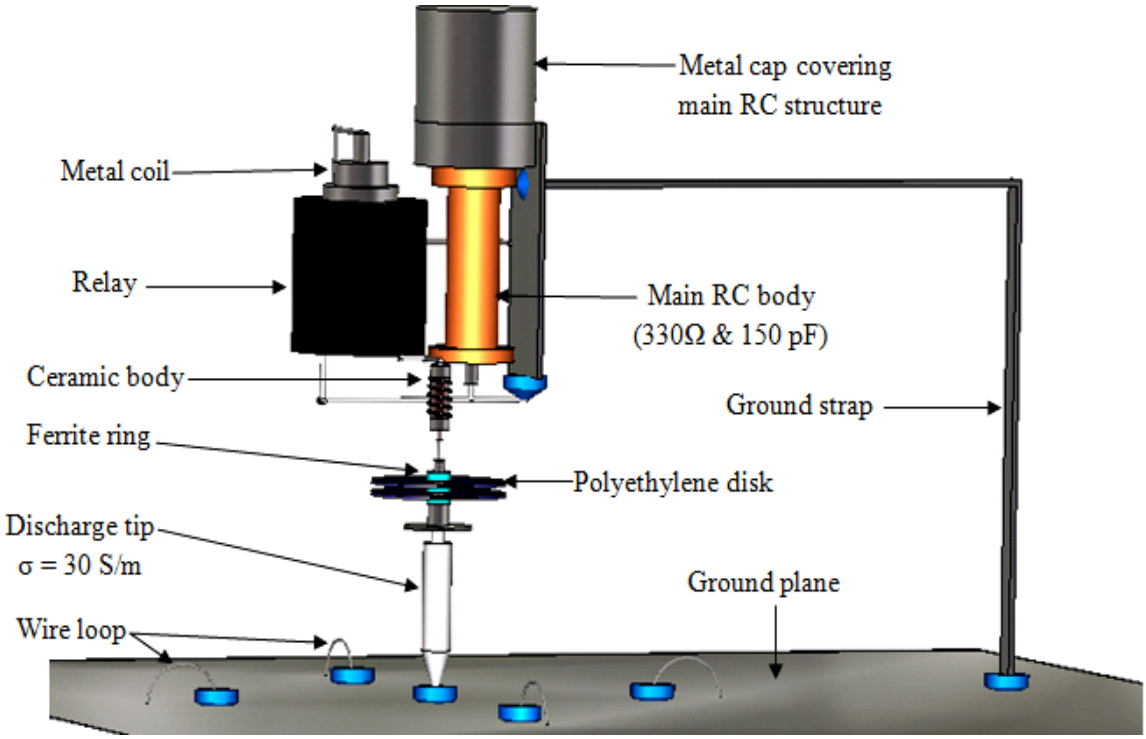

Figure 9.1. ESD generator geometry in full wave simulation

9.2 MODELING OF INDIVIDUAL COMPONENTS

After necessary simplifications, the components of the relay, the main R-C body, ceramic body, the ferrite ring and the polyethylene disk of Noise Ken ESD generator were considered for modeling purposes. These components were modeled and verified

separately and then combined together to form the complete generator model. The detailed modeling of the individual components is included in the sections below.

9.2.1. Modeling of relay. Different relays work differently but the basic principle of all of them with regard to ESD generators is that there is a metal contact (relay blade) between the two terminals. The relay blade is mechanically moved to make contact between the two terminals. When the charge voltage of the ESD generator is very high (in kV range) and the tip of the relay blade is close to the terminal, there is breakdown of the medium between the contacts (relay blade tip and terminal) resulting in an electrical spark between them. In different relays the exact process is carried out in different ways. The following discussion explains how the relay specific to the Noise Ken ESD generator works. Figure 9.2 shows the internal structure of the relay during the charging process.

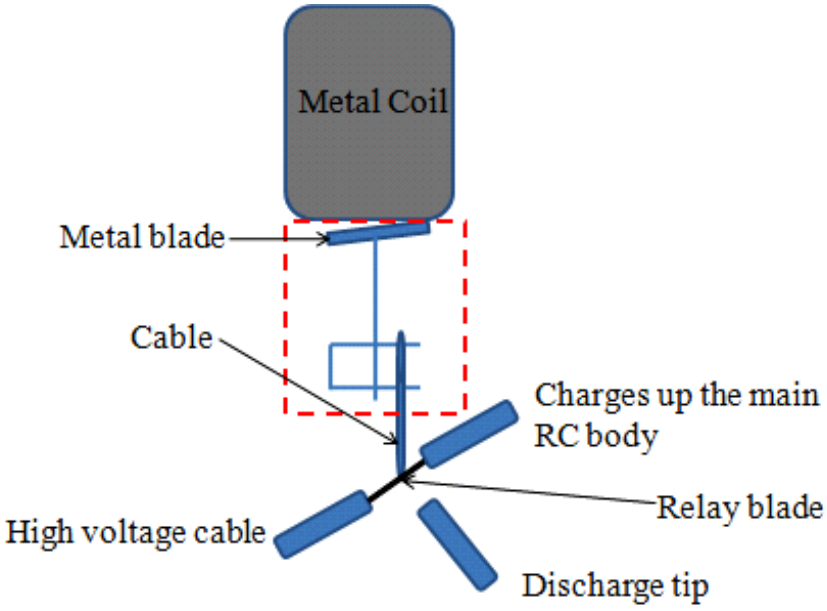

Figure 9.2. State of the relay during charging process

The metal coil (magnetic coil) generates a magnetic field when charged up by a voltage source of 23 V. The magnetic field causes the metal blade to swing in upward direction which in turn (through mechanical movement) makes the cable move. The cable is attached to the relay blade and in the process of its motion; the relay blade makes contact with the high voltage cable and main RC body on either side. Thus the main capacitor (150 pF) is charged up to the charge voltage of the ESD generator.

During the discharge process the relay blade, through the same mechanical movement, turns anticlockwise (shown by the arrow) and makes contact with the discharge tip. At this point all the charge stored in the main capacitor is discharged through the discharge tip by an electric spark between the main RC body pin and discharge tip pin. Figure 9.3 shows the state of the relay during the discharge process.

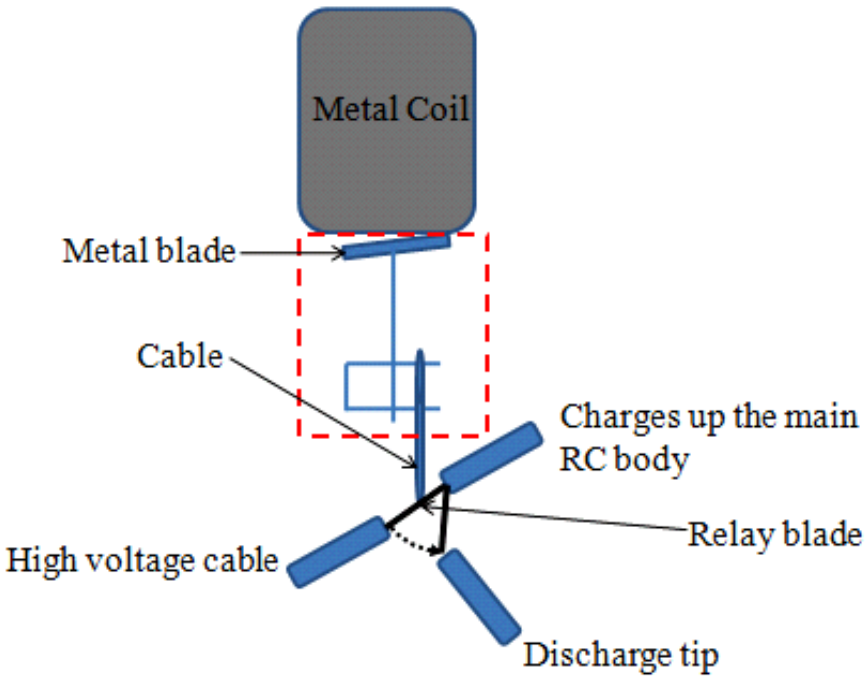

Figure 9.3. State of the relay during discharge process

This is the basic operating principle of the relay in the Noise Ken ESD generator. Based on this process the port of this full wave model was placed in the relay, contacting with the main RC body pin and discharge tip pin. An internal view of the relay inside the Noise Ken ESD generator from the x-ray is shown on the left in Figure 9.4 . On the right is the relay modeled in CST.

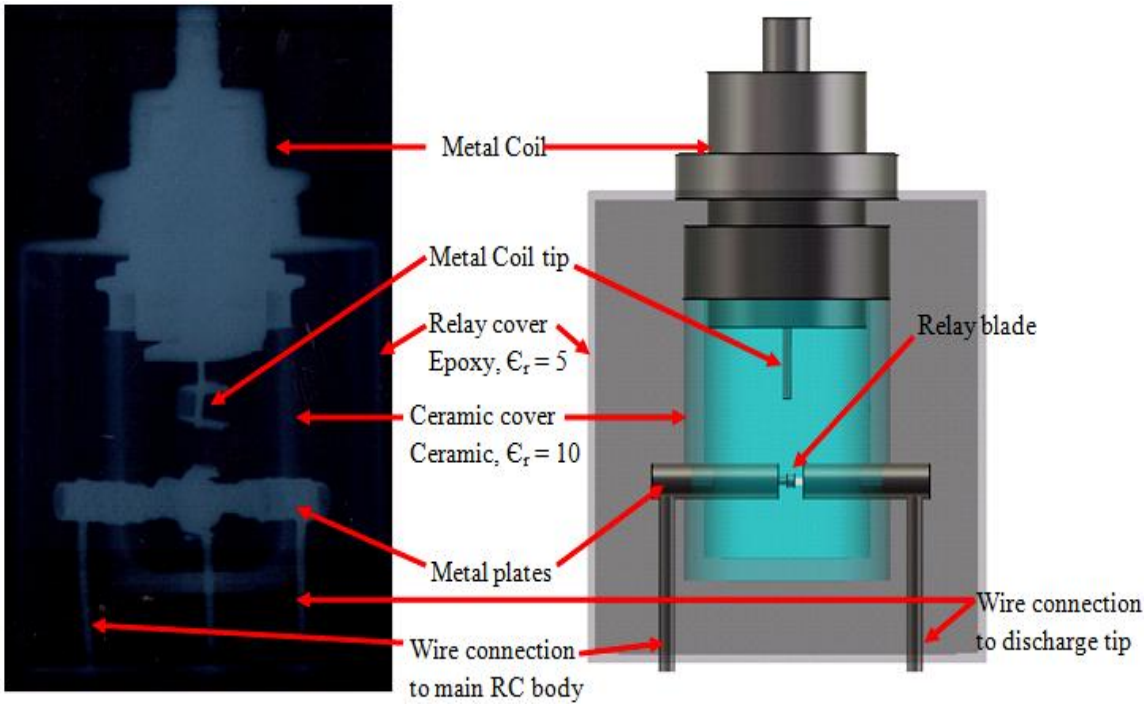

Figure 9.4. An internal view of the relay

All metals in the relay are modeled as PEC. The port is in the position of the relay blade. The excitation port is defined as an S parameter port with impedance of 25 Ω. Figure 9.5 shows the excitation signal on the port. It is a step function, with a rise time of

200 ps which represents the rapid voltage collapse at the beginning of the discharge process. It has been designed based on an integrated Gaussian pulse to ensure a smooth rising edge. The shape and rise time of this pulse allows us to adopt the RF spectrum of the ESD generator to approximately accommodate other ESD generator models.

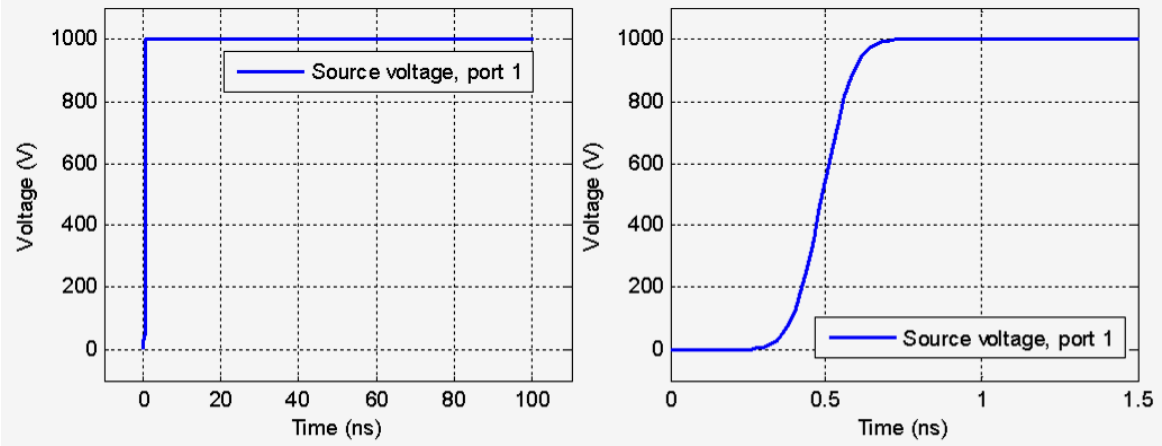

Figure 9.5. Excitation signal on the port

9.2.2. Modeling of R-C body. An internal view of view of the main discharging capacitor and resistor body is shown in Figure 9.6. The capacitor and resistor is covered with a Teflon covering indicated by the yellow color. The resistor body is modeled as a moderately conducting body.

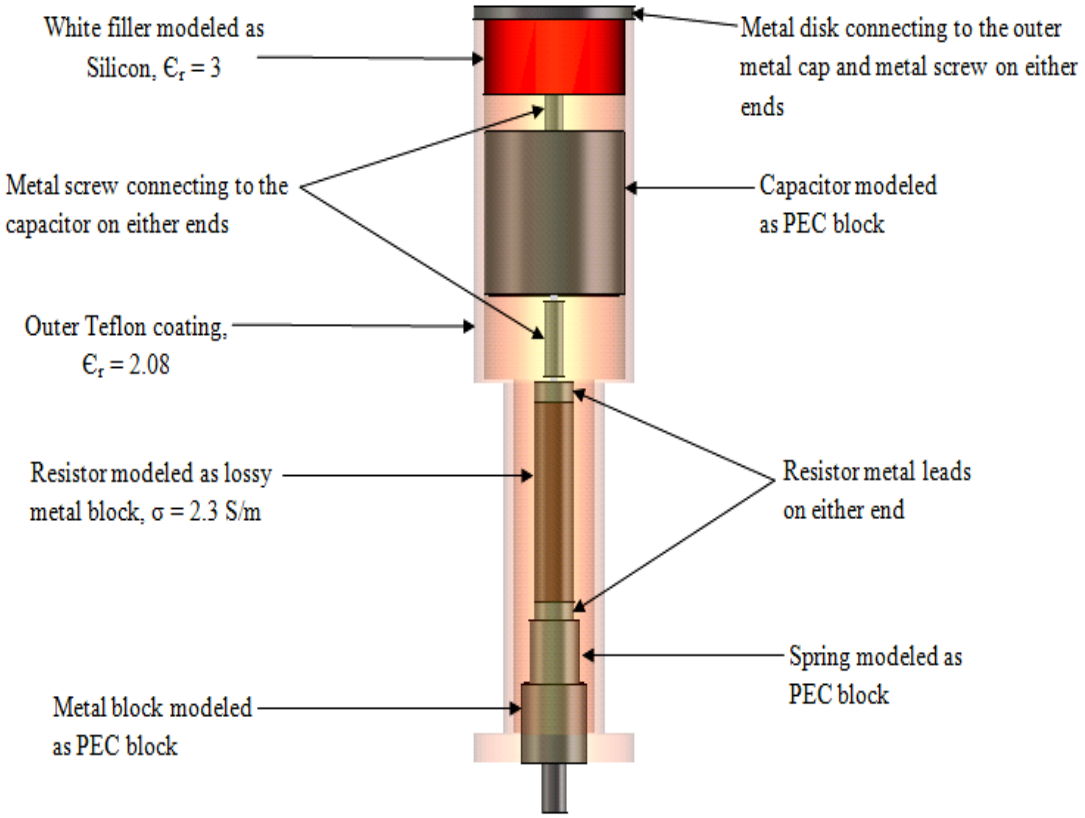

Figure 9.6. Internal view of the main discharging capacitor and resistor body

The dimensions of the resistor body is already known and the conductivity is calculated below,

Length (L) = 38 mm

Radius (r) = 4 mm

Cross sectional area (A) = 50.24 mm^2

Resistance (R) = 330 Ω

Therefore Conductivity (σ) = L/R*A = 2.3 Sm^{-1}

The resistor is modeled as a lossy metal cylinder with the above dimensions and conductivity of σ = 2.3 Sm^{-1}.

A Z11 measurement was performed on the main RC structure using the network analyzer in an attempt to validate the model in CST. The setup for the measurement is shown in Figure 9.7,

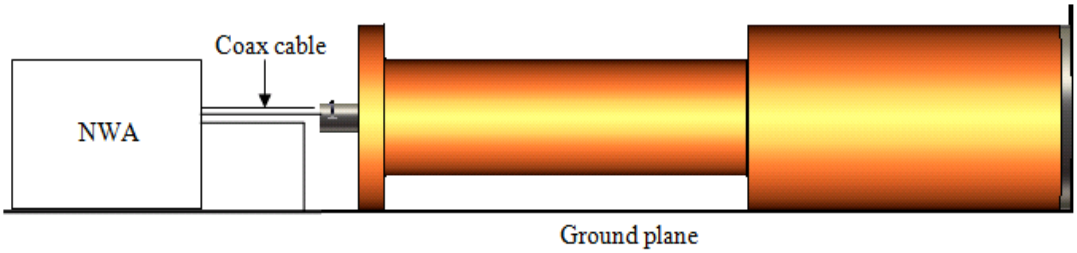

Figure 9.7. Experimental setup for measuring Z11 of R-C body

A CST model of the structure is created and the simulated data is compared to the measurement result. The CST model is shown in Figure 9.8.

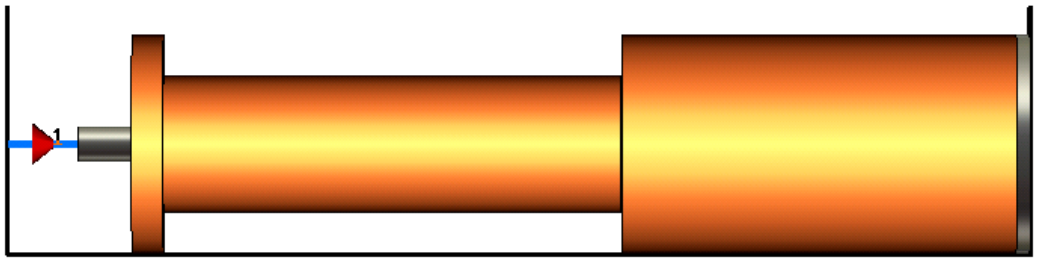

Figure 9.8. Frequency domain CST model of the main R-C body

The frequency range of simulation was set from 30 kHz to 3 GHz and the number of frequency samples was set to 50000. The S parameter voltage port was excited using a Gaussian pulse of duration 200 ns. A comparison of the measured and simulated impedance looking into the structure is shown in Figure 9.9.

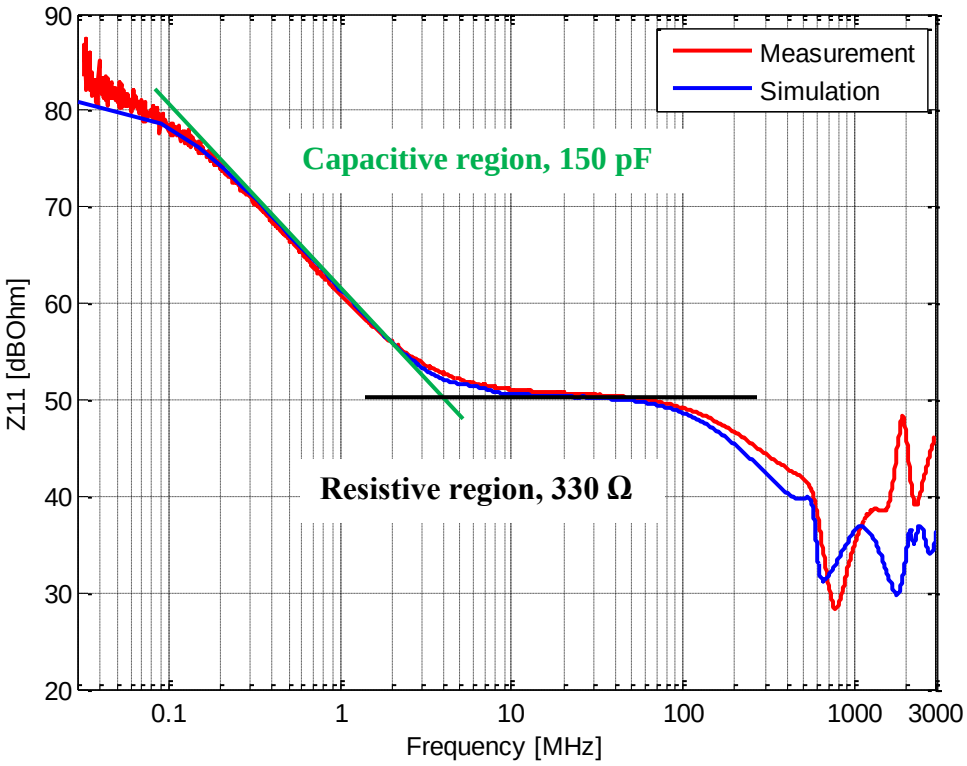

Figure 9.9. Comparison of measured and simulated Z11 for the main R-C body

The measured and simulated magnitude of Z11 matches very well up to 100 MHz. The deviation at frequencies above 500 MHz is attributed to uncertainties in the measurement.

9.2.3. Modeling of ceramic body. A detailed view of the ceramic body modeled in CST is shown in Figure 9.10. The ceramic body was modeled with a dielectric body combined with metal heads and coil. The dimensions are in accordance with the real component.

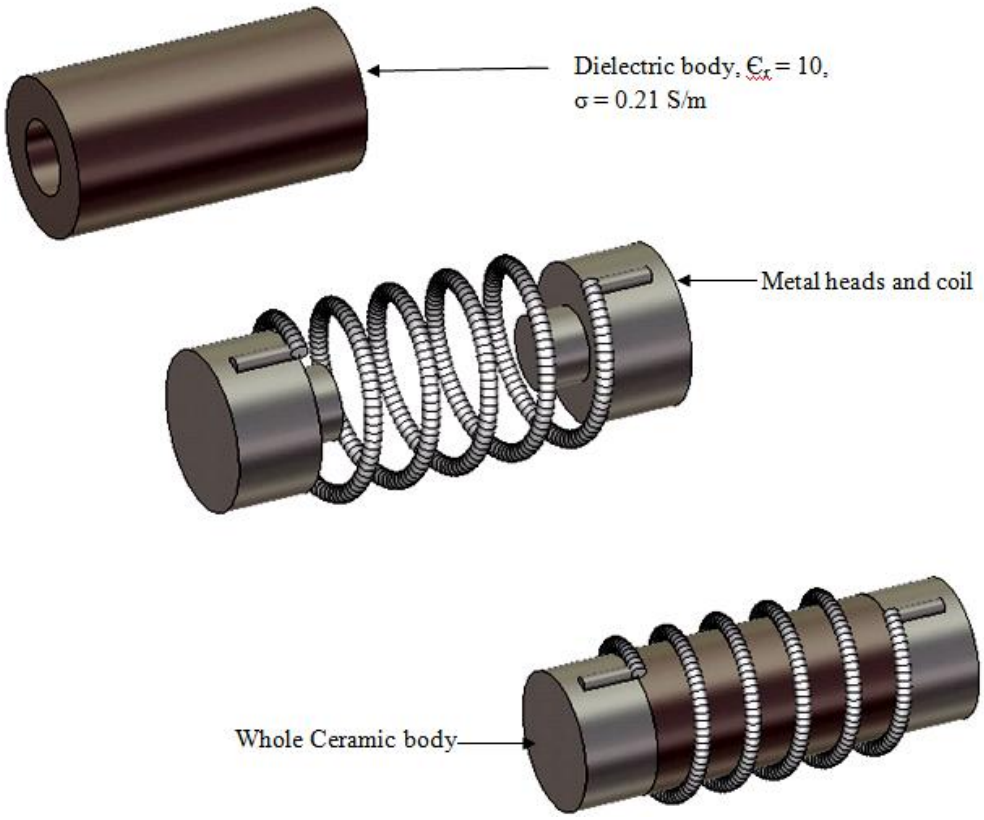

Figure 9.10. Different parts of the ceramic body developed in multiple steps

A Z11 measurement was performed on the ceramic body as well in an attempt to validate the model in CST. The experimental setup is shown in Figure 9.11.

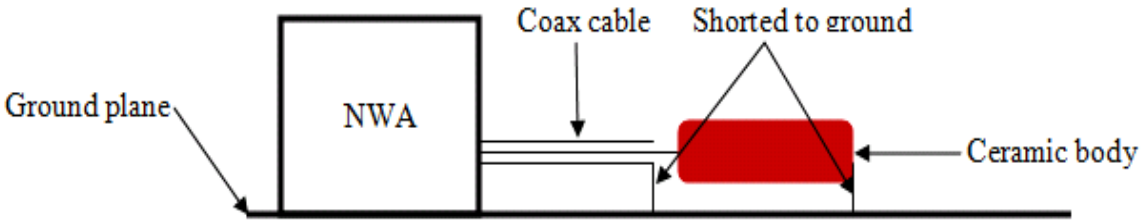

Figure 9.11. Experimental setup for measuring Z11 of ceramic body

The inner conductor is connected to one end of the ceramic body and the calibration plane is extended to the end of the cable. The outer conductor and the far end of the ceramic body are shorted to the ground plane using gaskets. A frequency domain simulation of the ceramic body was performed in CST. Figure 9.12 shows the frequency domain model of the ceramic body in CST.

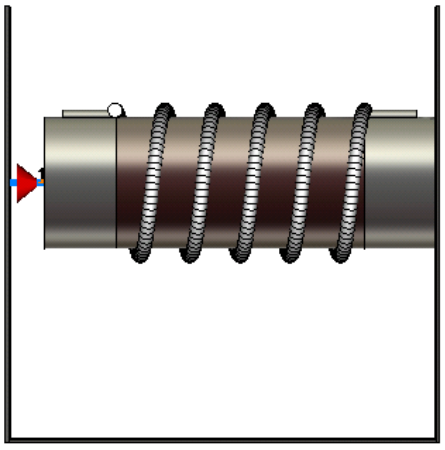

Figure 9.12. Equivalent frequency domain model of the ceramic body in CST

The network analyzer port is defined as an S-parameter port with 50 Ω source impedance. Figure 9.13 shows the comparison of the measured and simulated Z11 of the ceramic body.

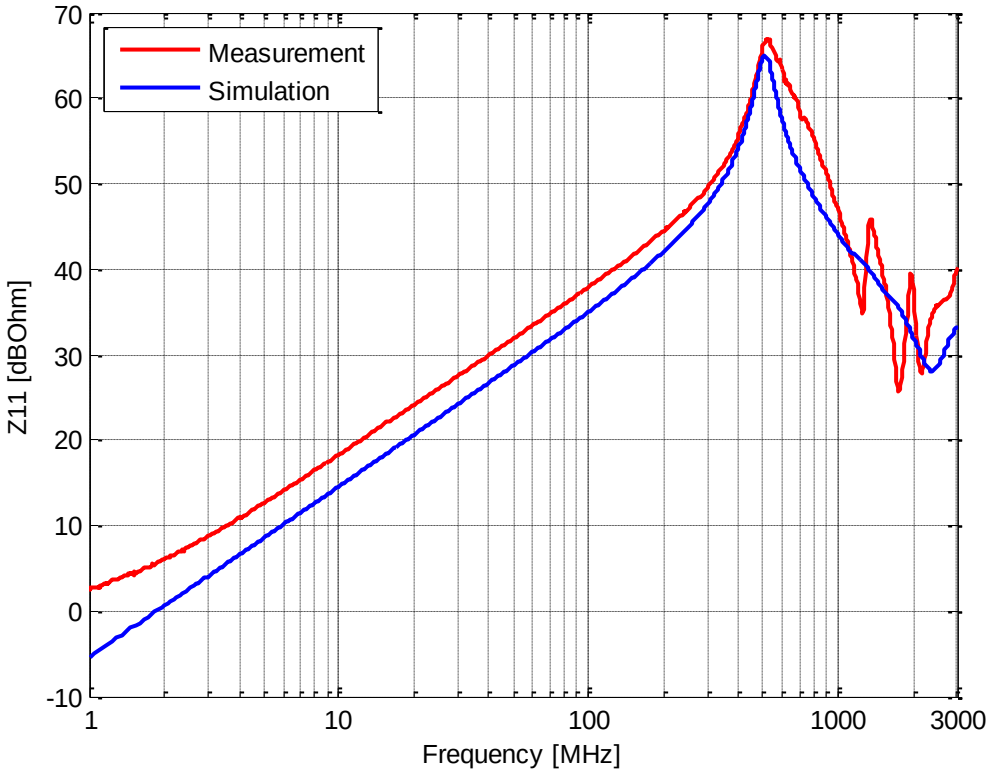

Figure 9.13. Comparison of Z11 of the ceramic body

The CST results match pretty well with the measurement results except for some deviations at higher frequencies.

9.2.4. Modeling of ferrite rings. The Noise Ken ESD generator has three ferrite rings in the discharging structure [21]. Just like the cceramic body, Z11 measurement was

performed on the ferrite in an attempt to obtain a frequency domain model in CST. The experimental setup is shown in Figure 9.14.

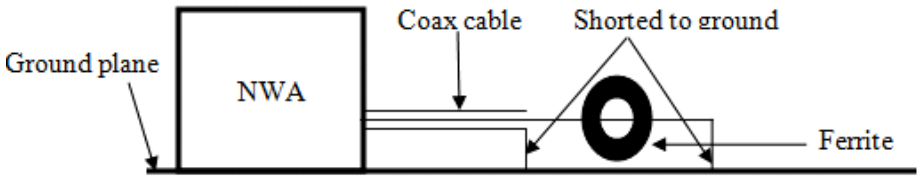

Figure 9.14. Experimental setup for measuring Z11 of ferrite

The coax cable is connected from the network analyzer. The inner conductor is passed through the ferrite and shorted at the far end to the ground plane using gaskets. An equivalent CST model of the ferrite ring is shown in Figure 9.15. Table 9.1 below shows the parameters used to model the ferrite ring in CST.

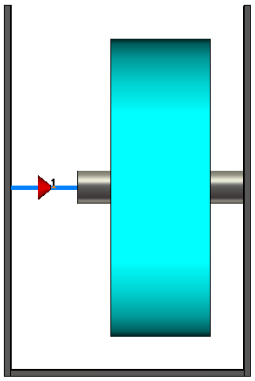

Figure 9.15. Equivalent frequency domain model of the ferrite ring in CST

Table 9.1. Parameters of the ferrite ring modeled in CST

Dielectric Dispersion	ϵ_∞	ϵ_{static}	**Relaxation time (ns)**
	7.5	16	0.45
Magnetic Dispersion	μ_∞	μ_{static}	**Relaxation time (ns)**
	1	1000	16

Figure 9.16 shows the comparison of the measured and simulated Z11 of the ferrite ring.

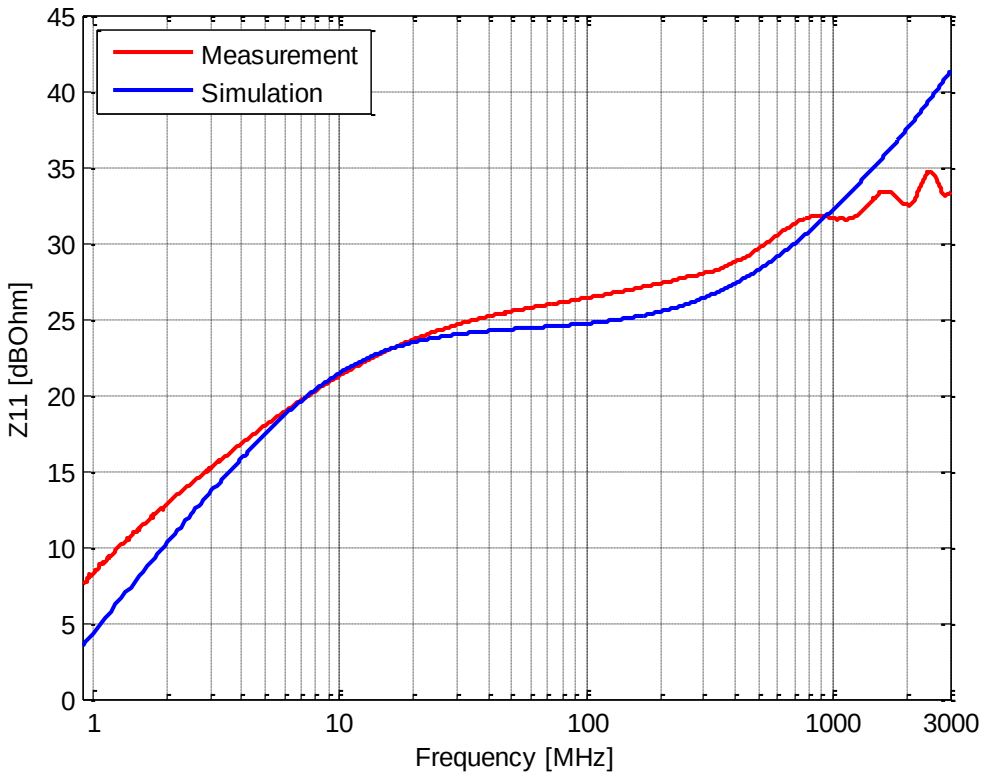

Figure 9.16. Comparison of Z11 of the ferrite ring

The simulation results match fairly well with the measurement results except for some deviations at higher frequencies.

9.2.5. Modeling of polyethylene disks. Figure 9.17 shows the picture of the polyethylene disk.

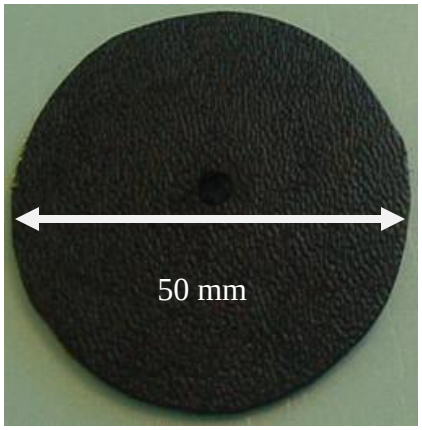

Figure 9.17. Picture of the polyethylene disk

The disk is modeled as a lossy dielectric material. It is modeled in CST as a circular disk with σ=100S/m and ϵ_r=40. Possible frequency dependence of the material is not taken into consideration. The contact to the disks is highly undefined in the real ESD generator, as the surface conductivity is highly variable. It might be that the disks are mainly field coupled such that the problem of having reliable contact is not critical.

9.3 MODELING OF THE WHOLE ESD GENERATOR

The full wave ESD generator model in CST MWS is shown in Figure 9.18.

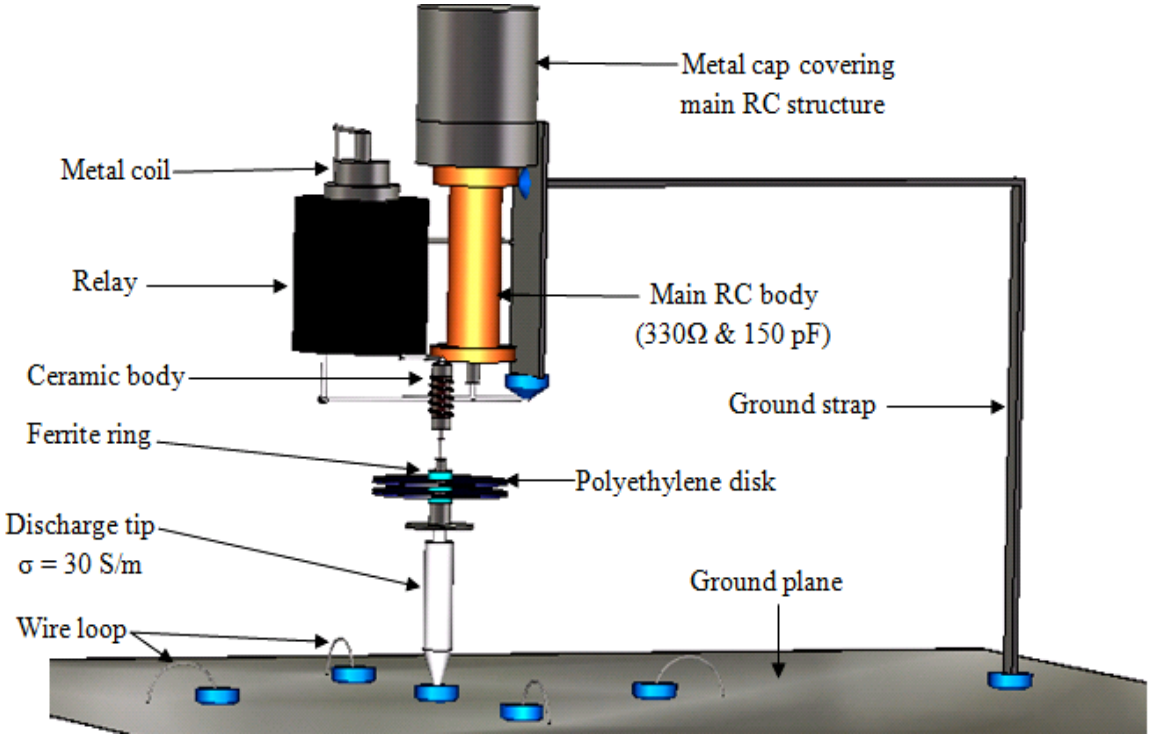

Figure 9.18. ESD generator geometry in full wave simulation

Every object in the model is PEC, in grey color, except the outer cover of the relay which is modeled as Epoxy, in black, outer cover of the capacitor which is modeled as Teflon, in yellow, an inner white filling material modeled as Silicon in red, the ferrite rings modeled in cyan and the polyethylene disks in violet. The losses in the model are distributed by assigning conductivity of σ = 4000 S/m to the interconnecting wires and conductivity of σ = 30 S/m to the discharge tip.

The above model of the Noise Ken ESD generator is with short ground strap. For long ground strap model, distributing inductance along the ground strap can well represent the effect of the long ground strap. Figure 9.19 show the long ground strap model.

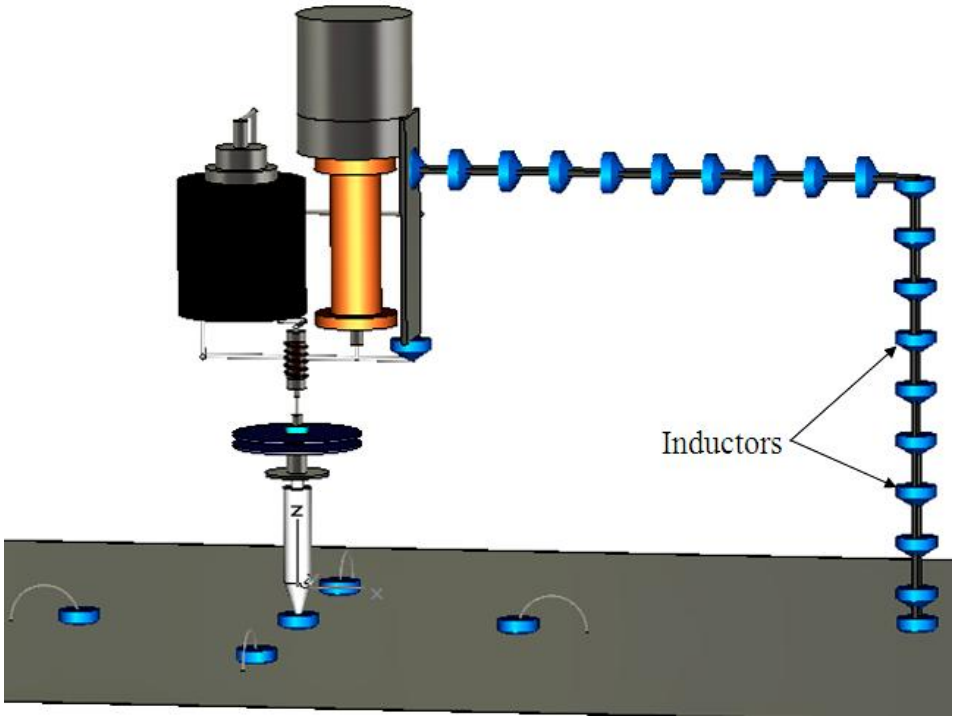

Figure 9.19. ESD generator with long ground strap in full wave simulation

9.4 VERIFICATION OF ESD DISCHARGE CURRENT

The current injected into a large ground plane is the main criterion for ESD generator performance. In order to validate the proposed full wave model, the discharge

current of the Noise Ken ESD generator was measured and compared with the simulated discharge current both with the short ground strap and long ground strap model.

Figure 9.20 shows the experimental setup for measurement of the discharge current. The oscilloscope was placed inside the chamber to avoid direct field coupling from the generator to the ports of the oscilloscope. An attenuator was used to protect the oscilloscope input. The current target was mounted on the wall of the chamber. After the ESD generator was charged to 1 kV, is was discharged by pushing the triggering button on the high voltage generator. Figure 9.20 gives the setup for long ground strap. For short ground strap, a shorter length of the ground strap is shorted to the ground plane.

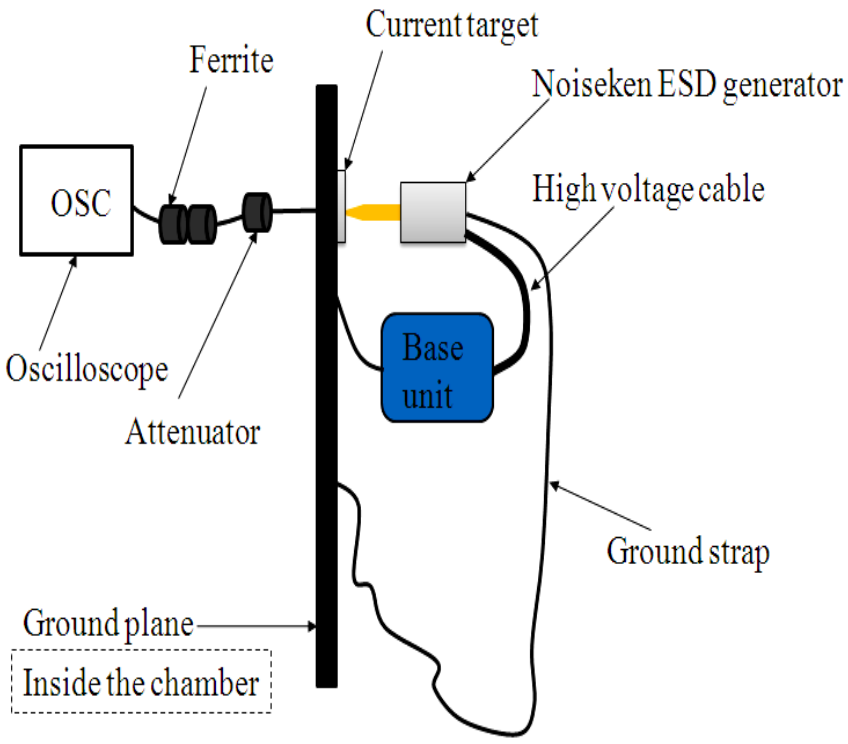

Figure 9.20. Measurement setup to measure the ESD discharge current

Figure 9.21 shows the comparison of the measured and simulated discharge current for short ground strap model.

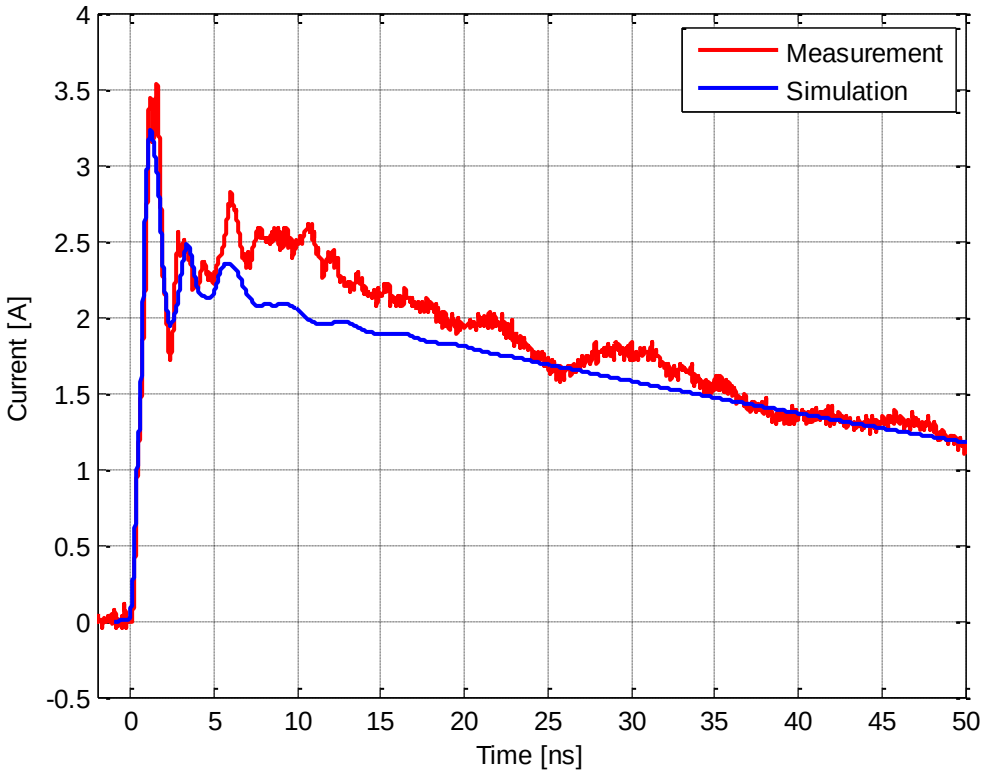

Figure 9.21. Comparison of discharge current for short ground strap

The peak value of the discharge current matches quite well. The length of the ground strap determines the position of the second peak of the current. The shorter length of the strap shifts the second peak to around 6 ns both with respect to measurement and simulation.

Figure 9.22 shows the comparison of the measured and simulated discharge current for the long ground strap model.

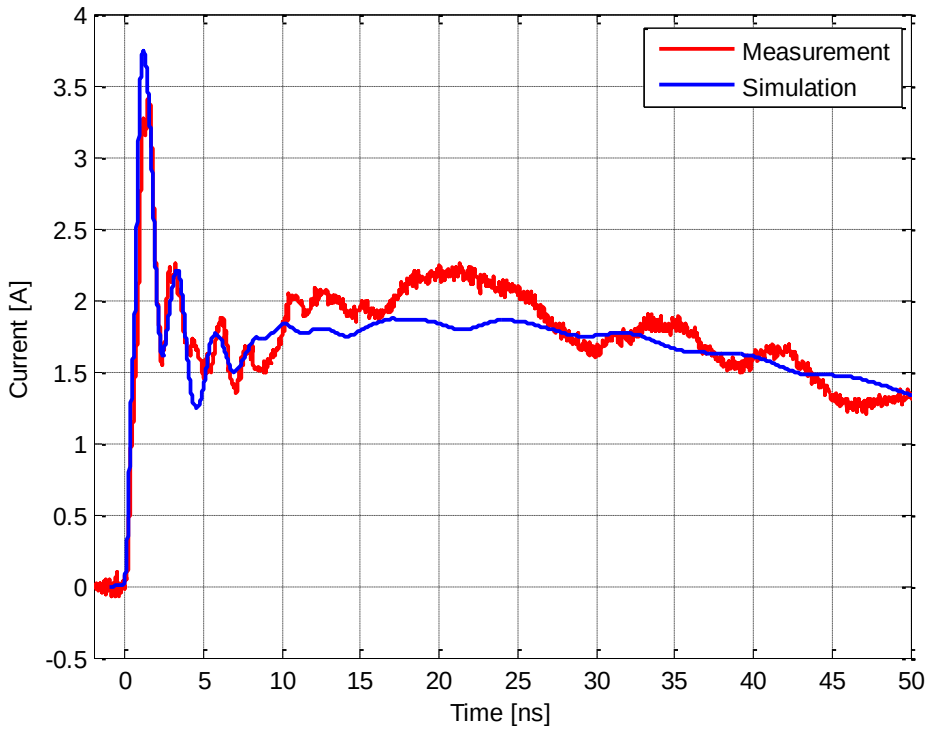

Figure 9.22. Comparison of discharge current for long ground strap

The simulated discharge current matches quite well with measured result. The fast rising and possibly ringing behavior of the first peak in the discharge current waveform, dominates the disturbances in electronic systems. In case of the long ground strap model the second peak of the discharge current shifts to ~ 20 ns as expected.

9.5 VERIFICATION OF INDUCED LOOP VOLTAGE

The ESD standard IEC 61000-4-2 is presently being revised to address the problems of ESD test result repeatability. One measure to better characterize an ESD

generators is the voltage induced in a loop close to the ESD generator. To avoid possible coupling into cables a ground plane mounted semi-circular loop is used. It is unshielded, thus, it is sensitive to the E and the H field. Its diameter is 28 mm and it is placed at a distance of 10 cm from the point of discharge. Such a loop represents a wire loop within an electronic system and is a better predictor for system level disturbances than the discharge current. Induced loop voltage was measured with the Noise Ken generator charged up to 1 kV at 4 different orientations (0, 90, 180 and 270 degree) and at 10 cm and 40 cm respectively from the discharge point. Figure 9.23 shows the experimental setup for the induced loop voltage measurement.

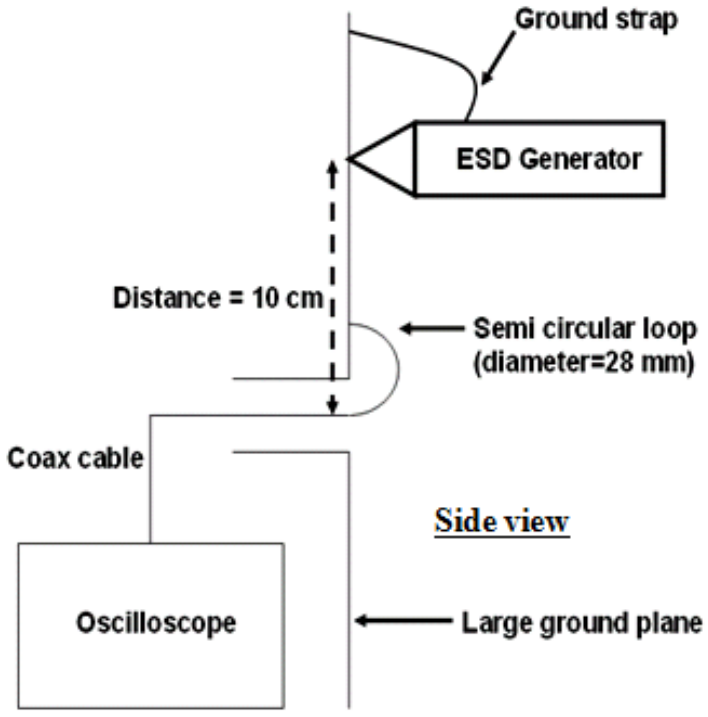

Figure 9.23. Experimental setup for induced loop voltage measurement

A comparison of the measured and simulated induced loop voltage in time domain at 10 cm for 0 degree orientation is shown in Figure 9.24.

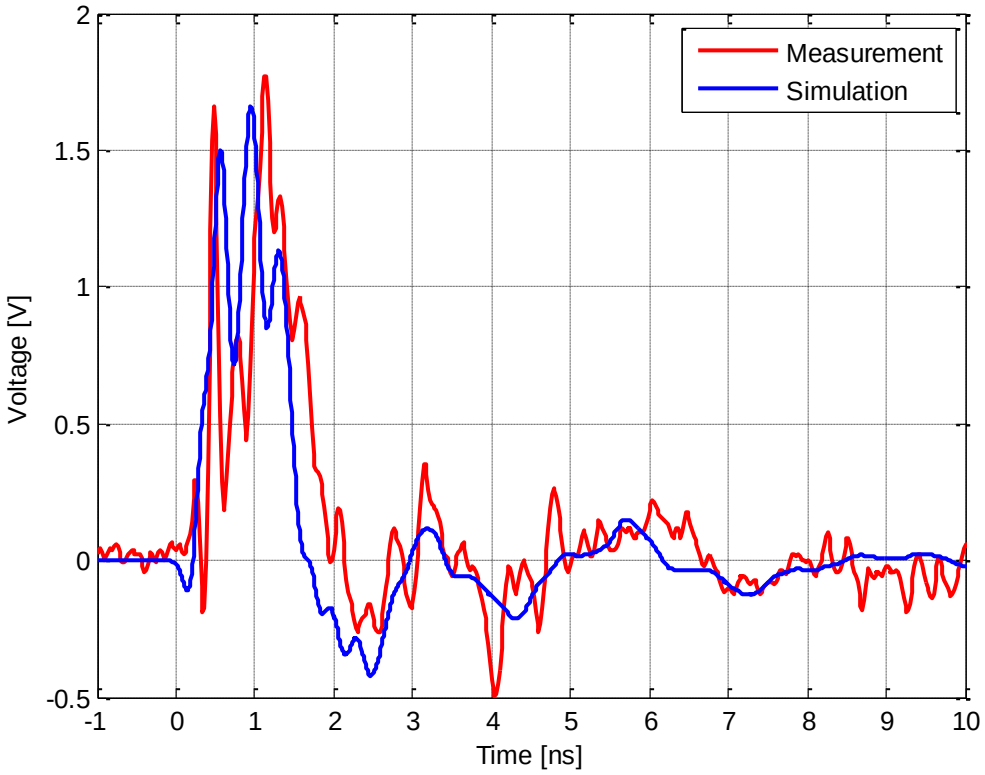

Figure 9.24. Comparison of induced loop voltage at 10 cm and 0 degree orientation

The comparison of the frequency spectrum of the induced loop voltage measured at 0 degree orientation is shown in Figure 9.25. The spectrum of the voltage waveform shows how accurately the full wave model is able to simulate the transient EM fields from the ESD generator. It is to be noted that the peak at 5 GHz is an artifact of the oscilloscope.

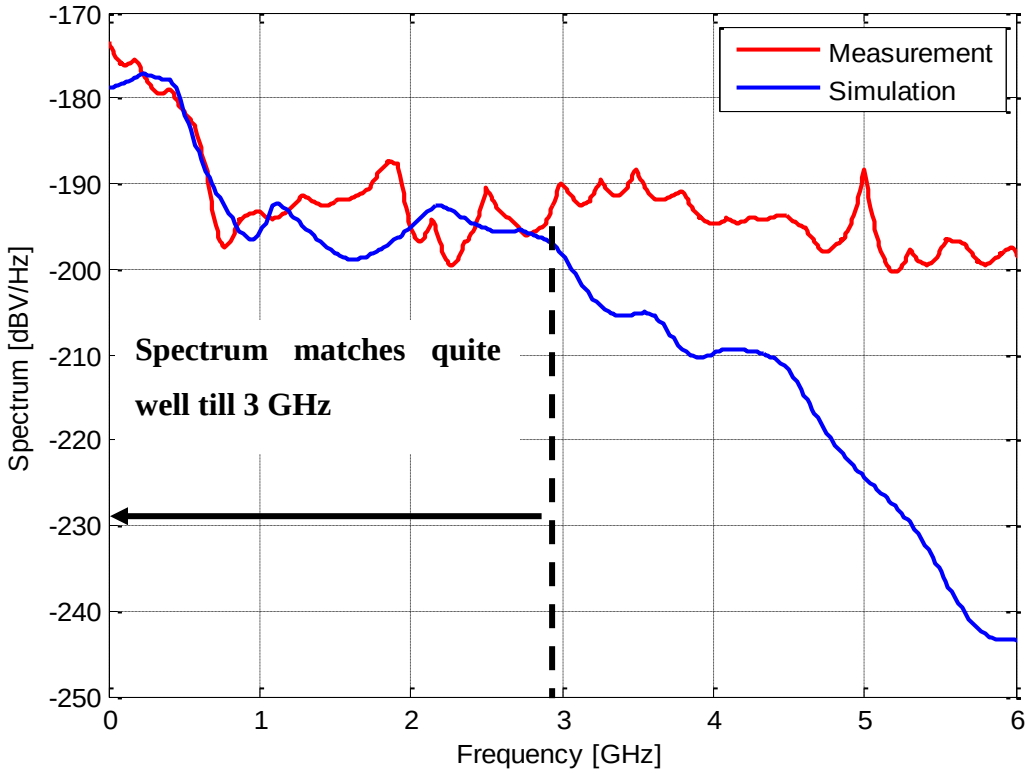

Figure 9.25. Comparison of spectrum of the loop voltage at 10 cm and 0 degree

From the above figure we see that the frequency spectrum of the induced loop voltage matches quite well up to ~ 3 GHz. A comparison of the induced loop voltage at 40 cm for 270 degree orientation is shown in Figure 9.26. The corresponding frequency spectrum of the induced loop voltage is shown in Figure 9.27. It is significantly more difficult to achieve a good match between the simulation and the measurement for an induced loop voltage relative to the injected current. The reason is the high pass behavior of the induced loop voltage and the field coupling. Thus, the generator model needs to be sufficiently accurate up to a few GHz.

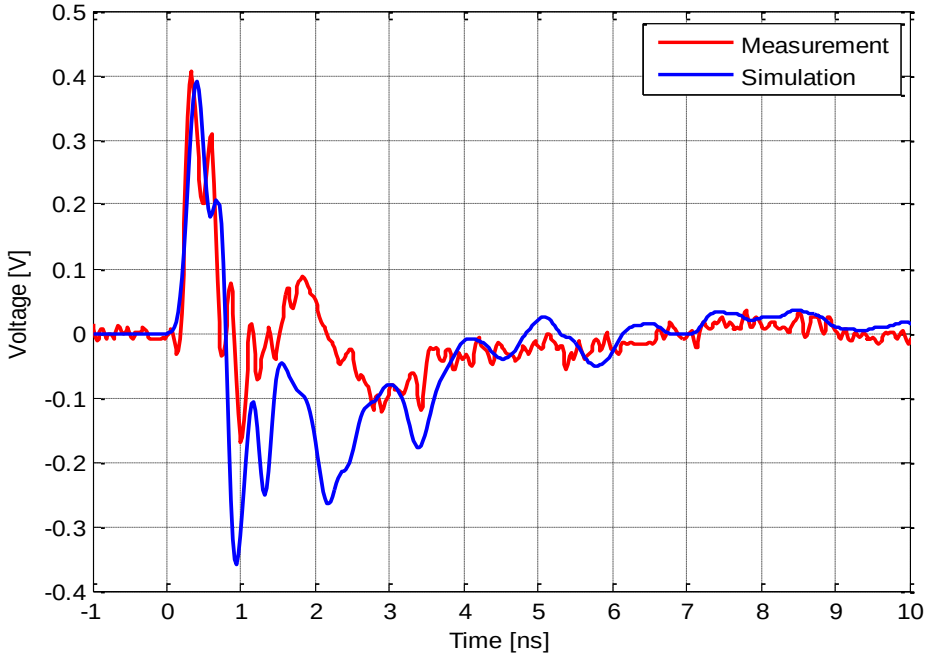

Figure 9.26. Comparison of induced loop voltage at 40 cm and 270 degree orientation

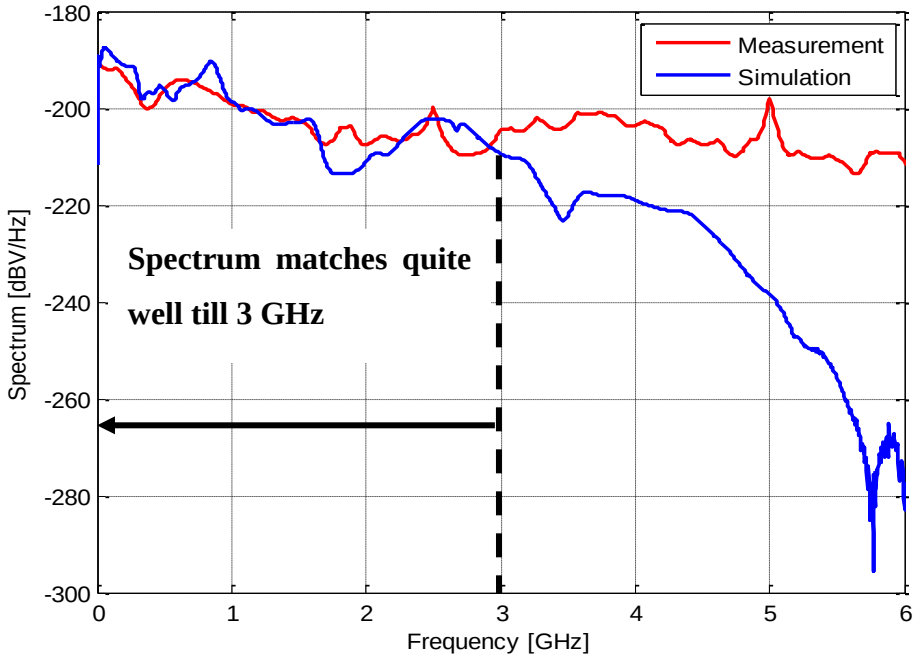

Figure 9.27. Comparison of spectrum of the loop voltage at 40 cm and 270 degree

From comparison of the frequency spectrum of the induced loop voltage we can say that the usable frequency range of the ESD generator model is up to about 3 GHz. Greater precision modeling of the components around the relay structure could provide a better match of the simulated waveform to the measured data.

9.6 CONCLUSION

Based on the geometries of the Noise Ken ESD generator, a full wave model has been proposed to simulate the discharge current and the transient EM field around the ESD generator. To validate the model, measured discharge current and induced loop voltage waveforms and their respective frequency spectrum were compared with the simulated results. On comparing ESD generators from different manufacturers, different transient fields will be measured. Thus, the numerical model must model the specifics of the ESD generator used in system level testing.

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VITA

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