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Design of Shallow Source/Drain Extension (SDE) Profiles in Improving Short-Channel Effect (SCE) in Nanoscale Devices

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***Abstract*—This paper purposed the design of shallow source/drain extension (SDE) in improving short channel effect (SCE) in nanoscale devices. In order to increase the mobility and the speed of the electronic devices, semiconductor technology researchers face the limitations such as short channel effect in MOSFET device as it is unavoidable in scaling. Thus, the aim of this project is to improve the short-channel effect in nanoscale devices. The design parameter standard structure of Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) were proposed referring to the International Technology Roadmap for Semiconductors (ITRS) 2011 edition and compared the structure with same standard structure of ITRS with modification to the junction depth that becomes more shallow source/drain extension (SDE). Silvaco's DEVEDIT software is used to design the structure of MOSFET with three different gate lengths, while Silvaco's ATLAS software is used to simulate the structure for data extraction to obtain the output graph. From the output, it shows that, as the size of MOSFET gate length becomes smaller, the threshold voltages also decrease. In improving the SCE, the value of threshold voltage, V_{th}, is slightly increases on shallower the source/drain extension (SDE). The value of "ON'' current (I_{ON}) also has been extracted for all designs of MOSFET.**

***Index Terms*—Short-Channel Effect (SCE); Shallow Source/Drain Extension (SDE); Nanoscale Devices; Silvaco.**

I. Introduction

For more than 30 years, the Metal - Oxide - Semiconductor Field-Effect Transistor (MOSFET) has continually been scale down in size in channel length from micrometers to sub-micrometers and then to sub-sub-micrometers range following Moore's Law. The channel length of MOSFET is reducing from 100nm to 45nm. The size reduction of the device makes great improvement to MOSFET operation. [1] However, there are many effects when reduction the scale size of the MOSFET. One of the effect is the short-channel effect [2].

Short-channel effect is an effect of the channel length of a MOSFET is the same order of magnitude as the depletion-layer widths of the source and drain junction and also behaves differently from other MOSFETs. There are two physical phenomenon of the short channel effect. The first is the limitation imposed on electron drift characteristics in channel and the second is the modification of the threshold voltage due to the shortening channel length [3]. In this project, the source/drain extension has been selected to be studied. The concept that influence for scaling the shallow source/drain extension (SDE) must be known for improving the short-channel effect. Finally, the design of shallow source/drain extension is proposed.

II. Devices Design and Simulate Process

Development of this project is divided into two stages. The first stage is gathering the information, analyzing and research on short-channel effect (SCE). For this project, the most important part is to design the shallow source/drain extension which is scaling the junction depth of MOSFET. All data and information collected is used when analysis the designs structure on all proposed design parameters were conducted.

For the second stage is designing process of the MOSFET. These designs were constructed by using Silvaco TCAD software. The criterion of all three gate length designs based on the structure of ITRS is proposed as the suitable parameters. The first step in this process is by designing the MOSFET by using the Silvaco's DEVEDIT software. All the dimension sizes are set according to the parameters that will be tested. Then, the base region and the desired impurities are being doped into the structure. For the shallow source/drain extension, the structure is the same as the ITRS structure but only modification is made to the junction depth of source/ drain extension that it becomes shallower. Subsequently, the MOSFET is tested, simulated and executed in the Silvaco's ATLAS software. Here, the desired graphs are plotted by Tonyplot software. From the graphs obtained, threshold voltage (V_{TH}) and "ON" current (I_{ON}) are extracted. Finally, analysis in improving SCE for the design structure was carried out. The standard structure (ITRS) and shallow source/drain extension structure are also compared.

III. Result and Analysis

A. Parameter design

Table 1 shows the parameter for design shallow source/drain extension structure. The Silvaco's DEVEDIT software is used to design the structure by referring to the parameters. The structures MOSFET design is shown in Figure 1-6.

B. Graphs Transfer Curves ID against VGS for Shallow Source/Drain Extension (SDE) Profiles Structure

Figure 7-12 shows the graphs of Transfer Curves ID against V_{GS} for Shallow Source/Drain Extension (SDE) Profiles Structure. From these graphs, we can obtained the

value of threshold voltage, V_{TH} for drain voltage, V_{DS} 0.7V and 50mV for the gate length 24nm, 16nm and 9.8nm.

Table 1
Overall Parameter for Shallow Source/Drain Extension (SDE) Structure with Gate Length 24nm, 16nm and 9.8nm

Parameters	Physical Gate Length		
	24 nm	16 nm	9.8 nm
Power Supply Voltage (V)	0.7	0.61	0.51
Channel Doping (Boron) (10^{18} / cm^3)	3.7	0.1	0.1
Silicon Dioxide (SiO_2) Thickness (nm)	0.9	0.8	0.7
Junction Depth (X_j) (nm)	5.0	4.0	3.0
Base Impurities (Arsenic) (10^{19} / cm^3)	1.0	1.0	1.0
MOSFET Body Dimension (nm)	80 x 20	80 x 20	80 x 20
Source/Drain Electrode Dimension (nm)	15 x 2	15 x 2	15 x 2

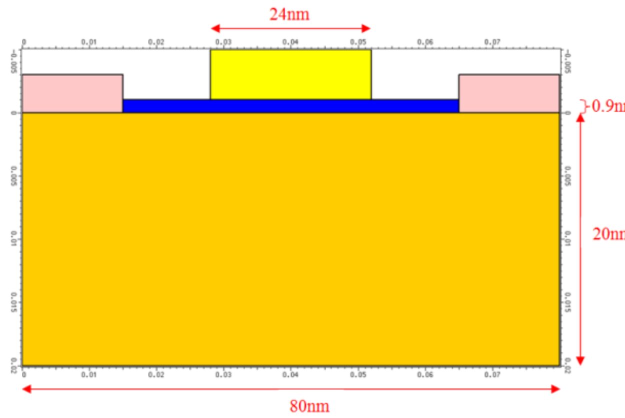

Figure 1: MOSFET design with 24nm gate length

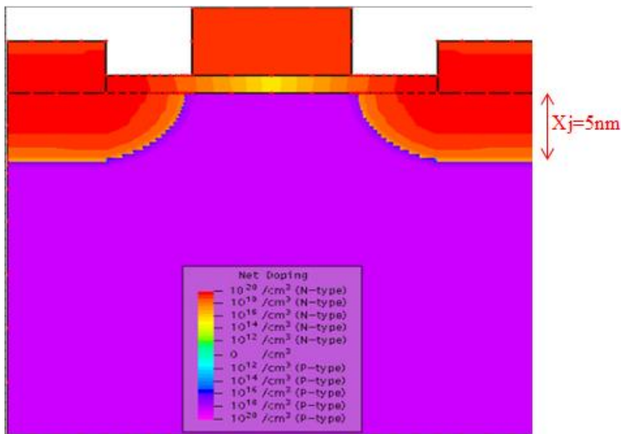

Figure 2: Contour structure with junction depth for 24nm gate length MOSFET design

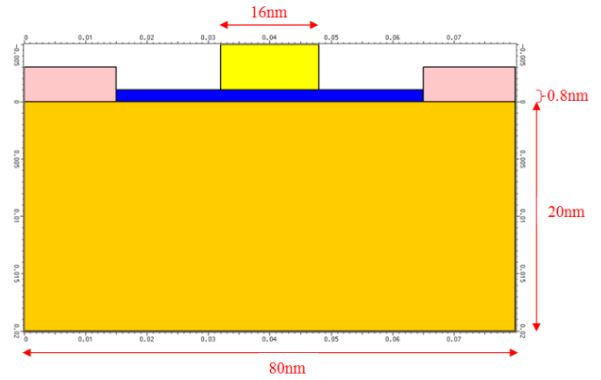

Figure 3: MOSFET design with 16nm gate length

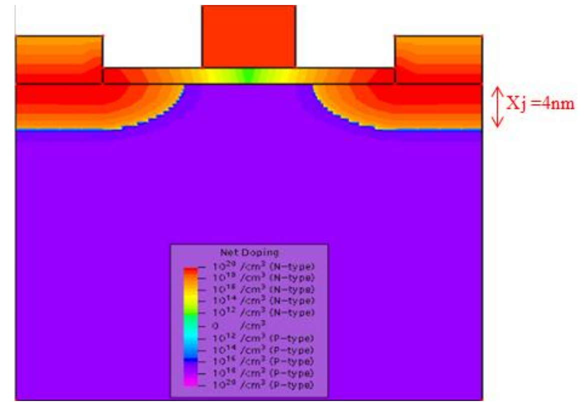

Figure 4: Contour structure with junction depth for 16nm gate length MOSFET design

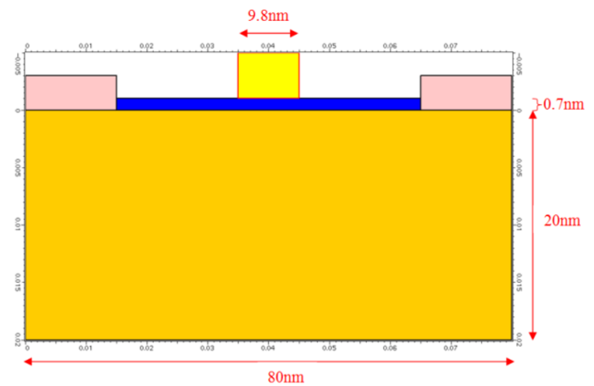

Figure 5: MOSFET design with 9.8nm gate length

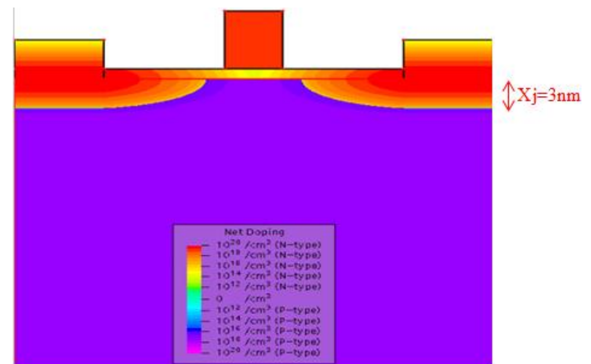

Figure 6: Contour structure with junction depth for 9.8nm gate length MOSFET design

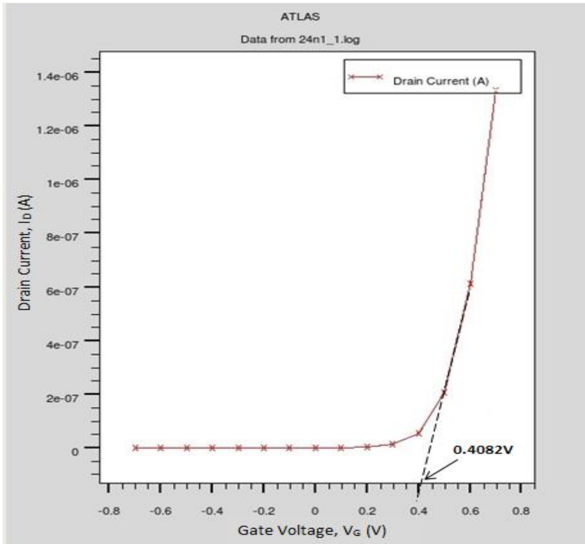

Figure 7: $I_D – V_{GS}$ curves of 0.7V drain voltage for 24nm gate length MOSFET

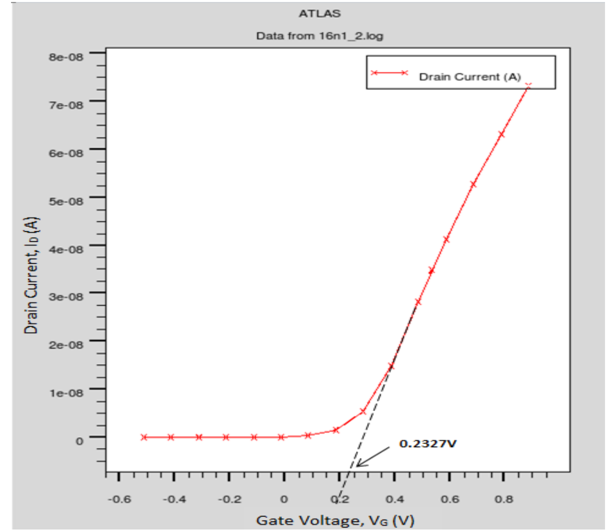

Figure 10: $I_D – V_{GS}$ curves of 50mV drain voltage 16nm gate length MOSFET

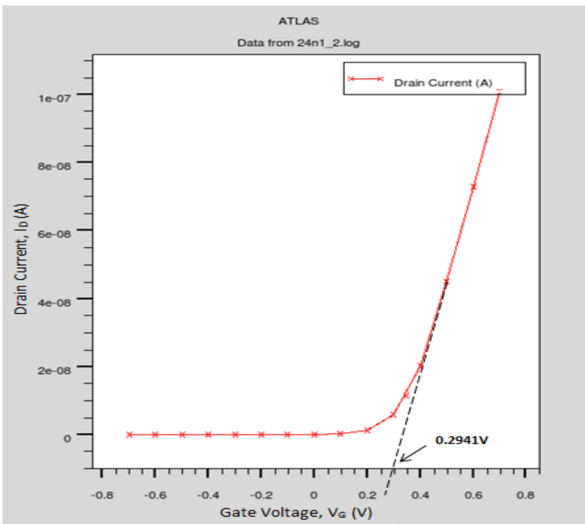

Figure 8: $I_D – V_{GS}$ curves of 50mV drain voltage 24nm gate length MOSFET

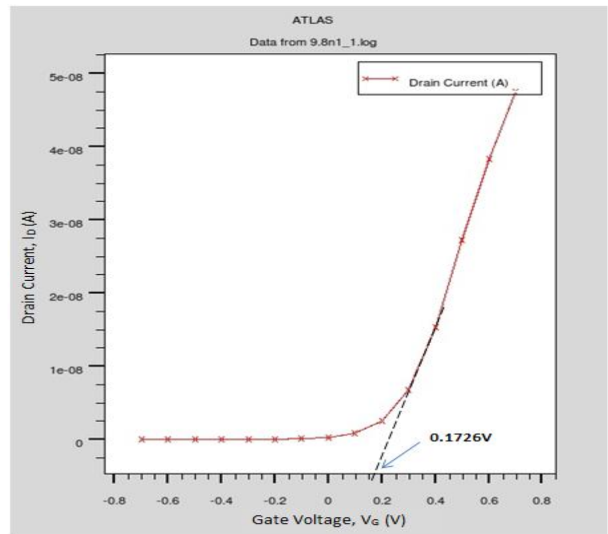

Figure 11: $I_D – V_{GS}$ curves of 0.7V drain voltage 9.8nm gate length MOSFET

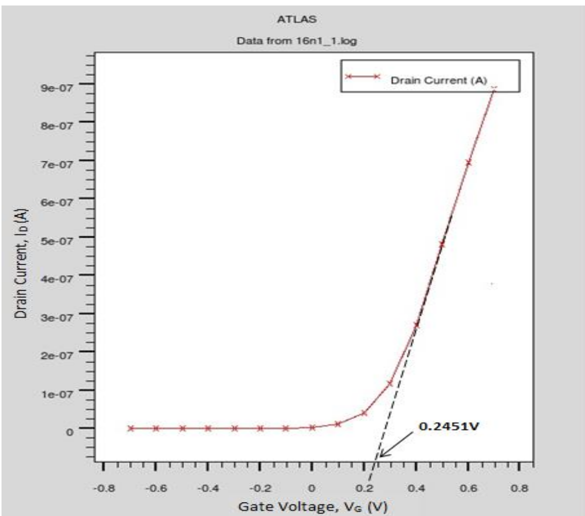

Figure 9: $I_D – V_{GS}$ curves of 0.7V drain voltage for 16nm gate length MOSFET

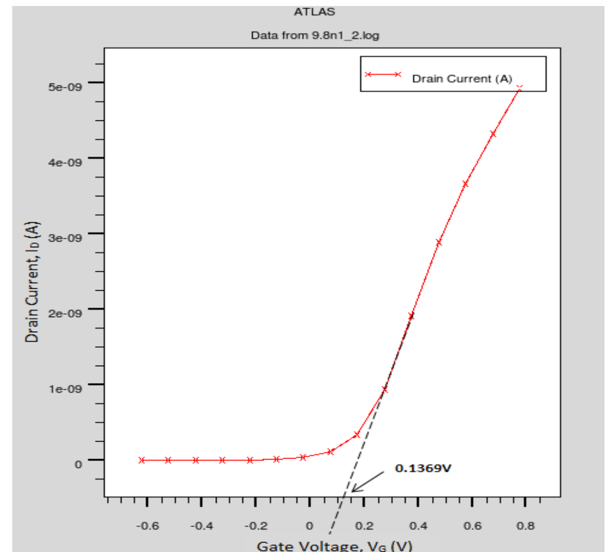

Figure 12: $I_D – V_{GS}$ curves of 50mV drain voltage 9.8nm gate length MOSFET

C. Graphs Subthreshold Curves Log ID against VGS with 50mV and 0.7V drain voltages for Source/Drain Extension (SDE) Profiles Structure

Figure 13-15 shows the graph of Subthreshold Curves Log I_D against V_{GS} with 50mV and 0.7V drain voltages for Source/Drain Extension (SDE) Profiles Structure. From these graphs, we can get the value of "ON" current, I_{ON} for drain voltage, V_{DS} 0.7V and 50mV with the gate length 24nm, 16nm and 9.8nm.

D. Comparison of the V_{TH} value between three Gate Lengths for Standard Structure (ITRS) with Shallow Source/Drain Extension (SDE) Profiles

For the shallow source/drain extension (SDE) profiles structure from DEVEDIT, the Figure 16 shows that the value of V_{TH} is increases from the standard structure (ITRS). When the short-channel effect reduces, the value of the V_{TH} will increase. In theory, the shorter the length gate, the value of the V_{TH} becomes lower [6]. Analysis for the V_{TH} shows that when the junction depth of SDE MOSFET becomes shallower, the V_{TH} increases. For V_{DS} = 0.7V, it was found that the V_{TH} increases by 40.08% when the junction depth, X_j reduces from 9nm to 5nm for gate length 24nm. For gate length 16nm, the V_{TH} increases by 80.49% when the junction depth, X_j reduces from 6nm to 4nm, while V_{TH} increases by 65.48% when the junction depth, X_j reduces from 3.7nm to 3nm for length gate 9.8nm.

Meanwhile, for V_{DS} = 50mV, it was found that the V_{TH} increases by 52.54% when the junction depth, X_j reduces from 9nm to 5nm for gate length 24nm. For gate length 16nm, the V_{TH} increases by 114.08% when the junction depth, X_j reduces from 6nm to 4nm, while V_{TH} increases by 36.49% when the junction depth, X_j reduces from 3.7nm to 3nm for length gate 9.8nm.

All the shallow source/drain extension structure MOSFET shows increases value of V_{TH}. Thus, the scaling the junction depth solved and improved the short-channel effect.

E. Overall Outputs

Table 2 shows the results for the overall output from the graph for V_D=0.7V and 50mV at the gate length 24nm, 16nm and 9.8nm before reducing the junction depth, X_j which are 9nm, 6nm and 3.7nm. The measurement output including the threshold voltage, V_{TH} and maximum current, I_{ON} from the graph.

Figure 18 shows the results for the overall output from the graph for V_D=0.7V and 50mV at the gate length 24nm, 16nm and 9.8nm after reduce the junction depth, X_j. The measurement output including the threshold voltage, V_{TH} and maximum current, I_{ON} from the graph.

IV. CONCLUSION

After finishing the studies, this project can be concluded that the design shallow source/drain extension (SDE) profiles is one of the alternatives in improving short channel effect. The element in designing shallow source/drain extension (SDE) profiles is decreasing the scale of junction depth, X_j from the standard structure (ITRS) NMOS transistor. This scaling modification also improves the performance on the NMOS transistor in nanoscale devices by having lower power consumption

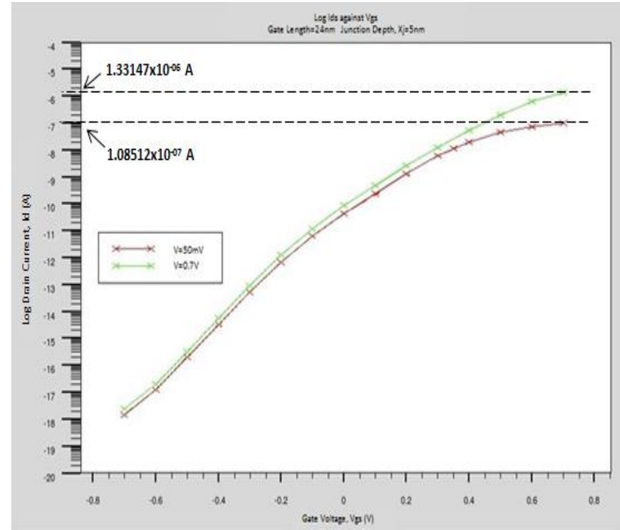

Figure 13: Log I_D – V_{GS} subthreshold curves with 50mV and 0.7V drain voltage for 24nm gate length MOSFET

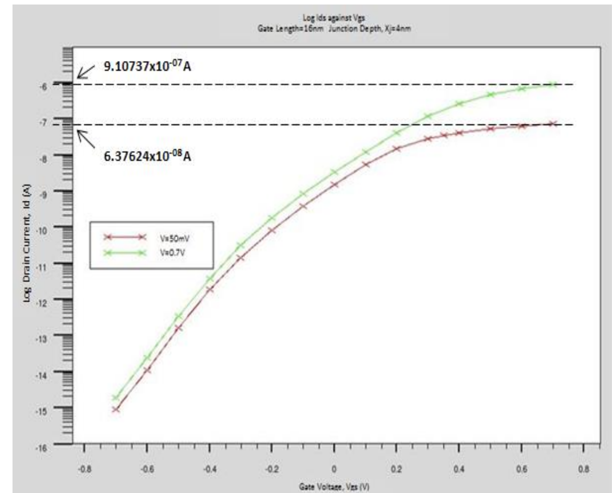

Figure 14: Log I_D – V_{GS} subthreshold curves with 50mV and 0.7V drain voltage for 16nm gate length MOSFET

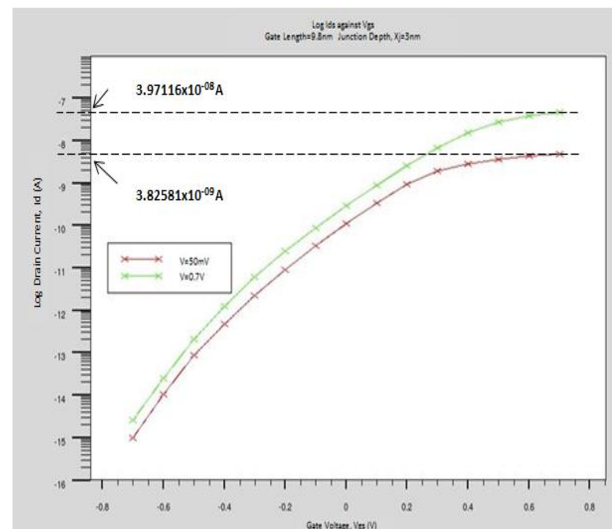

Figure 15: Log I_D – V_{GS} subthreshold curves with 50mV and 0.7V drain voltage for 9.8nm gate length MOSFET

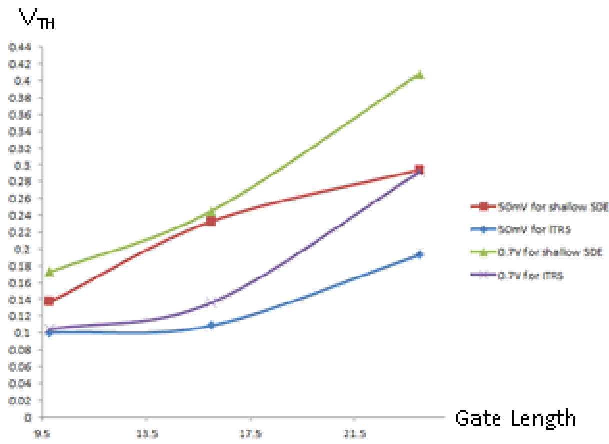

Figure 16: Graph Gate length, L_G against V_{TH} for standard structure (ITRS) and source/drain extension (SDE) profiles structure and standard structure (ITRS)

Table 2
Overall Output Data for Source/Drain Extension (SDE) Profiles Structure Before Reducing the Junction Depth

	V_{DS}	Gate Length 24nm	16nm	9.8nm
Threshold Voltage, V_{TH} (V)	0.7 V	0.2914	0.1358	0.1043
	50 mV	0.1928	0.1087	0.1003
Maximum Current, I_{ON} (A)	0.7 V	9.39024×10^{-5}	2.09029×10^{-6}	3.61309×10^{-7}
	50 mV	9.87347×10^{-6}	1.71038×10^{-7}	4.27614×10^{-8}

Table 3
Overall Output Data for Source/Drain Extension (SDE) Profiles Structure After Reducing the Junction Depth

	V_{DS}	Gate Length 24nm	16nm	9.8nm
Threshold Voltage, V_{TH} (V)	0.7 V	0.4082	0.2451	0.1726
	50 mV	0.2941	0.2327	0.1369
Maximum Current, I_{ON} (A)	0.7 V	1.33147×10^{-6}	9.10737×10^{-7}	3.9711×10^{-8}
	50 mV	1.08512×10^{-7}	6.37642×10^{-8}	3.82581×10^{-9}

The shallow source/drain extension (SDE) profiles have been designed virtually using TCAD Silvaco software. DEVEDIT in Silvaco software is used in this project to design the NMOS transistor and scaling the junction depth, X_j for shallow source/drain extension profiles. Besides, the ATLAS in Silvaco software is used to simulate the structure of design to obtain the outputs and graphs. Based on the simulation analysis, the threshold voltage, V_{TH} for shallow source/drain extension profiles slightly increase from the standard structure (ITRS) gate length 9.8nm, 16nm and 24nm when drain voltage is 50mV and 0.7V. The I_{ON} of both structure have a different values. I_{ON} shows the active region for the transistor. In theory, for shorter gate length, L_G, the threshold voltage, V_{TH} will decrease. The value of the V_{TH} from the output proved that the shallow source/drain extension profiles improve the short-channel effect.

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