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Computation of power plane pair inductance, measurement of multiple switching current components and switching current measurement for multiple ICs with an island structure

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COMPUTATION OF POWER PLANE PAIR INDUCTANCE, MEASUREMENT OF MULTIPLE SWITCHING CURRENT COMPONENTS AND SWITCHING CURRENT MEASUREMENT FOR MULTIPLE ICs WITH AN ISLAND STRUCTURE

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ABSTRACT

The first part of the thesis presents the computation of power / ground plane pair inductance based on Partial Element Equivalent Circuit (PEEC) method in power distribution network (PDN) design. An efficient approach for the inductance computation is investigated. Speed-up techniques are employed include using the faster decay of mutual coupling due to the "differential" currents (same magnitude but opposite directions) in the two planes. Also, an approximate rectangular mesh reduction method is introduced which allows a local increase in mesh density.

The second part presents a measurement-based data-processing approach to obtain parameters of multiple current components through a bulk decoupling capacitor for power integrity studies. A lab-made low-cost current probe is developed to measure the induced voltage due to the time-varying switching current. Then, a post data-processing procedure is introduced to separate and obtain the parameters of multiple current components.

The third part proposes a measurement methodology, when IC information is not available, to obtain the equivalent switching current of each IC in the case where multiple ICs are connected to a common power island structure. Time-domain oscilloscope measurements are used to capture the noise-voltage waveforms at a few locations in the power island. Combining with the multi-port frequency-domain S-parameter measurement among the same locations, an equivalent switching current for each IC is calculated. The proposed method is validated at a different location in the power island by comparing the calculated noise voltage using the equivalent switching currents as excitations with the actual measured noise voltage.

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1. INTRODUCTION

A power distribution network (PDN) is used to deliver power to the core logic and input / output (I / O) circuits on multilayer printed circuit boards (PCBs). Nowadays, the internal clock frequency of modern electronic devices has been more than several GHz, and the switching current is up to tens of amperes. With silicon technology going to nanometer feature dimension, the increasing number of I/Os in simultaneous transmission demand significant amount of transient current in PDN. With faster switching speed, higher circuit density, lower supply voltages and smaller feature size in integrated circuits (ICs) design, the voltage noise become a serious issue, affecting power and signal integrity (PI & SI) as well as causing electromagnetic interference (EMI) problems in high – speed electronic devices.

It is well known that the power / ground (PWR / GND) noise should be sufficiently suppressed, such as simultaneous switching noise (SSN) which is one of the main sources for many SI, PI and EMI issues. Decoupling capacitors in PWR and GND planes are widely used to stabilize the supply voltage levels in multilayer packages and PCB structures by supplying the charge needed for the switching current. However, the parasitic inductances due to the current loop in the power delivery and return path impede the current supplied to the chip, limiting the effectiveness of the decoupling capacitors to rapidly provide charge. Therefore, quantifying the parasitic inductance of PWR and GND planes is critical for problems associated with PDN design. Full-wave simulation methods have been used to model the PWR / GND layer pair to determine the impedance of the PDN, including the parasitic inductance. However, the full-wave methods may require long compute time and huge memory resources. An efficient approach based on partial element equivalent circuit (PEEC) is proposed for fast impedance calculation of parallel planes.

To evaluate the performance of a PDN, target impedance is a widely used guideline for PDN design. It is a reverse problem of PDN noise analysis to establish the target impedance specification for PDN design. In PDN noise analysis, the maximum noise voltage induced by IC switching currents can be simulated or calculated using an appropriate PDN model and switching currents. Conversely, target impedance for PDN design is obtained from the knowledge of switching currents and the maximum PDN

noise tolerance. Therefore, the waveform of IC switching currents in time domain is necessary to develop the target impedance. In some real-world hardware measurements, it is found that multiple current components could exist in the time-varying current flowing through a decoupling capacitor. Further, when the current through a bulk decoupling capacitor is of interest, it needs to be measured at the frequencies as low as a few hundred KHz. A lab-made low-cost current probe is developed with very small in size, suitable for dense-PCB applications and sensitive enough for low-frequency measurements. A post data-processing procedure is developed to separate the effects of different current components, and to obtain the parameters important for target impedance.

In some PDN designs, there are multiple ICs sharing a common power island structure. When detailed IC information is available, chip-level modeling is an effective way to obtain the switching current information. However, IC information is proprietary and usually unavailable for most PCB designers. A measurement-based method is developed to handle the situation where multiple ICs share a common power island and IC information is not available. The measured time-domain noise-voltage waveforms are converted into the frequency domain through the Fourier transform. Together with the S-parameter measurement of the multi-port power-island structure, equivalent switching currents including both magnitude and phase are obtained, which is important for optimized PDN design (such as target impedance).

PAPER I ACCURATE AND EFFICIENT COMPUTATION OF POWER PLANE PAIR INDUCTANCE

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ABSTRACT

Computation of power-plane inductance for multiple ports is an important part of power distribution network (PDN) design. In this paper, we present an efficient approach for the inductance computation. Since this PEEC approach is based on partial inductance computations, vias and other discontinuities can be accurately taken into account. Speed-up techniques are employed like the faster decay of mutual coupling due to the "differential" currents (same magnitude but opposite directions) in the two planes. Also, an approximate rectangular mesh reduction method is introduced which allows a local increase in mesh density.

1. INTRODUCTION

The internal clock frequency and input-output (IO) speed in modern high speed digital devices increase dramatically, and the current density becomes higher, which results in increased current demand from the PDN of the board. When numerous logic gates and buffers inside integrated circuits (ICs) switch simultaneously, they induce significant voltage drops or ripples in the PDN, resulting in critical power integrity issues and electromagnetic (EM) interference problems [1]. The power noise in the supply voltage can further couple to the signal traces transitioning through the power and reference (often denoted as “ground”) planes and result in signal integrity problems [2]. On-chip and off-chip decoupling capacitors are used to provide the needed charge for the switching current. Within the frequency range from megahertz to hundreds of megahertz, the off-chip decoupling capacitors in the power and ground planes are widely used to make the supply voltage stable in the printed circuit board (PCB) by achieving low power supply impedance [3]. However, the parasitic inductances due to the current loop in the power delivery and return path impede the current supplied to the chip, limiting the effectiveness of the decoupling capacitors to rapidly provide charge. Therefore, quantifying the parasitic inductance of the power and ground planes is critical for the problems associated with PDN design.

Many techniques are available today to determine the PDN impedance, including the parasitic inductance between power and ground planes. Full-wave electromagnetic modeling methods have been widely used to model the power/ground layer pair problem, such as finite-difference time domain (FDTD) [4], the finite-element method (FEM) [5] and the method of moments (MOM) [6]. However, full-wave methods require significant computing time and resources for complicated hierarchical PDN structures. Other approaches such as transmission-line methods [7] and the resonant cavity model [8] are usually much faster than full-wave numerical methods and can be easily included into circuit simulations, but the accurate computation of the inductances for power/ground plane pair with multiple decoupling capacitor placements can still be very time consuming.

In this paper, an efficient Plane Pair PEEC (PPP) approach is proposed. The decoupling capacitors can be modeled by single-lumped inductance macromodels assuming that the capacitive impedance is small at the frequencies of interest. The portions of the inductances associated with the parallel planes are calculated using the proposed PPP approach, and the remaining portions associated with the package of the capacitors, bonding pads and vias can be easily added with very little extra computation time.

In the PPP approach, the inductive coupling between different cells decays very fast, which is used to obtain a sparsification of the partial mutual inductance evaluation. Speed-up techniques are employed to save the computational time and memory usage. Both uniform and non-uniform mesh methods were investigated and validated. Our model is flexible to choose ports and change decoupling capacitor locations. Change of the plane pair inductance due to the change of decoupling capacitor locations can be easily calculated which provides useful guidelines for PDN designs.

2. THEORY AND FORMULATION

2.1. CONCEPTS OF PARTIAL INDUCTANCE

The definition of the inductance for a system of *N* loops is given as,

$$L_{ij} = \frac{\psi_{ij}}{I_j} \text{ for } I_k = 0 \text{ if } k \neq j \tag{1}$$

where ψ_{ij} is the magnetic flux in loop *i* due to the current I_j in loop *j*. The magnetic vector potential $\vec{A}$ at any observation point $\vec{r}$ generated by the current I_j is [9],

$$\vec{A} = \frac{\mu}{4\pi}\frac{I_j}{a_j}\oint_j \int_{a_j} \frac{d\vec{l}_j da_j}{r} \tag{2}$$

where $r = |\vec{r} - \vec{r}_j|$, $d\vec{l}_j$ is the element of conductor *j* with the direction along the axis of the conductor and a_j is the conductor cross section perpendicular to the current flow. A uniform current density is assumed in conductor *j* with a constant cross section a_j along the loop. The average magnetic flux ψ_{ij} in loop *i* can be related to the vector potential $\vec{A}_j$ as,

$$\psi_{ij} = \frac{1}{a_i}\oint_i \int_{a_i} \vec{A}_j \cdot d\vec{l}_i da_i \tag{3}$$

where a_i represents the constant cross section of conductor *i*. The mutual inductance for the loops *i* and *j* can be expressed as [9].

$$L_{ij} = \frac{1}{a_i a_j}\frac{\mu}{4\pi}\oint_i \int_{a_i} \oint_j \int_{a_j} \frac{d\vec{l}_i \cdot d\vec{l}_j}{r_{ij}} da_i da_j \tag{4}$$

Relations for the inductance between the parts of circuits can be further developed from Eq. (4). The integrations over the lengths can be expressed as summations over the straight loop segments and all segments are allowed to have a different cross section as show in Eq. (5) [9],

$$L_{ij} = \sum_{k=1}^{K}\sum_{m=1}^{M} \frac{\mu}{4\pi}\frac{1}{a_k a_m}\int_{a_k}\int_{a_m}\int_{b_k}^{c_k}\int_{b_m}^{c_m}\frac{d\vec{l}_k \cdot d\vec{l}_m}{r_{km}} da_k da_m \tag{5}$$

where the *i*th loop is divided into *K* segments while *j*th loop is consist of *M* segments. The starting points b_k, b_m and the ending points c_k, c_m are the limits in the integrals.

Partial inductance is defined as the argument of the double summation in Eq. (6) for the conductor segments as [9],

$$Lp_{km} = \frac{\mu}{4\pi}\frac{1}{a_k a_m}\int_{a_k}\int_{a_m}\int_{b_k}^{c_k}\int_{b_m}^{c_m}\frac{|d\vec{l}_k \cdot d\vec{l}_m|}{r_{km}} da_k da_m \,. \tag{6}$$

The sign of Lp_{km} is accounted for by a factor S_{km} as Eq. (7),

$$Lp_{ij} = \sum_{k=1}^{K}\sum_{m=1}^{M} S_{km} Lp_{km} \,. \tag{7}$$

S_{km} represents the sign (±1) associated with the particular partial inductance, which is positive by definition. S_{km} depends on the direction of current flow in the conductors.

Partial self-inductance is evaluated from the definition of partial inductance in Eq. (6), where integration *i* and integration *j* are both over the same conductor,

$$Lp_{ii} = \frac{\mu}{4\pi}\frac{1}{a_i a_{i'}}\int_{a_i}\int_{a_{i'}}\int_0^{l}\int_0^{l'}\frac{|d\vec{l}_i \cdot d\vec{l}_{i'}|}{r_{ii'}} da_i da_{i'} \,. \tag{8}$$

2.2. PEEC METHOD

The Partial Element Equivalent Circuit (PEEC) was developed by A. Ruehli in the 1970s and 1980s [10]. The PEEC method is used for numerical modeling of electromagnetic (EM) problems. It models electric-field interactions as capacitances and magnetic-field interactions as inductances. Using the PEEC method, problem under study is transferred from the EM domain to the circuit domain where the conventional SPICE-like circuit solvers can be employed to analyze the equivalent circuit. By applying the PEEC method, all electrical components e.g. passive components, sources, non-linear elements, ground, etc. can be easily integrated together. Moreover, by using the PEEC method it is easy to separate the resistive, capacitive or inductive effects.

To apply the PEEC method, all of the conductors in the problem must first be subdivided into N canonical primitive structures, such as rectangular bars, for which formulas for resistance, partial self-inductances, and partial mutual-inductances are known. For example, Figure 2.1 shows an interconnect with two signal traces and a plane return path. The conductors are subdivided to rectangular bars. The small, generically shaped conductors in Figure 2.1 are called branches. The resistances and inductances are then assembled into a complete circuit and solved with a circuit simulator. The accuracy improves with finer-grained subdivision of the original geometry [11].

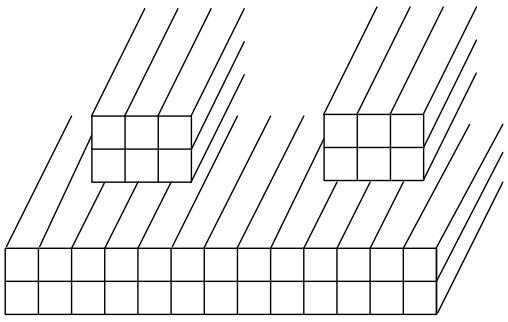


Figure 2.1. Division of conductors into segments.

Assume the current is uniform across the cross section of the branches. Then relatively simple DC resistance and static inductance formulas are applicable. The resistance and partial self-inductance of each branch is computed along with the partial

mutual-inductance between each pair of branches. Assemble the results into a diagonal $N \times N$ resistance matrix and an $N \times N$ partial inductance matrix. The voltage drops across the branches are,

$$\bar{V}_b = (\bar{\bar{R}} + j\omega\bar{\bar{L}})\bar{I}_b = \bar{\bar{Z}}_p \bar{I}_b \tag{9}$$

where $\bar{I}_b$ are the branch currents.

2.3. MODIFIED NODAL ANALYSIS (MNA)

The branches are connected together at a number of nodes. The number of the nodes, *M*, depends on the subdivision used. By satisfying Kirchhoff's voltage (KVL) and current laws (KCL), a dedicated solver for the PEEC method can be constructed.

Each branch voltage is defined by the difference of the two node voltages at the ends of the branch. It can be shown,

$$\bar{V}_b = \bar{\bar{A}}\bar{V}_n \tag{10}$$

where $\bar{\bar{A}}$ is the incident matrix, and stores all of the connection information in an $N \times M$ matrix, where *N* is the number of the branches. $\bar{\bar{A}}$ is constructed by setting $A_{bi} = 1$ and $A_{bj} = -1$ when the current flows from node *i* to node *j* through branch *b*.

The total currents into the nodes are given by,

$$\bar{I}_n = \bar{\bar{A}}^T \bar{I}_b \tag{11}$$

where $\bar{I}_n$ are the currents driven into the nodes by external sources, and $\bar{I}_b$ are the branch currents. In general, most of the $\bar{I}_n$ are zero since current is externally supplied only at the ports.

The Modified Nodal Analysis (MNA) is easy to implement algorithmically on a computer which is a substantial advantage for automated solution. There are two main aspects to be considered when choosing algorithms: accuracy and speed. The MNA has been proved to accomplish these.

The MNA applied to a circuit with passive elements, independent current and voltage sources and active elements results in a matrix equation of the form,

$$[A][x]=[z]. \tag{12}$$

For a circuit with M nodes and N independent voltage sources (branches), the A matrix is $(N+M) \times (N+M)$ in size, and consists only of known quantities. The A matrix is developed as the combination of 4 smaller matrices, B, C, D and G,

$$A=\begin{bmatrix} B & D \\ C & G \end{bmatrix}. \tag{13}$$

The B matrix is $N \times N$ in size and is zero if only independent sources are considered. The C matrix is $N \times M$ in size with only 0, 1 and -1 elements and is determined by the connection of the voltage sources (branches). The D matrix is $M \times N$ in size and is equal to the transposed C matrix. The G matrix is $M \times M$ in size and is determined by the interconnections between the circuit elements.

The x vector is $(N + M) \times 1$ in size, which holds the unknown quantities and is developed as the combination of two smaller vectors, v and i,

$$x=\begin{bmatrix} v \\ i \end{bmatrix}. \tag{14}$$

The v vector is $M \times 1$ in size and holds the unknown voltages. The i vector is $N \times 1$ in size and holds the unknown currents through the voltage sources (branches).

The z vector is also *(N + M)* × 1 in size, which is developed as the combination of two smaller vectors *p* and *q*,

$$z = \begin{bmatrix} p \\ q \end{bmatrix}. \tag{15}$$

The *p* vector is *M* ×1 in size with each element of the vector corresponding to a particular node. The value of each element of *p* is determined by the sum of current sources into the corresponding node. If there are no current sources connected to the node, the value is zero. The *q* vector is *N* × 1 in size with each element of the vector equal to the corresponding independent voltage source. If there is no independent voltage source, the value is zero.

2.4. THE PPP APPROACH

In the power distribution network of a multilayer printed circuit board, the inductance formed by two parallel planes and IC/decoupling capacitor vias (Figure 2.2) can be separated into two parts: the vertical via barrel inductance and plane pair inductance due to the changes of the horizontal plane current distribution adjacent to the vias (Figure 2.3).

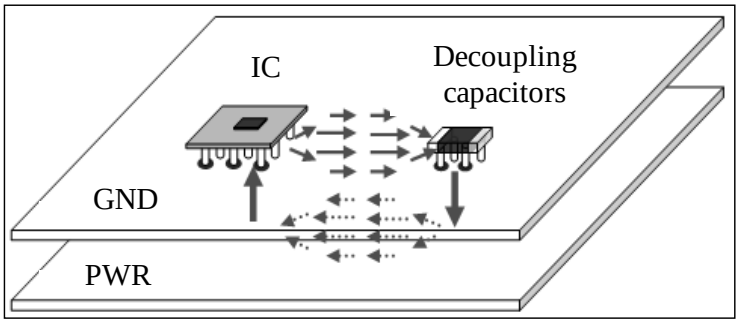


Figure 2.2. Power/Ground plane pair with IC and decoupling capacitors.

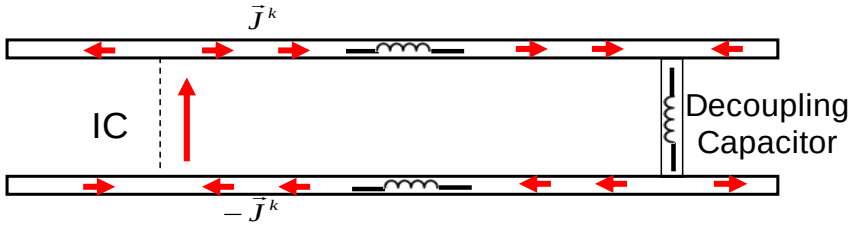


Figure 2.3. Current distribution on power and ground planes.

The power and ground planes are subdivided into commensurate cells using conventional PEEC meshing method [12] as shown in Figure 2.4. Non-orthogonal cells are avoided with rectangular mesh size, which makes coupling terms minimal. For example, Figure 2.4 shows a 4 × 4 plane subdivided into 16 squares with 1× 1 size. The currents flowing on the plane are divided into the *x* and *y* directions. Thus, the plane is also subdivided into cells in the *x* and *y* directions, respectively. The width of the cells on the edges is half of the cells inside so that by connecting the nodes in Figure 2.4, the equivalent circuit using partial inductances can be created as shown in Figure 2.5. This allows the subdivided plane sections to be connected in a systematic way. The same subdivisions are applied for both power and ground planes to make them symmetric.

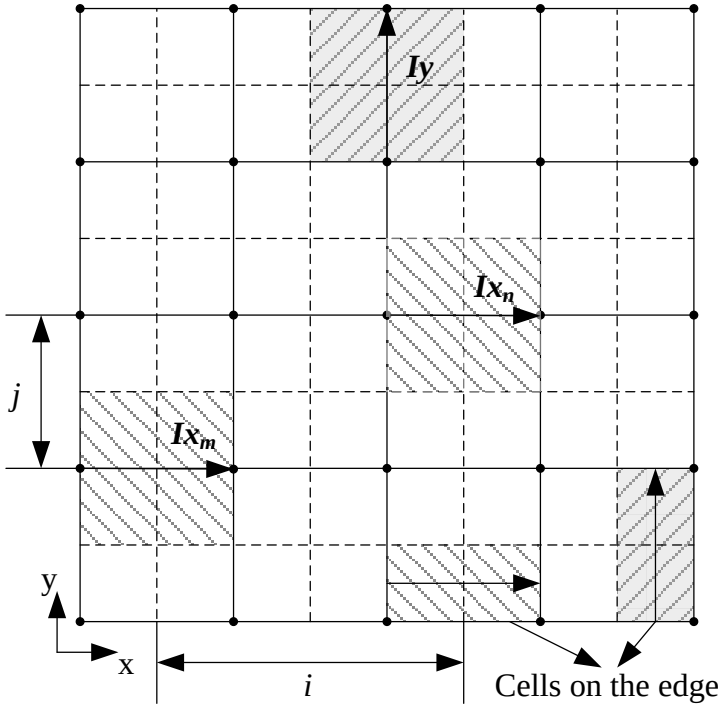


Figure 2.4. Plane subdivision

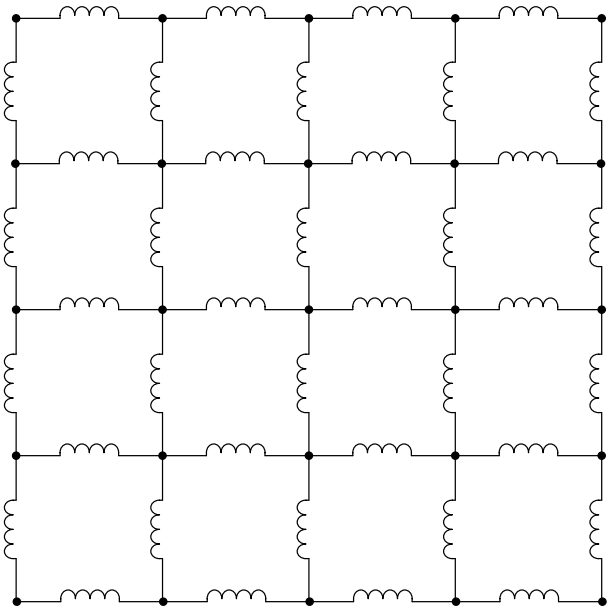


Figure 2.5. Partial inductance evaluation.

The closed-form formulation for mutual inductance between two parallel thin conductors as shown in Figure 2.6 is given in Eq. (16), which is called the thin tape – tape (TT) algorithm [9].

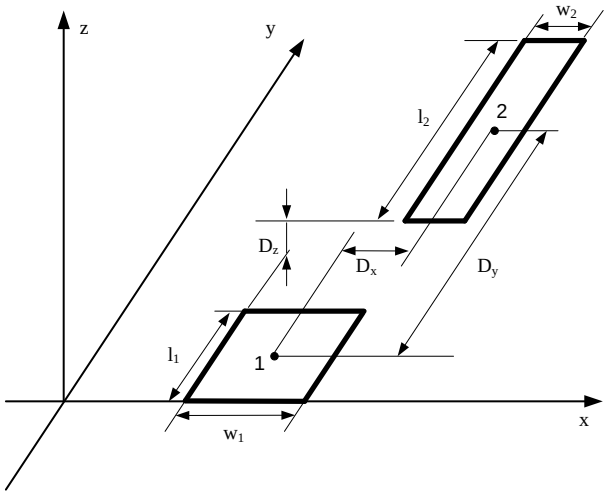


Figure 2.6. Two parallel thin conductors

$$
\begin{aligned}
L_{p12} &= \frac{\mu}{4\pi}\frac{1}{w_1 w_2}\sum_{i=1}^{4}\sum_{j=1}^{4}(-1)^{i+j}\Big[\frac{b_j^2 - D_z^2}{2}a_i \ln(a_i+\rho) + \frac{a_i^2 - D_z^2}{2}b_j \ln(b_j+\rho) \\
&\quad - \frac{1}{6}(b_j^2 - 2D_z^2 + a_i^2)\rho - b_j D_z a_i \tan^{-1}\frac{a_i b_j}{\rho D_z}\Big] \\
\rho &= (a_i^2 + b_j^2 + D_z^2)^{\frac{1}{2}} \\
a_1 &= D_x - \frac{l_1}{2} - \frac{l_2}{2},\ a_2 = D_x + \frac{l_1}{2} - \frac{l_2}{2} \\
a_3 &= D_x + \frac{l_1}{2} + \frac{l_2}{2},\ a_4 = D_x - \frac{l_1}{2} + \frac{l_2}{2} \\
b_1 &= D_y - \frac{w_1}{2} - \frac{w_2}{2},\ b_2 = D_y + \frac{w_1}{2} - \frac{w_2}{2} \\
b_3 &= D_y + \frac{w_1}{2} + \frac{w_2}{2},\ b_4 = D_y - \frac{w_1}{2} + \frac{w_2}{2}
\end{aligned}
\tag{16}
$$

For power/ground plane pair with opposing currents, two cells located on the top and bottom planes with the same *x* and *y* coordinates can be united to a cell pair called "section" [12] as shown in Figure 2.7. Due to the cancelling effect of the opposing currents in a cell pair (Figure 2.8), the inductive coupling between sections decays much faster with increasing distance [13].

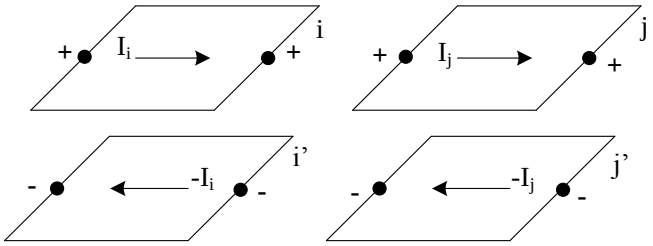


Figure 2.7. *i-th* and *j-th* section

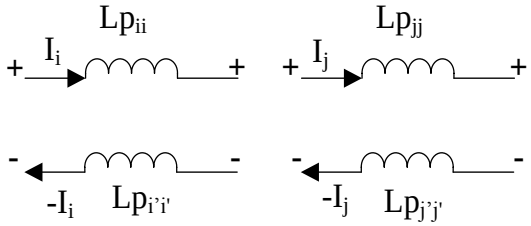


Figure 2.8. The corresponding equivalent circuit of *i-th* and *j-th* section

It has been shown that the mutual inductance between the *i-th* section and *j-th* section, Ls_{ij} can be expressed with the partial-mutual inductances of the cells, in which symmetry of the cells is applied to reduce by a factor of two in the number of the partial inductance evaluations [12]. Briefly, the voltage drop in the *i-th* section caused by the current in the *j-th* section can be expressed as,

$$Vs_i = sI_j(Lp_{ij} - Lp_{ij'} + Lp_{i'j'} - Lp_{i'j}) \quad (17)$$

Because of the symmetry of the cells, we have $Lp_{ij} = Lp_{i'j'}$ and $Lp_{ij'} = Lp_{i'j}$. The partial-mutual inductance between the *i-th* section and the *j-th* section can be expressed as,

$$Ls_{ij} = \frac{Vs_i}{sI_j} = 2(Lp_{ij} - Lp_{ij'}) \quad . \tag{18}$$

Similarly, the partial-self inductance of the *i-th* section can be expressed as,

$$Ls_{ii} = 2(Lp_{ii} - Lp_{ii'}) \quad . \tag{19}$$

The orthogonal cells are used in the PPP approach, which reduces the coupling a lot since only the coupling in the *x* direction or the *y* direction will be calculated. Non-orthogonal mesh can result in the mutual coupling between the *x* and *y* directed cells which is costly in computation.

A special case for the inductance of thin filamentary circuits *i* and *j* is given by the Neumann formula [9],

$$Lp_{ij} = \frac{\mu}{4\pi} \int_i \int_j \frac{d\vec{l}_i \cdot d\vec{l}_j}{r_{ij}} . \tag{20}$$

When the distance between two cells, r_{ij} is sufficiently large, the partial-mutual inductance between two cells can be approximated as,

$$Lp_{ij} = \frac{\mu}{4\pi} \frac{l_i l_j}{r_{ij}} \quad . \tag{21}$$

Define $q = h / r_{ij}$, where h is the plane to plane spacing, and r_{ij} is the distance between two sections. When the distance r_{ij} between two sections >> the size of the sections, the partial-mutual inductance between the sections shown in Figure 2.7 can be approximated as,

$$Ls_{ij} = 2(Lp_{ij} - Lp_{ij'}) = 0.2\Delta x\Delta x(1/r_{ij} - 1/r_{ij'}),\ \mu\text{H} \tag{22}$$

where $r_{ij'} = \sqrt{r_{ij}^2 + h^2} = r_{ij}\sqrt{1+q^2}$. The square root can be expanded in a Taylor series as,

$$\frac{1}{\sqrt{1+q^2}} = 1 - \frac{q^2}{2} + \frac{q^4}{8} - \ldots \tag{23}$$

.

When $q << 1$, $\frac{1}{\sqrt{1+q^2}} \cong 1 - \frac{q^2}{2}$. Eq. (22) can be expressed as,

$$Ls_{ij} = 0.1\Delta x\Delta x q^2 / r_{ij},\ \mu\text{H} \tag{24}$$

where $r_{ij} = \sqrt{(i\Delta x)^2 + (j\Delta y)^2}$ (Figure 2.4). For uniform mesh subdivision, the cell is square with $\Delta x = \Delta y$, and Eq. (24) can be written as Eq. (25). Thus, the coupling between sections decays very fast, which is proportional to $(1/r_{ij})^2$.

$$Ls_{ij} = 0.1\Delta x q^2 / \sqrt{i^2 + j^2},\ \mu\text{H} \tag{25}$$

Applying the approximation formula can speed up calculation of the mutual inductance coupling between sections, which is related to the section length, distance between sections and the plane pair spacing only. The relative error of the mutual inductance between sections obtained by the original closed-form expression and the approximation formula is given by Eq. (26).

$$err = \frac{|\, Ls_{ij} - Ls_{ij(apprx)} \,|}{Ls_{ij}} \times 100\% \tag{26}$$

To find out the criteria for the application of the approximation formula, the defined error was set as 3% to achieve enough accuracy. Different plane pair spacing was applied. Here we show an example of 0.5mm × 0.5mm cell size and 0.2mm plane spacing. The partial-mutual inductance between two sections with various distances is calculated using the closed-form expression and the approximation formula, and the results are shown in Figure 2.9. The relative error calculated by Eq. (26) is shown in Figure 2.10.

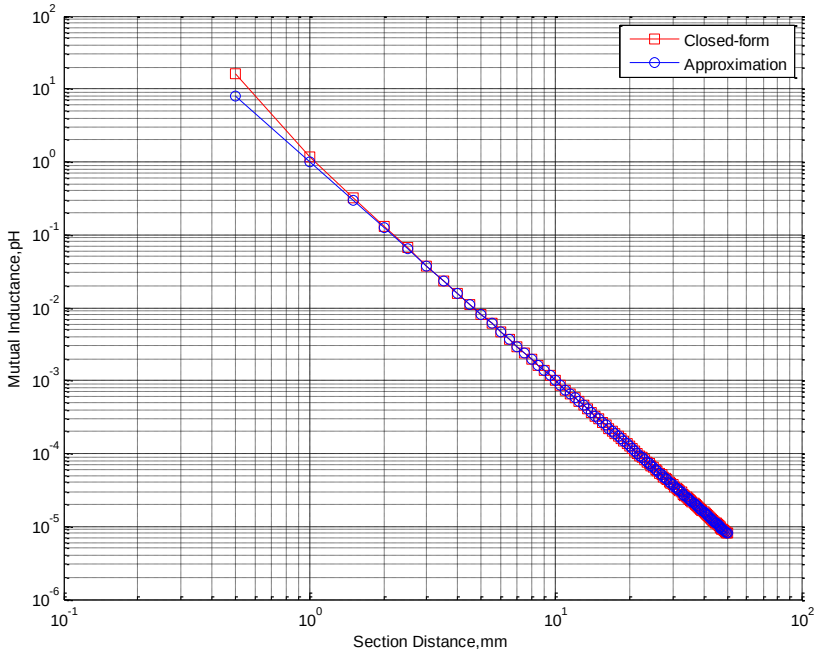


Figure 2.9. Partial-mutual inductance between two sections calculated by the closed-form formula and the approximated method.

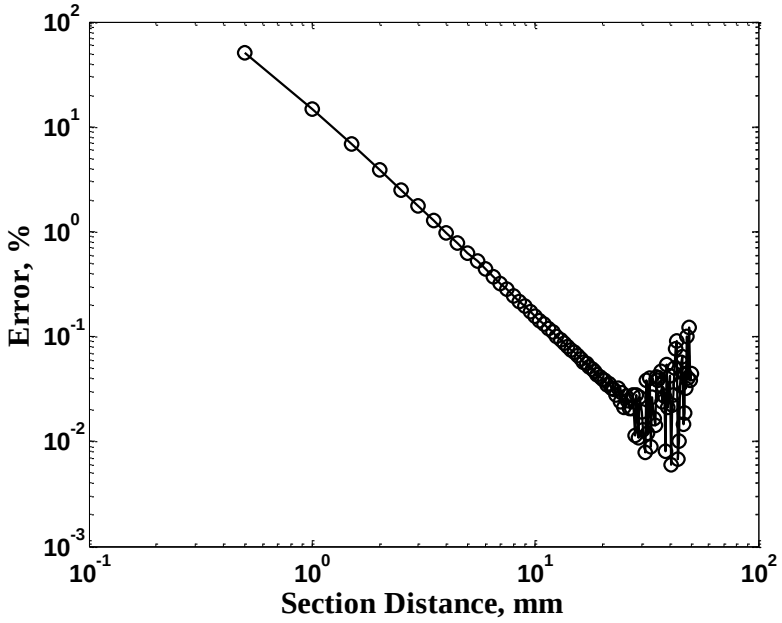


Figure 2.10. Relative error between the closed-form formula and approximation.

The relative – error criteria is set as 3 %. It can be seen that when the section distance is larger than 2.5mm, which is 5 times of the cell size, the relative error is already less than 3 %.

Normalize the partial-mutual inductance between two sections to the partial-self inductance of the section, Ls_{ij} / Ls_{ii} as shown in Figure 2.11. It is obviously that the partial-mutual inductance decays very fast. When the distance between two sections is 5mm, which is 10 times of the cell size, the coupling is already less than 10^{-4} of the partial-self inductance. Therefore, the coupling can be approximated as zero when the distance between two sections is large enough.

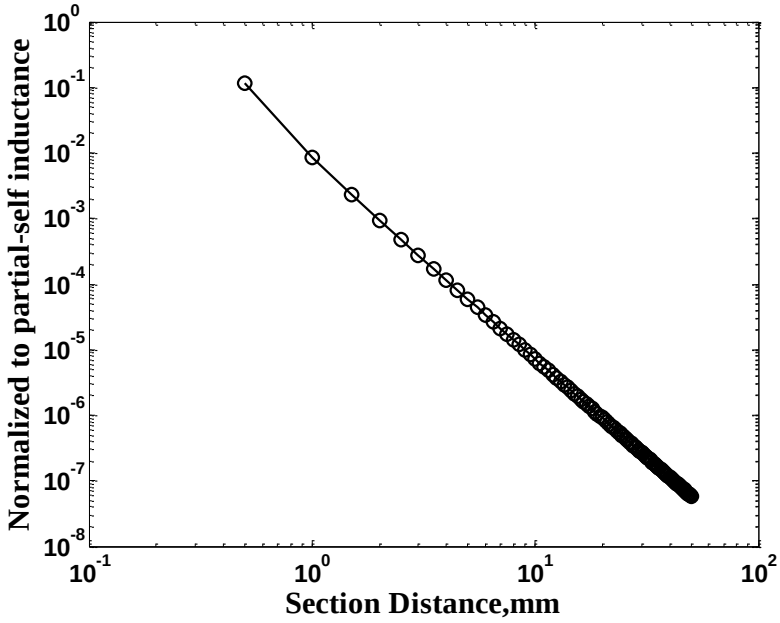


Figure 2.11. Normalized to partial-self inductance.

Vary the plane pair spacing from 0.1mm to 2mm. For each spacing value, the section length was changed from 0.1mm to 2mm, and the minimum section distance at which the relative error is no more than 3% was recorded as shown in Figure 2.12. The minimum section distance to satisfy the relative – error criteria requirement can be related to either section size or plane spacing, whichever is larger, by multiplying a factor.

Here we use the section with 0.5mm plane pair spacing as an example. Table 2.1 shows the section size, and the corresponding minimum section distance at which the relative error is less than 3 %. If section size is smaller than the plane spacing, the minimum section distance is roughly 5 times of the plane spacing. If section size is larger than the plane spacing, similar relationship can be found between the minimum section distance and section size. When section size is equal to the plane spacing, the minimum section distance is only 2 times of section size or the plane spacing. However, we can still set the minimum section distance equal to 5 times of section size or plane spacing. We will show that this estimated relationship gives high enough accuracy later.

Table 2.1 Minimum section distance to satisfy 3 % *err*, plane spacing = 0.5 mm

Section Size, mm	Minimum Section Distance, mm
0.1	2.8
0.2	2.6
0.25	2.5
0.5	1
1	5
2	12
5	30

It has been found that if the distance between sections is less than 5 times of the larger value of section length and plane spacing, called *ds*, the relative error is higher than 3 % and the closed-form expression needs to be applied to calculate the mutual inductance between two sections. If the distance between sections is larger than *ds*, the approximation formula can be applied with the relative error less than 3 %. If the distance between sections is larger than 2*ds*, the mutual inductance can be estimated as zero. Figure 2.13 shows the schematic of how to determine the calculation formulation for the mutual coupling. Applying the approximation criteria can speed up computations [12], which will be shown in an example later, and make the partial inductance matrix sparse due to the zero terms.

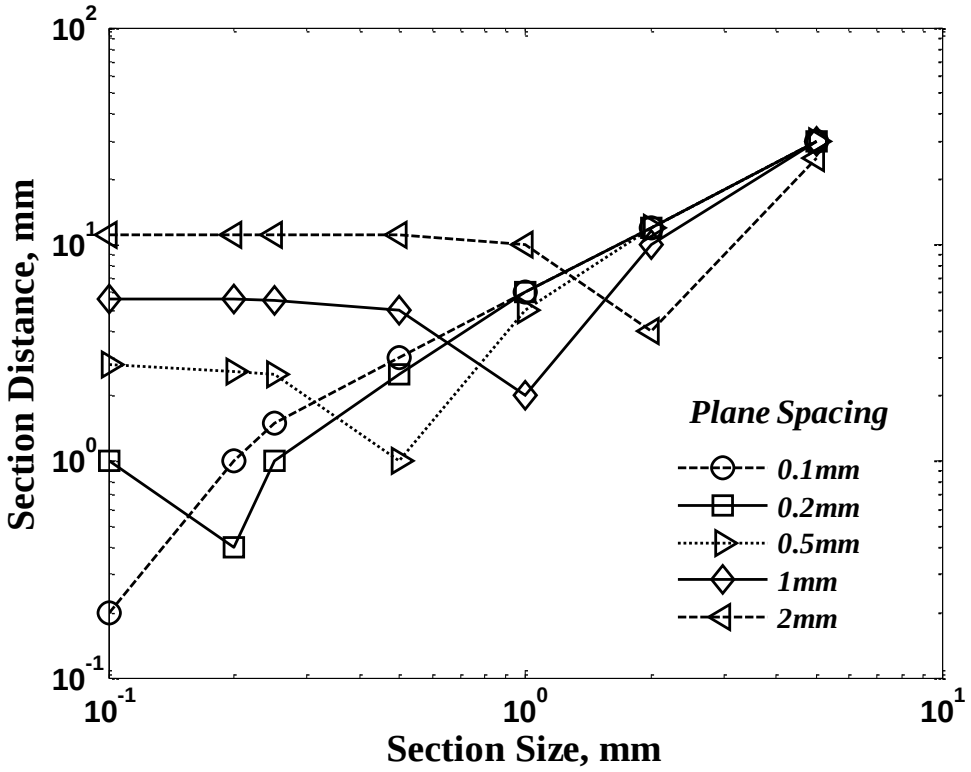


Figure 2.12. Criteria to apply the approximation formula

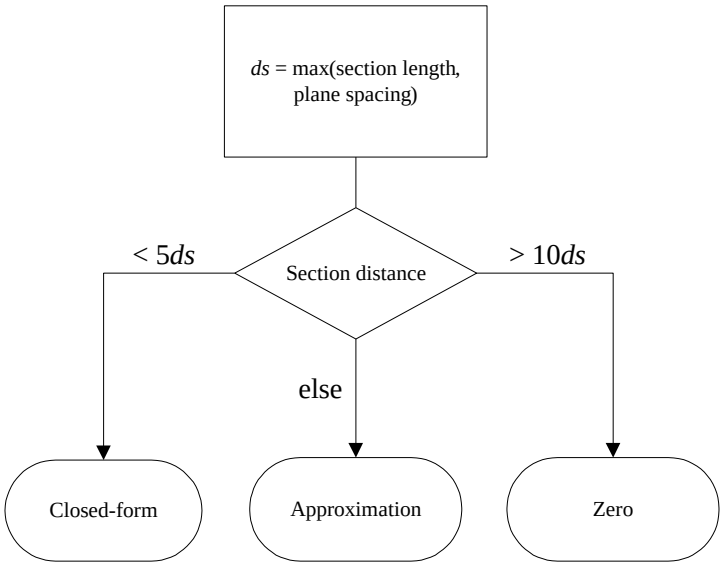


Figure 2.13. Schematic of criteria determination when *err* = 3%.

3. UNIFORM AND NON-UNIFORM MESH

3.1. ASSEMBLY OF MNA

By stamping in the appropriate contribution circuit element in a conventional Modified Nodal Analysis (MNA) method, the circuit matrix can be set up to model the plane pair [12]. Briefly, the MNA matrix is composed by KVL, KCL and partial inductance matrices. By solving the matrix, the voltage at each node and the current in each branch can be obtained. Thus, all desired inductances like the inductance of the plane pair can be calculated.

Figure 3.1 shows an example with the smallest structure. Subdividing the example with the conventional PEEC mesh (Figure 3.1 (a)), the corresponding partial inductance evaluation in *x* and *y* direction is shown in Figure 3.1 (b). Since the geometry shown here is subdivided with the least amount of mesh, the cells in both *x* and *y* directions are cells on the edge. It is worth to note that the currents we are talking here, I*x* and I*y* are differential currents as shown in Figure 2.8.

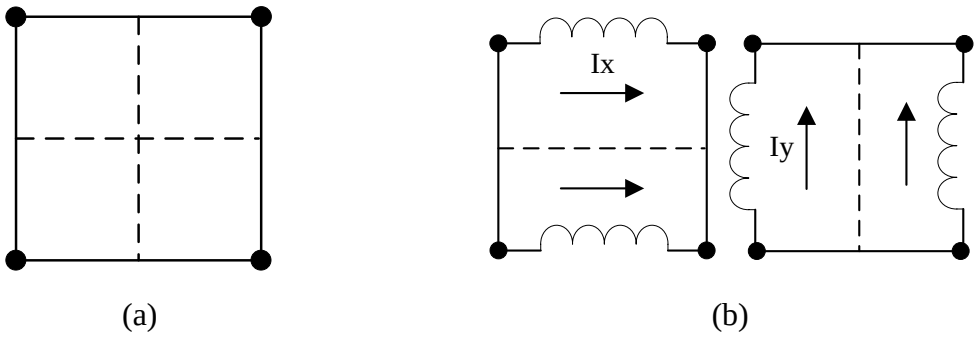


Figure 3.1. Example with the smallest structure. (a) Mesh in x and y direction. (b) Partial inductance in *x* and *y* direction.

The corresponding equivalent circuit for the example in Figure 3.1 is shown in Figure 3.2. Node 1 is defined as the current source with the current, *Is* injected into. Node 4 is defined as the short connected to ground, which is the datum node with the voltage of zero. The branch number and corresponding nodes at two ends are listed in Table 3.1.

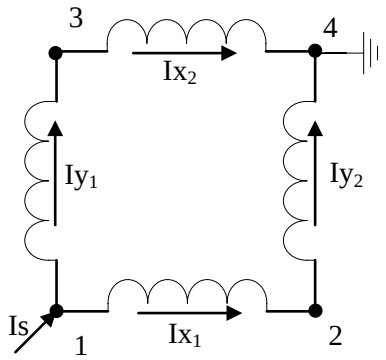


Figure 3.2. Equivalent circuit of the example with the smallest structure.

Table 3.1 Branch number and corresponding nodes at the ends

Branch No.	Beginning Node	End Node
1	1	2
2	3	4
3	1	3
4	2	4

Table 3.2 Branch voltage

Branch Voltage	Node Voltage			
	V_{N1}	V_{N2}	V_{N3}	V_{N4}
V_1	1	-1	0	0
V_2	0	0	1	-1
V_3	1	0	-1	0
V_4	0	1	0	-1

According to Eq. (10), the voltage drop on the branch is determined by the voltage of the nodes at the ends as shown in Table 3.2. The incident matrix of voltage, $\overline{\overline{V}}$ can be expressed as,

$$\overline{\overline{V}} = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix}. \tag{27}$$

Table 3.3 Node current

	Branch Current			
	Ix_1	Ix_2	Iy_1	Iy_2
Node 1	1	0	1	0
Node 2	-1	0	0	1
Node 3	0	1	-1	0
Node 4	0	-1	0	-1

The current flowing through each node is calculated by KCL as shown in Table 3.3. Define the current flowing out of the node as "+" and the current flowing into the node as "-". The incident matrix of current is,

$$\overline{\overline{I}} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ -1 & 0 & 0 & 1 \\ 0 & 1 & -1 & 0 \\ 0 & -1 & 0 & -1 \end{bmatrix}. \tag{28}$$

Same as Eq. (11), we have $\bar{\bar{I}} = \bar{\bar{V}}^T$. The source current injected into node 1 and the short current at node 4 are not included in $\bar{\bar{I}}$, and they will be included in the final assembled MNA matrix.

Since the cell is orthogonal, the coupling is only in *x* or *y* direction. The partial inductance matrix, $\bar{\bar{L}}$ is expressed as,

$$\bar{\bar{L}} = \begin{bmatrix} Lpx_{11} & Lpx_{12} & 0 & 0 \\ Lpx_{21} & Lpx_{22} & 0 & 0 \\ 0 & 0 & Lpy_{33} & Lpy_{34} \\ 0 & 0 & Lpy_{43} & Lpy_{44} \end{bmatrix}. \tag{29}$$

Assemble $\bar{\bar{V}}$, $\bar{\bar{I}}$ and $\bar{\bar{L}}$ with an all-zero 4 × 4 matrix to form *A* matrix as shown in Eq. (12). The circuit equation for the smallest structure is shown in Eq. (30). A column and a row are added into *A* matrix as the last column and row, which are used for the stamping of short current and voltage, respectively. *Is* in the right-hand-side of Eq. (30) represents the source current injected into node 1. By solving Eq. (30), the voltage of each node and the current on each branch can be obtained. Therefore, the impedance of the smallest structure is give by $L_{11} = V_{N1} / sIs$. All other inductance like L_{21}, L_{31} can also be calculated.

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & 0 & -1 & 1 \\ 1 & -1 & 0 & 0 & Lpx_{11} & Lpx_{12} & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & Lpx_{21} & Lpx_{22} & 0 & 0 & 0 \\ 1 & 0 & -1 & 0 & 0 & 0 & Lpy_{33} & Lpy_{34} & 0 \\ 1 & 0 & -1 & 0 & 0 & 0 & Lpy_{43} & Lpy_{44} & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{N1} \\ V_{N2} \\ V_{N3} \\ V_{N4} \\ sIx_1 \\ sIx_2 \\ sIy_1 \\ sIy_2 \\ sI_{sh} \end{bmatrix} = \begin{bmatrix} sIs \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{30}$$

It is important that for much larger and more realistic geometry, the structure of the MNA matrix is similar as that in Eq. (30). The source current can be injected into any node(s) we want to calculate the inductance at, and the short(s) can be placed at any node(s) where the capacitors are located.

3.2. BOOKKEEPING OF NODES

In the previous work, the port was represented with a single node in the model [12]. Here, we included the port dimension into the model to make it more general for the real case. Firstly, subdivide the plane to commensurate cells as shown in Figure 2.4, and label each node with a global number. The nodes in the corresponding port region are treated as one node. Then use bookkeeping to assign a local number for each node. An example is shown in Figure 3.3. Nodes with the global number of 1,2,5 and 6 form the port of short, and nodes with the global number of 11,12,15 and 16 form the port of source. Assign the local number of 1 to the nodes on the port of short and the local number of 2 to the nodes on the port of source. Then assign a local number to other nodes in sequence to build the node system. Table 3.4 shows the global number and the local number of each node.

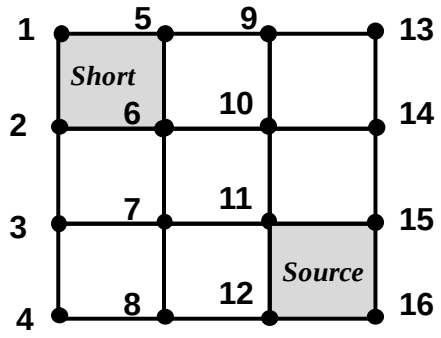


Figure 3.3. Bookkeeping of the nodes.

Table 3.4 Bookkeeping of the nodes

Global Node No.	Local Node No.	Node Property
1	1	short
2	1	short
3	3	-
4	4	-
5	1	short
6	1	short
7	5	-
8	6	-
9	7	-
10	8	-
11	2	source
12	2	source
13	9	-
14	10	-
15	2	source
16	2	source

3.3. COMPUTATION SPEED-UP.

Although the approximated formulation is helpful to speed up computation, the model may still be time consuming since a huge number of partial-self and partial-mutual inductance need to be calculated if the plane size is large or the mesh is very dense. Due to the symmetry of the uniform mesh subdivision, we can only calculate the partial-self and partial-mutual inductance of one section, and the partial-self and partial-mutual inductance of other sections can be obtained directly from the results of the section we calculate. Figure 3.4 shows an example of the smallest circuit to calculate the partial-self and partial-mutual inductance in x direction.

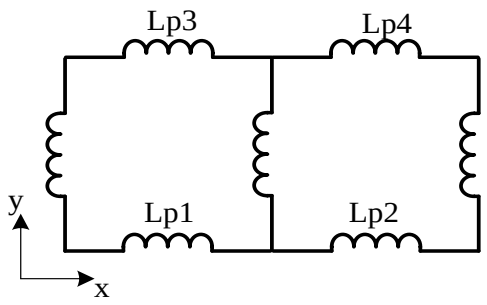


Figure 3.4. Example for partial-self and partial-mutual inductance calculation.

The partial-self inductance of section 1, Lp_{11} and the partial-mutual inductance Lp_{12}, Lp_{13} and Lpx_{14} can be calculated using the formulations in Eq. (16) and Eq. (25). It's noticed that for section 2, we have $Lp_{21}=Lp_{12}$, $Lp_{22}=Lp_{11}$, $Lp_{23}=Lp_{14}$ and $Lp_{24}=Lp_{13}$. The partial-self and partial-mutual inductance of section 2 can be obtained from the results of section 1 by building a transfer matrix shown in Eq. (31). For more realistic case with many partial inductance components, the transfer matrix can be built with similar structure.

$$\begin{bmatrix} Lp_{21} \\ Lp_{22} \\ Lp_{23} \\ Lp_{24} \end{bmatrix} = \begin{bmatrix} Lp_{11} & Lp_{12} & Lp_{13} & Lp_{14} \end{bmatrix} \begin{bmatrix} 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} \tag{31}$$

3.4. COMPUTE TIME ANALYSIS

The total compute time to solve the MNA matrix is determined by the number of unknowns in Eq. (30), which are V_{Ni}, Ix_i and Iy_i. To find the relationship between the number of unknowns and compute time, we can increase the problem size by keeping the same mesh size while increasing the geometry size. The plane size is changed from 20mm × 20mm to 140mm × 140mm with the plane spacing of 0.2mm while the mesh size is kept as 1mm × 1mm. The total compute time, time for stamping MNA matrix and time for solving MNA matrix are recorded and listed in Table 3.5. It is obviously that the total compute time is determined by the time for stamping and solving MNA matrix, and most time is spent on stamping MNA matrix.

Table 3.5 Compute time with different plane sizes

Plane size, mm × mm	Unknowns	Total Time, sec	Stamp MNA, sec	Solve MNA, sec
20	1282	0.7	0.38	0.17
30	2822	1.56	0.76	0.58
40	4962	3.34	1.66	1.4
50	7702	6.48	2.96	3.08
60	11042	10.95	5.47	4.8
70	14982	17.53	9.11	7.36
80	19522	25.73	14.68	9.48
90	24662	39.32	21.98	14.87
100	30402	57.25	32.59	21.18
110	36742	77.28	46.29	25.83
120	43682	112.41	69.38	36.18
130	51222	139.87	87.4	43.18
140	59362	190.62	122	56.76

Figure 3.5, Figure 3.6 and Figure 3.7 show the total compute time, time for stamping MNA matrix and time for solving MNA matrix vs. the number of unknowns,

respectively. In all three figures, the exponential is around 1.5, which agrees with our expectation.

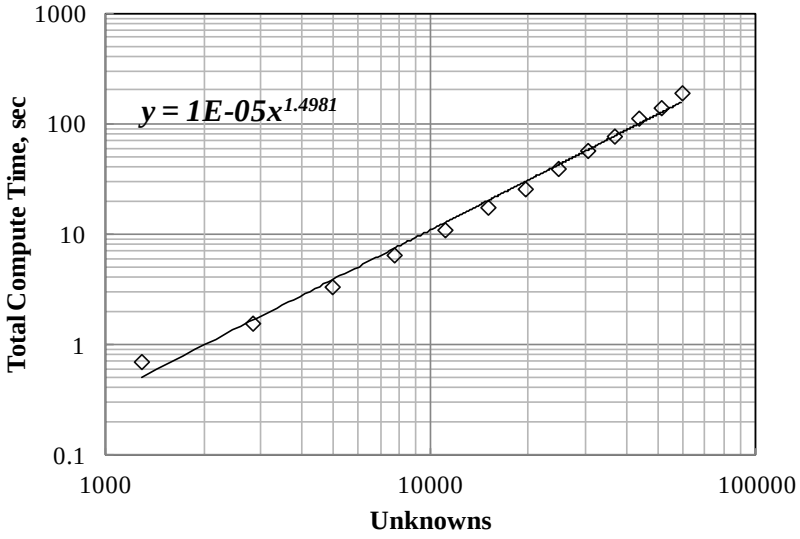


Figure 3.5. Total compute time vs. unknowns

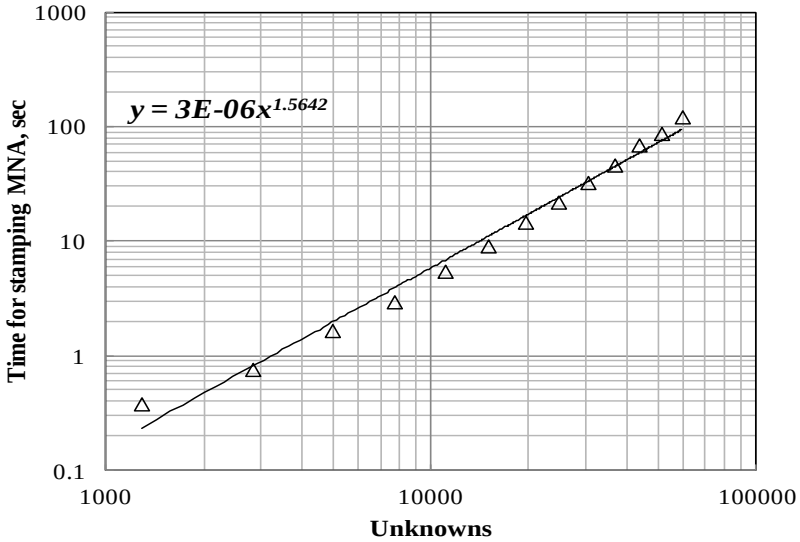


Figure 3.6. Time for stamping MNA matrix vs. unknowns

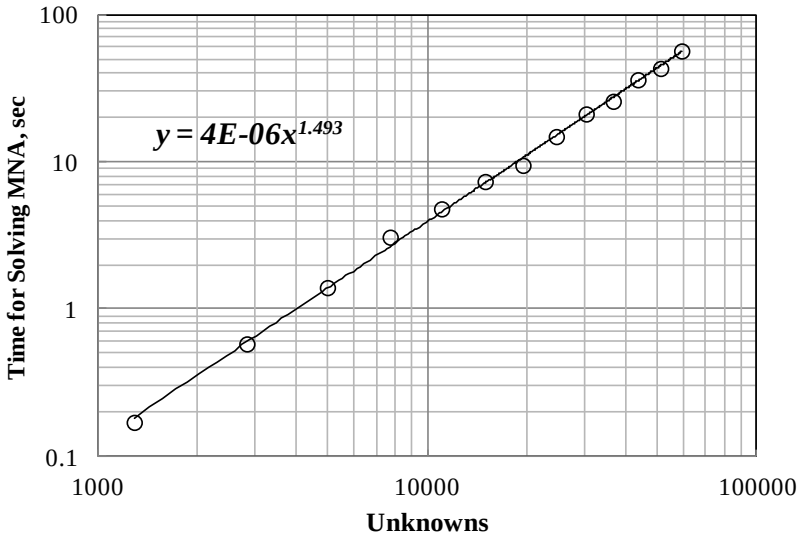


Figure 3.7. Time for solving MNA matrix vs. unknowns

3.5. NUMERICAL EXPERIMENT

Here we give the results for a plane pair with 20mm × 20mm plane size and 0.8mm plane spacing as shown in Figure 3.8. The short center is located at (x=5mm, y=5mm), and the source center is located at (x=13mm, y=13mm). The port size for both short and source is 2mm × 2mm. The mesh size is set as 0.5mm × 0.5mm. The software of PowerPEEC from IBM [14] is used to validate the results. The calculated results are listed in Table 3.6. The results from PPP approach agree well with the result using PowerPEEC, and the relative error is less than 0.5 %.

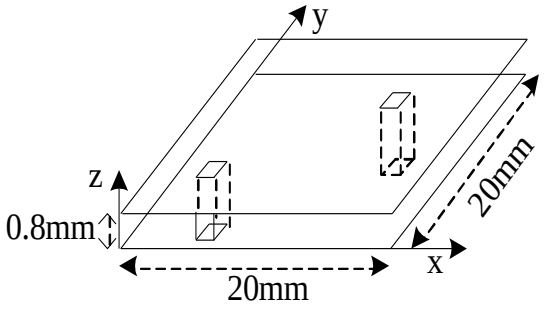


Figure 3.8. Test geometry

Table 3.6 Calculation results with different methods

	Unknowns	Inductance	Time
w/o Apporx	4834	729.97 pH	31.3 sec
w/ Approx	4834	727.95 pH	7.5 sec
PowerPEEC	-	727.15 pH	85.4 sec

The calculated plane pair inductance using the PPP approach matches well with PowerPEEC. The result obtained with the approximation criteria applied is very close to that calculated using closed-form expression, and *err* is less than 0.5 %. The total compute time with approximation applied is reduced to about a quarter of the total time using closed-form expression with losing the accuracy, which is very helpful when plane size is large.

3.6. MULTIPLE CONTACTS

In real PDN design, multiple decoupling capacitors are placed between power and ground plane (Figure 3.9). In PPP approach, these decoupling capacitors are represented using short vias. Here, we show an example with 10 shorts shown in Figure 3.10. The plane pair is 50mm × 50mm with the plane spacing of 0.2mm. The via size is 2mm × 2mm, and mesh size is 1mm × 1mm. The locations of the source and 10 shorts are shown in Figure 3.10**.**

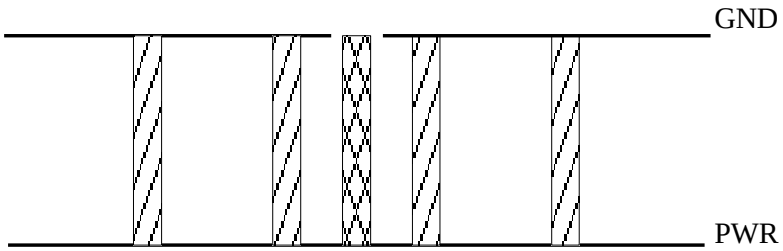


Figure 3.9. PWR/GND pair with multiple vias.

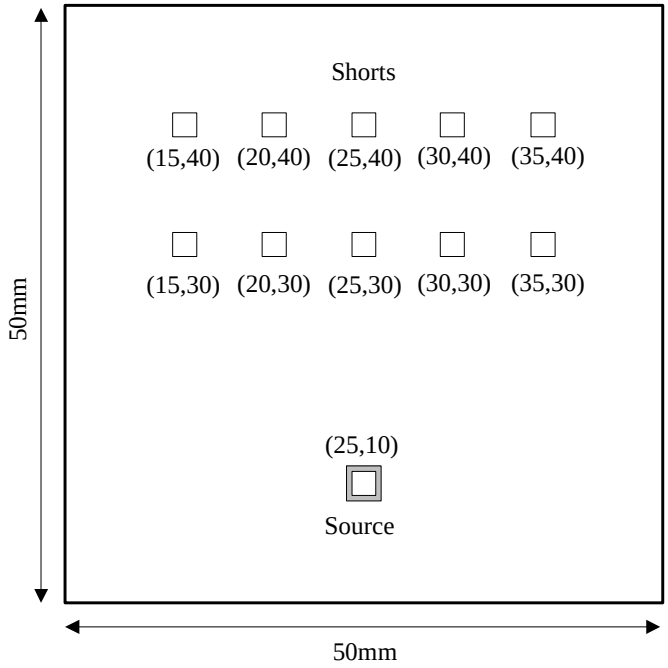


Figure 3.10. Test geometry with 10 contacts.

The inductance of the plane pair structure shown in Figure 3.10 is calculated using the PPP approach and compared to PowerPEEC (Table 3.7). The PPP approach shows enough accuracy, and the relative error between two methods is only 2.4 %.

Table 3.7 Plane pair inductance with 10 shorts

Plane Pair Inductance		Relative error
PPP Approach	PowerPEEC	
165.75 pH	161.89 pH	2.4 %

Next, we show that the PPP approach is very efficient taking multiple vias into account compared to other methods, like cavity model [8]. We use the test geometry shown in Figure 3.11 to test the compute time of PPP approach and the cavity model. The plane pair is 50mm × 50mm with plane spacing 0.2mm. The source port is fixed at a location, and multiple shorts are spread on the board around the port.

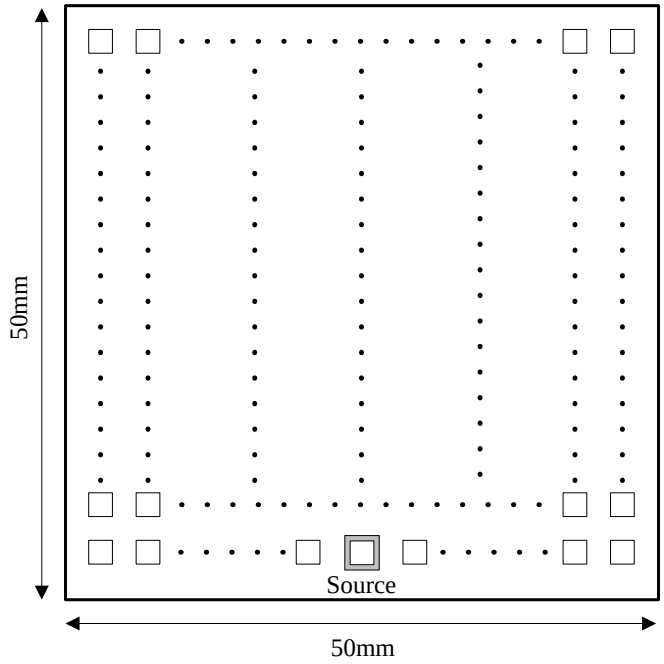


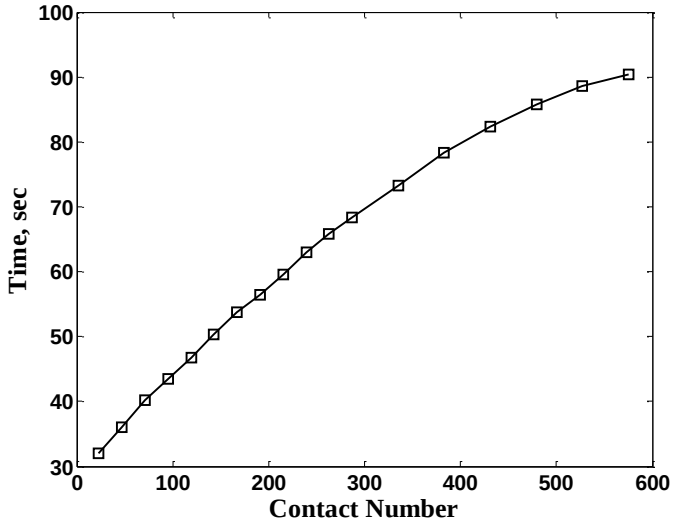
Figure 3.11. Test geometry for multiple shorts

The number of increased unknowns due to the increasing of vias is a small portion compared to the total amount of unknowns in the MNA matrix, which determines the total computational time. For example, when the number of shorts is increased from 10 to 20, the number of unknowns increases 10 which is only 0.13 % of the total amount of unknowns (Table 3.8). Thus, the total compute time of the PPP approach will not increase much by increasing the number of shorts.

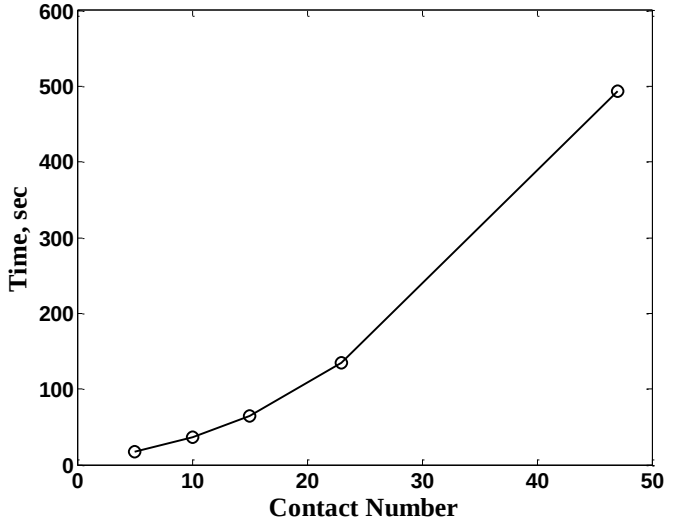
Table 3.8 Multiple shorts

Contact No.	Unknowns	Increased portion
10	7711	-
20	7721	0.13 %

As shown in Figure 3.12, for the same geometry, the running time for the PPP approach is almost linear to the contact number. However, the running time for cavity model is exponential to the contact number. It is apparently that the PPP approach is more efficient to handle the case with multiple contacts.



(a)



(b)

Figure 3.12. Compute time comparison for multiple contacts. (a) PPP approach. (b) Cavity model.

3.7. NON-UNIFORM MESH

Since the current distribution is concentrated near the port region, non-uniform mesh may be applied to reduce the size of MNA matrix and increase calculation speed. Sub-mesh is applied to the region near the ports. For the region away from the ports, sparse mesh is used (Figure 3.13 (a)). The zoom-in of the interface currents in both x and y directions is also shown in Figure 3.13 (b) and (c), respectively.

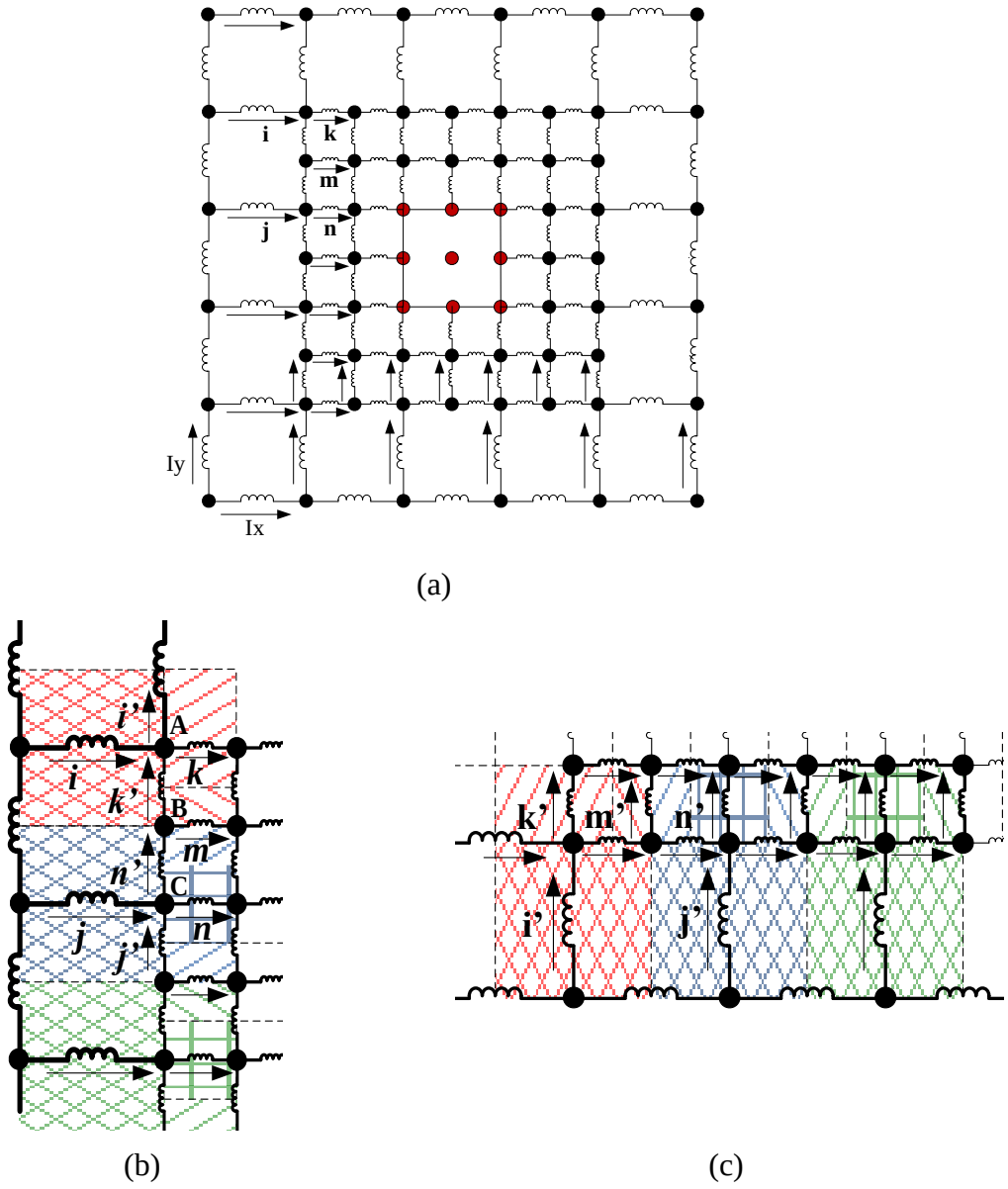


Figure 3.13. Non-uniform mesh. (a) Sub-mesh near the port region. (b) Zoom-in of the interface in *x* direction. (c) Zoom-in of the interface in *y* direction.

The size of the dense mesh is set as half of the size of the sparse mesh (Figure 3.13). The incident matrix of the voltage is similar as that of the uniform mesh. The incident matrix of the current is changed due to the re-distribution of the current at the interface between sparse mesh region and sub-mesh region. To generate incident matrix of current, $\overline{\overline{I}}$ for the interface, we assume that the current flows uniformly through the cell.

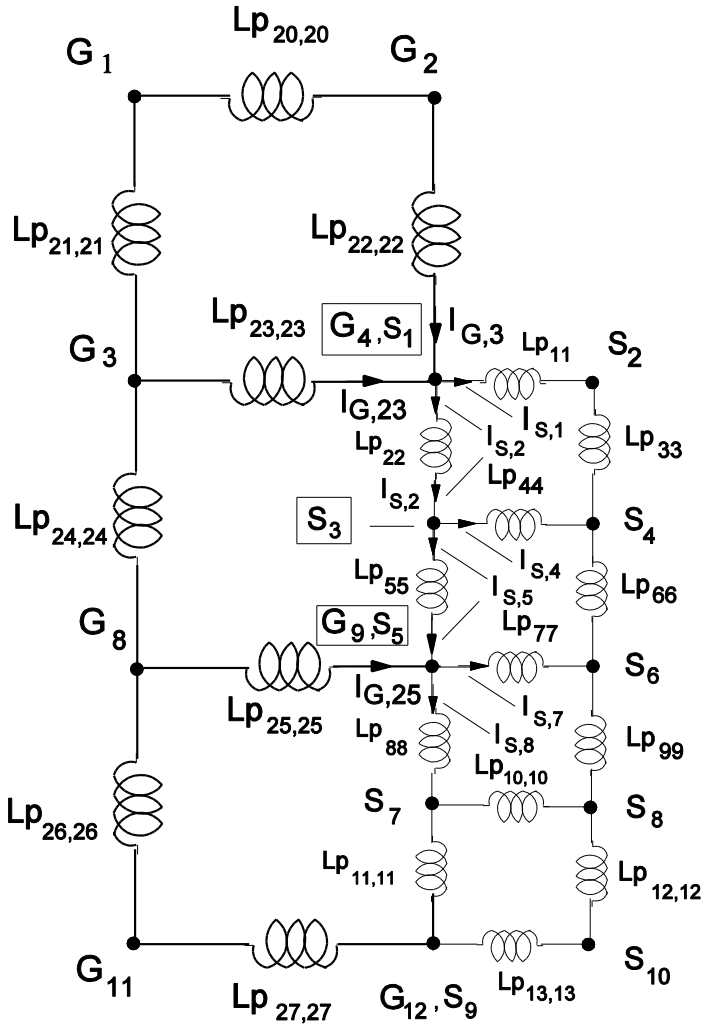


Figure 3.14. Transition between mesh density.

Figure 3.14 shows the equivalent circuit for the transition between mesh density as shown in Figure 3.13. There are three types of nodes that are of importance for the transition between the two regions. Type I node is the corner node between the transition regions, i.e., node A in Figure 3.13 or node ([G_4, S_1]) in Figure 3.14. Type II node is the nodes next to the corner nodes occur only in the reduced size mesh, i.e., node B in Figure 3.13 or node S_3 in Figure 3.14. Type III node is different from the side node and there is a direct connection to the coarse mesh, i.e., node C in Figure 3.13 or node ([G_9, S_5]) in Figure 3.14.

Based on the ratio of the corresponding cross section length, the weighted KCL equations for the three types of nodes can be obtained. For node A, the cross section that current Ix_k flows out is 75% of that current Ix_i flows in. For node B, the cross section Ix_m flows out is 25% of the cross sections Ix_i and Ix_j flows in. For node C, the cross section Ix_n flows out is 50% of that Ix_j flows in. All coarse-fine mesh nodes are handled same way. Eq. (32) shows the weighted KCL equations for the three types of nodes in the equivalent circuit shown in Figure 3.14. Stamping the coefficients in Eq. (32) into to $\bar{\bar{I}}$ generate a new weighted KCL matrix as shown in Table 3.9. Again, the current we talk about here is the differential current as shown in Figure 2.8.

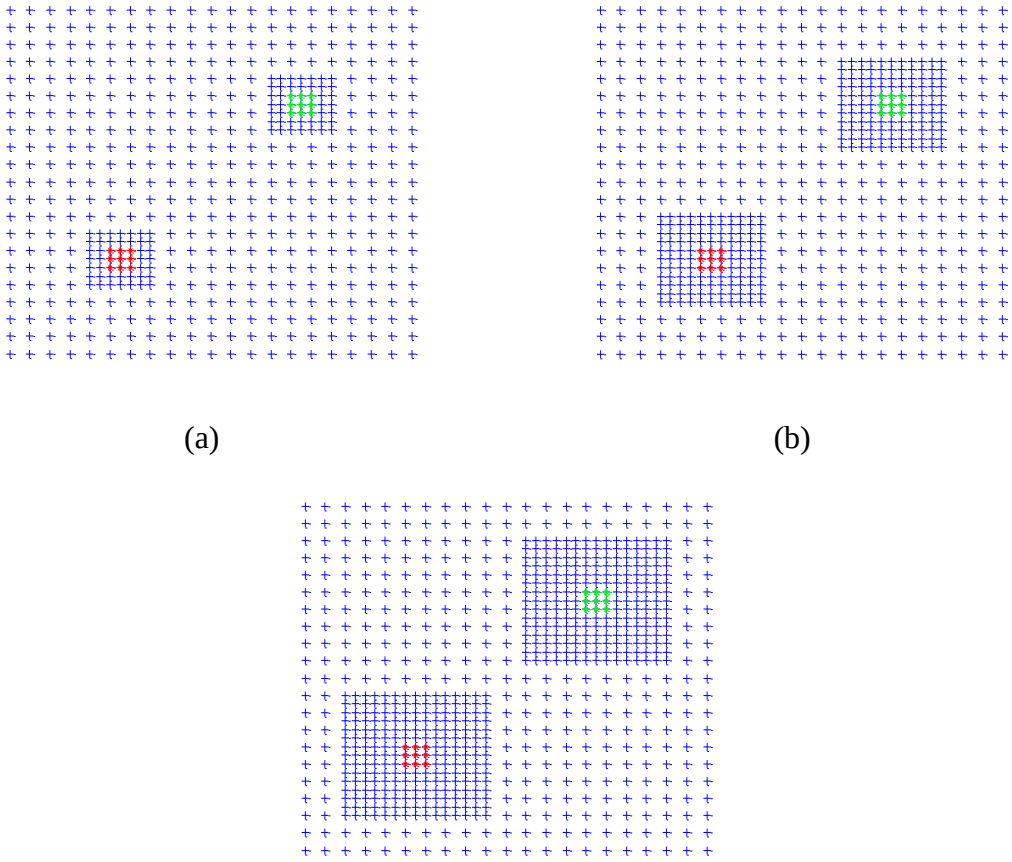
$$\begin{aligned}
&\text{Type I Node: } -0.75I_{G,23} + I_{S,1} + I_{S,2} - 0.75I_{G,3} = 0 \\
&\text{Type II Node: } -0.25I_{G,23} - 0.25I_{G,25} + I_{S,4} + I_{S,5} - I_{S,2} = 0 \\
&\text{Type III Node: } -0.5I_{G,25} + I_{S,7} + I_{S,8} - I_{S,5} = 0
\end{aligned} \tag{32}$$

Table 3.9 Weighted KCL matrix

	$I_{G,23}$	$I_{G,25}$	$I_{S,1}$	$I_{S,4}$	$I_{S,7}$	$I_{G,3}$	$I_{S,2}$	$I_{S,5}$	$I_{S,8}$
[G_4, S_1]	-0.75	0	1	0	0	-0.75	1	0	0
S_3	-0.25	-0.25	0	1	0	0	-1	1	0
[G_9, S_5]	0	-0.5	0	0	1	0	0	-1	1

3.8. NUMERICAL EXPERIMENT FOR NON-UNIFORM MESH

A test geometry of 20mm × 20mm plane size with 0.2mm plane pair distance is used to check the performance of the non-uniform mesh approach. The source center is located at (14.5mm, 14.5mm), and the short center is located at (5.5mm, 5.5mm). The via size is 1mm × 1mm. Two uniform mesh sizes, 1mm and 0.5mm, are applied in uniform mesh method, respectively. For non-uniform mesh approach, the sub-mesh size is 0.5mm and the sparse mesh size is 1mm. The convergence of the sub-mesh method is tested by increasing the sub-mesh area around the source via and short via as shown in Figure 3.15.



(a) (b)

(c)

Figure 3.15. Sub-mesh around the vias.

The inductance obtained using both uniform mesh and sub-mesh methods are shown in Table 3.10. The sub-mesh method shows enough accuracy compared to the uniform mesh method. The amount of unknowns of sub-mesh method is much less than the unknowns of uniform mesh approach without losing the accuracy, which leads to much smaller MNA matrix size and benefits total compute time. By increasing the area of sub-mesh region, the result is convergent.

Table 3.10 Inductance calculated using uniform mesh and sub-mesh methods

	Uniform Mesh Size		Sub-mesh Size		
			0.5mm		
	1mm	0.5mm	Sub-mesh area		
			3mm×3mm	5mm×5mm	7mm×7mm
Unknowns	1268	4922	1428	1732	2180
Inductance	268.95 pH	276.15 pH	275.05 pH	275.86 pH	276.06 pH

3.9. CLOSE VIAS

When the vias are very close, we can use only one sub-mesh region to cover all the vias (Figure 3.16), so that there are enough meshes between the vias to increase the accuracy.

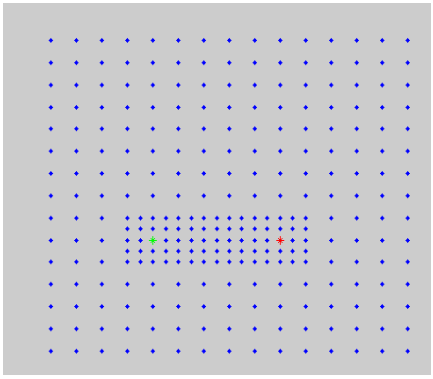


Figure 3.16. Close vias covered by one sub-mesh region.

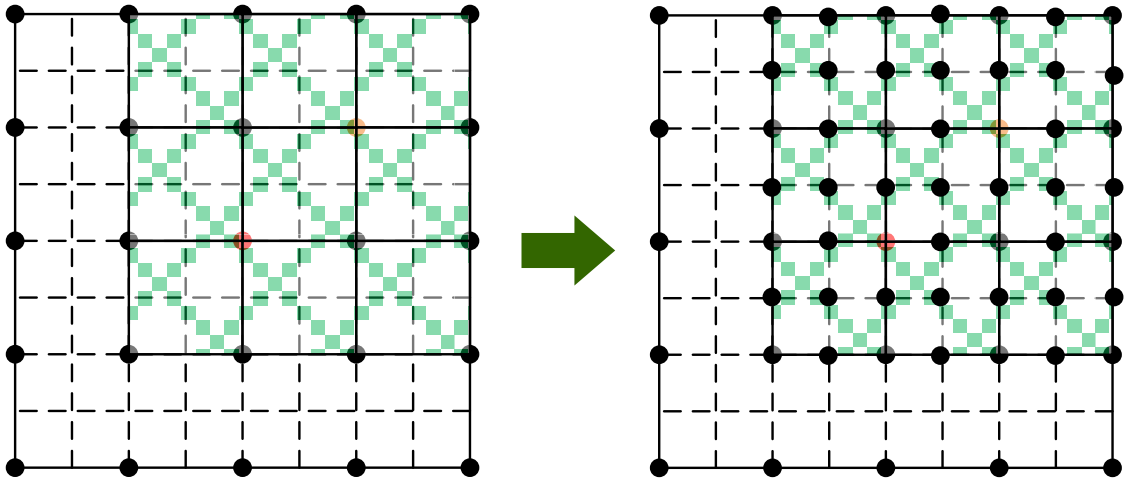


Figure 3.17. Define the sub-mesh region around the vias.

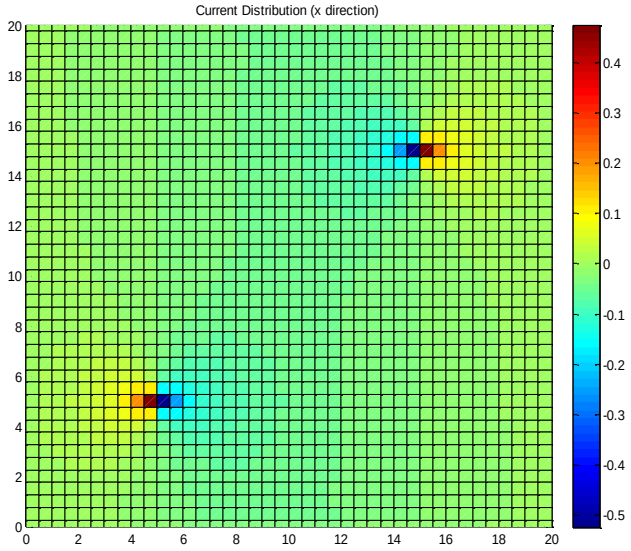
Define $X = m\Delta x$ and $Y = n\Delta y$, where X and Y are the distance between two vias in x and y direction, respectively, and Δx and Δy are the uniform cell length in x and y direction, respectively. Usually we have $\Delta x = \Delta y$. The sub-mesh area for close vias is defined as $(m + k)(n + k)\Delta x\Delta y$, $k = 2, 4, 6, \ldots$ (Figure 3.17) .

3.10. DETERMINE SUB-MESH REGION

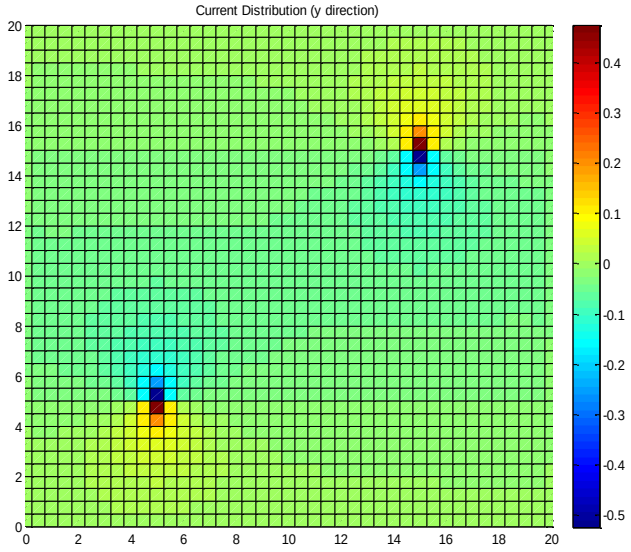
To apply sub-mesh method, we need to know how large the sub-mesh region we should use. Figure 3.18 shows the current distribution on the plane where uniform mesh is applied. It is clearly that the current distribution is concentrated in the region close to the source via and short via in both x and y directions. The current decays very fast in the region away from the vias.

From Figure 3.18, it can be seen that most of the current in x direction is concentrated within 6 uniform cells around the via, 3 cells on the left side and 3 cells on the right side (Figure 3.18 (a)). Same phenomena can be observed for the current distribution in y direction. Since the decay of the coupling between the sections is proportional to $1/r^2$ from Eq. (25). For the 4^{th} section away from the via, the coupling to the via decays to 1/16 of the coupling between the via and the 1^{st} section next to the via.

Thus, the area of the sub-mesh region should be $6\Delta x \times 6\Delta y$, which will give enough accuracy.



(a)



(b)

Figure 3.18. Current distribution on the plane. (a) *x* direction; (b) *y* direction.

3.11. VALIDATION OF SUB-MESH METHOD

A test geometry in reference [8] is used for the inductance calculation with sub-mesh method and changing several geometrical factors is shown in Figure 3.19 (a). The square parallel planes with the size of 50mm × 50mm and two rectangular vias with the size of 0.5mm × 0.5mm are shown in Figure 3.19. Two values for the spacing between two planes, *d*, 0.2mm and 1mm, are tested. Two values for the spacing between two vias, *l*, 1.5mm and 25.5mm are tested as two extreme cases. The locations of two vias are symmetrical along the y-axis in the test geometry, i.e., (25, 25-*l*/2) mm and (25, 25+*l*/2) mm. The calculated plane net inductances (Table 3.11) are compared to the values obtained using hybrid method and PEEC solver (PowerPEEC) in reference [8]. The comparison in Table 3.11 shows that the results obtained using PPP approach agrees with hybrid method and PowerPEEC.

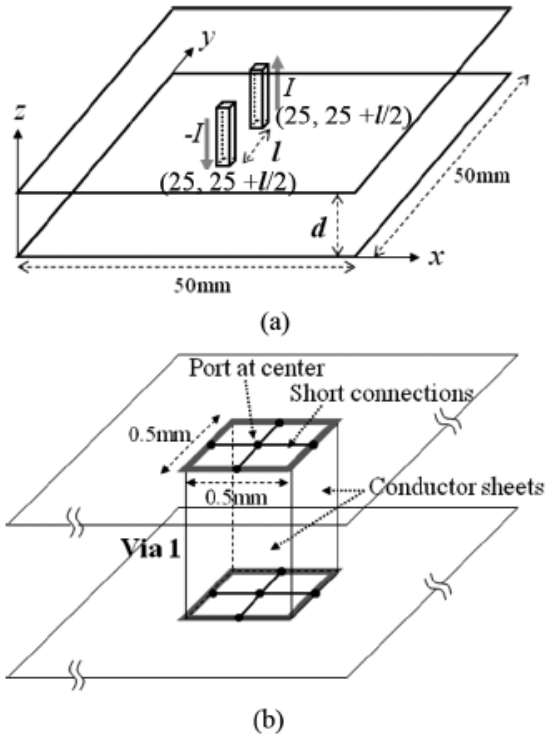


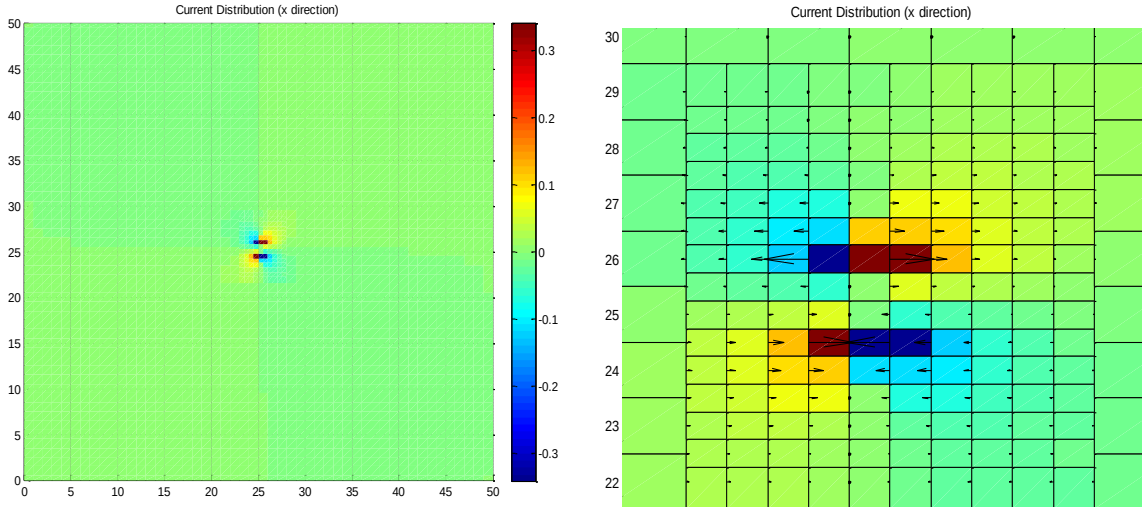
Figure 3.19. Test geometry for the inductance calculation [8]. (a) Variables are spacing between two vias, *l* , and separation between two planes, *d*. (b) Port condition.

Table 3.11 Plane net inductances from the hybrid, PEEC solver and PPP methods

d (mm)	l (mm)	L_{planei} (pH)			Diff. to Hybrid	Diff. to PEEC Solver
		Hybrid [8]	PEEC Solver [8]	PPP Approach		
0.2	1.5	51.2	54.8	53.8	4.8 %	1.8 %
	25.5	179.4	193	174.0	3.1 %	10.9 %
1	1.5	143.6	121.1	118.1	21.6 %	2.5 %
	25.5	734.8	732.3	715.4	2.7 %	2.4 %

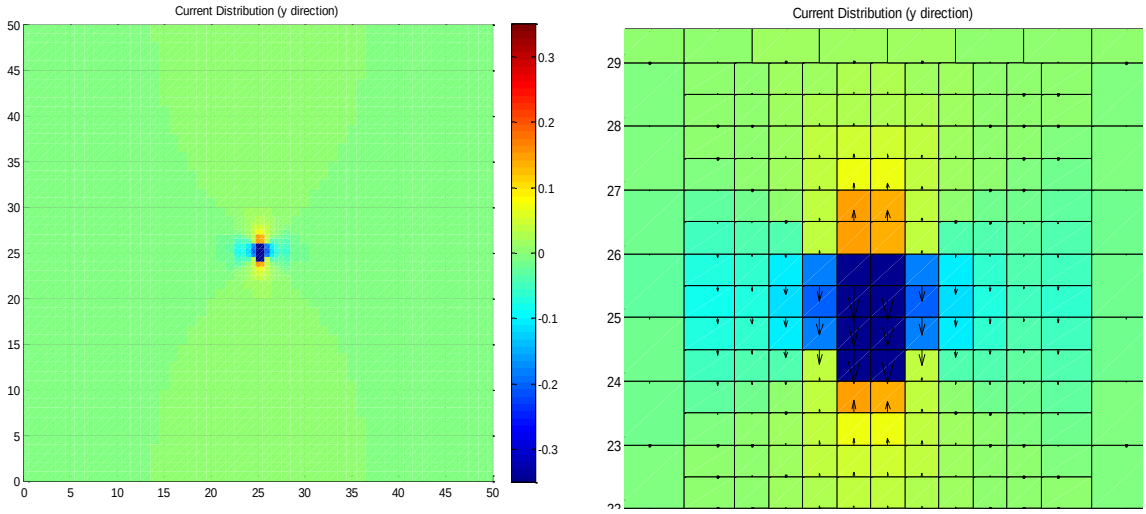
3.12. CURRENT DISTRIBUTION ANALYSIS

The current flowing on each branch can be calculated from MNA matrix. Here we use the geometry shown in Figure 3.19 as the example. The plane spacing, d is set as 1mm, and the via distance, l is set as 1.5mm and 25.5mm, respectively.



(a) (b)

Figure 3.20. Current distribution in x direction on the plane with d = 1mm and l = 1.5 mm. (a) Total current distribution in x direction. (b) Current vector in x direction at the source and short.



(a) (b)

Figure 3.21. Current distribution in *y* direction on the plane with *d* = 1mm and *l* = 1.5 mm. (a) Total current distribution in *y* direction. (b) Current vector in *y* direction at the source and short.

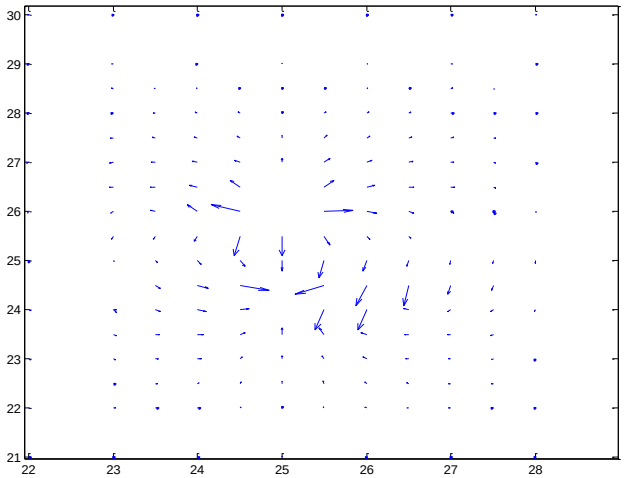
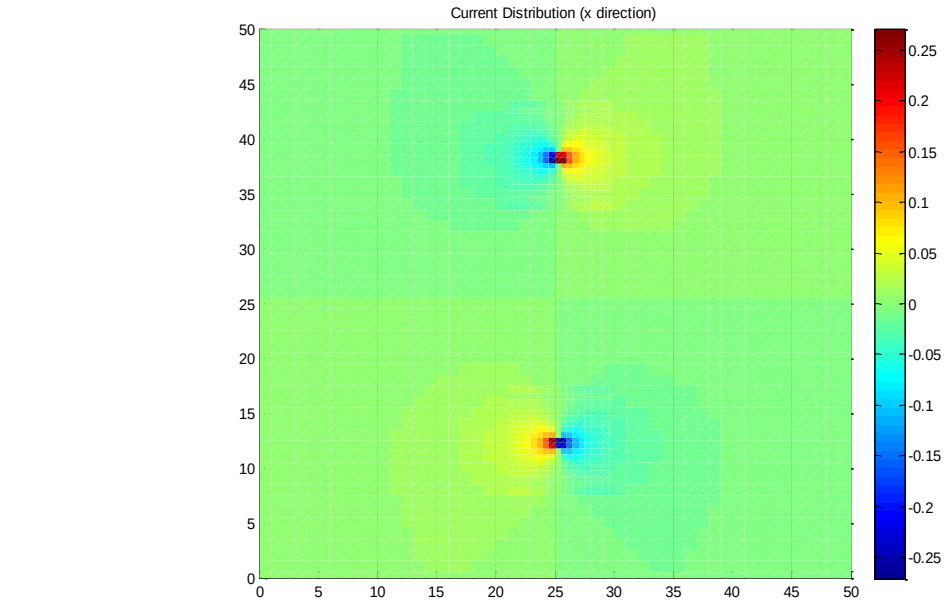
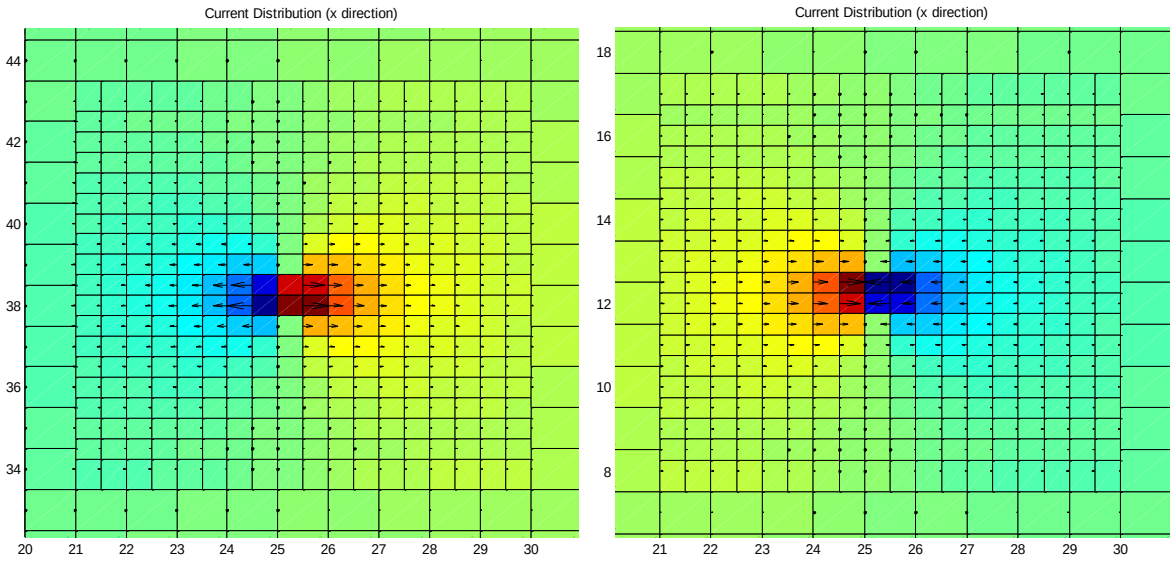


Figure 3.22. Zoom-in of current vector at source and short on the plane with *d* = 1mm and *l* = 1.5 mm.

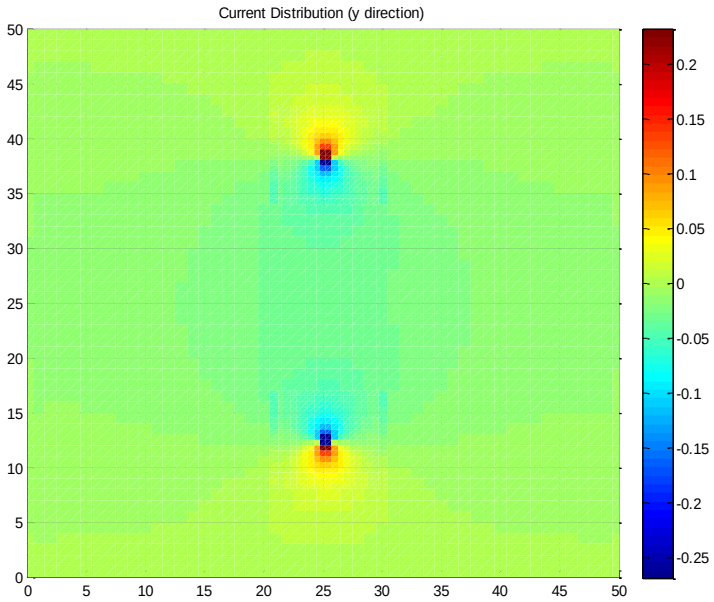


(a)

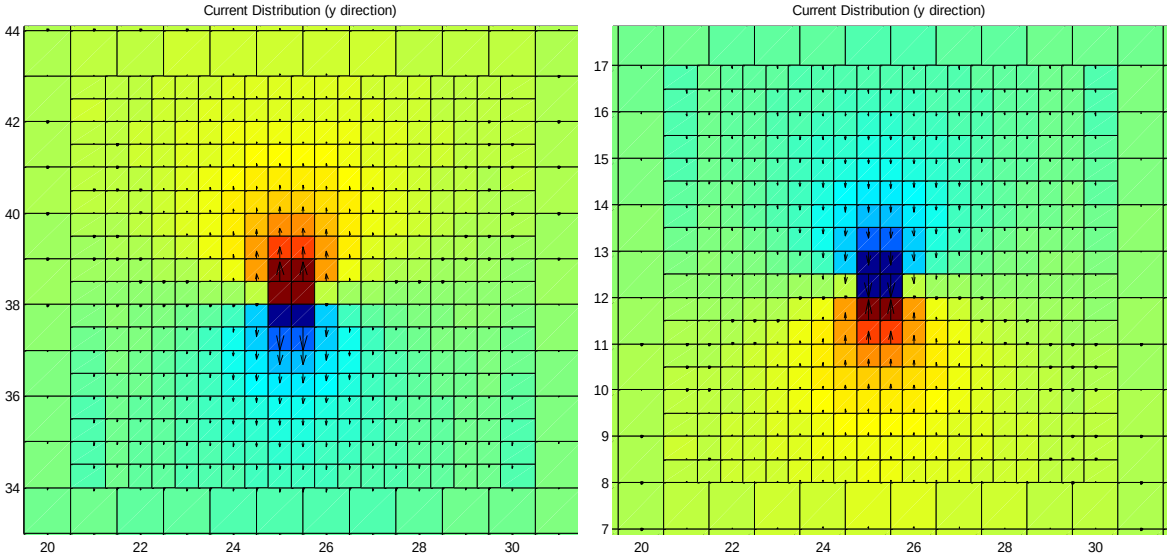


(b) (c)

Figure 3.23. Current distribution in *x* direction on the plane with *d* = 1mm and *l* = 25.5 mm. (a) Total current distribution in *x* direction. (b) Current vector in *x* direction at the source port. (c) Current vector in *x* direction at the short.



(a)



(b) (c)

Figure 3.24. Current distribution in *y* direction on the plane with *d* = 1mm and *l* = 25.5 mm. (a) Total current distribution in *y* direction. (b) Current vector in *y* direction at the source. (c) Current vector in *y* direction at the short.

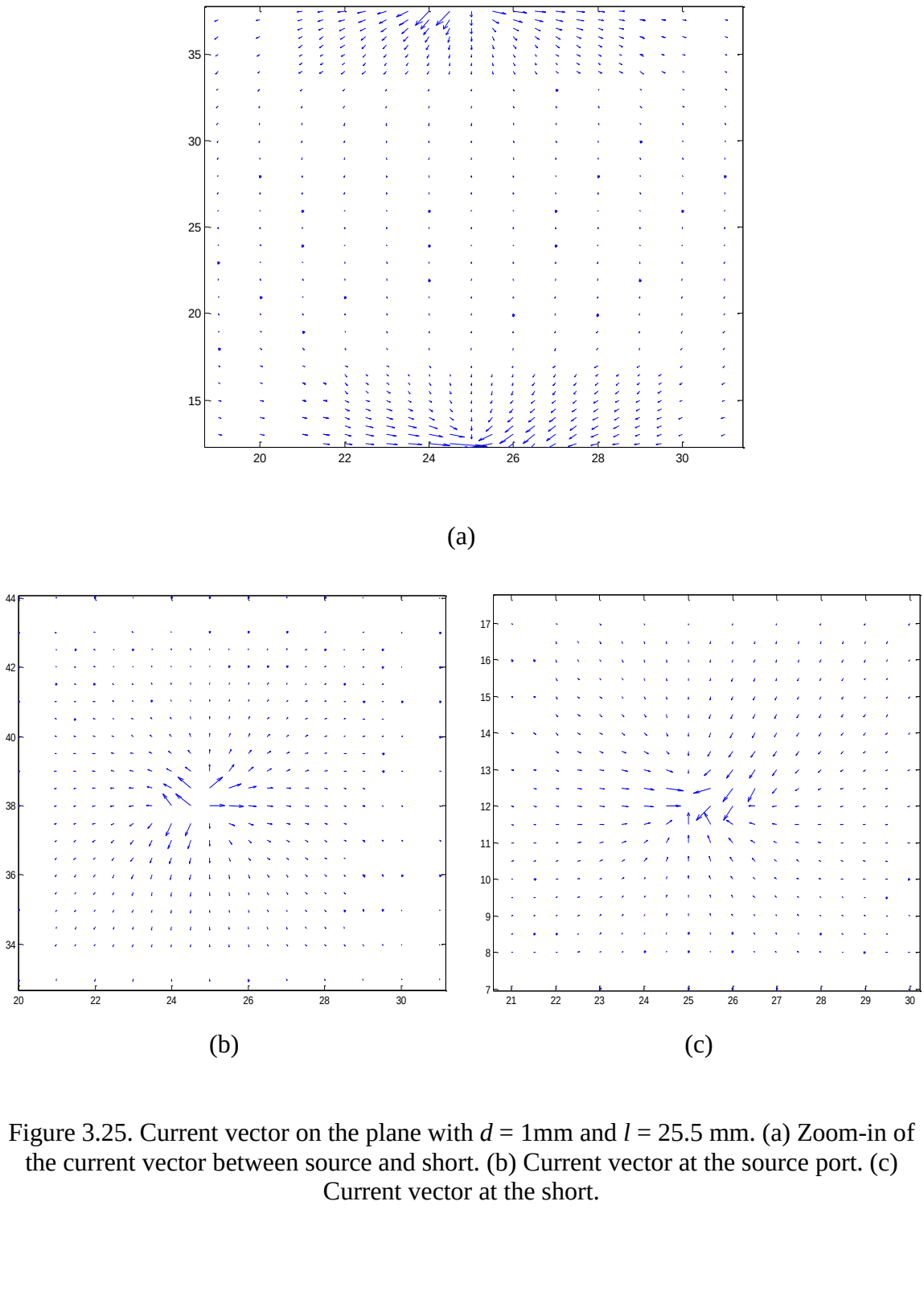


Figure 3.25. Current vector on the plane with d = 1mm and l = 25.5 mm. (a) Zoom-in of the current vector between source and short. (b) Current vector at the source port. (c) Current vector at the short.

The current distribution is plotted in *x* and *y* direction separately, and current vector is also plotted to show the direction that current flows to. For both close via (Figure 3.20 - Figure 3.22) and far via (Figure 3.23 - Figure 3.25) examples, the current vector clearly shows that the current flows out of the source and flows into the short. The current density is high in the region near the source and short, and low in the region far away from the source and short.

3.13. EFFICIENCY OF SUB-MESH METHOD

We use a larger plane pair with 100mm × 100mm plane size and 0.2mm plane spacing as the test geometry. The short center is located at (x = 20.5mm, y = 20.5mm), and the source center is located at (x = 50.5mm, y = 50.5mm). The port size for both short and source is 1mm × 1mm. For the sub-mesh method, the area of the sub-mesh region is 3mm × 3mm with 0.5mm sub-mesh size, and the sparse mesh size is 1mm. For the uniform mesh method, the mesh size is 0.5mm. The comparison between two approaches is shown in Table 3.12.

Table 3.12 Comparison between sub- and uniform mesh methods

	Unknowns	Inductance	Time
Sub-mesh	30548	351.21 pH	87 sec
Uni-mesh	120762	350.57 pH	6384 sec

With the sub-mesh method, the number of unknowns is significantly reduced, resulting much less running time, and the result is very close to that obtained using uniform mesh approach (difference < 0.2%). The sub-mesh approach is also memory usage saving due to the much smaller size of the MNA matrix compared to uniform mesh approach. It’s worth to note that all results are from the Matlab program which is slower than C++.

3.14. VIA INDUCTANCE

The side walls of a via can be represented using 4 zero-thickness metal sheets shown in Figure 3.26. The partial inductance of the parallel sheets can be calculated using Eq. (16), and the partial inductance of the orthogonal sheets as shown in Figure 3.27 is given as Eq. (33) [15].

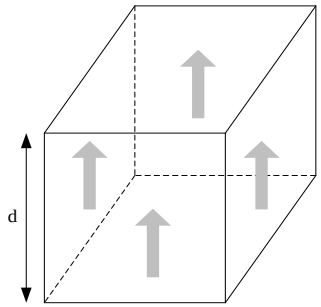


Figure 3.26. Via constructed with 4 metal sheets.

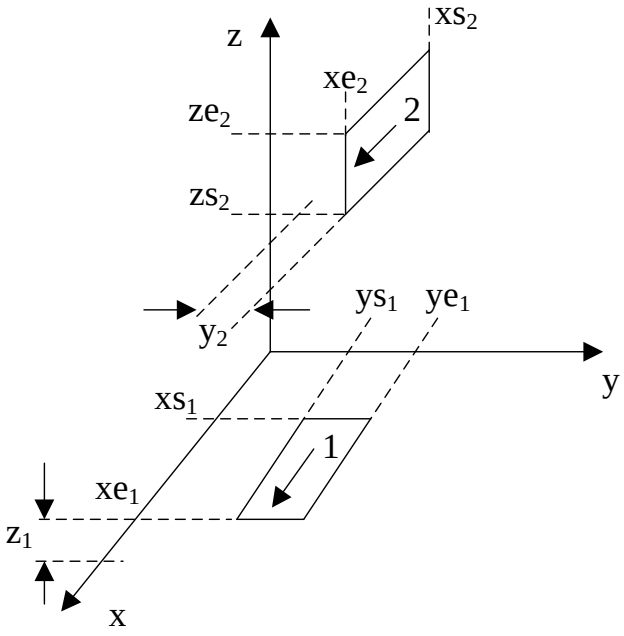


Figure 3.27. Zero thickness conductors at 90 deg angle.

$$L_{p12} = \frac{\mu}{4\pi}\frac{1}{(ye_1 - ys_1)(ze_2 - zs_2)}\sum_{k=1}^{4}\sum_{m=1}^{2}\sum_{l=1}^{2}(-1)^{l+m+k+1}[(\frac{a_k^2}{2} - \frac{c_l^2}{6})c_l \ln(b_m + \rho)$$
$$+(\frac{a_k^2}{2} - \frac{b_m^2}{6})b_m \ln(c_l + \rho) + a_k b_m c_l \ln(a_k + \rho) - \frac{b_m c_l}{3}\rho - \frac{a_k^3}{6}\tan^{-1}\frac{b_m c_l}{a_k \rho}$$
$$-\frac{b_m^2 a_k}{2}\tan^{-1}\frac{a_k c_l}{b_m \rho} - \frac{a_k c_l^2}{2}\tan^{-1}\frac{a_k b_m}{c_l \rho}] \quad (33)$$

$$a_1 = xs_2 - xe_1,\ a_2 = xe_2 - xe_1$$
$$a_3 = xe_2 - xs_1,\ a_4 = xs_2 - xs_1$$
$$b_1 = y_2 - ys_1,\ b_2 = y_2 - ye_1$$
$$c_1 = ze_2 - z_1,\ c_2 = zs_2 - z_1$$
$$Z = \frac{ze_2}{2} + \frac{zs_2}{2} - z_1,\ \rho = \sqrt{a_k^2 + b_m^2 + Z^2}$$

Figure 3.28 shows the current flows through source via and short via, respectively. The height of via, *d*, and the distance between the vias, *l*, are chosen as the values listed in Table 3.11. For example, with *d* = 0.2 mm and *l* = 1.5 mm, the partial inductances of the sheets of source via are calculated and listed in Table 3.13.

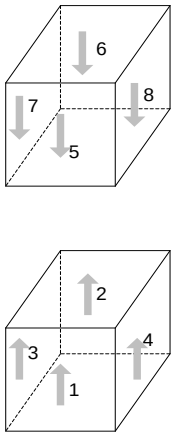


Figure 3.28. Source via and short via

Table 3.13 Partial inductance of the source via, pH, d = 0.2 mm, l = 1.5 mm

Lp11	*Lp12*	*Lp15*	*Lp16*	*Lp13*	*Lp14*	*Lp17*	*Lp18*	*Lp1*
35.78	7.39	2.64	1.99	16.28	16.28	3.92	3.92	63.26
Lp22	*Lp21*	*Lp25*	*Lp26*	*Lp23*	*Lp24*	*Lp27*	*Lp28*	*Lp2*
35.78	7.39	3.91	2.64	16.28	16.28	5.36	5.36	58.46
Lp33	*Lp34*	*Lp37*	*Lp38*	*Lp31*	*Lp32*	*Lp35*	*Lp36*	*Lp3*
35.78	7.39	2.71	2.56	16.28	16.28	5.36	3.92	61.18
Lp44	*Lp43*	*Lp47*	*Lp48*	*Lp41*	*Lp42*	*Lp45*	*Lp46*	*Lp4*
35.78	7.39	2.71	2.56	16.28	16.28	5.36	3.92	61.18

The partial inductance of sheet 1 is calculated using Eq. (34), and the partial inductances of other sheets can be calculated using the similar formula.

$$Lp1 = Lp11 + Lp12 + Lp13 + Lp14 - Lp15 - Lp16 - Lp17 - Lp18 \tag{34}$$

The partial inductance of the via is obtained using Eq. (35). The total inductance of the plane pair is obtained by adding the partial inductances of the plane and via together as shown in Table 3.14.

$$Lpvia = Lp1 \,||\, Lp2 \,||\, Lp3 \,||\, Lp4 \tag{35}$$

Comparing to the partial inductance of via and total inductance obtained using other methods [8], the PPP approach shows agreement with hybrid method and PEEC solver. When via length is long, i.e., 1 mm, and vias are close, i.e., 1.5 mm, some difference is found between the values of via inductance obtained using closed-form expression (Eq. (33)) and other two methods. Eq. (35) shows that the 4 sheets on the via sides are connected in parallel. Thus, the top and bottom of the via are shorted in this method and the current is assumed to flow uniformly on the sheet, which causes the difference compared to other methods.

Table 3.14 Comparison of partial inductance of via and total inductance

d, mm	*l*, mm	PPP Approach			$L_{via\ i}$ [8]		L_{total} [8]	
		$L_{plane\ i}$	$L_{via\ i}$	L_{total}	Hybrid	PEEC solver	Hybrid	PEEC solver
0.2	1.5	53.8	15.24	138.1	14.6	16.0	131.5	141.7
	25.5	174.0	18.72	385.44	17.1	18.6	393.0	423.0
1	1.5	118.1	167.42	571.0	190.4	189.6	668.0	621.4
	25.5	715.4	257.33	1945.5	251.8	252.4	1973.2	1969.4

3.15. PLANE INDUCTANCE WITH DIFFERENT SHORT LOCATIONS

The plane inductance changes when the decoupling capacitor is placed at different locations on the board. When the decoupling capacitor is placed at different locations on the whole board, the entire information of the board inductance can be easily obtained by applying the PPP approach, which is helpful in PDN design. Figure 3.29 shows the geometry for board inductance test. The plane size is 50 mm × 50 mm with the spacing of 0.2 mm. The via size is 0.5 mm × 0.5 mm. The source current is fed at the center of the plane and at a corner of the plane, respectively. The short via is placed around the source from as close as 1 mm to the edge of the board.

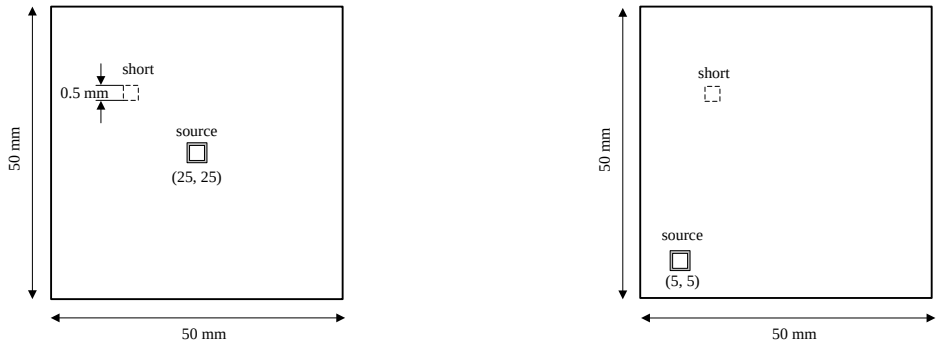


Figure 3.29. Geometry for board inductance test. (a) Source fed at center. (b) Source fed at a corner.

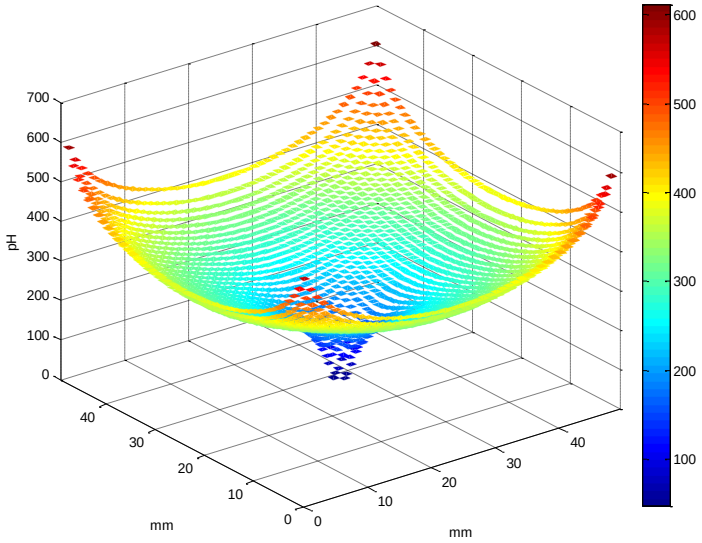


Figure 3.30. 3D plot for inductance with the source fed at center and the short placed at different locations on the board.

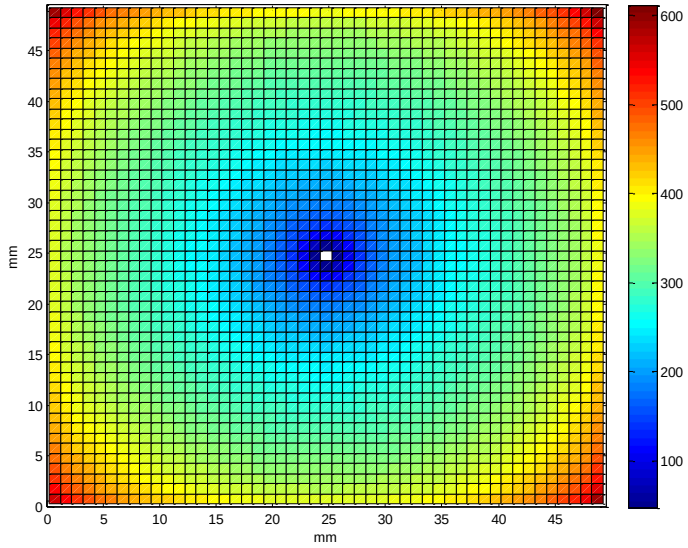


Figure 3.31. 2D plot for inductance (pH) with the source fed at center and the short placed at different locations on the board.

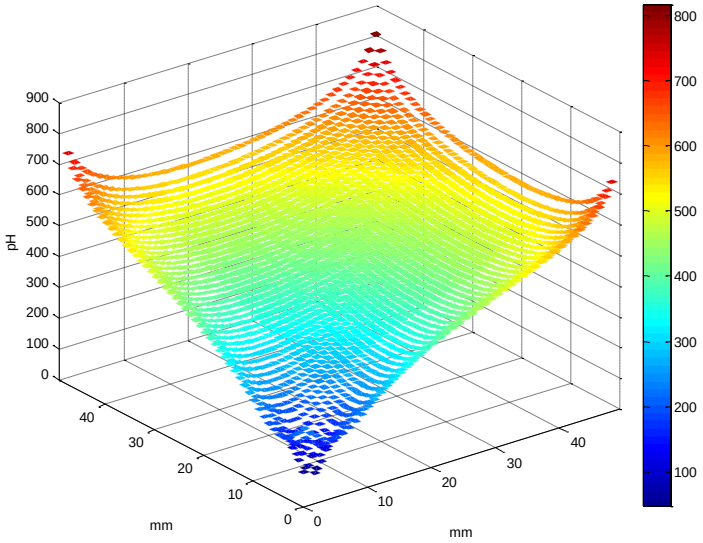


Figure 3.32. 3D plot for inductance (pH) with the source fed at corner and the short placed at different locations on the board.

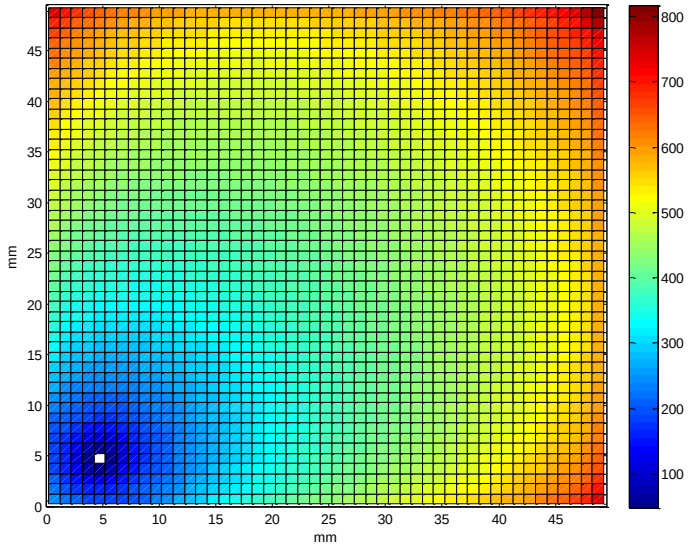


Figure 3.33. 2D plot for inductance (pH) with the source fed at corner and the short placed at different locations on the board.

Figure 3.30 and Figure 3.31 show the plane inductances with the source fed at center and the short at different locations plotted in 3D and 2D, respectively. Figure 3.32 and Figure 3.33 show the plane inductances with the source fed at a corner plotted in 3D and 2D, respectively. The plane inductance increases with increasing distance between the source and short. The largest inductances occur when short is at the corners of the board.

When the source location is fixed, the plane inductance at any location on the board can be easily obtained from the plotted inductance figure. In PDN design, the information of inductance is helpful for designer to determine where to place the decoupling capacitor on the board.

3.16. APPLICATION IN PDN DESIGN

The PPP approach can be applied in PDN design to determine the portion of the inductance in plane. However, we need to consider the limitation of memory usage and simulation time. The capability of the code performance is tested on the computer with 32 GB memory and 2 processors (Intel(R) Xeon(R) CPU X5450 @ 3.00 GHz 2.99GHz).

The largest plane size that can be handled is found to be 150 mm × 150 mm when sub-mesh method is applied with 1mm uniform cell size. The total simulation time to get the inductance value is 1400 sec, and peak memory usage is 99 % (Table 3.15). If plane size is larger, it's not efficient in either simulation time or memory usage to apply the PPP approach.

Table 3.15 Code performance for large geometry

Plane Size	Unknowns	Memory Usage	Time
150mm × 150 mm	68248	30 GB	1400 sec

The inductance of a pair of PWR/GND planes can be separated as the via partial inductance and plane partial inductance as shown in Table 3.14. When the plane pair spacing is small, i.e., 0.2 mm, the plane partial inductance is more dominant than the via partial inductance no matter two vias are close or far. Both plane partial inductance and

via partial inductance increase with increasing plane pair spacing, i.e., 1mm. However, the via partial inductance is more dominant than plane partial inductance when plane pair spacing is large and two vias are close. The plane partial inductance increases as the distance between two vias increasing. If the distance between two vias is sufficiently large, the plane partial inductance is less affected with an additional increase of the distance between two vias.

The above observation gives the proper limitation to apply the PPP approach, and also gives insights and design guide lines in PDN design for the placement of vias in PWR/GND planes.

4. CONCLUSION

An accurate and efficient approach to fast calculate the plane pair inductance is proposed base on the PPP approach. The approximation criterion is studied to speed up calculation without loss of the accuracy. Compute time analysis shows that most time is spent on stamping MNA matrix and solving it. The total compute time is proportional to the number of unknowns with the exponential of 1.5. Compared to cavity model, the PPP approach shows much higher efficiency to calculate plane inductance when multiple contacts exist. Non-uniform mesh method is studied to reduce the size of MNA matrix. The minimum area of sub-mesh region to get enough accuracy is investigated. By plotting the current vector on the plane, it can be clearly seen that the current flows out of the source and flows into the short. With applying sub-mesh near the via region, the calculation is much faster and memory usage saving with enough accuracy.

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II MEASUREMENT OF MULTIPLE SWITCHING CURRENT COMPONENTS THROUGH A BULK DECOUPLING CAPACITOR

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ABSTRACT

This paper presents a measurement-based data-processing approach to obtain parameters of multiple current components through a bulk decoupling capacitor for power integrity studies. A lab-made low-cost current probe is developed to measure the induced voltage due to the time-varying switching current. Then, a post data-processing procedure is introduced to separate and obtain the parameters of multiple current components. The results obtained by the proposed method are validated with other approaches.

1. INTRODUCTION

Modern digital integrated circuits (ICs) can operate at an internal clock frequency of more than several GHz and consume a current of up to tens of amperes. A large portion of the total current is time-varying, which inevitably generates voltage fluctuations in the power distribution network (PDN) [1][2][3]. With faster switching speed, higher circuit density, lower supply voltages and smaller feature size in IC design, the voltage fluctuations become a serious issue, affecting power and signal integrity (PI & SI) as well as causing electromagnetic interference (EMI) problems [4], [5].

To counter the effect of the PDN noise, decoupling capacitors can be added near the ICs [6][7][8], which act as local sources of charge for switching circuits and reduce the voltage fluctuations in the PDN. Other solutions may include the usage of a thin power/ground plane pair, multiple vias for decoupling capacitor connections, etc., to decrease the impedance of the PDN. An optimal design for power integrity highly depends on the accurate model of the PDN and the knowledge of the switching current drawn from the PDN by ICs.

For most printed circuit board (PCB) designers, the switching current information is usually unavailable. This makes measurement techniques more attractive for practical power integrity designs. In consumer electronic products, usually power traces are used for supplying voltage. In this case, the switching current of an IC can be approximately obtained by measuring the current flowing through the decoupling capacitors placed adjacent to the IC [9].

However, in some real-world hardware measurements, it is found that multiple current components could exist in the time-varying current flowing through a decoupling capacitor. This challenging issue of measuring multiple current components was not addressed in [9]. In this paper, a post data-processing procedure is developed to separate the effects of different current components, and to obtain the parameters important for power integrity studies.

Further, when the current through a bulk decoupling capacitor is of interest, it needs to be measured at the frequencies as low as a few hundred KHz. Usually simple loop probes do not work well when frequency is below a few tens of MHz, due to their poor sensitivity. Typical commercial low-frequency current probe uses the Rogowski coil

structure, and the current under measurement needs to flow through the probe. In other words, to measure the current through a decoupling capacitor, a wire needs to be added in series with the decoupling capacitor and the wire has to go through the probe. The added wire can introduce unwanted parasitic inductance. Furthermore, in compact consumer electronic products, components on PCB are typically very dense. In some cases, it is very difficult to modify the PCB and add the required wire for current measurement using a Rogowski-coil current probe. In this paper, a lab-made low-cost current probe is developed to deal with these difficulties. The simple probe is very small in size, suitable for dense-PCB applications. In addition, it is sensitive enough for low-frequency measurements, and it does not require any modifications in PCB.

2. PROPOSED CURRENT PROBE

The time-varying current through a bulk decoupling capacitor has frequency components usually ranging from a few hundred KHz to a few MHz. As mentioned earlier, a simple loop probe does not have enough sensitivity at these low frequencies with a small size. In this paper, a current probe is proposed based on a surface mount common-mode choke. Although the size is very small, the ferrite core in the choke can significantly increase the sensitivity of the proposed probe. As shown in Figure 2.1, the common-mode choke has a bottom ferrite shield and two sets of copper-wire coils at opposite directions. To modify the choke to a loop probe, the bottom ferrite shield needs to be removed and only one coil needs to be used, as sketched in Figure 2.1.

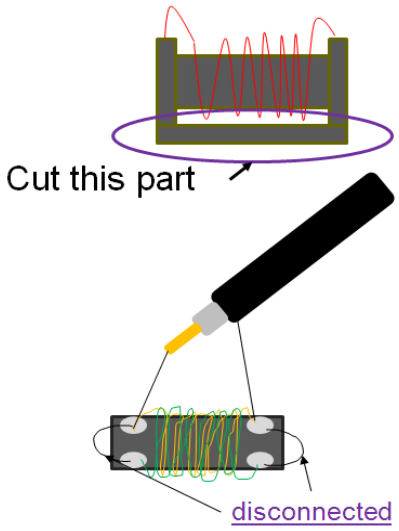


Figure 2.1. Structure of the proposed low-cost probe.

To calibrate the lab-made low-frequency probe for bulk-capacitor current measurement, it was first characterized using the experimental setup as shown in Figure 2.2. A bulk capacitor with the same package size as the one used in the real product was soldered in a 50 ohm trace. One end of the 50 ohm trace was connected to port 1 of a network analyzer and the other end was terminated with a 50 ohm load. The current probe was placed above the bulk capacitor with the coil perpendicular to the direction of

the current flow. Port 2 of the network analyzer was connected to the probe output, and the S_{21} parameter was measured. The equivalent circuit of this measurement setup is shown in Figure 2.3. From the S_{21} measurement, the transfer coefficient between the induced voltage at the probe output and the current flowing through the bulk capacitor can be calculated. As shown in Figure 2.4, this transfer coefficient can be well characterized using a mutual inductance of 12.5 nH in the frequency range from 100 KHz to 10 MHz.

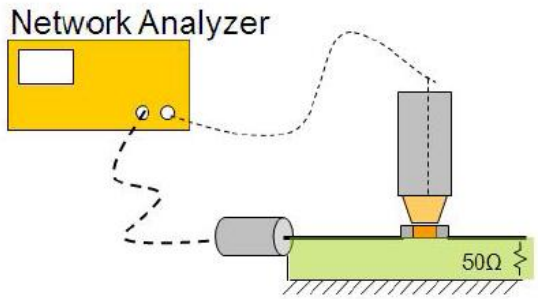


Figure 2.2. Measurement setup for current probe calibration.

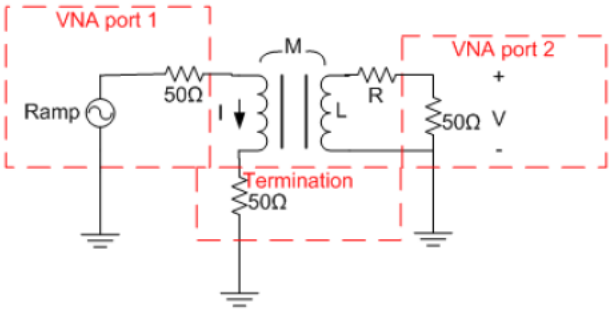


Figure 2.3. Equivalent circuit of the measurement setup shown in Figure 2.2.

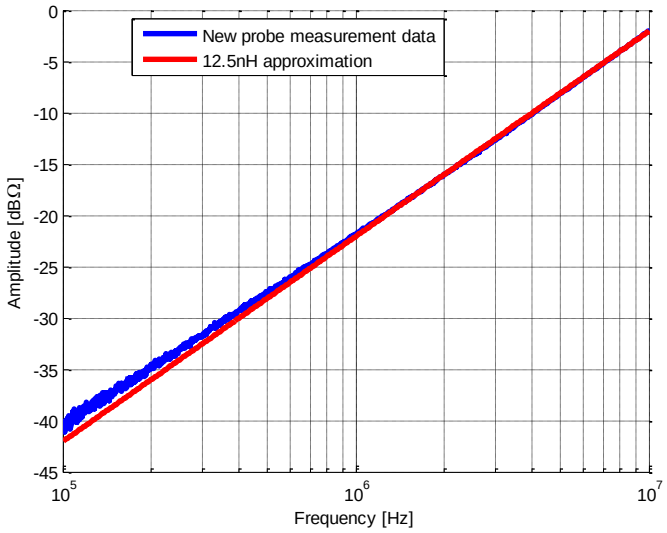


Figure 2.4. Transfer coefficient of the lab-made current probe for a specific bulk capacitor package.

3. SEPARATION AND CHARACTERIZATION OF MULTIPLE CURRENT COMPONENTS

When using the lab-made current probe to measure the time-varying current flowing through the bulk decoupling capacitor, the current can be obtained from the measured voltage at the probe output as Eq. (1),

$$I = \frac{1}{M}\int V dt \tag{1}$$

where M is the mutual inductance obtained in Figure 2.4, and V is the induced voltage in the probe as a function of time that can be measured using an oscilloscope. In this paper, as shown in Figure 3.1 the current flowing through a 10 μF bulk decoupling capacitor in a functioning hardware of a real electronic device was measured using the lab-made current probe. The bulk decoupling capacitor has the same package size as the one used in the calibration and the mutual inductance was found to be 12.5 nH.

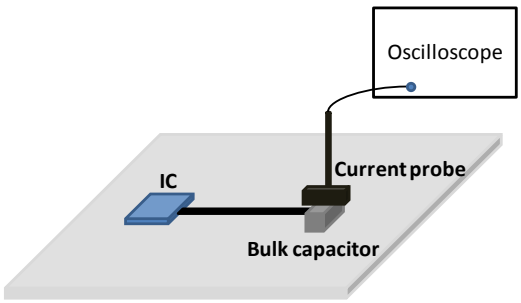
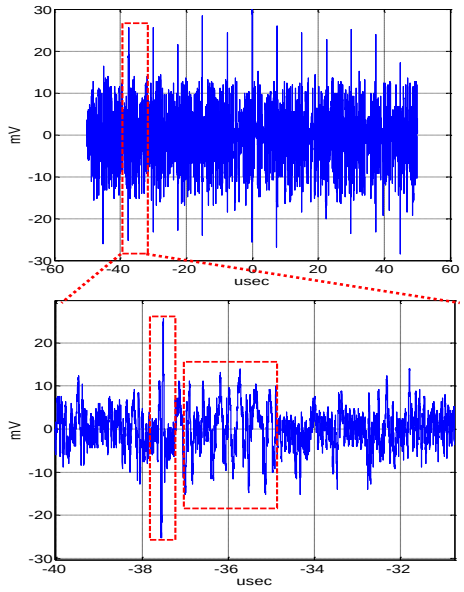


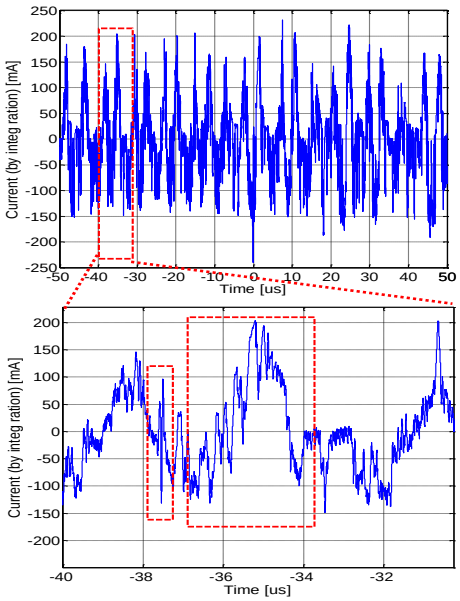
Figure 3.1. Experimental setup of the bulk capacitor current measurement using the lab-made current probe.

The voltage induced in the current probe and the current calculated from Eq. (1) are shown in Figure 3.2 (a) and (b), respectively. It is found that the peaks in Figure 3.2 (a) have a pulse width of approximately 50 ns. On the other hand, the higher peaks in Figure 3.2 (b) have a transition time of approximately 1 μs. The current pulses with a 50 ns transition time can also be observed in Figure 3.2 (b), but with lower magnitudes. In

other words, there are two current components, with the transition times of 50 ns and 1 μs, respectively. The fast component results in the induced voltage peaks due to the inductive nature of the current probe, even though its magnitude is lower.



(a)



(b)

Figure 3.2. Induced voltage and corresponding current. (a) Measured induced voltage in the current probe; (b) Current calculated from Eq. (1).

It is very difficult, if not impossible, to extract the accurate information about the multiple current components directly from Figure 3.2 (b), although the information of the current component that contributes to the induced voltage peak (50 ns in this case) can be obtained relatively easily. The highest peak in Figure 3.2 (a) can be triggered, and multiple measurements can be performed. Then, by averaging the multiple measured results, a clear voltage waveform can be obtained as shown in Figure 3.3. In this waveform, only the portion related to the 50 ns current component exists. Random noise and other current components that are not synchronized are mostly eliminated through this procedure. Unfortunately, only one current component can be measured using this method.

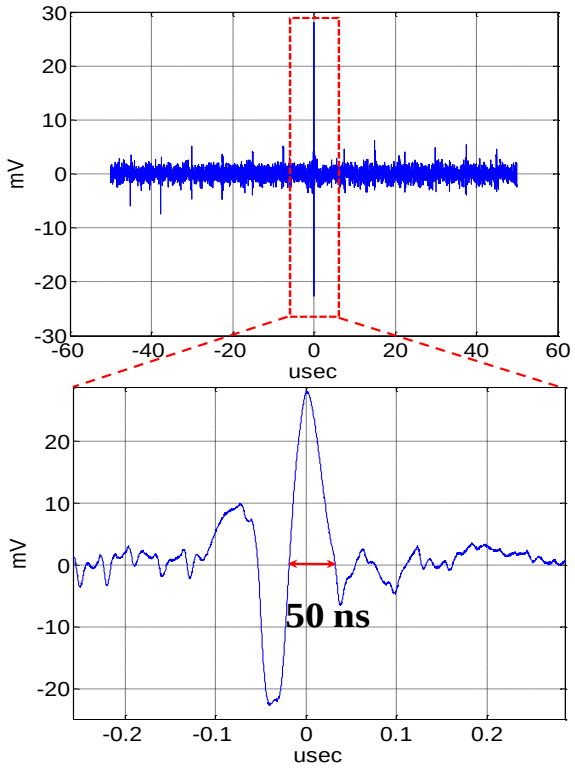


Figure 3.3. Measured current component that results in the induced voltage peaks using the triggered averaging technique.

In this paper, a post data-processing procedure is developed to separate the different current components from the induced voltage measurement in Figure 3.2 (a). First of all, as shown in Figure 3.4, a digital signal processing (DSP) low-pass filter with

a cut-off frequency of 5 MHz is applied to the induced voltage data to obtain the portion due to the slower current component. Secondly, subtract the portion due to the slower current component from the original induced voltage data to get the remaining portion due to the faster current component. Then, the current waveform for each component is calculated by integrating the corresponding voltage waveform as in Eq. (1). The procedure is performed for multiple measurements. Finally, using the previously mentioned triggered-averaging technique, a clear waveform for each current component is obtained with random noise eliminated. Through this procedure, different current components are thus separated, and their peaks as well as transition times are accurately measured.

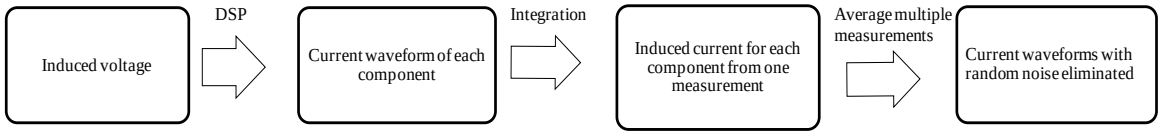
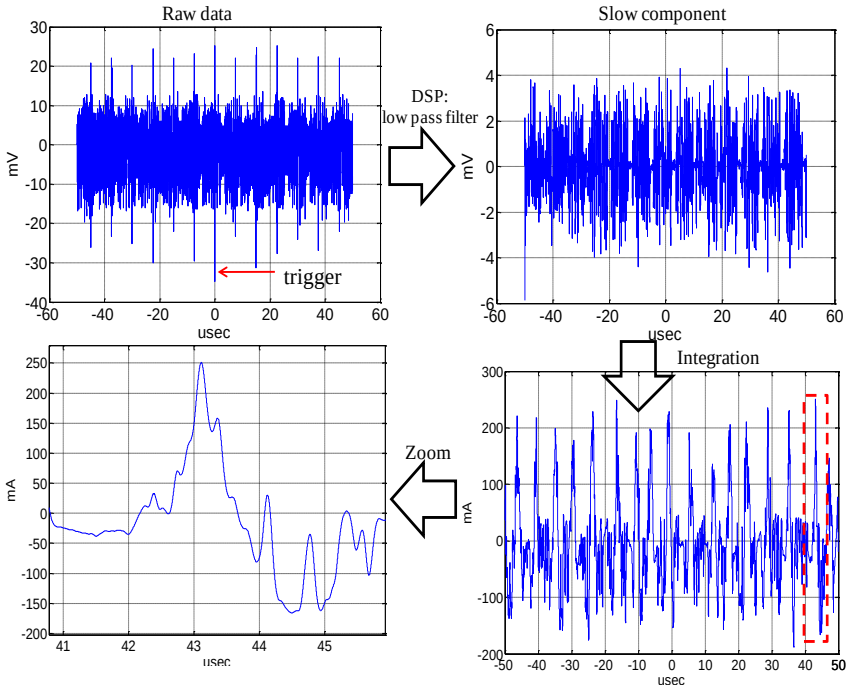


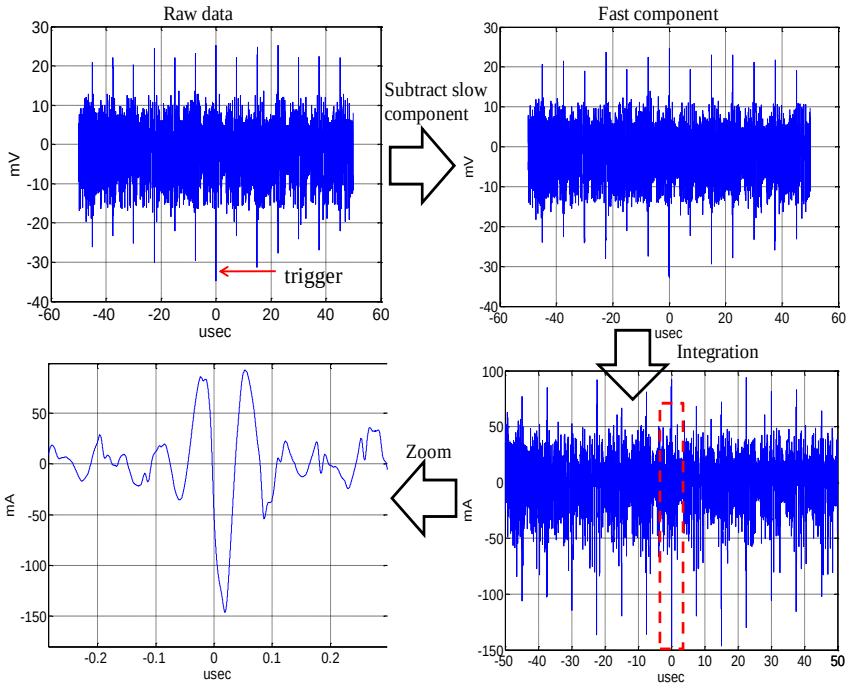
Figure 3.4. The proposed post data-processing procedure.

An example of applying the proposed post data-processing procedure is shown in Figure 3.5, where two current components are separated and their corresponding current waveforms are obtained. Then the highest peak in each waveform is identified and "triggered". This same procedure is performed for multiple measurements, and then multiple current waveforms for each current component are shifted according to the "triggered" peak and averaged. The final results for the slower and faster components are shown in Figure 3.6 (a) and (b), respectively.

The peak current and transition time values can be further obtained from Figure 3.6. The slower and faster current components have the peak values of 250 mA and 140 mA, respectively. Their corresponding transition time values are 0.7 μs and 40 ns. The parameters for the faster current component are approximately close to those calculated from Figure 3.3 (114 mA and 50 ns).



(a)



(b)

Figure 3.5. Post data processing to obtain the highest peak for current components with slow (a) and fast (b) transient time.

The parameters of the slower current component were validated using a commercial current probe, Tektronix CT-2, with a transfer coefficient of 1mV/1mA. Because this probe has a flat frequency response in its working band, the peak induced voltage in this probe is due to the slower current component since it has a higher magnitude. Then, using the same triggered-averaging technique, the peak current and transition time for the slower component were found to be 225 mA and 0.9 μs, respectively, which again are very close to the results obtained from the proposed data-processing procedure with the lab-made current probe.

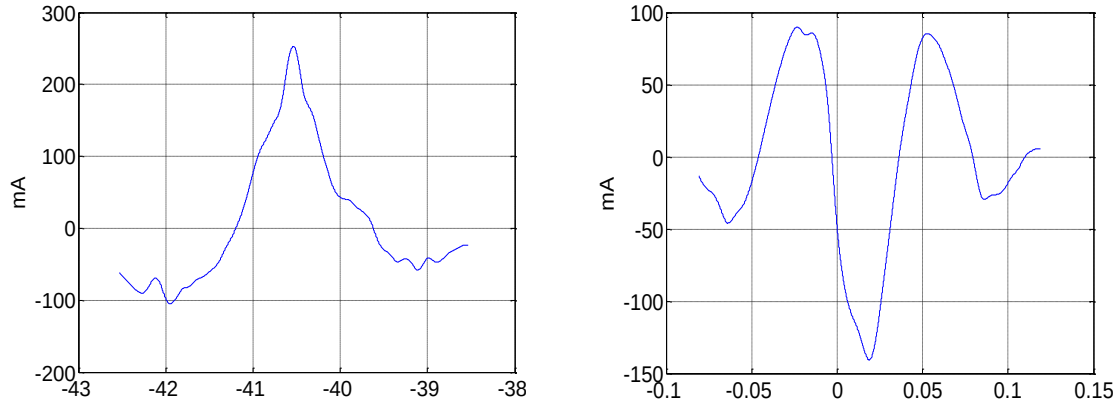


Figure 3.6. Averaged current waveforms for (a) slower and (b) faster current components when the bulk capacitor value is 10 μF.

4. CONCLUSION

In PDN design, IC switching current needs to be accurately characterized for power integrity studies. A lab-made low-cost current probe is proposed and fabricated from an off-the-shelf surface mount common-mode choke. It is very small in size, suitable for dense PCB applications. The frequency range of the developed current probe is from 100 KHz to 10 MHz. In addition, a post data-processing procedure is proposed to separate multiple current components that may exist in the switching current. This procedure relies on a low-pass DSP filter to separate the slower current component from the faster one. Triggering and averaging are also used to eliminate random noise for better measurements. The proposed procedure is validated with other measurement methods that require multiple current probes, demonstrating its effectiveness and efficiency in bulk-capacitor current measurements.

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III SWITCHING – CURRENT MEASUREMENT FOR MULTIPLE ICs SHARING A COMMON POWER ISLAND STRUCTURE

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ABSTRACT

Switching currents in active integrated circuits (ICs) generate noise in the power distribution network (PDN), which is one of the main sources for many signal/power integrity and electromagnetic interference issues in high-speed electronic devices. Accurate knowledge of the switching currents is the key to ensure a good PDN design. This paper proposes a measurement methodology, when IC information is not available, to obtain the equivalent switching current of each IC in the case where multiple ICs are connected to a common power island structure. Time-domain oscilloscope measurements are used to capture the noise-voltage waveforms at a few locations in the power island. Combining with the multi-port frequency-domain S-parameter measurement among the same locations, an equivalent switching current for each IC is calculated. The proposed method is validated at a different location in the power island by comparing the calculated noise voltage using the equivalent switching currents as excitations with the actual measured noise voltage.

1. INTRODUCTION

Modern high-speed digital systems have an increased number of integrated circuits (ICs) in printed circuit board (PCB). They could operate at an internal clock frequency up to several GHz and draw a large amount of switching current with a fast dI/dt ramping rate from the power distribution network (PDN) of the board. When multiple logic gates in ICs switch simultaneously, they induce a voltage drop in the PDN. This momentary voltage drop, when seen by the active circuits in an IC, could affect the normal operations of the IC. Further, the voltage disturbance can easily propagate in the PDN, resulting in various noise coupling and interference issues.

As the ultimate source of the PDN noise, switching currents in active devices are a key factor in PDN design. Without the accurate information, meaningful design criterions such as target impedance cannot be well defined. Further, analysis and co-modeling of signal/power integrity and interference issues become inadequate without the exact information of the potential noise sources. When detailed IC information is available, chip-level modeling has proven to be an effective way to obtain the switching current information [1], [2]. Unfortunately, IC information is proprietary and usually unavailable for most PCB designers. Measurement-based methods thus are desirable in this case for practical engineering applications. Switching currents can be directly measured using the zero-Ohm method [3], using a magnetic loop probe [4], [5], or a giant magneto-impedance (GMI) probe [6]. These direct methods can only measure the current of a single power or ground pin of the IC under study. Alternatively, switching currents can be obtained indirectly, such as based on near-field scanning [7], or by examining the silicon function status of the IC [8]. The indirect methods are usually complicated and still require a certain amount of IC information.

In this paper, a measurement-based method is developed to handle the situation where multiple ICs share a common power island and IC information is not available. Since many power pins are connected to the same power net and the ball grid array (BGA) type package does not allow access to most of these pins, direct current measurement for individual pins is impossible. However, an equivalent total switching current of each IC, instead of the exact pin currents, can still be obtained, which could effectively provide the necessary information for PDN design in the PCB level.

This work is an extension of the approach reported in [9] and [10], where the equivalent switching currents (magnitudes only) of a Field Programmable Gate Array (FPGA) associated with both the core and I/O PDNs were obtained through S-parameter and spectrum analyzer measurements. The lack of the phase information in the obtained equivalent switching currents, due to the spectrum analyzer limitation, could result in issues for optimized PDN (such as target impedance) design [4]. To address the phase issue, time-domain oscilloscope measurements are used in this work. The measured time-domain noise-voltage waveforms are then converted into the frequency domain through the Fourier transform. Together with the S-parameter measurement of the multi-port power-island structure, equivalent switching currents including both magnitude and phase are obtained.

2. THEORY AND MEASUREMENT SETUPS

According to the statistical study in [11], the total effect of multiple switching currents of an IC can be equivalently described by a single switching current located at the center of the IC footprint with acceptable accuracy, if frequency is small enough such that $d/\lambda < 0.2$, where d is the diagonal dimension of the IC package and λ is the corresponding wavelength in the PCB dielectric media. In this work, the frequency range of interest is 10 MHz to 1 GHz, which satisfies the condition. In other words, for the multiple ICs connected to the same power island structure, a single equivalent switching current can be used to describe the behavior of each IC and the current is located somewhere close to the center of the IC.

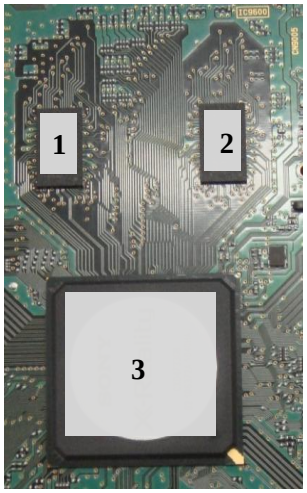
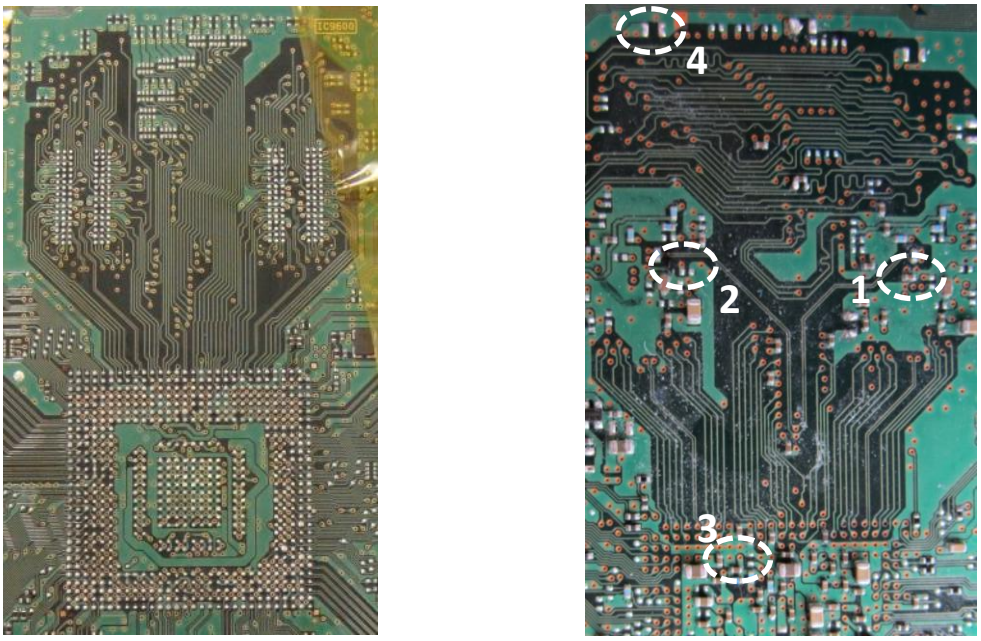


Figure 2.1. A picture of the functioning board under study: three ICs sharing a common power island structure.

A portion of the functioning PCB under study is shown in Figure 2.1, where three ICs are connected to a 1.5 V power island. The corresponding board with the ICs removed is shown in Figure 2.2. Ports 1-3 between the 1.5 V power island and the ground plane were selected for ICs 1-3, respectively, located near the centers of their footprints. Port 4 was selected at a location relatively far away from all the ICs, again between the 1.5 V power island and the ground. The fourth port is used for the validation of the proposed methodology.



(a) (b)

Figure 2.2. Same board with (a) three ICs removed (top layer) and (b) port locations (bottom layer).

As discussed earlier, each IC is assumed to draw an equivalent switching current at its corresponding port. Then, the power island under study can be modeled using a simple four-port network as shown in Figure 2.3. The Z-parameter matrix of the network can be obtained from frequency-domain S-parameter measurements.

In this work, the internal impedance between the 1.5 V and ground of each IC looking into its corresponding port is assumed to be much higher than the impedances of the power island in the board. In other words, ideal current sources I_{S1}-I_{S3} are used in Figure 2.3 to approximately model the equivalent switching currents at Ports 1-3. The S-parameters among the four ports can be measured using a board with the ICs removed, as shown in Figure 2.2. Four probes made from semi-rigid cable and SMA connector with approximately the same length were soldered to the ports, as shown in Figure 2.4. A four-port vector network analyzer (Agilent N5245A) was used to take the S-parameter

measurement. To eliminate the effects of the test fixture (probes), port extensions were performed to rotate the reference planes right to the ports.

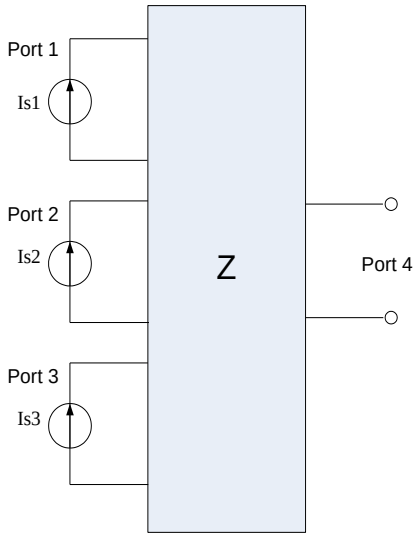


Figure 2.3. A simple four-port network describing the behaviour of the power island.

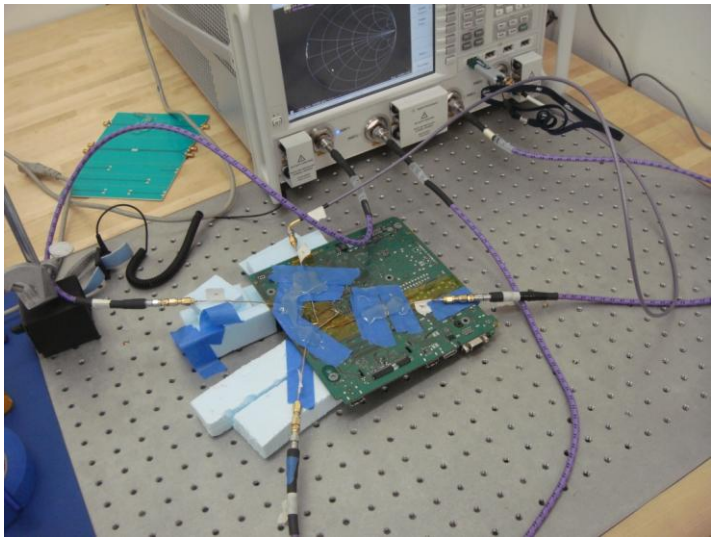


Figure 2.4. Setup of multiport S-parameter measurement.

In the equivalent network shown in Figure 2.3, the port voltages and currents are related as Eq. (1),

$$\begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \begin{bmatrix} I_{S1} \\ I_{S2} \\ I_{S3} \\ 0 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \tag{1}$$

where the impedance matrix $[Z]$ is obtained from the measured S-parameter matrix $[S]$ as Eq. (2).

$$[Z] = Z_0 \frac{[I]+[S]}{[I]-[S]} \tag{2}$$

$[I]$ is the 4 × 4 identity matrix, and $Z_0 = 50\Omega$ is the port impedance. It can be easily shown from Eq. (1) that,

$$\begin{bmatrix} I_{S1} \\ I_{S2} \\ I_{S3} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix}^{-1} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{3}$$

and

$$V_4 = \begin{bmatrix} Z_{41} & Z_{42} & Z_{43} \end{bmatrix} \begin{bmatrix} I_{S1} \\ I_{S2} \\ I_{S3} \end{bmatrix}. \tag{4}$$

In other words, the equivalent switching currents drawn by the three ICs can be easily calculated from the port voltages, which can be obtained from measurements. A 4-

channel oscilloscope (Agilent MSO8104A) was used in this work. The time-domain voltages at the four ports were simultaneously measured and recorded, when the device under study was active under the normal operation. Both the magnitudes and phases of the noise voltages can be obtained from the time-domain oscilloscope measurement through the Fourier transform. As a result, the phase information of the equivalent switching currents can also be obtained, which provides unique advantages in PDN design as discussed earlier. The setup of the oscilloscope measurement is shown in Figure 2.5. To reduce the setup effect for time-domain measurement, the input impedance of the oscilloscope is 50 ohm to avoid reflection, and cables with same length and the same length semi-rigid probes with SMA connectors were used for all 4 ports.

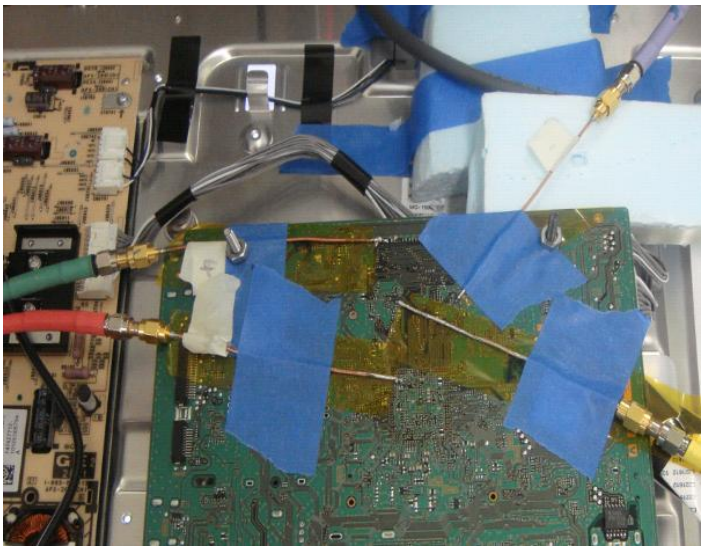


Figure 2.5. Setup of oscilloscope measurement.

To test the effectiveness of the proposed methodology, two different board conditions were studied. In the first case, a 10 μF capacitor was located at Port 4, while the capacitor was removed in the second case. The effect of the capacitor was included in the S-parameter measurement, when it was present in the board. Thus, the same equations of Eq. (3) and (4) were used for both cases, except that the Z-parameters were different.

3. RESULTS AND DISCUSSIONS

The measured noise-voltage waveforms were recorded first, and then transformed to the frequency domain using the Fast Fourier Transform (FFT). The magnitude spectra of the noise voltages at the IC ports (Ports 1-3), without the 10 μF decoupling capacitor placed at Port 4, are shown in Figure 3.1 in the frequency range of 10 MHz to 1 GHz. Similar voltage spectra at the ports were observed with the decoupling capacitor placed at Port 4 and are plotted in Figure 3.2. Comparing Figure 3.1 and Figure 3.2, it can be seen that the magnitudes of the low-frequency spectral components can be slightly reduced by the decoupling capacitor.

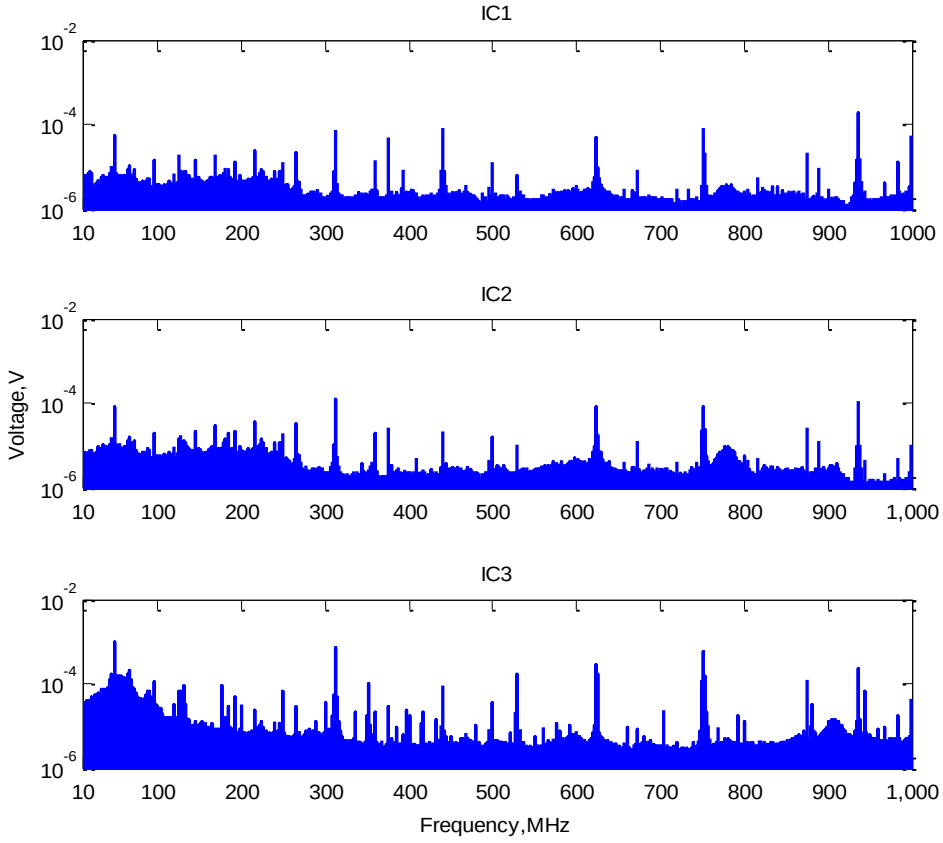


Figure 3.1. Magnitude spectra of the noise voltages at the IC ports (Ports 1-3) in the frequency range of 10 MHz to 1 GHz: without the 10 μF decoupling capacitor placed at Port 4.

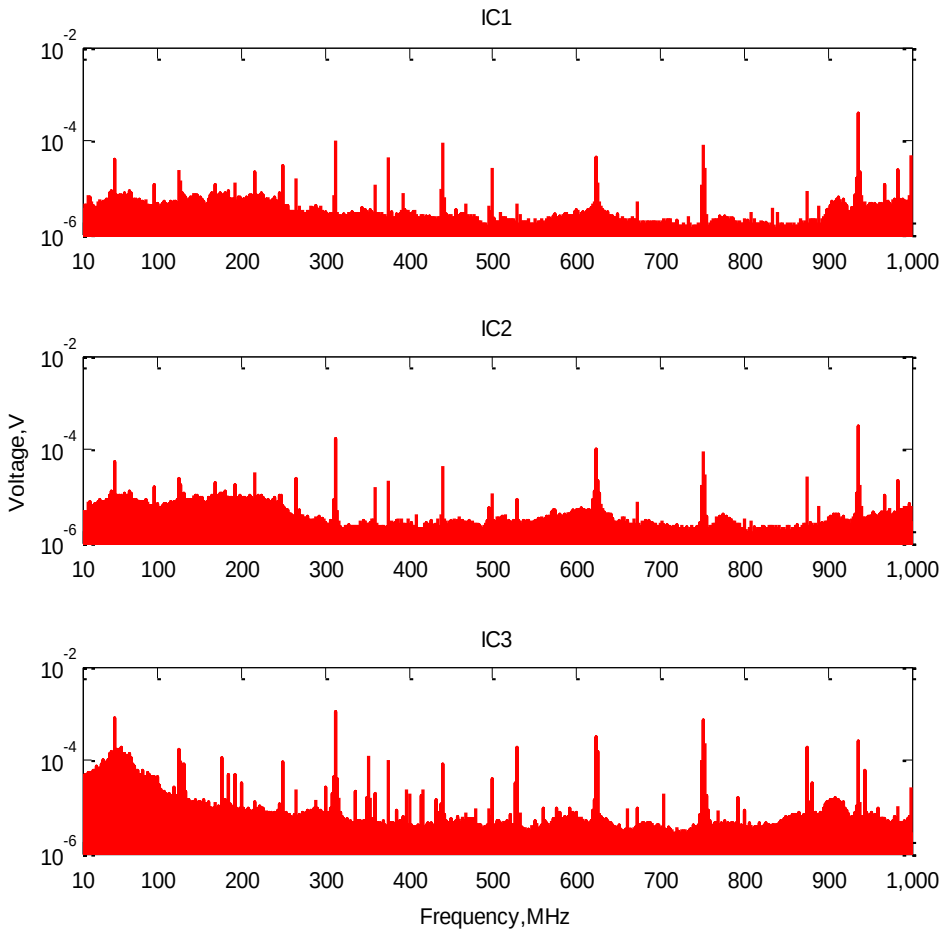


Figure 3.2. Magnitude spectra of the noise voltages at the IC ports (Ports 1-3) in the frequency range of 10 MHz to 1 GHz: with the 10 μF decoupling capacitor placed at Port 4.

After the noise voltages and the multiport S-parameters were measured, the equivalent switching currents drawn by the ICs were calculated from Eq. (3). It is worth pointing out that the number of the frequency points in the S-parameter measurement (6401 in this example) was much smaller than what was used in the FFT for the noise-voltage spectra. Interpolation was then applied to the measured S-parameters to match the frequency points in the FFT outputs.

The magnitudes of the calculated equivalent switching currents drawn by ICs 1-3 are shown in Figure 3.3, Figure 3.4, and Figure 3.5, respectively. In each figure, the results of the two cases, with and without the decoupling capacitor at Port 4, are compared. Under the assumption that the internal power/ground impedances of the ICs are much higher than the impedances of the power island structure, the change of the impedance of the power island with or without the decoupling capacitor is relatively small compared to the impedance of ICs. Thus, the equivalent switching current drawn by each IC shall remain the same regardless of the existence of the decoupling capacitor at Port 4, and the current source model can be extracted from measurement to represent each IC. However, some differences can be clearly observed in all three figures. This is partially due to the fact that the assumption may not be accurate, especially at high frequencies. Other possible reasons include measurement accuracy and the simplification of noise sources. Further improvement of the methodology is needed.

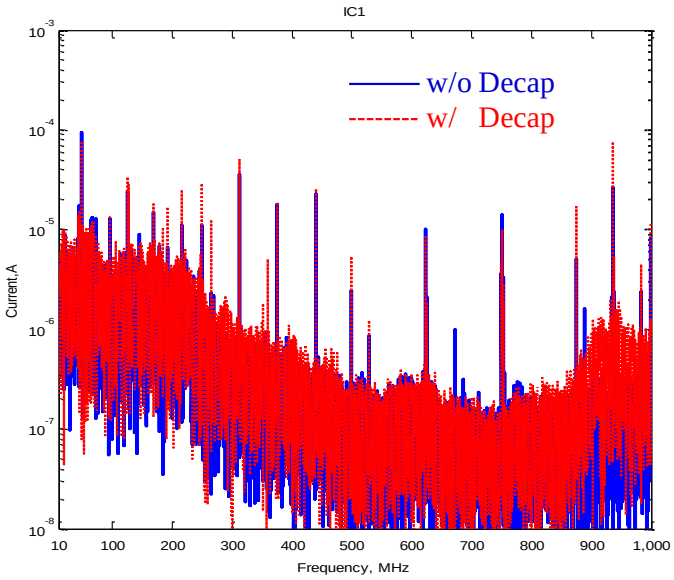


Figure 3.3. Magnitudes of the calculated equivalent switching current drawn by IC 1 for both cases of with and without the decoupling capacitor at Port 4.

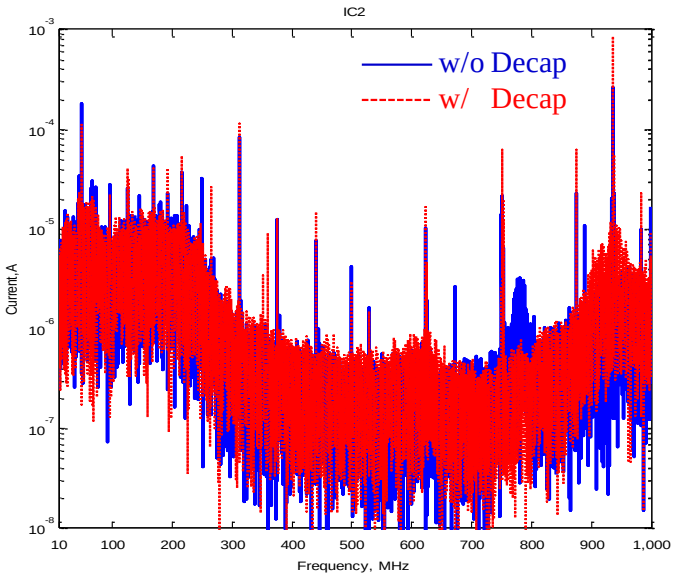


Figure 3.4. Magnitudes of the calculated equivalent switching current drawn by IC 2 for both cases of with and without the decoupling capacitor at Port 4.

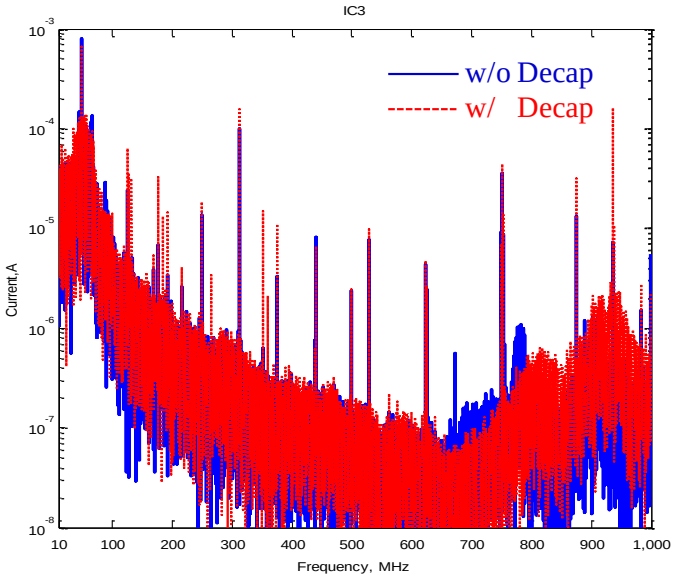


Figure 3.5. Magnitudes of the calculated equivalent switching current drawn by IC 3 for both cases of with and without the decoupling capacitor at Port 4.

The voltage at Port 4 calculated from the equivalent switching currents at Ports 1-3 by Eq. (3) provides further validation of the proposed methodology. The calculated voltage magnitudes for the two cases of without and with the decoupling capacitor at Port 4 are compared with the measured voltage in Figure 3.6 and Figure 3.7, respectively. It can be seen that some agreement has been achieved, with differences in magnitudes. The correlations presented in both Figure 3.6 and Figure 3.7 are similar. Comparing the calculation and measurements in Figure 3.6 and Figure 3.7, the calculation showed little impact of the decoupling capacitor, i.e., at 950 MHz, while measurements showed impact in current magnitude. The calculation is based on the assumption that the ICs currents drawn from the power island do not change much with or without the decoupling capacitor at Port 4, which makes the current source model simplified but also introduces some errors. Some difference in current spectra of each IC with and without the decoupling capacitor at Port 4 can be observed in Figure 3.3, Figure 3.4 and Figure 3.5, indicating the change of the current drawn from the power island due to the effect of the decoupling capacitor. Thus, measurement showed the impact due to the capacitor and calculation didn't. The results demonstrate the possibility of the proposed methodology where actual multi-pin switching-current measurements can be simplified to the equivalent switching-current estimation. Although the accuracy at this stage needs further improvement, the methodology provides useful current information, acceptable for practical engineering applications.

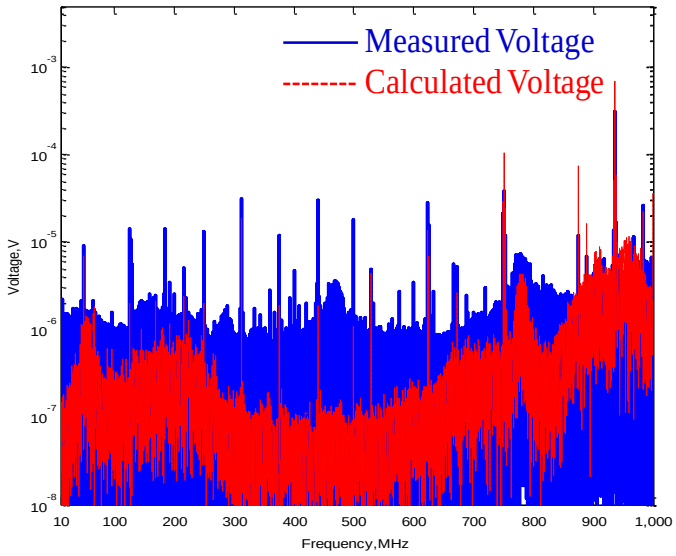


Figure 3.6. Magnitude comparison between the calculated and the measured noise voltages at Port 4, without the decoupling capacitor placed at Port 4.

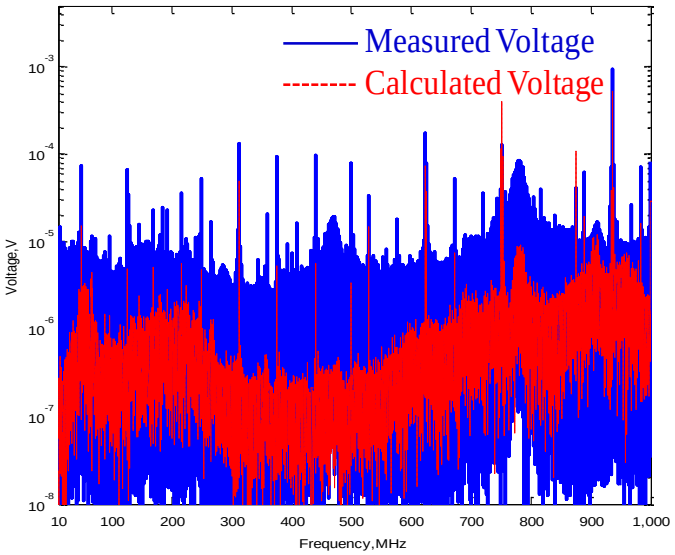


Figure 3.7. Magnitude comparison between the calculated and the measured noise voltages at Port 4, with the decoupling capacitor placed at Port 4.

4. CONCLUSION

A methodology to obtain the equivalent switching current drawn by an IC is proposed in this paper, which can be used in the cases where current measurement for every power/ground pin is not possible. The proposed methodology was applied to a power island structure connected with three ICs. Based on the oscilloscope measurement of the noise voltages at specially-selected ports, as well as the S-parameters among the ports, the equivalent switching current of each IC was calculated. The time-domain measurement of the noise voltages can provide phase information, which is important to achieve better PDN designs. The proposed methodology was validated by studying two different cases of with and without a decoupling capacitor placed at a fourth port, and by comparing the calculated noise voltage at the fourth port from the equivalent switching currents at the ICs with the directly measured noise voltage at Port 4. The results demonstrate the possibility of the methodology in engineering applications, although the accuracy needs more improvement. Full wave simulation will be applied to improve the methodology. A simple geometry with power island structure will be created, and multiple current sources can be added to represent ICs in the simulation tool, which will provide important insights for assumption evaluation and algorithm improvements, such as sensitivity of the methodology to the location of Port 4, error analysis as a function of frequency, etc.

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SECTION

2. CONCLUSIONS

Three topics related to PDN design are studied and discussed in the thesis, including plane pair inductance calculation, measurement and characterization of the switching currents through the bulk decoupling capacitor, and measurement of switching currents of ICs sharing a common power island structure.

In the first topic, an accurate and efficient approach to fast calculate the plane pair inductance is proposed base on the plane pair PEEC method. By applying the differential cell pair in the model, the coupling between differential cell pairs decays much faster compared to the coupling between the cells, and the number of unknowns is reduced by factor 2. The approximation criterion is studied and proposed. With approximation method applied, the calculation time is reduced significantly, and the accuracy keeps high. Compute time analysis shows that the total compute time is proportional to the number of unknowns with the exponential 1.5, which is determined by the time spending on stamping and solving MNA matrix. When multiple shorts exist, the proposed plane pair PEEC approach shows much higher efficiency to calculate the plane pair inductance compared to the cavity model. The current distribution shows that the current is concentrated near the via, and non-uniform mesh method is studied to reduce the size of MNA matrix. The weighted KCL equation for the transition between the uniform mesh and non-uniform mesh is created. With applying the non-uniform mesh near the via region, the calculation is much faster and memory usage saving with enough accuracy. Later on, the via inductance and capacitance of the decoupling capacitor can be easily implemented into the MNA matrix to obtain the impedance of the board.

In the second topic, the measurement and characterization of current components of the bulk decoupling capacitor is studied. A lab-made low-cost current probe is proposed and fabricated to achieve the requirement of high sensitivity and low frequency range. A post data-processing procedure is proposed to separate multiple current components existing in the switching current. A low-pass DSP filter is applied in this procedure to separate the slower current component from the faster one. The proposed

procedure is demonstrated for the effectiveness and efficiency in bulk-capacitor current measurements by validating with other measurement methods.

In the third topic, the methodology to obtain the equivalent switching currents drawn by three ICs sharing a common power island structure is proposed. The noise voltage of each IC is measured at the specially-selected port using oscilloscope, and the phase information of the noise voltages can be obtained through FFT. The S-parameter among multiple ports can be measured, and the equivalent switching current of each IC is calculated with the information of noise voltages and impedance. The proposed methodology is validated by using two different cases of with and without a decoupling capacitor placed at a fourth port. By comparing the calculated noise voltage and the measured noise voltage at the fourth port, it demonstrates the possibility of the methodology in engineering applications. The accuracy of this method needs more improvement. In the future work, full wave simulation can be applied to improve the methodology, which will provide more important insights for assumption evaluation and algorithm improvement.

APPENDIX

The code to calculate the plane pair inductance described in Chapter 1 is implemented using MATLAB. Three packages of codes are implemented for uniform mesh method, sub-mesh method with far vias and sub-mesh method with close vias. The equations used to build MNA matrix using different mesh methods are also presented in Chapter1. Detail comments can be found in the codes for easy understanding.

The code for uniform mesh method can handle the case with one short via or multiple short vias. The code for sub-mesh method can only handle the case with one source via and one short via.

In the beginning of the code, the plane pair geometry needs to be manually defined. For the code applied to uniform mesh method, the input parameters include plane size, plane pair spacing, via size, cell size and coordinates of vias. For example,

```
x = 20; % mm, plane size in x direction
y = 20; % mm, plane size in y direction
h = 0.8; % mm, plane pair spacing

xsize = 1/2 ; % mm, uniform mesh size in x direction
ysize = 1/2 ; % mm, uniform mesh size in y direction

short = [4 4]; %mm, x and y coordinates for single short
% short = load ( 'short.txt' ); % for multiple shorts

source = [12 12]; % In general, only one source is applied.
% source = load ('source.txt');

ptx_size = 2 ;% mm, port size in x direction. If the port is a node, set the port size as zero.
pty_size = 2  ;% mm, port size in y direction
```

Here *x* and *y* represent the plane dimension in x and y directions. *h* represents the plane pair spacing. The port shape is set as rectangular with the size defined in x and y directions. If the port is treated as a node, the port size needs to be set as zero. The uniform cell size cannot be larger than the port size if the port size is not zero. The value of the plane size divided by the uniform cell size must be an integer when choosing the cell size. If the port size is not zero, the coordinates of short or source are defined as the

low-left corner of the via. For multiple short vias, their coordinates can be saved in a txt file and loaded into MATLAB.

For the code applied to sub-mesh method, an additional parameter needs to be set besides the parameters shown above. The number of uniform cells ("adaptive_num") adjacent to the via which are subdivided into sub-mesh cells needs to be set. In the code for far via case, "adaptive_num = 1" means that along each diagonal of the via, the sub-mesh region is extended to 1 uniform cell in each side of the diagonal and the total sub-mesh region is the area covered by connecting these uniform cells adjacent to the via. In the code for close via case, "adaptive_num = 1" means that along each diagonal of the rectangular area between the two vias, the sub-mesh region is extended to 1 uniform cell in each side of the diagonal and the total sub-mesh region is the area covered by connecting these uniform cells in x and y directions. For example,

```
adaptive_num = 2 % define the number of uniform cells adjacent to port which are
                   subdivided into sub-mesh cells.
```

In output, the matrix equation to solve the unknowns is expressed as [A][C]=[B], where C is the matrix contains unknowns including the voltage of each node and the current on each partial inductance. The parameter with the name "unknowns" gives the total number of unknowns solved in C matrix. The parameter with the name "L" gives the calculated plane pair inductance.

VITA

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