Implementation of SOI-Based Rib Waveguide for High-Speed Optical Interconnect

Siti Sarah Binti Md Sallah¹, Sawal Hamid Md Ali¹, P.Susthitha Menon², Nurjuliana Binti Juhari³, Md Shabiul Islam^{2,4}

¹Faculty of Engineering and Build Environment, Universiti Kebangsaan Malaysia, 43650 Bangi, Selangor, Malaysia.
 ²Institute of Microengineering and Nanophotonics (IMEN), Universiti Kebangsaan Malaysia, 43650 Bangi, Malaysia.
 ³School of Microelectronic Engineering, Universiti Malaysia Perlis, Campus Pauh, 02600, Arau, Perlis, Malaysia.
 ⁴Faculty of Engineering, Multimedia University, 63000 Cyberjaya, Selangor, Malaysia.
 sitisarah.mdsallah@gmail.com

Abstract—Silicon based photonics have generated strong interest in recent years, mainly in optical waveguide interconnects for microelectronic circuits. This paper presents a single mode condition (SMC) of SOI-based rib waveguide for high-speed Optical Interconnect (OI) implementation at a circuit level. In OptiBPM, a correlation analysis between two parameters, etched rib thickness (r) and effective index (n_{eff}) was investigated to identify the effects of width (W) on the rib waveguide. The waveguide performance of the OI links such as output power, propagation loss and propagation delay was recorded based on OptiSPICE simulation. A wavelength (λ) of 1550 nm has the advantages of low power loss and delay which makes it reliable for high-speed OI applications.

Index Terms—Effective Index (neff); Etch Depth (d); Optical Interconnect (OI); Rib Waveguide; Slab Height (h); Width (W).

I. INTRODUCTION

The downsizing activity in reducing complementary metal oxide semiconductor (CMOS) transistor dimensions will lead to higher components integration and increase the complexity of copper-based wire interconnects within a finite chip area, especially in large chips [1]. Therefore, on-chip Optical Interconnect (OI) is perceived as the key solution to overcome major limitations of copper-based wire interconnects, mainly in high speed interconnect applications [2]. The advantages of OI links at the chip level include providing a much higher bandwidth density, minimizing lower power consumptions, and decreasing interconnect delays, and noise [3][4].

The theory of OI in an electronic chip was introduced by Goodman in 1984 [5]. Since then, OI has been widely used in the telecommunications field and has been applied to a board-level interconnection. The main components of OI systems are as shown in Figure 1, which contains a chip laser, an optical modulator, a waveguide, and a photodetector. The transmitter contains an electro-optical modulator and a driver circuit. The modulator converts data from electrical signal to optical signal, while the receiver a photodetector and contains an amplifier. The photodetector is a semiconductor device that receives the optical signal and converts it into electrical signal. The optical waveguide is used as a transmission path to transfer the optical signal from transmitter to receiver. Optical waveguide consists of a core, in which light is confined, and a cladding or substrate surrounding the core.

Implementation of OI into VLSI technology needs compatibility with CMOS technology. This requirement significantly limits the choice of materials and processing available for fabrication of optical components. The main challenge regarding OI is the absence of an efficient siliconbased laser that can be monolithically integrated [1]. Therefore, this paper only considers off-chip laser implementation.



Figure 1: Optical interconnect data path

Silicon photonics on silicon-on-insulator (SOI) substrates are considered an interesting platform for these OIs waveguide because of the CMOS compatible fabrication process [6]. This allows full integration between the CMOS layers and the optical layers [7]. Besides that, the silicon improves energy efficiency photonic and cost competitiveness compared to the conventional electrical interconnect [8]. This paper focuses on the optical waveguide design and the optimization to be used in the OI links. OI systems can be operated at the wavelength 800 nm, 1300 nm, and 1550 nm [9]. In the case of high-speed OI, a wavelength (λ) of 1550 nm is used in the operation to maximize the bandwidth system with low propagation loss, as well as its compatibility with silicon waveguide and InGaAs photodetector [10]. The aim of this paper is to show that low propagation loss and delay can be achieved using a large etched rib waveguide structure on SOI substrate.

II. RIB WAVEGUIDE DESIGN

Optical waveguide can be analyzed since its size and propagation delay depends on the waveguide geometry and its refractive index depends on the wavelength of light. There are many materials available for CMOS waveguide, such as silicon-on-insulator (SOI) [11]-[13], silica-onsilicon [14] and SiGe/ Si [15][16]. A single mode condition (SMC) waveguide is the basis of various waveguide devices. Silica waveguide can be easily designed to be a single mode, while SOI waveguide with dimensions larger than a few hundred nanometers in a cross-section support multiple modes [17][18]. However, SOI is an ideal material for waveguiding in photonic integration due to its large scale chip, high quality, and cost-effectiveness [19]. The use of SOI substrates to realize on-chip OI has the advantage of compatibility with existing CMOS technology. Several works have been done on the theoretical study, design optimization, and optical characterization of waveguide structure to ensure light distribution with rid/ridge and buried structure using SOI substrate.

The silicon rib waveguide with rectangular cross-section is widely used in SOI waveguide devices. The rib waveguide consists of a core region surrounded by a finite cladding. The basic dimension of rib waveguide structure is shown in Figure 2, where W is the width of the rib waveguide, H is the thickness of silicon layer, h is the slab height, and d is the waveguide etch depth.



Figure 2: SOI-based rib waveguide with rectangular cross-section

Previous researchers [20]-[22] optimized their waveguide dimensions based on their effective index, n_{eff} to obtain a maximum coupling efficiency, low propagation loss and strongly optical confinement for practical implementation. The design and optimization of SOI-based rib waveguides considered in this work is based on 1550 nm wavelength, which is suitable for high-speed applications. The refractive index of the core was set to $n_{core} = 3.477$ corresponding to silicon, which is commonly used for optical transmission. The refractive index of substrate was set to $n_{sub} = 1.444$ corresponding to silicon dioxide, and the refractive index of the top cladding layer was set to $n_{clad} = 1$ corresponding to air. In general, there are two different formulas for rib waveguide: large etch rib and shallow etch rib.

A. Large Etched Rib Waveguide

Large etched rib waveguides in SOI could be designed to be monomodal. These waveguides have been studied extensively by numerous researchers to find the single mode behavior and low loss propagation. Large rib waveguides are interesting because there are multi-microns in crosssectional dimensions (in the order of 5 μ m) facilitating the low loss coupling and from optical fibers.

Soref et al. [12][23] introduced a large rib waveguide for SMC with a simple expression using the mode matching technique with the formula:

$$\frac{W}{H} \le 0.3 + \frac{r}{\sqrt{1 - (r)^2}}$$
 (1)

For
$$0.5 \le r \le 1$$
 (2)

where H is the rib height or thickness of the silicon layer, h is the slab height, W is the rib width, r = h/H, which represents the ratio of the slab height to the overall rib height, and W/H is the ratio of waveguide to the overall rib height. The analysis of the waveguides in Equation (1) is limited to shallow etched ribs (r>0.5) and the waveguide dimensions are assumed to be larger than the operating wavelength.

B. Small Etched Rib Waveguide

Chan et al. [11][17] have proposed a design guideline for relatively small rib waveguides with deep etched depth (r<0.5) for SMC with the formula:

$$\frac{W}{H} \le 0.05 + \frac{(0.94 + 0.25H)r}{\sqrt{1 - r^2}}$$
(3)

for
$$0.3 < r < 0.5$$
 and $1.0 < H < 1.5$ (4)

Equation (4) represents a clear separation between the boundary of a single-mode and multimode regions over a large range of etch depth and rib width values. Both Equation (1) and Equation (3) are for waveguides with air top cladding. A rib waveguide structure with different dimensions in SMC is discussed in the next section.

III. SIMULATION OF RIB WAVEGUIDE DESIGN USING OPTIBPM TOOLS

The beam propagation method (BPM) is a step-by-step technique of stimulation for the route of light through any wave guiding medium. A large etched rib waveguide was chosen for the OI link to get a low propagation loss and delay.

The waveguide geometry is shown in Figure 2. The material of the waveguide core is silicon, while the waveguide substrate is silicon dioxide. Theoretically, the refractive index of the core is $n_{Si} = 3.477$, and the refractive index of substrate is $n_{SiO2} = 1.444$. Considering a large rib waveguide, the waveguide structure with various dimensions of h, d, and W was performed using the OptiBPM mode solver in order to record the n_{eff} value in SMC optical profile under TE mode. The SMC can be verified through r and W/H values for each dimension as in Equation (1) and Equation (2).

A. Varied Slab Height (h) and Etch Depth (d)

Table I shows the profile pattern of SMC launched under TE mode using 1550 nm central wavelength for 1.0 μ m thickness of silicon guiding layer (H) with varied slab height (h) and etch depth (d). The values of d were varied between 0.1 μ m to 0.4 μ m and the values of h were varied from 0.6 μ m to 0.9 μ m. The value of W was kept constant, 0.5 μ m during the simulation in order to investigate the influence of h and d to its effective index (n_{eff}).

Table 1 shows a direct relationship between n_{eff} and h where the values of n_{eff} increased slightly as the value of h was increased. Since the value of n_{eff} was between the core refractive index and substrate refractive index, $1.44 < n_{eff} < 3.4$, the waveguide was assumed to be in guided mode. Therefore, there were fewer loss and strong optical confinement.

h,	d,	W,	r	<u></u>	n _{eff}	SMC profile under	
(um)	(µm)	(µm)		H		TE	
0.6	0.4	0.5	0.6	0.5	3.261	1.011	
						·····	
						> *0.044	
						-1 022	
						-2.000	
0.7	0.3		0.7		3.283	1811 — ×	
						0.932	
						- -	
						-2.0000.500 _0.256 _0.011 _0.233 _0.470	
0.8	0.2		0.8		3.307	1.211	
						0.933	
						5 0.044	
						-	
			0.0			-2.000 0.256 0.256 0.011 0.255 0.478	
0.9	0.1		0.9		3.315	_	
						0.933	
						≻ •••••	
						-1.022	
						-2.000 -0.256 -0.011 -0.255 -0.470	

Table 1Effective Index (n_{eff}) Changes in Rib Waveguide at $\lambda = 1550$ nm

B. Varied Rib Width (W)

Table 2 shows the output profile pattern of SMC launched under TE mode using 1550 nm central wavelength for 1.0 μ m thickness of silicon guiding layer (H) with varied dimensions of W. The values of W were varied between 0.2 μ m, 0.5 μ m, and 0.8 μ m, while the values of h and d were kept constant as 0.8 μ m and 0.2 μ m respectively for all width. This was done for the purpose of finding the parameters that can produce a single mode profile. The dimension of rib waveguide must be in the range of 0-10 mm, which was at the chip level (intra-chip).

Table 2 Effective Index (n_{eff}) Changes in Rib Waveguide at λ =1550 nm





Besides, Table 2 shows a direct relationship between n_{eff} and W, where the values of n_{eff} increased as the value of W increased.

C. Correlation between r and n_{eff}

Figure 3 shows the correlation between r and n_{eff} with three different width dimensions, 0.2 μ m, 0.5 μ m, and 0.8 μ m. r is the ratio of slab height, h to overall rib height, H. The graph shows a linear characteristic where n_{eff} increased with the increase of r value.

For OI applications, we chose $h = 0.8 \ \mu m$, $d = 0.2 \ \mu m$, and $W = 0.5 \ \mu m$ as the rib waveguide dimension with their effective index value of 3.307 to produce the SMC output.

D. Output Power (Pout) for Rib Waveguide

The output power (P_{out}) for each optical waveguide dimension can be investigated based on the OptiBPM simulation. The output power is shown in Figure 4 for the value of h = 0.8 µm, d = 0.2 µm, and W = 0.5 µm. This dimension was chosen based on the OptiBPM simulation results obtained previously. The output at the starting waveguide was equal to 1, while the output power decreased with the distance of the waveguide. Therefore, the final output power was 0.9975.



Figure 3: The Correlation between r and neff



Figure 4: Output power in rib waveguide using OptiBPM

E. Output Power (P_{out}) of Rib Waveguide at Different Wavelengths

The output power of 1500 nm was compared with 1300 nm. In optics, a multi-mode condition normally operates at 1300 nm, while a single mode condition (SMC) is optimized at 1550 nm. The results of the two different wavelengths are acceptable considering the SMC output in the simulation results. The measurements of P_{out} at different λ for rib waveguide are recorded in Table 3.

Table 3 Output Power at Different Wavelength, (λ) for Rib Waveguide

Slab Height(h), µm	Etch Depth(d), μm	Core Width (W), µm	Wavelength, (λ) , nm	Output Power (P _{out})
0.8	0.2	0.5	1550 1300	0.9975 0.9979

Figure 5 shows the relationship between P_{out} and λ . The relationship between P_{out} and λ was found to be inversely proportional, where the P_{out} decreases as the value of λ increases.



Figure 5: The relationship between P_{out} and $\,\lambda$

IV. SIMULATION OF OPTICAL INTERCONNECT LINK USING OPTISPICE TOOLS

OptiSPICE is a circuit design software for analysis of integrated circuit including integration of optical and electronic components. The OI link in a circuit was simulated in OptiSPICE tools using rib waveguide dimensions. The OI links consist of continuous (CW) source, modulator, waveguide, and photodetector. Based on Table I and Table 2, the effective index (n_{eff}) value for a 3.307 of rib waveguide structure was then used in this simulation to calculate the power consumption, power loss, and propagation delay of rib waveguide. Figure 6 shows the partial of the OI link circuit designed in the OptiSPICE tools.



Figure 6: Simulation circuit of OI link

In this receiver stage, the power consumption represented the energy necessary to convert the input current generated by the photodetector into electric logical levels. The output power of the receiver must be in the range of the receiver's sensitivity, which is the lowest power possible at which the receiver can detect the signal and demodulate the data. The photodetector used in the simulation was PIN (InGaAs) photodetector. PIN photodiodes are more suitable for high speed and short distance communication link since PIN operates at a standard power supply of 5-15 V and has lower cost compared to Avalanche (APD) photodiodes [24].

In this section, the discussion focuses on the rib waveguide performance of the OI link in circuit level based on output power (P_{out}), power loss (P_{loss}) and propagation delay (τ_{wg}).

A. Power Loss (Ploss) of Rib Waveguide in OI Link

The total propagation loss or power loss (P_{loss}) for the rib waveguide in OI link can be calculated by the formula below:

$P_{loss(waveguide)} = P_{waveguide(in)} - P_{waveguide(out)}$ (8)

Based on the OptiSPICE simulation, the P_{out} for input waveguide was 8.849 dBm, whereas the P_{out} for output waveguide was 7.664 dBm. Therefore, the total power loss for 1 cm length of silicon rib waveguide with the dimension of $h = 0.8 \mu m$, $d = 0.2 \mu m$, and $W = 0.5 \mu m$ was 1.185 dB.

B. Propagation Delay (τ_{wg}) of Rib Waveguide in

Optical Interconnect (OI) Link

The delay of an OI link is given by Equation (9) [25]:

$$\tau_{OI} = \tau_{tx} + \tau_{wg} + \tau_{rx} \tag{9}$$

where τ_{tx} is the delay of the transmitter, τ_{wg} is the delay of the waveguide, and τ_{rx} is the receiver delay. The delay through the optical waveguide is expressed as:

$$\tau_{Wg} = n_{eff} \frac{L}{c} \tag{10}$$

where n_{eff} is the effective index of the mode in the waveguide medium, c is the speed of light in vacuum, and L is the waveguide length. Therefore, the delay for 1 cm of length rib waveguide was 110 ps.

C. Summary of Waveguide Performance

Table 4 attempts to compare the power loss from previous works. The propagation loss strongly depends on the cross section of the waveguide core and on the wavelength of light for a given core size. However, the delay of waveguide strongly depends on n_{eff} and the length of waveguide as in Equation (10). Our simulation has the advantage of low power loss, which was 1.185 dB with 110 ps of propagation delay, the lowest delay compared to 123 ps [26] and 113 ps [27]. Both of the loss and delay figures are useful as a benchmark for further development of silicon based photonics on an SOI platform.

 Table 4

 Comparison of Waveguide Power Loss

Waveguide Material	Waveguide Structure	Wavelength (λ) , nm	Dimensions	Power loss (P _{loss}), dB/cm
SOI (This work)	Rib Waveguide	1550	W=0.5 μm d=0.2 μm h=0.8 μm H=1 μm L=1 cm	1.185
SOI [2]	Spiral Waveguide	1550	W=2 μm d=0.05 μm H=0.25 μm L=64 cm	0.274
SOI [28]	Rib Waveguide	3800	$W=2 \ \mu m$ $d=1.2 \ \mu m$ $h=0.8 \ \mu m$ $H=2 \ \mu m$ $L=1 \ cm$	3.400
SOI [29]	Rib Waveguide	1550	$W=9 \ \mu m$ $d=5 \ \mu m$ $h=0.65 \ \mu m$ $H=1 \ \mu m$ $L=1.1 \ cm$	4.300
SOI [30]	Strip Waveguide	1550	W=0.5 μm d=0.22 μm H=1 μm L=1 cm	2.400
SOI [31]	Strip Waveguide	1500	W=0.445 μm H=0.22 μm L=2.1 cm	3.600

V. CONCLUSION

In this work, we investigated and successfully analyzed rib waveguide geometry for 1550 nm wavelength to be used in Optical Interconnect (OI) links. The rib waveguides can be made into a single mode condition (SMC) by setting the dimension of rib height, depth, and width. Our simulation shows that the effective index (n_{eff}) increased with r. The results reported in this paper demonstrates that rib-based distribution have propagation loss as small as 1.185 dB with 110 ps of propagation delay that can be used for the OI interconnect link with acceptable compactness.

ACKNOWLEDGMENT

The authors are grateful UKM and IMEN for useful discussions, supports, and the encouragement given for completing this research.

REFERENCES

- M. Haurylau, N. Nelson, D. Albonesi, P. M. Fauchet, and E. G. Friedman, "Electrical and Optical On-Chip Interconnects in Scaled Microprocessors," in 2005 IEEE International Symposium on Circuits and Systems, pp. 2514–2517, 2005.
- [2] P. Dong, W. Qian, S. Liao, H. Liang, C. C. Kung, N. N. Feng, R. Shafiiha, J. Fong, D. Feng, A. V. Krishnamoorthy and M. Asghari, "Low loss silicon waveguides for application of optical interconnects," *IEEE Photonics Society Summer Topicals*, vol. 1, no. c, pp. 191–192, 2010.
- [3] S. S. Md Sallah, S. H. Md Ali, P. S. Menon, N. Juhari, and M. S. Islam, "Implementation of On-chip Optical Interconnect in High Speed Digital Circuit: Two-stage CMOS Buffer," Asian Journal of Scientific Research, pp. 1–10, 2017.
- [4] P. Shen, A. Hosseini, X. Xu, Y. Hei, Z. Pan and R. T. Chen, "Multiple-Input Multiple-Output Enabled Large Bandwidth Density On-Chip Optical Interconnect," *Journal of Lightwave Technology*, vol. 34, no. 12, pp. 2969–2974, 2016.
- [5] G. Chen, H. Chen, M. Haurylau, N. Nelson, and P. M. Fauchet, "Predictions of CMOS Compatible On – Chip Optical Interconnect," *International Workshop on System Level Interconnect*, pp. 13-20,

2005.

- [6] T. Spuesens, F. Mandorlo, P. Rojo-romeo, P. Régreny, N. Olivier, and J. Fédeli, "Compact Integration of Optical Sources and Detectors on SOI for Optical Interconnects Fabricated in a 200 mm CMOS Pilot Line," *Journal of Lightwave Technog.*, vol. 30, no. 11, pp. 1764– 1770, 2012.
- [7] E. Yablonovitch, "Can nano-photonic silicon circuits become an INTRA-chip interconnect technology?," *International Conference on Computer Aided Design*, pp. 309, 2007.
- [8] W. Bae, G. S. Jeong, Y. Kim, H. K. Chi, and D. K. Jeong, "Design of silicon photonic interconnect ICs in 65-nm CMOS technology," *IEEE Transactions on Very Large Scale Integration (VLSI) Sysems.*, vol. 24, no. 6, pp. 2234–2243, 2015.
- [9] J. W. Shi, Y. H. Cheng, J. M. Wun, K. L. Chi, Y. M. Hsin, and S. D. Benjamin, "High-Speed, high-efficiency, large-area p-i-n photodiode for application to optical interconnects from 0.85 to 1.55 μm Wavelengths," *Journal of Lightwave Technology.*, vol. 31, no. 24, pp. 3956–3961, 2013.
- [10] O. I. Dosunmu, D. D. Cannon, M. K. Emsley, L. C. Kimerling, and M. S. Unlu, "High speed resonant cavity enhanced Ge photodetectors on reflecting Si substrates for 1550 nm operation," *IEEE Photonics Technologu Letters*, vol. 17, no. 1, pp. 148–149, 2004.
- [11] S. P. Chan, C. E. Png, S. T. Lim, G. T. Reed, and V. M. N. Passaro, "Single-Mode and Polarization-Independent," *Journal of Lightwave Technology*, vol. 23, no. 6, pp. 2103–2111, 2005.
- [12] S. P. Pogossian, L. Vescan, and A. Vonsovici, "The Single-Mode Condition for Semiconductor Rib Waveguides with Large Cross Section," *Journal of Lightwave Technology*, vol. 16, no. 10, pp. 1851– 1853, 1998.
- [13] O. Powell, "Single-mode condition for silicon rib waveguides," Journa of Lightwave Technology, vol. 20, no. 10, pp. 1851–1855, 2002.
- [14] L. Wosinski, "Silica-on-silicon technology for photonic integrated devices," Proc. of International Conference of. Transparent Optical Networks, vol. 2, pp. 274–279, 2004.
- [15] P. Chaisakul, D. M. Morini, J. Frigerio, D. Chrastina, M.S. Rouifed, S. Cecchi, G. Isella and L. Vivien, "High quality SiGe waveguide platform for Ge photonics on bulk silicon substrates," *International Conference on Group IV Photonics (GFP)*, pp. 108–109, 2014.
- [16] S. Ren, Y. Rong, S. A. Claussen, R.K. Schaevitz, T. I. Kamins, J. S. Harris and D.A.B. Miller, "Ge / SiGe Quantum Well Waveguide Modulator Monolithically Integrated With SOI Waveguides," *IEEE Photonics Technology Letters*, vol. 24, no. 6, pp. 2011–2013, 2012.
- [17] M. M. Milosevic, P. S. Matavulj, B. D. Timotijevic, G. T. Reed, and G. Z. Mashanovich, "Design Rules for Single-Mode and Polarization-Independent Silicon-on-Insulator Rib Waveguides Using Stress Engineering," *Journal of Lightwave Technology*, vol. 26, no. 13, pp. 1840–1846, 2008.
- [18] Y. Liu, J. M. Shainline, X. Zeng, and M. A. Popović, "Ultra-low-loss CMOS-compatible waveguide crossing arrays based on multimode Bloch waves and imaginary coupling," *Opt. Letters.*, vol. 39, no. 2, pp. 335–338, 2014.
- [19] Y. U. Jinzhong, C. shaowu, X. jinsong, W. Zhangtao, F. Zhongchao, L. Yanping, L. Jingwei, Y. Di and C. Yuanyuan, "Research progresses of SOI optical waveguide devices and integrated optical switch matrix," *Science in China Ser. F Information Sciences*, vol. 48, no. 2, pp. 234–246, 2005.
- [20] M. Muzafar, M. Noorazlan, and S. Zainuddin, "Numerical Method Approaches in Optical Waveguide Modeling," *Applied Mechanics* and Materials, vol. 54, pp. 2133–2137, 2011.
- [21] X. Xu, S. Chen, Z. Li, Y. Yu, and J. Yu, "SOI submicron rib waveguides : Design, Fabrication and Characterization," *Proceeding* of *IEEE International Conference on Group IV Photonics*, pp. 137– 139, 2008.
- [22] M. M. Ismail, M. A. M. Said, M. A. Othman, M. H. Misran, H. A. Sulaiman, and F. A. Azmin, "Buried vs . Ridge Optical Waveguide Modeling for Light Trapping into Optical Fiber," in *International Journal of Engineering and Innovative Technology*, vol. 2, no. 1, pp. 273–278, 2012.
- [23] R. Soref, J. Schmidtchen, and K. Petermann, "Large Single-Mode Rib Wave-Guides in Gesi-Si and Si-on-Sio2," *IEEE Journal of Quantum Electronics*, vol. 27, no. 8, pp. 1971–1974, 1991.
- [24] S. S. Md Sallah, S. H. Md Ali, P. S. Menon, N. Juhari, and S. A. Ahmad, "Investigation on Optical Interconnect (OI) Link Performance using External Modulator," in *IEEE Regional Symposium on Micro and Nanoelectronics (RSM)*, pp. 1–4, 2015.
- [25] S. Rakheja and V. Kumar, "Comparison of electrical, optical and plasmonic on-chip interconnects based on delay and energy considerations," *Internation Symposium on Quality Electronic Design*, pp. 732–739, 2012.

- [26] S. Yegnanarayanan, D. Trinh, F. Coppinger, and B. Jalali, "Compact Silicon-Based Integrated Optic Time Delays," *IEEE Photonics Technology Letters*, vol. 9, no. 5, pp. 634–635, 1997.
 [27] K. H. Koo, P. Kapur, and K. C. Saraswat, "Compact performance
- [27] K. H. Koo, P. Kapur, and K. C. Saraswat, "Compact performance models and comparisons for gigascale on-chip global interconnect technologies," *IEEE Transaction Electron Devices*, vol. 56, no. 9, pp. 1787–1798, 2009.
- [28] M. M. Milošević, D. J. Thomson, X. Chen, D. Cox, and G. Z. Mashanovich, "Silicon waveguides for the 3-4 µm wavelength range," in *IEEE International Conference on Group IV Photonics*, pp. 208–210, 2011
- [29] S. Chen, Q. Yan, Q. Xu, Z. Fan, and J. Liu, "Optical waveguide propagation loss measurement using multiple reflections method," *Optics Communications.*, vol. 256, no. 1–3, pp. 68–72, 2005.
 [30] P. Dumon, W. Bogaerts, V. Wiaux, J. Wouters, S. Beckx, J. V.
- [30] P. Dumon, W. Bogaerts, V. Wiaux, J. Wouters, S. Beckx, J. V. Campenhour, D. Taillaert, B. Luyssaert, P. Bienstan, D. V. Thourhout and R. Baets, "Low-loss SOI photonic wires and ring resonators fabricated with deep UV lithography," *IEEE Photonics Technology Letters*, vol. 16, no. 5, pp. 1328–1330, 2004.
- [31] Y. A. Vlasov and S. J. McNab, "Losses in single-mode silicon-oninsulator strip waveguides and bends.," *Optics Express*, vol. 12, no. 8, pp. 1622–1631, 2004.