

Selective Harmonic Elimination Pulse Width Modulation for Five-Level Cascaded Inverter

Chun Yi H'ng, Baharuddin Ismail, Muzamir Isa and Mohamad Nur Khairul Hafizi Rohani
*Centre of Excellence for Renewable Energy, School of Electrical System Engineering,
 Universiti Malaysia Perlis, Pauh Putra Campus, 02600 Arau, Perlis, Malaysia.
 chunyi_hng@yahoo.com*

Abstract—This paper presents an efficient selective harmonics elimination method for a five-level cascaded inverter by using the Newton-Raphson method. The aim of this project is to eliminate selected low-order harmonics by solving non-linear equations using the programming developed based on Newton-Raphson method. Meanwhile, at the same time, the fundamental component is retained efficiently. Instead of single switching, multiple switching in quarter cycles has been introduced to increase the number of harmonic orders that should be eliminated. In addition, the low-order harmonics up to the 5th order for single switching and 17th order for multiple switching are eliminated from the inverter output voltage waveform for entire modulation index. The calculated switching angles have been inserted into the simulation model of the five-level inverter by using PSIM software. Moreover, the calculated switching angles for single and multiple switching are then tested by using a prototype of a five-level inverter that has been built in the laboratory. The simulation results are verified with the experimental results for single and multiple switching.

Index Terms—Selective Harmonic Elimination; Multilevel Inverter; MATLAB Programming; Newton-Raphson.

I. INTRODUCTION

In recent years, multilevel inverters continuously to gain popularity due to their capability to operate at high voltage, low switching losses, high efficiency and electromagnetic interference (EMI) with low output. The word multilevel starts with the three-level converter. Nowadays, the multilevel inverter has been gained more attention for medium and high-power applications such as motor drives, flexible AC transmission system (FACTS) equipment, high voltage direct current (HVDC) and renewable energy systems which can operate at high switching frequencies while producing lower order harmonic components and lower electromagnetic interference [1,2].

Multilevel inverters have received great concern in medium-voltage and high-power applications compared to conventional two-level inverters because of their lower switching losses, high efficiency, smaller common-mode (CM) voltage and more electromagnetic compatibility. When the number of levels of multilevel inverter increased, the output voltage steps generating waveform increased synchronously and at the same time, the total harmonic distortions are decreased [3,4].

Some power circuits have been proposed with the amendments in the traditional inverter circuit in order to achieve acceptable performance operation. The multilevel inverter has been considered as the best option for supplying better quality power to the load among the varied topologies. Basically, there are three conventional topologies for

multilevel inverters which are diode clamp, flying capacitor, and cascaded multilevel inverter with separate DC sources. Cascaded multilevel inverters have received more attention from all the above multilevel inverter topologies because of their modularity and simplicity of control method [5-7].

Selective harmonic elimination pulse width modulation (SHEPWM) provides numerous advantages if compared to the other approaches such as lower switching frequency, improved DC source utilization and direct control over low-order harmonics. SHEPWM is an efficient method that commonly used to precisely eliminate the selective harmonics in the waveform of output voltage waveform. Selective harmonic elimination is principally used for achieving the desired fundamental component and eliminating or minimizing the selective harmonics [5-12].

The appropriate switching angle must be calculated and the power switching devices have to be switched consequently in order to remove the selected lower harmonics from the output voltage/current waveform of the cascaded multilevel inverter. From lately reported research events on selective harmonic elimination methods, it is discovered that the transcendental equations were generally solved by Newton-Raphson or genetic algorithms (GA). In the Newton-Raphson method, a good preliminary guess that should be very near to the precise solution is needed. This method can work appropriately if a good preliminary guess is obtainable [5,7].

II. CASCADED FIVE-LEVEL INVERTER

The cascaded H-bridge inverter has attracted great interest because of greater needs of high-powered and intermediate voltage inverter [1,5]. A Cascaded H-Bridge inverter of single-phase five-level is shown in Figure 1.

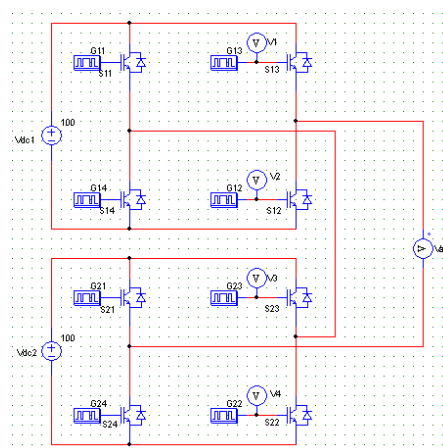


Figure 1: Cascaded five-level inverter

When compared to any other topology, cascaded H-bridge cell inverter use the least number of power electronic devices [13-16]. However, cascaded H-bridge inverters require isolated power sources in each cell which in turn requires a large isolating transformer. The corresponding output voltage of this multilevel topology was equal to zero after the switches S_{a1} , S_{a2} , S_{b3} and S_{b4} are ON and S_{a3} , S_{a4} , S_{b1} and S_{b2} are OFF.

III. SELECTIVE HARMONIC ELIMINATION PWM

The popular selective harmonic elimination method is also called fundamental switching frequency method which is based on the harmonic elimination theory [5]. The multilevel fundamental switching scheme inherently provides the opportunity to eliminate certain lower order harmonics by varying the times at which certain switches are turned ON and turned OFF.

A staircase output voltage waveform is generated by switching ON and OFF the switching devices in the multilevel inverters once during one fundamental cycle is shown in Figure 2. This diminishes the switching losses in the devices. In this method, each switch is turned ON and turned OFF once in a switching cycle and switching angles are usually chosen based on specific harmonic elimination or minimization of total harmonic distortion (THD) in the output voltage. The way to eliminate lower order harmonics is by computing the switching angles using SHE methods.

Due to the symmetrical assumption, the required switching angles to eliminate lower order harmonics i.e. 5th at the fundamental switching frequency for five-level cascaded inverters is calculated by solving the following Equations:

$$\cos\theta_1 + \cos\theta_2 = m_a \quad (1)$$

$$\cos(5\theta_1) + \cos(5\theta_2) = 0 \quad (2)$$

where, m_a is limited to $0 < m_a \leq 1$.

The switching angles θ_1 and θ_2 must satisfy the following condition:

$$0 < \theta_1 < \theta_2 < \frac{\pi}{2} \quad (3)$$

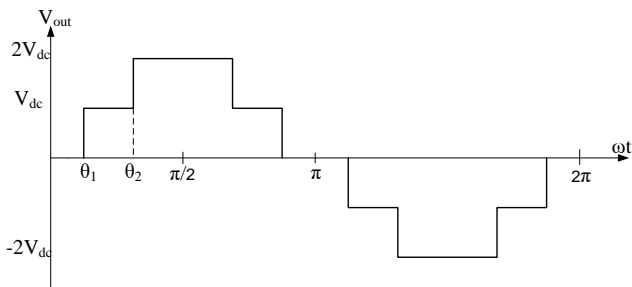


Figure 2: Single switching with angles determined by selective harmonic elimination

IV. NEWTON-RAPHSON METHOD

The non-linear equations can be solved by the iterative Newton-Raphson method to determine the switching angles, θ_1 and θ_2 lies in between 0 and $\pi/2$. The NR method approach is capable of finding analytical solutions for limited ranges. The input variables include:

- number of DC voltage sources (which gives the number of output voltage levels);
- number of harmonics to be eliminated; and
- the switching combination (how many angles for each level, i.e. N_1, N_2, \dots).

The steps of the main computational process to solve the SHEPWM are described as follows:

1. Given an initial guess of a set of values of θ :

$$\theta^0 = [\theta_1^0 \ \theta_2^0 \ \theta_3^0 \ \dots \ \theta_{PM}^0]^T \quad (4)$$

2. Determine the values of:

$$b(\theta^0) = b^0 \quad (5)$$

3. Linearize b about θ^0 using partial differentiation:

$$b + \left[\frac{\partial b}{\partial \theta^0} \right] x d\theta = 0 \quad (6)$$

where:

$$\left[\frac{\partial b}{\partial \theta} \right] = \begin{bmatrix} -\sin\theta_1 & +\sin\theta_2 & \dots & \pm\sin\theta_{PM} \\ -5\sin 5\theta_1 & +5\sin 5\theta_2 & \dots & \pm 5\sin 5\theta_{PM} \\ \vdots & \vdots & \ddots & \vdots \\ -n\sin n\theta_1 & +n\sin n\theta_2 & \dots & \pm n\sin n\theta_{PM} \end{bmatrix} \quad (7)$$

is an $P_M \times P_M$ matrix.

Evaluate θ and $d\theta = [d\theta_1 \quad d\theta_2 \quad \dots \quad d\theta_{PM}]^T$

in Step 3.

4. Solve for $d\theta$.
5. The steps from 1-4 are repeated by using improved guesses:

$$\theta^1 = \theta^0 + d\theta \quad (8)$$

V. RESULTS AND DISCUSSION

The single switching angles calculated for a different modulation index (m_a) of the five-level cascaded inverter is shown in Table 1. It covers the range of $0.3 \leq m_a \leq 0.95$. These sets of switching angles are applied for both simulation circuit and hardware testing.

Table 1
Single switching angles calculated for different modulation index

Modulation Index (m_a)	Switching angles 1 ($^\circ$) θ_1	Switching angles 2 ($^\circ$) θ_2
0.3	53.6127	89.6127
0.35	50.4069	86.4069
0.40	47.1285	83.1285
0.45	43.7605	79.7605
0.50	40.2825	76.2825
0.55	36.6686	72.6686
0.60	32.8851	68.8851
0.65	28.8861	64.8861
0.70	24.6062	60.6062
0.75	19.9454	55.9454
0.80	14.7361	50.7361
0.85	8.6526	44.6526
0.90	0.8592	36.8592
0.95	15.2991	20.7009

The simulation and experimental results for five-level cascaded inverter are shown in details by using the PSIM Software and an oscilloscope, respectively. The DC voltage source of the simulation circuit is $100 V_{dc}$ for each block and the total voltage for two blocks is $200 V_{dc}$ for the simulation circuit in PSIM software.

For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either wye or delta configuration.

In hardware testing, prototypes of single phase five-level cascaded inverter with Field Programmable Gate Array (FPGA) and an Android Apps which named as “Multilevel Inverter Apps” are used. The calculated switching angles are inserted and save in the database of this apps. Next, by using Bluetooth, the database is connected and uploaded to the FPGA inverter. The output voltage waveforms and Fast Fourier Transform (FFT) is captured by using an oscilloscope.

The simulation of output voltage waveforms for modulation index $=0.80$ using single switching scheme is shown in Figure 3 and the experimental of output voltage waveforms for modulation index $=0.80$ using single switching scheme is shown in Figure 4.

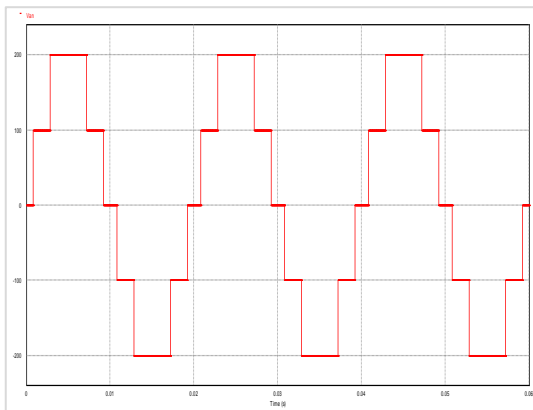


Figure 3: Simulation output voltage waveforms for $m_a = 0.80$

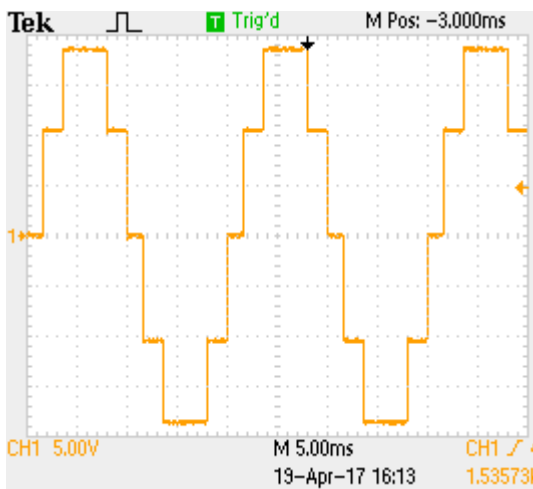


Figure 4: Experimental output voltage waveforms for $m_a = 0.80$

The FFT analysis for simulation and experimental with modulation index, 0.80 using single switching scheme are shown in Figure 5 and 6 with the THD results are 17.05% and 17.1%, respectively.

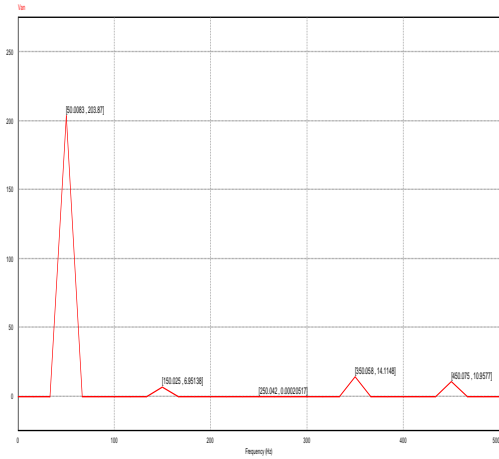


Figure 5: Simulation Fast Fourier Transform (FFT) analysis for $m_a = 0.80$

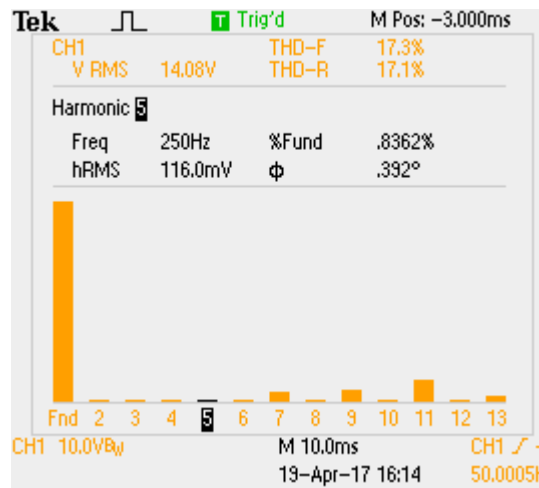


Figure 6: Experimental Fast Fourier Transform (FFT) analysis for $m_a = 0.80$

The calculated switching angles for multiple switching at modulation index, 1.00 are $\theta_1 = 31.80$, $\theta_2 = 36.92$, $\theta_3 = 46.32$, $\theta_4 = 70.88$, $\theta_5 = 78.82$, and $\theta_6 = 85.41$. The phase voltage output waveforms from simulation and experimental with modulation index, 1.00 using multiple switching schemes are shown in Figure 7 and 8, respectively.

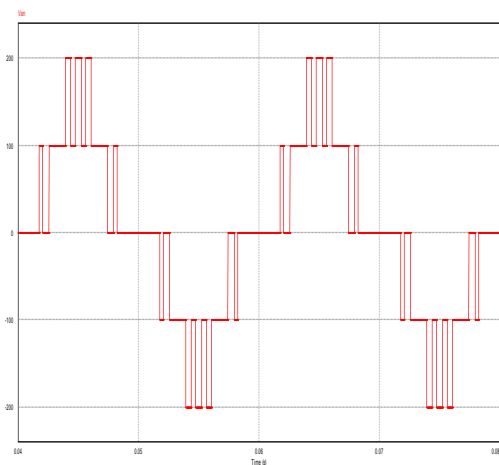


Figure 7: Simulation phase voltage output waveforms for $m_a = 1.00$

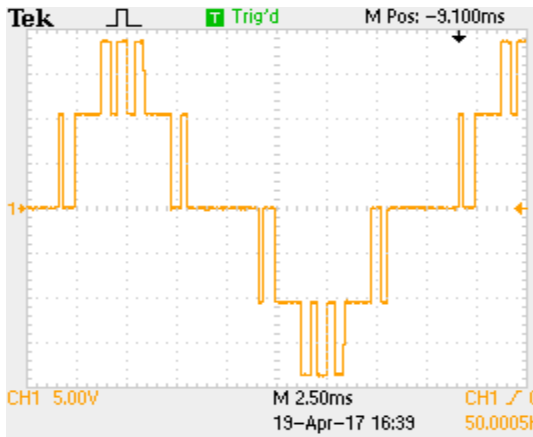


Figure 8: Experimental phase voltage output waveforms for $m_a = 1.00$

The FFT analysis for simulation and experimental with modulation index, 1.00 using multiple switching schemes are shown in Figure 9 and in Figure 10, respectively. It can be seen that the 5th, 7th, 11th, 13th and 17th are eliminated. The THD results are 45.1% for simulation and 45.2% for experimental.

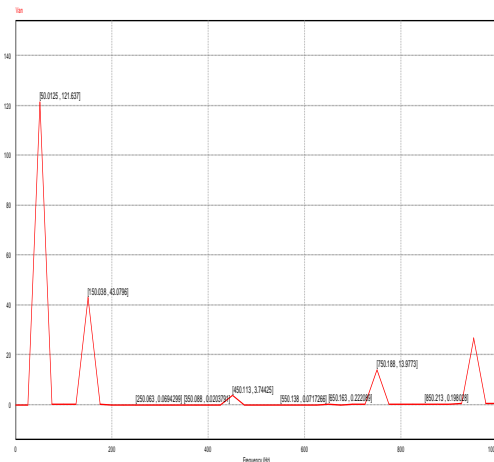


Figure 9: Simulation Fast Fourier Transform (FFT) analysis for $m_a = 1.00$

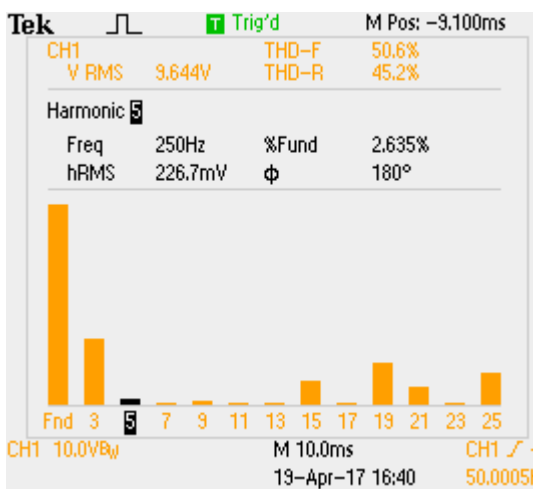


Figure 10: Experimental Fast Fourier Transform (FFT) analysis for $m_a = 1.00$

By constructed the system in three-phase, the output voltage waveforms for simulation with modulation index, 1.00 using multiple switching schemes is shown in Figure 11 and the FFT analysis for m_a , 1.00 for line-to-line voltage is

shown in Figure 12. From Figure 12, it is obviously can be seen that the low-order harmonic including the triplen harmonics up to 17th harmonics are efficiently eliminated.

The output voltage waveform from experimental is nearly identical to the result obtained from the PSIM simulation. From the results of FFT analysis by using single switching scheme (Figures 5 and 6), it is obviously can be seen that the low order harmonic (5th harmonic) is eliminated successfully and at the same time the fundamental component is retained effectively. Moreover, for multiple switching schemes (Figure 9 and 10), low order harmonic (5th, 7th, 11th, 13th and 17th) are eliminated. The results that obtained from the experimental and simulation are almost similar.

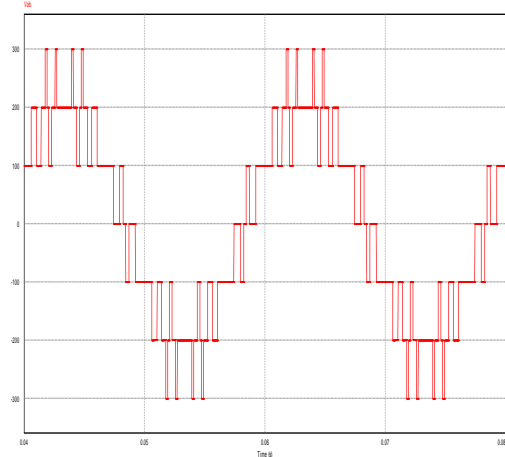


Figure 11: Simulation line-to-line voltage output waveforms for $m_a = 1.00$

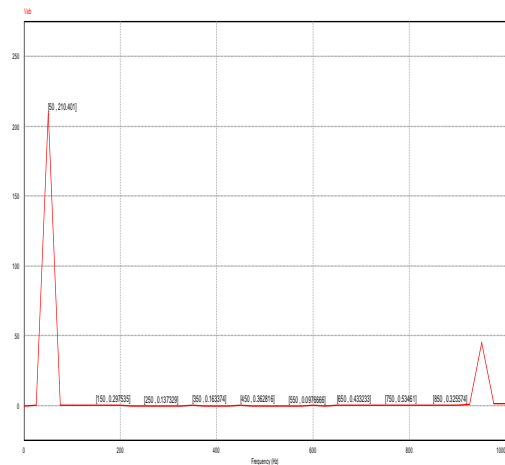


Figure 12: Simulation Fast Fourier Transform (FFT) analysis for $m_a = 1.00$

A harmonic is a triplen harmonic if its frequency is an integer multiple of three times the fundamental frequency. For balanced three-phase systems, each phase voltage will contain triplen harmonics equal in both magnitude and phase to the triplen harmonics of the other two phases. Therefore, all triplen harmonics will cancel in the line-to-line voltages. As a result, the triplen harmonics such as 3rd, 9th, 15th is not compulsory to eliminate in the three-phase system because these harmonics can be eliminated automatically from line-to-line voltage.

From the FFT analysis shown in Figure 12 which is constructed in a three-phase system using multiple switching scheme, it is obviously can be seen that the low-order harmonic including the triplen harmonics up to 17th harmonics are efficiently eliminated. As the result, line-to-

line voltage THD can be automatically reduced without increasing the number of levels and the number of switching angles in SHEPWM method.

From all the simulation and experimental results, it is obviously can be seen that the all the desired low order harmonics are minimized or eliminated effectively and the THD of the output voltage is enhanced even better than the typical switching schemes.

It can be observed that the low order harmonic which is 5th harmonic is less than 1% of the fundamental component and nearly zero by using single switching scheme. Besides, it can be obviously to be observed that the low order harmonics which are 5th, 7th, 11th, 13th, and 17th harmonics are also less than 1% of the fundamental component and nearly zero by using multiple switching schemes.

By constructed the system in three-phase using multiple switching schemes, it is obviously can be seen that all of the low-order harmonic including the triplen harmonics up to 17th harmonics are efficiently eliminated and less than 1% of the fundamental component and nearly zero for simulation result from the FFT analysis which as shown in Figure 12.

VI. CONCLUSION

In this paper, elimination of desired low order harmonics using SHEPWM method was presented. The switching angles are able to calculate by resolving the non-linear equations using the Newton-Raphson method. The designed and constructed of five-level cascaded inverter was able to produce phase voltage output waveform. In addition, the low-order harmonics up to the 5th order for single switching and 17th order for multiple switching are eliminated from the inverter voltage output waveform for entire modulation index. The hardware of five-level cascaded inverter with FPGA was successfully investigated by using the calculated switching angles. Both simulation and experimental testing were obtained the similar results. From the FFT analysis of using multiple switching scheme, it is obviously can be seen that the low order harmonics such as 5th, 7th, 11th, 13th, and 17th harmonic are successfully eliminated.

ACKNOWLEDGMENT

The authors would like to thank Ministry of Education for financially supported under MTUN COE grant number 9016-00007.

REFERENCES

- [1] A. B. Ashok, "Selective harmonic elimination of multilevel inverter using SHEPWM technique," *International Journal of Soft Computing and Engineering (IJSCE)*, pp. 79-82, 2013.
- [2] J. Kumar, B. Das and P. Agarwal, "Selective harmonic elimination technique for a multilevel inverter," *Fifteenth National Power Systems Conference (NPSC)*, pp. 608-613, 2008.
- [3] J. Kumar, B. Das and a. P. Agarwal, "Harmonic reduction technique for a cascade multilevel inverter," *International Journal of Recent Trends in Engineering*, pp. 181-185, 2009.
- [4] N. K. Sharma and N. K. Sahu, "Analysis of total harmonic distortion and its elimination by multilevel inverter," *International Journal of Digital Application & Contemporary Research*, pp. 1-8, 2015.
- [5] B. Ismail, S. I. S. Hassan, R. C. Ismail, A. R. Haron and A. Azmi, "Selective harmonic elimination of five-level cascaded inverter using particle swarm optimization," *International Journal of Engineering and Technology (IJET)*, pp. 5220-5232, 2014.
- [6] B. Ismail, M.H Arshad and S. Thangaprakash, "FPGA based implementation of selective harmonic elimination PWM for cascade inverter," *International Review on Modelling and Simulations (IREMOS)*, pp. 1919-1926, 2012.
- [7] D. K. N and D. P. Kaur, "Selective harmonic elimination PWM technique implementation for a multilevel converter," *International Journal of Engineering Research*, pp. 303-308, 2015.
- [8] N.Karthika, R.Rajalakshmi, S. Deepika and T.Shalini, "Selective harmonic elimination technique based cascaded multilevel inverter with reduced number of switches," *International Journal of Science and Research (IJSR)*, pp. 2177-2181, 2013.
- [9] V. Sundar and A. ovaiz, "Cascaded multilevel inverter with selective harmonic elimination-PWM technique for statcom applications," *International Journal on Applications in Engineering and Technology*, pp. 24-29, 2015.
- [10] K.Ganesan, K.Barathi, P.Chandrasekar and D.Balaji, "Selective harmonic elimination of cascaded multilevel inverter using BAT algorithm," *Procedia Technology 21 (2015) 651 – 657*, pp. 1-7, 2015.
- [11] Krismadinata, N. A. Rahim, H. W. Ping and J. Selvaraj, "Elimination of harmonics in photovoltaic seven-level inverter with Newton-Raphson optimization," *Procedia Environmental Sciences 17, 2013*, 519 – 528, pp. 1-10, 2012.
- [12] R.Saravanakumar, R.M.Anusuya, V.Kavitha and A.Gopi, "Selective harmonic elimination in seven level cascaded inverter," *International Conference on Renewable Energy and Sustainable Energy [ICRESE'13]*, pp. 51-57, 2013.
- [13] N.Karthika, R.Rajalakshmi, S. Deepika and T.Shalini, "Selective harmonic elimination technique based cascaded multilevel inverter with reduced number of switches," *International Journal of Science and Research (IJSR)*, pp. 2177-2181, 2013.
- [14] D. Subramanian and R. Rasheed, "Nine-level cascaded H-bridge multilevel inverter," *International Journal of Engineering and Innovative Technology (IJEIT)*, pp. 201-205, 2013.
- [15] M. Murugesan, R.Pari, R.Sivakumar and S.Sivaranjani, "Different types of multilevel inverter topologies – A technical review," *International Journal of Advanced Engineering Technology*, pp. 149-155, 2016.
- [16] A. E. Joseph and J. Jacob, "A hybrid cascaded nine level inverter," *ISSN (PRINT): 2393-8374, (ONLINE): 2394-0697, vol. 2, no. 10, pp. 1-5, 2015*.