Design and Analysis of 15 nm MOSFETs

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***Abstract*—We present the design and analysis of 15 nm NMOS transistors, fabricated on three different substrate materials -- namely silicon, indium nitride and indium arsenide. Close inspection on the I-V characteristic curves reveals that the saturation voltage and current of the indium arsenide transistors are significantly higher than the other two counterparts. We attribute this result to the high mobility of carriers in indium arsenide substrate. It is also observed that the breakdown voltages of the indium arsenide transistors are also one of the highest. The breakdown behaviour shows that transistors fabricated on indium arsenide substrate renders reasonably high robustness. Due to high channel length modulation effect, it could also be seen that current variation between saturation and breakdown currents is the highest in the conventional silicon transistors. Our analysis suggests that indium arsenide could be an alternative substrate material in the design and fabrication of nano-scale MOSFETs. For devices which may require high power consumption (and therefore high current and voltage), indium arsenide can also be considered as an appropriate substrate material.**

***Index Terms*—Breakdown; MOSFET; nMOS; Saturation; Short Channel Effects.**

I. Introduction

As CMOS technology advances, the feature size of a transistor is being pushed to nanometric dimensions [1]. For the past 50 years, MOSFET transistor has seen significant reduction in size. Transistors with the size of 50 µm in the 1960s have shrunk to less than 45 nm in the 2010s [2 – 3]. As the feature size continues to shrink towards the sub-nanometer range (with the 90 nm node and beyond), the channel length is found to be gradually approaching the mean free path of the carriers in the inversion layer [4 – 5]. In order to continue to enhance the performance of the transistors, some of the semiconductor foundries have resorted to the three-dimensional FinFET transistors [6]. Although FinFETs offer numerous advantages over conventional planar FET technologies, it comes with quite a few challenges/drawbacks as well. These include design-rule complexity, high resistance, etc. [7]. Hence, the fabrication of planar FETs is still a preferable option to many other foundries. In order to further enhance the performance of planar FET devices, Prasher et al. [5] have suggested using III-V compound semiconductors as the channel materials. This is because III-V compounds, such as indium-based materials, generally possess higher mobility than silicon. The authors have demonstrated that the performance of a transistor can be improved when a layer of indium antimonide InSb is grown onto the channel regime. In their study, however, comparison between the performance of a MOSFET with the typical silicon Si channel and that with the InSb channel is not illustrated. Moreover, fabrication steps to suppress short channel effects are not addressed in their analysis as well.

In this paper, we present the design and analysis of 15 nm nMOS transistors, fabricated on three different substrate materials – silicon (Si), indium nitride (InN), and indium arsenide (InAs). In order to provide a more realistic analysis, we have applied both Lightly Doped Drain (LDD) and halo implantations to suppress short channel effects in our nano-scale design. We compare and analyze the I-V characteristic curves for the three types of MOSFETs to determine the output current density I_D and robustness of the devices.

II. Design of the 15 nm Transistor

The design of the 15 nm Si nMOS transistor is scaled based on the 140 nm Si nMOS transistor design in [2]. The simulation recipes of the 140 nm transistors are reduced to the size of the 15 nm transistors using constant field scaling. As there is a drastic reduction in the feature size (from 140 nm to 15 nm), adjustments are to be performed at the doping densities and the dimensions of the devices from time to time. Once the designs of the silicon Si nMOS transistors are validated, the other two indium-based nMOS transistors are then developed by modifying the silicon transistor. The fabrication processes are simulated using the 2D-DDCC TCAD tool. Figure 1 depicts the cross-section of the 15 nm MOSFET drawn using 2D-DDCC. As the channel length approaches the nano-scale regime, the transistor may be susceptible to short channel effects – particularly, hot electron effect, punch-through, and Drain Induced Barrier Lowering (DIBL) [8 – 10]. In order to suppress these effects and to ensure proper operation of the transistors, additional steps are to be employed in the fabrication process. As can be seen in Figure 1, we have applied Lightly Doped Drain (LDD) implantation to minimize hot electron effect and halo implantation to suppress both punch-through and DIBL.

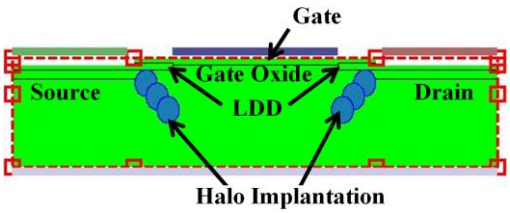

Figure 1: Cross section view of a 15 nm MOSFET

III. Results and Discussion

The parameters of the nMOS transistors are given in Table 1. In the design of the transistors, the dopant densities are carefully adjusted in order to obtain IV characteristics of an operational MOSFET. It can be seen that the dopant densities vary with different substrate materials.

To validate our designs, we connect the gate terminal to voltage source V_G and substrate terminal to ground (i.e. V_{SB} = 0). We then determine the drain current I_D by varying the drain voltage V_D. Figures 2 to 4 depict the drain current I_D to drain voltage V_D I-V characteristic curves of the transistors, at gate voltage V_G = 1.0 V; whereas, Figs. 5 to 7 show the characteristic curves at V_G = 1.5 V. When V_G increases, it can be seen that the saturations and breakdowns increase accordingly. This behaviour agrees with the ideal output characteristic of an enhancement mode MOSFET transistor.

Table 1
Parameters of 15 nm nMOS Transistors

Substrate	Parameters		
Si	Drain/Source	Dopant density	2.0×10^{29} cm^{-3}
		Activation energy	0.06 eV
		Length	10.5 nm
		Thickness	1.2 nm
	Substrate	Dopant density	1.0×10^{18} cm^{-3}
		Activation energy	0.01 eV
		Length	44.0 nm
		Thickness	8.2 nm
	Gate oxide	Thickness	0.6 nm
InN	Drain/Source	Dopant density	2.0×10^{25} cm^{-3}
		Activation energy	0.06 eV
		Length	10.5 nm
		Thickness	1.2 nm
	Substrate	Dopant density	1.0×10^{20} cm^{-3}
		Activation energy	0.1 eV
		Length	44.0 nm
		Thickness	8.2 nm
	Gate oxide	Thickness	0.6 nm
InAs	Drain/Source	Dopant density	2.0×10^{29} cm^{-3}
		Activation energy	0.06 eV
		Length	10.5 nm
		Thickness	1.2 nm
	Substrate	Dopant density	1.0×10^{20} cm^{-3}
		Activation energy	0.025 eV
		Length	44.0 nm
		Thickness	8.2 nm

As can be observed from the figures, the saturation and breakdown of the transistors vary significantly from each other. In order to provide a clearer elucidation on the performance of these transistors, we summarize the saturation voltages $V_{D(sat)}$ and currents $I_{D(sat)}$ in Tables 2 and 3 and breakdown voltages $V_{D(break)}$ and currents $I_{D(break)}$ in Tables 4 and 5. From Tables 2 and 3, it can be seen that InAs MOSFETs give the highest saturation current. Si MOSFETs, on the other hand, show the lowest saturation. Current density is closely affected by the mobility of the carriers. As can be seen in Table 6, the mobility of electrons and holes at room temperature are the highest in InAs. Clearly, the high saturation current found in InAs transistors can be attributed to the high mobilities of its carriers. It is however interesting to see that the saturation currents in InN transistors are higher than its Silicon counterpart.

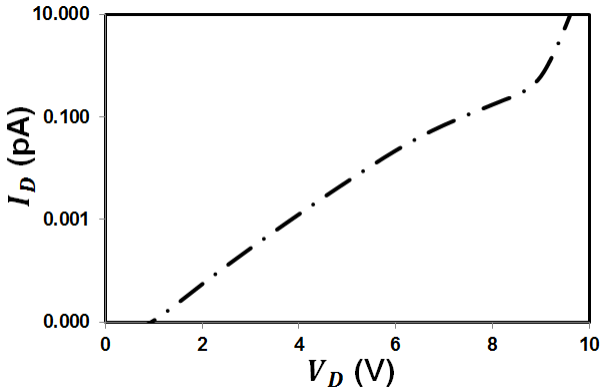

Figure 2: Output characteristics of Si nMOS transistor, at V_G = 1.0 V

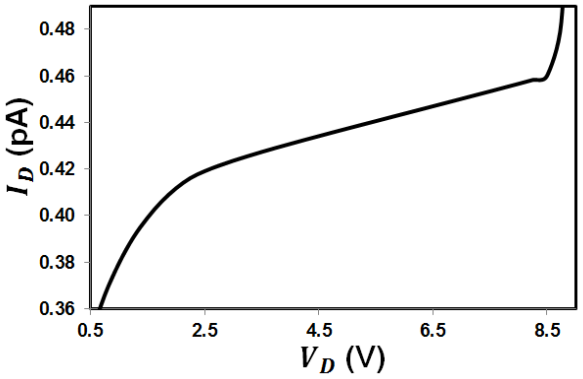

Figure 3: Output characteristics of InAs nMOS transistor, at V_G = 1.0 V

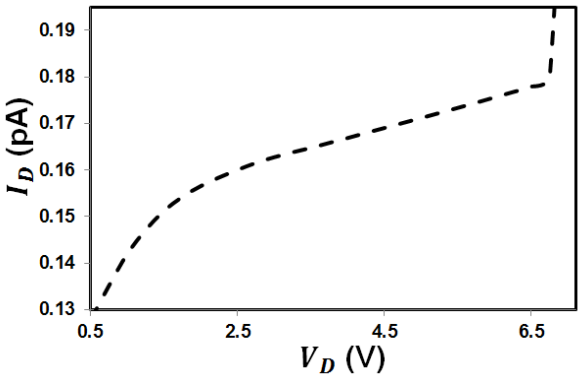

Figure 4: Output characteristics of InN nMOS transistor, at V_G = 1.0 V

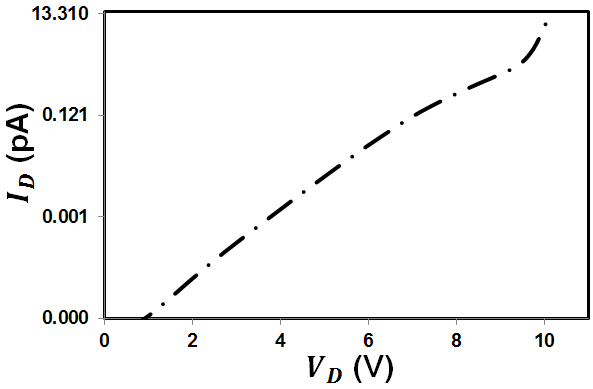

Figure 5: Output characteristics of Si nMOS transistor, at V_G = 1.5 V

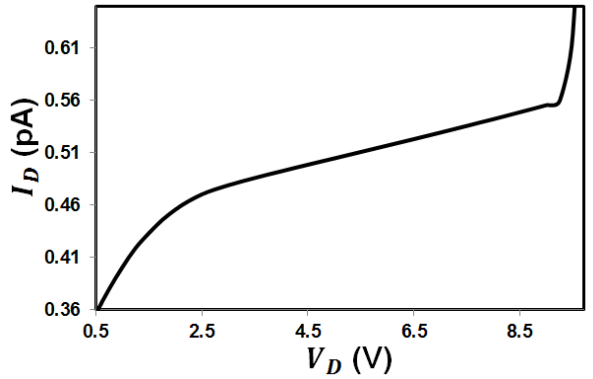

Figure 6: Output characteristics of InAs nMOS transistor, at V_G = 1.5 V

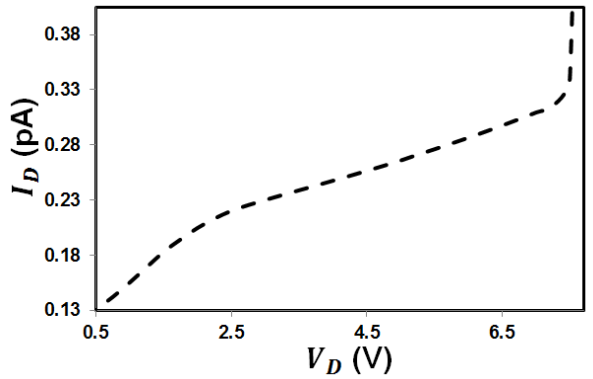

Figure 7: Output characteristics of InN nMOS transistor, at V_G = 1.5 V

Table 2
Saturation of nMOS transistors at V_G = 1.0 V

Substrate	$V_{D(sat)}$	$I_{D(sat)}$
Si	5. 5 V	0.011 pA
InAs	1.25 V	0.40 pA
InN	1.5 V	0.14 pA

Table 3
Saturation of nMOS transistors at V_G = 1.5 V

Substrate	$V_{D(sat)}$	$I_{D(sat)}$
Si	5.75 V	0.021 pA
InAs	2.0 V	0.45 pA
InN	1.75 V	0.20 pA

Table 4
Breakdown of nMOS transistors at V_G = 1.0 V

Substrate	$V_{D(break)}$	$I_{D(break)}$
Si	9.0 V	0.61 pA
InAs	8.5 V	0.46 pA
InN	6.75 V	0.18 pA

Table 5
Breakdown of nMOS transistors at V_G = 1.5 V

Substrate	$V_{D(break)}$	$I_{D(break)}$
Si	9.5 V	1.41 pA
InAs	9.25 V	0.56 pA
InN	7.25 V	0.31 pA

Table 6
Properties of Semiconductor at room temperature T = 300 K

Semiconductor	Electron mobility, μ_n ($\frac{cm^2}{Vs}$)	Energy gap, E_g (eV)
Si	1200	1.1
InAs	33000	0.40
InN	300	0.608

Upon close inspection on Figs. 2 to 7, we can also see that all transistors have high current variation between saturation and breakdown, particularly in Si transistors. This is due to the high channel length modulation effect found in the transistors.

Since breakdown is closely affected by the bandgap of the material, silicon which has wider bandgap (refer to Table 6) can, therefore, support higher breakdown. As a result of this, breakdown voltages are found to be the highest in Si transistors (refer Tables 4 and 5).

It can be observed that the breakdown voltages in InAs transistors turn out to be comparable with its Si counterpart. The high saturation and breakdown found in InAs transistors suggest that InAs MOSFETs could be considered as an alternative in the design and fabrication of nano-scale MOSFETs, replacing conventional Si transistors. Due to its ability to withstand high breakdown voltages and currents, InAs transistors are found to be robust. Hence, for electronic devices which require high currents and voltages, InAs MOSFETs could be an appropriate candidate in integrated circuit design.

Figures 8 to 10 show the variation of drain current I_D as a function of gate voltage V_G when V_D = 4 V, for the 15 nm nMOS transistors. The drain current I_D with V_G = 0 (I_{off}) and I_D with $V_G = V_{DD}$ = 4 V (I_{on}) and the threshold voltage (V_{TH}) estimated from the figures are summarized in Table 7. It can

be seen that the threshold voltages for the three transistors are close, with the Si transistor having the lowest and InAs the highest. InAs transistor also has the highest I_{on}; while InN has the lowest I_{off}.

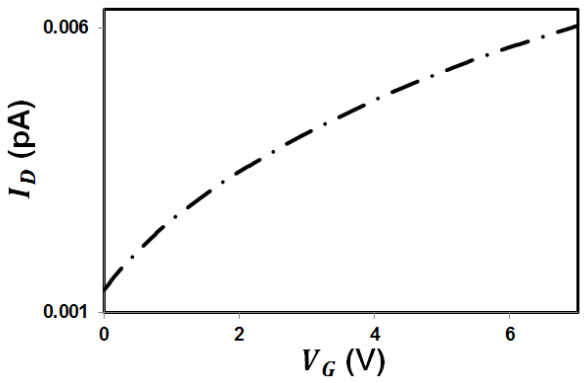

Figure 8: I_D as a function of V_G for Si nMOS transistor, at V_D = 4.0 V

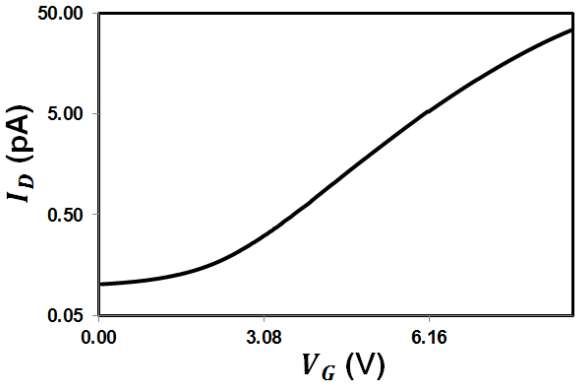

Figure 9: I_D as a function of V_G for InAs nMOS transistor, at V_D = 4.0 V

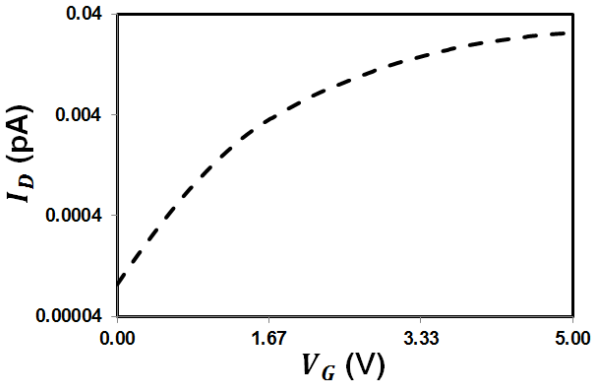

Figure 10: I_D as a function of V_G for InN nMOS transistor, at V_D = 4.0 V

Table 1
Parameters of 15 nm nMOS Transistors

Substrate	I_{off}	I_{on}	V_{th}
Si	7.21×10^{-4} pA	3.35×10^{-3} pA	0.8 V
InAs	1.03×10^{-1} pA	7.29×10^{-1} pA	0.95 V
InN	8.38×10^{-5} pA	2.07×10^{-2} pA	0.87 V

IV. Conclusion

We have designed and analysed the performance of 15 nm nMOS transistors, fabricated using three different substrate materials – namely, silicon Si, indium arsenide InAs, and indium nitride InN. The output characteristics curves suggest that InAs can be a good candidate to replace Si, in the fabrication of nano-scale transistors. This is because besides having the highest saturation voltages and currents, the breakdown voltages and currents of InAs MOSFETs are also found to be reasonably high. Because of its high breakdown, InAs is also found to be a robust material for transistor fabrication.

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