A Simple THD Minimization Technique for Transistor-Clamped H-Bridge-Based Cascaded Multilevel Inverter

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***Abstract*— This paper presents a simple modulation technique that minimizes the output voltage total harmonic distortion (THD) without eliminating the lowest order harmonics. It uses the voltage-angle equal concept of sinusoidal reference waveform to generate the step output voltage of a single-phase transistor-clamped H-bridge (TCHB)-based cascaded multilevel inverter. The real implementation of the modulation technique for a various range of modulation indices is built using an Altera field-programmable gate array (FPGA). It is found that the proposed modulation method resulted in a dramatic decrease in the inverter's output voltage THD when increasing the number of output steps up to thirteen levels.**

***Index Terms*—Multilevel Inverter; Total Harmonic Distortion (THD); THD Minimization.**

I. Introduction

Nowadays, multilevel inverter technologies have attracted attention as a convenient solution in many industrial applications. Multilevel inverters are frequently used in many applications such as reactive power compensation, back-to-back intertie systems, renewable energy systems, and variable speed drives [1]. They reduce output harmonic content and the voltage stress on switches and increase the quality of output voltage and current.

The most common topologies of the multilevel inverter are diode-clamped or neutral point-clamped (NPC), a capacitor-clamped or flying capacitor (FC), and cascaded H-bridge (CHB) [1]. Research on them seeks to improve their capability and control technique, while also minimizing component count and manufacturing costs. These factors have led to the emergence of a new family of multilevel inverters known as a transistor-clamped converter (TCC) [2,3]. The TCC topology provides a simple approach to increase the output levels by connecting a bidirectional switch to the series stacked DC-link capacitors. The function of the bidirectional switch is to control the bidirectional current flow.

Generally, the modulation strategies for the multilevel inverters, on the basis of their switching frequencies, are divided into two categories: low-switching frequency (fundamental frequency) and high-switching frequency methods. In high power applications, frequencies above 1 kHz are considered to be in a high-frequency range [1]. The overall performance of the multilevel inverters is strongly affected by the modulation strategy, as it helps to determine the voltage and current harmonics as well as the switching losses [4].

This paper is concerned with the transistor-clamped H-bridge (TCHB)-based cascaded multilevel inverter to produce an AC output voltage with low total harmonic distortion (THD). It is one of several distinct static power converter circuits that can produce three and more voltage levels. This work contributes to the modulation strategy with a low-switching frequency that minimizes voltage THD for the 13-level TCHB-based cascaded multilevel inverter. The gating signals of the adopted inverter are produced from the correlation of the voltage-angle equal criteria of sinusoidal reference waveform and through some combinational logic. The experimental tests are carried out in order to validate the proposed modulation technique.

II. The 13-Level TCHB-Based Cascaded Multilevel Inverter Configuration

Figure 1 shows the 13-level transistor-clamped H-bridge (TCHB)-based cascaded multilevel inverter configuration [5]. The adopted inverter consists of three independent DC voltage sources. The adopted configuration is sufficient to produce a high-quality output up to thirteen levels when three TCHB cells are applied. In order to acquire equal voltage steps, it is assumed that the DC voltage sources have the same values and consider large capacitance (i.e., 3300 μF) at the DC link.

Each TCHB inverter unit is added with one bidirectional switch, comprising one transistor with four diodes, to a conventional H-bridge inverter. However, a very attractive feature of the bidirectional switch is that it allows for a bidirectional current flow and enables five output voltage levels of 0, $\pm\frac{1}{2}V_{DC}$ and $\pm V_{DC}$ for a single unit of TCHB inverter.

The power switches and diodes in the adopted topology have different standing voltages. The four switches in the H-bridge, i.e. $S_{i1} - S_{i4}$, each has a standing voltage equal to V_{DC}. With regard to balance capacitor voltage condition, the standing voltage for each component of the bidirectional switch, i.e. diodes and switch S_{i5} are equal to $\frac{1}{2}V_{DC}$. Table 1 lists five modes of operation for a single cell of the adopted TCHB inverter. Half of the output voltages are produced through the proper switching of S_{i5} and S_{i2} /or S_{i4}, where 'i' is the number of TCHB cells.

It can be noticed that when the TCHB cells are connected in cascade, the total output voltage V_{inv} is given by:

$$V_{inv} = V_1 + V_2 + \ldots + V_i \quad (1)$$

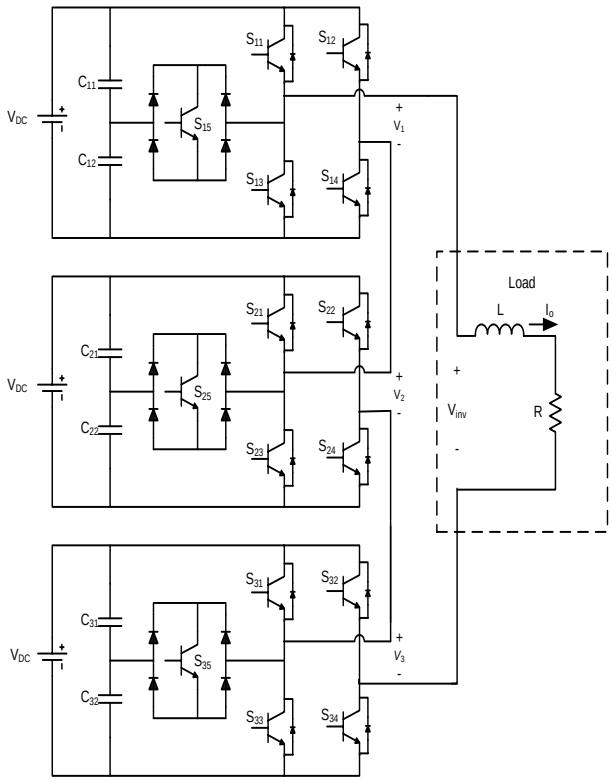


Figure 1: The 13-level TCHB based cascaded multilevel inverter topology.

Table 1
The Switching States and The Voltage Levels of 5-level TCHB Inverter.

Mode	Switches ON	V_i
1	S_{i1}, S_{i4}	$+V_{DC}$
2	S_{i4}, S_{i5}	$+½\ V_{DC}$
3	S_{i1}, S_{i2} (or S_{i3},S_{i4})	0
4	S_{i2}, S_{i5}	$-½\ V_{DC}$
5	S_{i2}, S_{i3}	$-V_{DC}$

Generally, the adopted topology has $4i + 1$ output levels (i is the number of TCHB cells). When they are considered for symmetry TCHB inverter with an equal voltage source V_{DC}, connecting three units of the TCHB inverter in series can produce a 13-level output voltage (0, $\pm½V_{DC}$, $\pm V_{DC}$, $\pm1½V_{DC}$, $\pm2V_{DC}$, $\pm2½V_{DC}$ and $\pm3V_{DC}$). There are a total of six equal steps in a quarter of the output waveform for a single-phase 13-level TCHB inverter, as illustrated in Figure 2.

III. Proposed Modulation Strategy

A. Background of proposed modulation strategy

In general, there are two different aims when using low-switching frequency modulation techniques [6,7]: 1) to eliminate specific lower-order (odd) harmonics of the inverter voltage THD; 2) to minimize the inverter voltage THD. This paper considered the second aim, minimization of the voltage THD. As a first step, the starting point is selected from the minimum voltage THD with selective harmonic elimination (SHE) in [5].

As referred to the staircase output waveform of the 13-level inverter in Figure 2, the Fourier series expansion of the inverter output voltage V_{inv} waveform can be expressed as:

$$V_{inv}(\omega t) = \frac{2V_{DC}}{n\pi} \sum_{n=1,3,5..}^{\infty} [\cos(n\theta_1) + .. + \cos(n\theta_6)]\sin(n\omega t) \quad (2)$$

where the set of the switching angles $\theta_1 < \theta_2 < \ldots < \theta_6 < \pi/2$ are the switching angles at each level in the first quarter waveform.

From Equation (2), the expression for the fundamental voltage V_1 is given by:

$$\frac{2V_{DC}}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \ldots. + \cos(\theta_6)] = V_1 \quad (3)$$

The modulation index M can be defined from (3) as:

$$M = \frac{\pi V_1}{2sV_{DC}} \quad (4)$$

where s is the number of positive steps in a quarter waveform. In the case of the 13-level inverter, s is six.

The quality of the 13-level TCHB inverter is judged by the quality of its output voltage waveform. The harmonic spectra measurement of the voltage THD can be calculated as:

$$THD(\%) = \frac{\sqrt{\sum_{n=2}^{\infty} V_n{}^2}}{V_1} \times 100\% \quad (5)$$

where V_n is the rms value of harmonic components and V_1 is the rms value of the fundamental component.

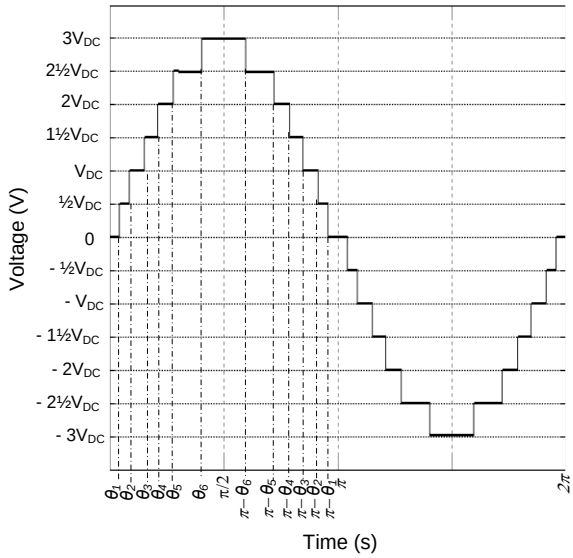


Figure 2: The inverter output voltage V_{inv} waveform.

There are four simple steps for implementing the proposed modulation method for a 13-level TCHB inverter:

1) Determine the modulation index of the minimum voltage THD and the respective switching angles based on the Newton-Raphson calculation for SHE from [5]. The minimum voltage THD with the harmonic elimination of Newton-Raphson iteration for a 13-level TCHB inverter is found at the modulation index M = 0.691, and the switching angles are 4.9°, 16.8°, 28.3°, 41.2°, 58.9°, and

87.2°. This will be the initial point for the adopted inverter.

2) Derive the trigonometric functions of switching angles obtained from Step 1 by calculating the equivalent voltage-angle area of the sinusoidal reference.
3) Determine all possibilities of switching angles for other modulation indices in the range $0 \le M \le 1$ by using the derivation of trigonometric functions.
4) Perform the combination logic for generating switching signals.

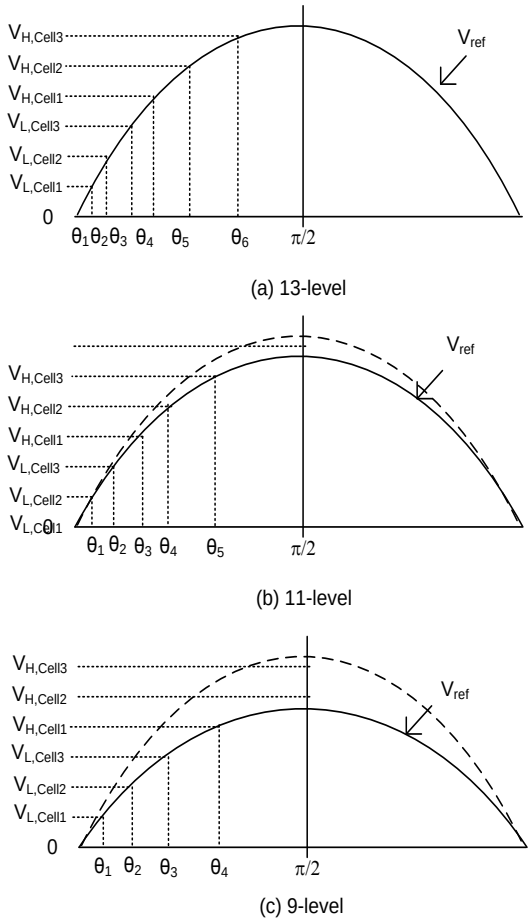


Figure 3: Various changes in output level.

The proposed modulation technique of the 13-level inverter manipulates one sinusoidal reference signal with six voltage levels ($V_{L,Cell1}$, $V_{H,Cell1}$, $V_{L,Cell2}$, $V_{H,Cell2}$, $V_{L,Cell3}$ and $V_{H,Cell3}$) during the positive half-cycle waveform, as shown in Figure 3(a). The reference voltage V_{ref} is defined as:

$$V_{ref} = M \sin(\omega t) \qquad (0 \le M \le 1) \qquad (6)$$

where M is the modulation index with ranges from 0 to 1.

In general, by using the voltage-angle equal criteria, a simple calculation for the triggered voltage levels was derived from the calculated switching angles ($\theta_1 - \theta_6$) for the 13-level TCHB inverter, which can be computed as follows:

$$\left.\begin{aligned} V_{L,Cell\,i} &= \sin(\theta_i \times \pi/180) \times M \\ V_{H,Cell\,i} &= \sin(\theta_{2i} \times \pi/180) \times M \end{aligned}\right\} \qquad (7)$$

where i is the number of TCHB cells in the adopted inverter topology. All calculations in Equation (6) and (7) are made in the radian basis. While maintaining the triggered voltage levels of $M = 0.691$, the switching angles for any output level can be obtained by adjusting the reference voltage according to the modulation index.

Figures 3(a) to (c), respectively illustrate the step voltages by reducing the amplitude modulation index from 13-level to 11-level and 9-level cases. When M is lower than the specific voltage levels for the 13-level TCHB topology, the number of switching angles is reduced. In order to avoid over-burdening in any particular cell, the sequence is chosen in a way that cell 1 operates at angles θ_1 & θ_3, cell 2 operates at angles θ_2 & θ_4 and cell 3 operates at angles θ_3 & θ_6, respectively.

Table 2 shows the range of modulation index M and the number of switching angles for the 13-level TCHB inverter. Moreover, similar approaches can be applied to any angle, to any number of voltage levels, and to any type of multilevel inverter topologies.

Prior to hardware implementation for verification of the proposed modulation technique, calculation of switching angles was performed in MATLAB. Figure 4 shows the switching angles values for modulation indices M ranged from 0.199 to 1 for a 5-level up to a 13-level TCHB inverter. However, this figure does not show the switching angles for modulation index less than 0.199, as it will produce a very low output of 3-level voltage or voltage with a magnitude of ½ V_{DC}.

Table 2
The number of Angles and Maximum Voltage of 13-level TCHB Inverter According to The Modulation Index.

Modulation index, M	Number of Angles	Maximum Voltage
$0.691 \le M \le 1$	6	3 V_{DC}
$0.593 \le M < 0.691$	5	2½ V_{DC}
$0.456 \le M < 0.593$	4	2 V_{DC}
$0.328 \le M < 0.456$	3	1½ V_{DC}
$0.199 \le M < 0.328$	2	V_{DC}
$0.059 \le M < 0.199$	1	½ V_{DC}
$0 < M < 0.059$	0	0

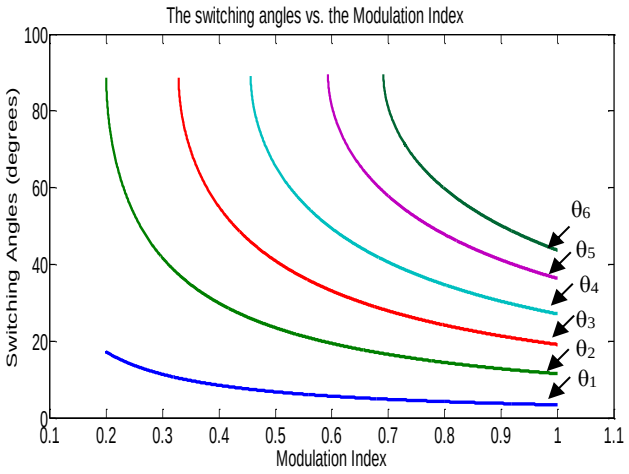


Figure 4: The switching angles with respect to modulation indices.

B. *Design of the logic circuit*

According to the switching function in Table 1, switches S_{i1}, S_{i3}, and S_{i5} (where i is the cell number) are operated by comparing the reference signal with the triggered voltage levels and through the simple combinational logic gates,

while S_{i2} and S_{i4} are operated complementarily in the half cycle of the reference signal. Hence, the general logic expressions for the gating signals by using combinational logic as follow:

$$\left.\begin{aligned} S_{i1} &= (C_{i1} \,.\, p180\ ref) + (\overline{C_{i2}} \,.\, \overline{p180\ ref}) \\ S_{i2} &= \overline{p180\ ref} \\ S_{i3} &= (C_{i1} \,.\, \overline{p180\ \text{ref}}) + (\overline{C_{i2}} \,.\, p180\ ref) \\ S_{i4} &= p180\ ref \\ S_{i5} &= \overline{C_{i1}} \,.\, C_{i2} \end{aligned}\right\} \quad (8)$$

where C_{i1} and C_{i2} are the outputs of comparators and the *p*180*ref* signal is the 180° reference based on a 50 Hz signal, which is also identified as the S_{i4} signal.

Figure 5 shows the overall design of proposed modulation strategy in FPGA for the adopted TCHB inverter. There are five sub-modules in the modulator architecture. One module is designated for the sine LUT as the voltage reference V_{ref} signal. In this case, the reference frequency used is 50 Hz, and a clock of 1 MHz is used for the overall FPGA modulator. One module is designated for the assigned level voltages and three modules are designated for the comparator and combinational logic derived for the switches in each 5-level TCHB inverter cell.

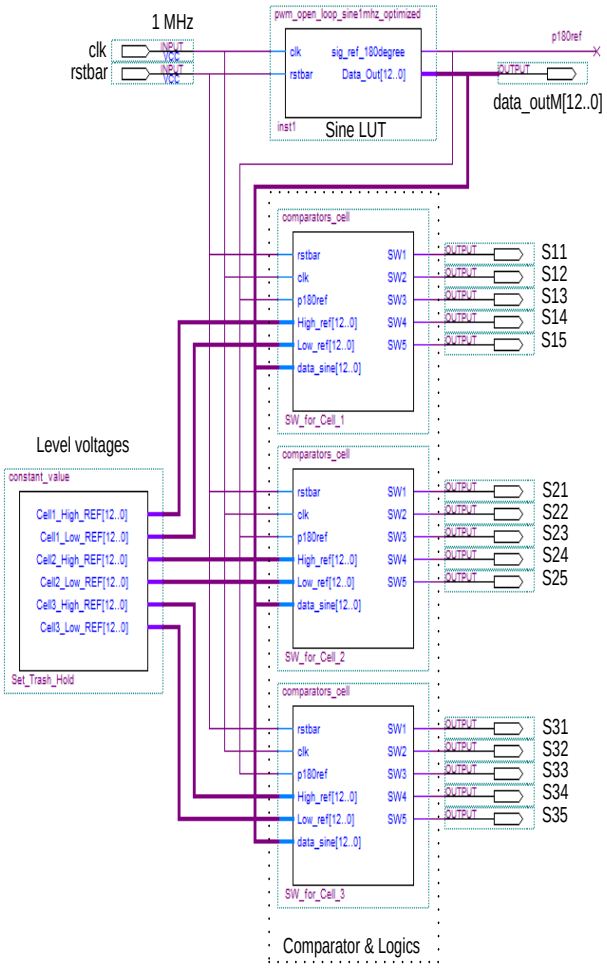


Figure 5: The digital modulator structure in FPGA.

The sinusoidal reference generator of a 50 Hz signal is stored in the LUT with a resolution of 1 MHz sampling frequency. The 180° reference signal *p180ref* is generated based on the first 10,000 counter in logic low, and the next 10,000 sequences in logic high. This will be continuously repeated. The assigned level voltages module is the representative for the calculated switching angles. The corresponding voltages are stored in FPGA memory, and the switching patterns are then formed through some combinational logic for real-time application.

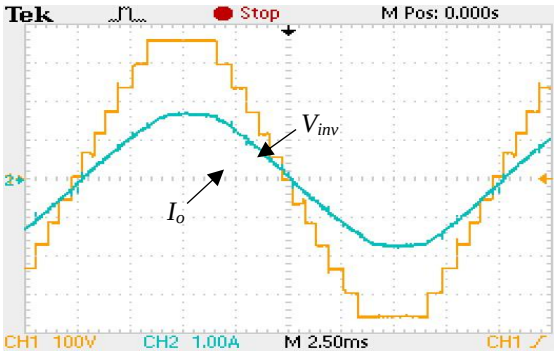
IV. Experimental Results and Discussion

For a verification of the proposed modulation technique, testing, measurement, and data collection were carried out from the developed prototype hardware. The 13-level TCHB inverter prototype was tested by using an *RL* load. Table 3 lists the parameters for the adopted TCHB multilevel inverter.

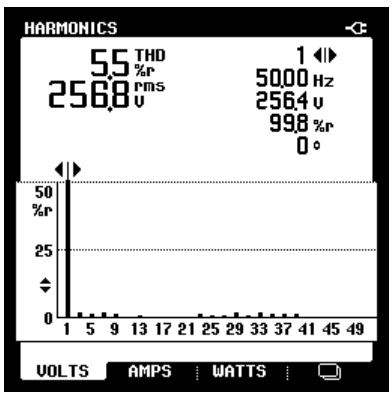
Table 3
The Inverter Specifications.

Parameter	Values
DC source for each TCHB module	120 V
Load resistance, *R*	200 ohm
Load inductor, *L*	81 mH
Fundamental frequency, *f*	50 Hz
Modulation index, *M*	0.546, 0.68, 0.793

Test experiments were performed by changing the reference voltage with respect to the modulation index. Figures 6(a) to (c), respectively show the inverter output voltage and current waveforms, voltage THD, and current THD for the 13-level case at M = 0.793. It can be seen that the measured values of THD are 5.5% for the voltage and 2.3% for the current waveforms.



(a)



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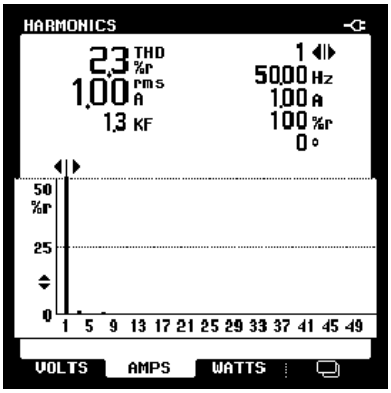
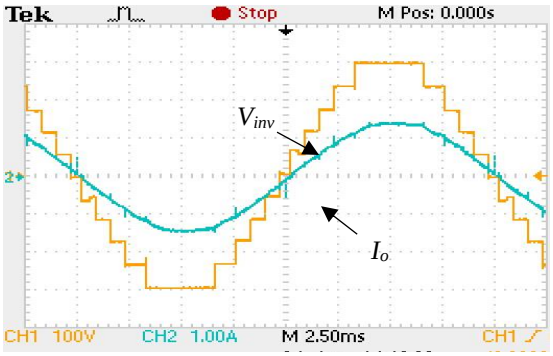
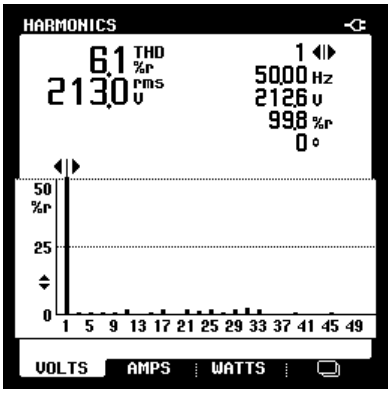


(c)

Figure 6: The 13-level TCHB inverter case (a) The V_{inv} and I_o (b) The THD of V_{inv} (c) The THD of I_o.



(a)



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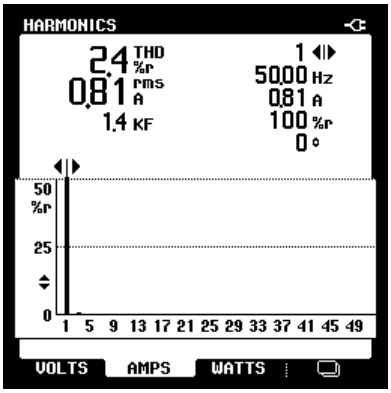
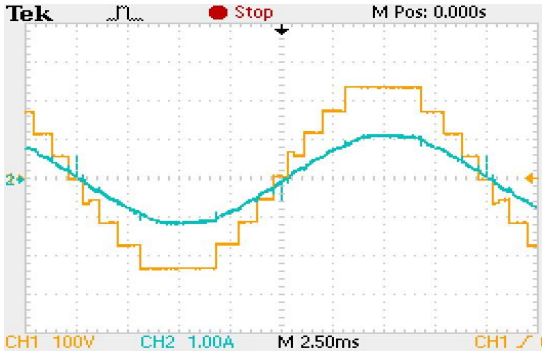
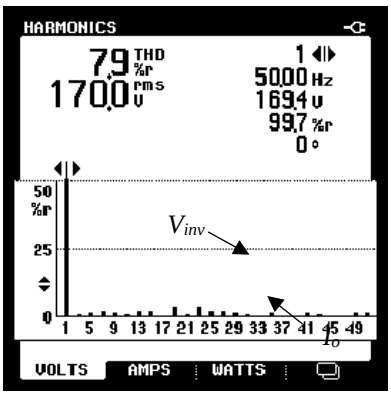


(c)

Figure 7: The 11-level TCHB inverter case (a) The V_{inv} and I_o (b) The THD of V_{inv} (c) The THD of I_o.



(a)



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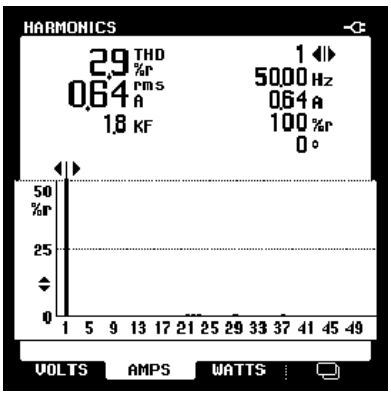

(c)

Figure 8: The 9-level TCHB inverter case (a) The V_{inv} and I_o (b) The THD of V_{inv} (c) The THD of I_o.

Another case for 11-level at M = 0.68, the inverter output voltage and current waveforms are illustrated in Figure 7(a). In this case, the voltage THD of 6.1% and current THD of 2.4% are shown in Figures 7(b) and 7(c), respectively.

Figure 8(a) is the inverter output voltage and current waveforms for the 9-level case at M = 0.546. The resulted voltage THD of 7.9% and current THD of 2.9% are illustrated in Figures 8(b) and (c), respectively.

From the experimental results, it can be seen that the voltage THD can be minimized effectively using the proposed modulation technique. In this paper, the voltage THD results for 13-level and 9-level are less than voltage THD results using SHE control scheme as given in [5]. The voltage THDs of 5.5% and 7.9%, respectively, for the 13-level and 9-level cases are achieved here, though the lowest harmonics are not being eliminated. In [5], the voltage THDs are 6.5% and 8.1%, respectively, for the 13-level and 9-level cases. For all tests, the current THDs are below 3%.

V. CONCLUSION

The most significant criteria in the multilevel inverter is the minimization of harmonics in the inverter output voltage/current. The harmonic distortion and operating switching frequency could be reduced with the increased number of levels in the inverter output voltage using certain control schemes. In this paper, the proposed switching technique of the adopted inverter was simple and capable of producing output voltage with minimal THD. The experimental results validate the proposed modulation methods for various numbers of output level. The relative merits of proposed modulation technique are assessed based on output quality. From the findings, the voltage and current THDs decreased significantly when the number of output level increased. The proposed modulation method can be extended to other multilevel inverter topologies at any level of output. The proposed technique can be used further in the closed-loop system as future work.

ACKNOWLEDGMENT

Authors would like to thank Universiti Teknikal Malaysia Melaka (UTeM), University of Malaya (UM) and Ministry of Higher Education for supporting this research under FRGS (FRGS/1/2015/TK04/FKE/03/F00256).

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