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2.5 AMPERE DC SOLID STATE
POWER CONTROLLER

BY

JOHN ANTHONY GILBERT, 1947-

A THESIS

Presented to the Faculty of the Graduate School of the

UNIVERSITY OF MISSOURI-ROLLA

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2.5 AMPERE DC SOLID STATE POWER CONTROLLER

ABSTRACT

The 2.5 Ampere DC Power Controller presented in this paper is a device which combines the properties of both relays and circuit breakers solely by means of solid state circuitry to perform the power functions that (1) provide DC power to electrical loads by means of power transistor switching, and (2) provide electrical protection by generating trip out characteristics similar to those of thermal circuit breakers. Furthermore, the control of this device is completely computer compatible, i.e., it is commandable from digital logic levels.

The text of this report discusses the requirements, specifications, and design of this power controller. In addition, performance results obtained from the breadboard prototype when controlling resistive, capacitive, inductive, lamp, and motor loads at various temperatures and bus voltage levels are illustrated. These results are then reviewed, providing insight to the special problems associated with remote DC power switching and control of each of these loads.

ACKNOWLEDGEMENT

I wish to thank the McDonnell Douglas Corporation for investing the time and expense necessary to analyze, design, and test a 2.5 Ampere Direct Current Solid State Power Controller. This work, specifically performed as an aid to Company development in the field of Electrical Power Conditioning and Control, has presented one of those rare occasions when Corporation, individual, and engineering equally benefit. For this rewarding occasion, I am grateful.

John A. Gilbert, Author

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PROLOGUE

Projected goals in both space endeavors (e.g., the Space Shuttle, Planetary Probes, etc.) and air travel (consider the F15, B1, and A7-D to name a few) require exceptional engineering ingenuity and application. Today's state of the art has generated air and space vehicles of outstanding life, reliability, and accuracy of operation; but future designs will require further extension of these qualities. Increased complexity and sophistication in control of on-board systems will provide the impetus for extending these characteristics with advanced design principles.

Advanced design will incorporate extremely fast and accurate data processing techniques in order to maintain vehicular system control. Such data processing will be accomplished mainly by a programmed on-board digital computer. Naturally, the accuracy, life, and most important the reliability of this computer is extremely critical. Nevertheless, on equal footing with computer integrity, is the system design problem of gathering subsystem test point data and controlling subsystem processes. The subsystem of specific interest in this thesis is the electrical power system.

Past electrical power system design employed electro-mechanical devices--relays, fuses and circuit breakers -- to provide control and electrical protection to both system and load. Future designs will require computer compatibility -- a quality lacking of manually operated circuit breakers and fuse links. Control commands for power switching to all types of electrical loads must be handled via electrical

signals if fast and accurate control plus data processing by the flight computer are to be realized. The sophisticated air or spacecraft system does not have time to wait for a busy pilot to reset a manual circuit breaker. Thus, the use of solid state switching devices seems to offer the best feasible solution to this control problem.

In January, 1960, work was initiated which was specifically directed toward the development of an advanced electrical system for aircraft. Ling - Temco - Vought (LTV) led the industry in the early stages, developing new design concepts for the Navy, Air Force and NASA. Their early work included defining the requirements necessary for solid state AC and DC load bus controllers, bus monitoring, Built-In Test, data multiplexing and associated control logic. Many of the requirements for DC power controllers that were an outcome of these studies consisted of nothing more than extensions of the military standards (specifically MIL-STD-704A, Electric Power, Aircraft, Characteristics and Utilization of) to which relay manufacturers and power system designers were already forced to adhere. Other controller requirements -- such as slow turn on/off risetimes and current limiting levels -- were initially defined from these studies. As an end product, an advanced power system utilizing solid state controls and switching devices was introduced as SOSTEL (SOLID STATE Electric Logic).

In the mid to late 1960's, both the Leach and Westinghouse Corporations entered the field of solid state power controllers. Leach concentrated on developing the type of AC and DC power controller specified by LTV for their A-7 aircraft program. Westinghouse, on the hand,

not only developed both types of power controllers, but also the system design (i.e., interface and multiplex) necessary to control these solid state circuit breakers. To date, Westinghouse is presently delivering solid state power controllers to North American Rockwell for the B1 aircraft program.

As an outgrowth of the work performed by these three companies -- LTV, Leach and Westinghouse -- the Military specification, MIL-P-81653, Power Controller, Solid State, General Specification for, was generated. This specification, although preliminary, finally brought together in one document design criteria for solid state power controllers. It was also at this time when a number of companies -- including Teledyne Relays and General Electric -- entered the field of designing solid state power controllers.

NASA had been following the development of these power controllers in light of possible application for Skylab, Space Shuttle and future space programs. However, existing power controllers were being designed to MIL-P-81653 -- the specification developed mainly for aircraft application. Spacecraft design required a different animal.

In 1969, NASA/MSFC (Marshall Space Flight Center) contracted to Spacecraft, Inc., (SCI) a program that would develop a power controller possessing those characteristics applicable to spacecraft system design. From this program, a slightly different approach was taken in the design of a remote-controlled solid state power controller.

The 2.5 Ampere DC Solid State Power Controller is yet another approach in the quest for an optimum power controller. It is hoped that by its development, insight and understanding to the problems associated with the design and application of DC Solid State Power Controllers will eventually aid the realization of those "projected goals".

INTRODUCTION

Typical problems associated with electromechanical control of electrical loads continually degrade DC power quality in both aircraft and space power systems. Inductive voltage and inrush current transients produced by power switching various electrical and electronic loads create this undesirable degradation. As a result, system power quality suffers.

Solid state power controllers can ease this "suffering" by significantly reducing power quality degradation. These power controllers combine the power functions that provide DC power and electrical protection to loads -- similar to the functions of electromechanical components -- in a device that controls the rate of current or voltage during turn on/turn off to these loads. This rate control function is accomplished entirely by means of electronic circuit design; and it is this control that enhances power quality as well as power distribution design.

In addition, power controllers possess computer compatibility, i.e., high power can be controlled by low power digital signals. This quality solves the problem of remote controlled power switching. It also allows for direct interface to computer controlled data multiplexed systems, similar to those considered in the design of the F15 (reference 1) and B1 aircraft, and NASA Space Shuttle (reference 2).

This paper discusses the development, design, and performance of a 2.5 Ampere DC Power Controller. Development of this controller involves (1) a realistic investigation of the problems associated with electronically controlled power switching and the power system in which it is designed to operate; and (2) from this investigation, defines a composite of desirable design characteristics. Design of this controller incorporates off the shelf integrated circuits and semiconductors in circuits fulfilling these characteristics. Finally, performance data is reviewed from the operation of a prototype 2.5 Ampere DC Power Controller switching numerous loads at various temperature conditions and power levels.

DC POWER CONTROLLER REQUIREMENTS

A summary of the desirable characteristics for a remote controlled DC power controller that have been generated from previous load controller studies and designs (references 2 through 6) are shown in Figure 1.

As to the quality of these characteristics, there are mixed opinions. Some attempt of universality has been made in MIL-P-81653, Power Controller, Solid State, General Specification for. Nevertheless as one manufacturer states:

This specification [MIL-P-81653] is not yet widely accepted because RPC [Remote Power Controllers] are a new concept and development is not complete enough to cast final performance requirements (reference 3).

For the most part, remote power controllers should be designed to specifically fit the application -- then controller characteristics could be maximized for that particular situation. But to achieve a universal power controller, as many characteristics as possible should be standardized. However due to its complexity and multiple function performance, it becomes exceedingly difficult to standardize for every conceivable application.

The following list of specifications, shown in Figure 2, are those to which the 2.5 Ampere DC Solid State Power Controller was designed. These requirements were considered to be the most important of the overall specifications in MIL-P-81653. Additional requirements were felt

to be part of system design or system interface for a particular application.

- LOW CONTACT VOLTAGE DROP ACROSS POWER SWITCH
- PROVIDE SYSTEM PROTECTION FROM OVERLOADS
- REMOTELY CONTROLLED FROM LOWER VOLTAGE SIGNALS
- SOFT CURRENT OR VOLTAGE TURN ON/OFF RAMPS
- ELECTRICAL INDICATION OF CONTROLLER STATUS
- OPERABLE OVER VOLTAGE TRANSIENTS OF MIL-STD-704A
- ELECTRICAL ISOLATION OF CONTROL CIRCUIT FROM POWER SWITCH
- LARGE OPERATING TEMPERATURE RANGE, -55°C TO 125°C
- HIGH OPERATING EFFICIENCY – 95%
- MINIMUM QUIESCENT POWER DRAIN
- SHORT CIRCUIT PROTECTED
- POSITIVE LOAD SWITCHING
- MINIMAL SIZE AND WEIGHT
- INFINITE OPERATIONAL LIFE

FIGURE 1 DESIRABLE D.C. POWER CONTROLLER CHARACTERISTICS

- LOW VOLTAGE POWER SWITCH CONTACT DROP, 0.5 VOLT MAX. AT RATED LOAD
- POSITIVE LOAD SWITCHING
- INVERSE TIME TRIP OUT FOR OVERLOADS UP TO 7 TIMES RATED
- IMMEDIATE TRIP OUT FOR ALL LOADS GREATER THAN 7 TIMES RATED
- SOFT CURRENT TURN ON/OFF RAMPS, ONE MILLISECOND MINIMUM
- REMOTELY ACTUATED FROM A LOW VOLTAGE, BINARY SIGNAL
- OPERABLE OVER VOLTAGE TRANSIENTS OF MIL-STD-704A
- SHORT CIRCUIT PROTECTED
- OPERATING TEMPERATURE RANGE -40°C TO $+85^{\circ}\text{C}$
- COMPLETELY SOLID STATE
- HIGH EFFICIENCY – 95%
- DESIGNED FROM CONVENTIONAL “OFF-THE-SHELF” COMPONENTS.

FIGURE 2 2.5 AMPERE POWER CONTROLLER DESIGN REQUIREMENTS

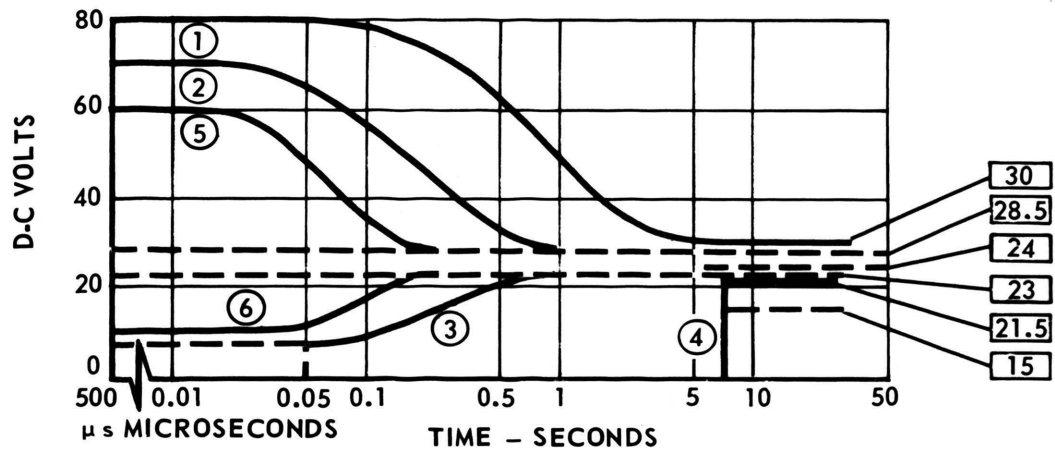
CIRCUIT DESIGN CONSIDERATIONS

Compliance with Voltage Transients of MIL-STD-704A

One critical requirement to which the electronic circuitry of such a controller must be designed is the voltage bus variations of MIL-STD-704A, Electrical Power, Aircraft, Characteristics and Utilization of, shown in Figure 3. The controller must operate between the No. 1 and No. 6 curves of Figure 3 without either damage to itself or degradation of its performance. This requirement restricts, somewhat, the direct use of multifunctioned electronic integrated circuits, due to their limited power supply range. The power controller designer is forced to either design all controller circuitry to operate from the +10 to +80 volt range by employing discrete circuit components, or create an internal regulated supply from which these integrated circuits can operate. Either choice requires specialized electronic circuit design. MIL-STD-704A also specifies an additional +600 volt transient for operating DC equipment. Fortunately, the duration of these transients is short enough and their source impedance should be high enough that zener diode protection near the power controller will suppress these transients. Then, 600 volt rated components need not be employed in power controller circuitry.

Low Voltage Drop Across Power Switch

The .5 volt power switch maximum voltage drop eliminates the use of a silicon controlled rectifiers for power switching. Minimum operating voltage drop of these devices is approximately .7 volt. Power transistors driven deep into saturation offer the solution to this .5 volt limit, since V_{ce} (i.e., transistor collector to emitter voltage) of .2



**FIGURE 3 LOCUS OF EQUIVALENT STEP FUNCTIONS
OF THE SEVEREST OVERVOLTAGE SURGE**

to .3 volts can be achieved at high collector currents with utilization of proper switch design. Thus for switching of the positive lead (assuming negative lead grounded), the PNP transistor switch configuration shown in Figure 4(a), can be driven into saturation by current sinking the required base drive. This arrangement can achieve this low (.2 to .3 volts) saturation voltage -- V_{cesat} . The NPN transistor configuration, shown in Figure 4(b), cannot be driven directly to the low V_{cesat} by its very nature. Base current is supplied, in this case, and thus both base current and collector current flow in the load. But to turn this transistor on, the base emitter junction diode must be forward biased. This junction saturation voltage, V_{besat} is nominally .7 volts. Consequently, maximum achievable V_{cesat} of the NPN switch in the prescribed configuration is V_{besat} -- the NPN transistor cannot stay "on" below this potential. In order for the NPN power switch to meet the .5 volt switch drop limit, its base (or its collector) must be driven from a voltage source higher than bus potential. This allows the emitter to pull up to the high potential of +V minus V_{cesat} . However, to accomplish this, dc/dc conversion is required within the power controller.

Choice of either switch has its disadvantages. Use of the NPN switch for positive switching necessitates dc/dc conversion. The PNP switch eliminates the dc/dc converter, but this polarity has limited availability at high currents and voltages due mainly to special manufacturing processes (reference 7).

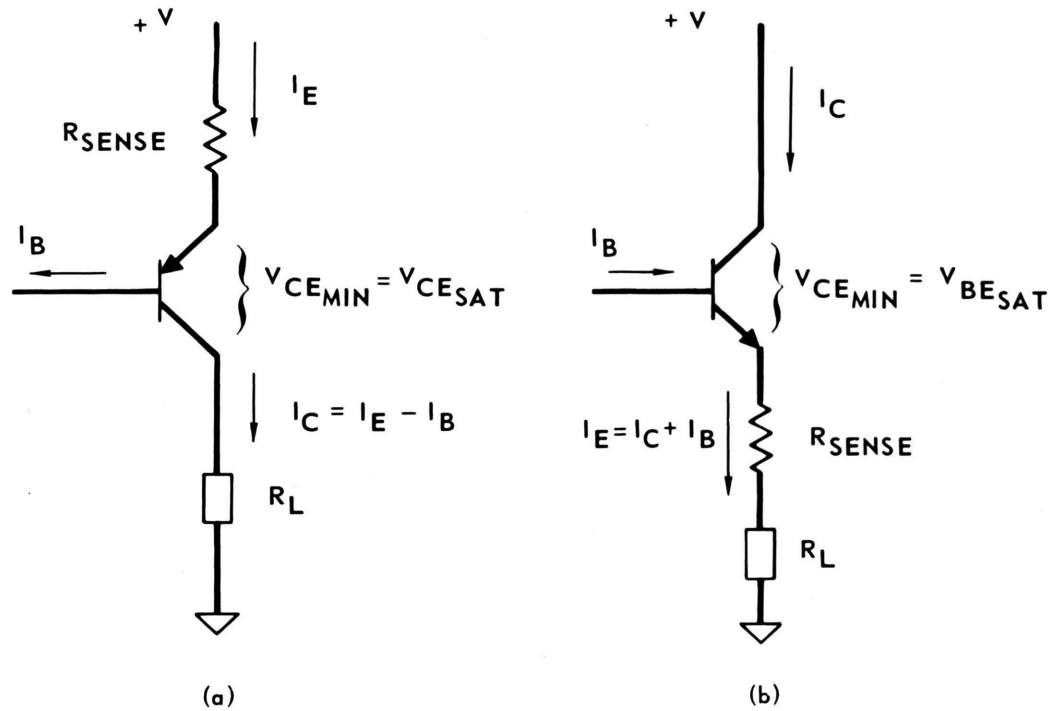


FIGURE 4 PNP AND NPN POWER SWITCH CONFIGURATIONS

Trip Out and Short Circuit Protection

The inverse time trip out function generated by the power controller imposes only one constraint on the power switch -- that the switch be sufficiently sized in current carrying capability and power dissipation to handle overload currents of up to 7 times rated (e.g., during motor start up) for short time durations. In the case of overloads greater than 7 times rated, short circuit protection must be employed to avoid damage to both system and controller. But this requirement -- that an oversized current carrying power switch be employed for inverse trip times -- complicates the design of short circuit protection. Depending on how deeply the power switch is in saturation determines the response time and base drive necessary to limit fault current and force the transistor switch to cut off when a short circuit is applied. Current limiting will protect the power switch from destruction but this limiting level is most important from a system standpoint. High inrush current loads, such as filter capacitors, require that this limit be at least 3 times rated, (to minimize charge time) while up to 10 times rated is needed for motors starting under load. Thus, the current limit that is chosen must be sufficiently large to accommodate these high inrush current loads but yet low enough to protect the transistor from destruction.

Soft Current Turn On/Off Ramps

One of the features of solid state switching over conventional electromechanical switching is that turn on/off current or voltage ramps (i.e., risetimes and falltimes) can be made time dependent. This is to say that the speed at which a solid state switch goes from cut off to

saturation, or vice versa, can be controlled. This property is extremely valuable for high inrush current loads during turn on and highly inductive loads during turn off in the suppression of voltage and current transients. However, the method by which one controls these ramps, whether it be open or closed loop, current or voltage, is critical for the type of load being controlled. For example, application of closed loop current feedback for ramp control may cause response problems if the load is dynamic, as with fast switching regulators. On the other hand, open loop ramp control may exhibit variations in ramp slopes dependent on the gain of the power switch. In either case, ramp control will aid power quality for all types of electrical loads.

DESIGN OF THE 2.5 AMPERE DC POWER CONTROLLER

Figure 5 is a block diagram of the 2.5 Ampere, Remote Controlled, Solid State, DC Power Controller. Each block represents a particular circuit within the power controller that is necessary to satisfy the requirements stated in Figure 2 for resistive, capacitive, inductive, lamp, and motor loads.

Latch Pulse Circuit

One of the requirements listed is remote activation from low voltage digital control signals. The latch pulse circuit accomplishes this function within a signal range of 10 VDC, minimum, to a maximum of controller bus potential. At nominal bus voltage, 28 VDC and 25°C, control current is 1.0 ma. The latch pulse circuit also performs a dual control function: first, it converts the low voltage control signal to the same voltage level from which the power controller will operate; and secondly, it sets a set/reset flip-flop which essentially holds the power controller in the "on" mode of operation until tripped-out or commanded "off". The control signal is not directly isolated from the power controller. If isolation is required, optical coupling can be incorporated.

Control Latch

The control latch -- a set/reset flip-flop energized by the latch pulse circuit -- is a memory device that begins the power controller turn on sequence. This latch is reset by the inverse time trip out, the immediate trip out function, or the Boolean inverse of the control signal. The control latch provides the control necessary to energize

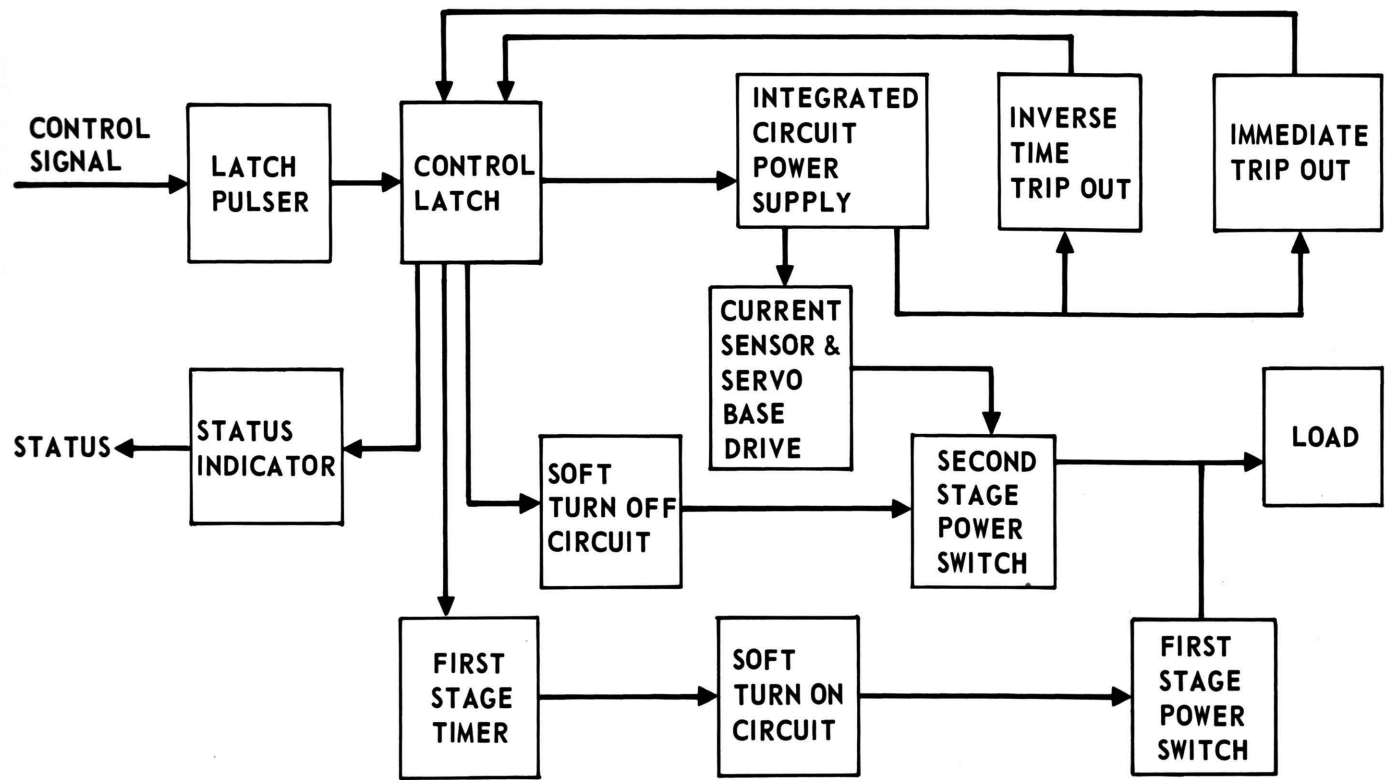


FIGURE 5 BLOCK DIAGRAM OF 2.5 AMP D.C. POWER CONTROLLER

the first stage power switch timer, the current sense control amplifier and comparator power supply, and initiate the soft turn off current ramp to deenergize the second stage power switch. In this design, the latch is referenced to the same power return as the power switch in order to perform the above functions; thus, the control latch is exposed to the voltage extremes of MIL-STD-704A and subsequently must be designed to withstand the 80 volt bus surges. This adverse condition requires the latch transistors to be at least 80 V_{ceo} (sustaining voltage, collector to emitter). Approximately 2 ma of current is required by the control latch in the "off" mode.

Integrated Circuit Power Supply

The requirement that off-the-shelf semiconductors and integrated circuits be utilized in power controller design is satisfied by the use of the voltage comparators necessary for the two trip out functions, plus the amplifiers needed for current sensing and base drive power switch control. Unfortunately, maximum operational voltage differential of these devices is well below the 80 volt surge limit. External supplies to power these integrated circuits obviously defeat the idea of a self-contained, self-powered solid state controller. Rather, the integrated circuit power supply should derive its power from the same power bus to which the power controller is connected. This, then, imposes three conditions on the integrated circuit power supply:

- (1) maximum supply voltage differential of 10 VDC;
- (2) maximum 10 VDC regulation for bus voltage variations up to 80 VDC; and
- (3) an artificial (or floating) voltage reference due to the mode of operation for both operational amplifiers and voltage comparators.

The integrated circuit power supply consists of two matched, temperature stable, low current zener diodes in series with three parallel constant current diodes, energized from bus power by means of a transistor switch. The matched zener diodes supply voltage differentials of +4.89 volts. The constant current diodes hold the zeners in regulation for all load and temperature variations, and limit zener current for the 80 volt bus surges.

First Stage Power Switch Timer

When the control latch is energized, a time pulse circuit is initiated to begin the actual power switching of bus power to load. This timer energizes and controls the first stage of a dual stage power switch. The pulse of the timer is strictly a "one shot" operation, and can be reenergized only after the controller has tripped out or has been reset. Pulse duration is 150 milliseconds. Similar to the latch pulser, control latch, etc., this timer circuit is designed to operate in the range of +10 to +80 volts.

Soft Turn On Circuit

The first stage of the power switch must be the stage that satisfies the soft turn on (one millisecond, minimum) requirement since it is this stage that allows the initial power transfer from bus to load. The soft turn on circuit approximately integrates the turn on command from the first stage timer to effectively slow down the base drive of the first stage power switch. In this way, the collector current (which is the load current) of the power switch can only increase at this base drive rate times its own current gain. This controlled method

of turn on is entirely open loop, with a constant rate of turn on; turn on time increases with increasing load current.

First and Second Stage Power Switch

The 2.5 Ampere DC Power Controller employs a dual stage power switch arrangement. The first stage -- that which is controlled by the soft turn on function -- is a timed, passively current limited switch. Maximum current for this stage is three times rated load for the 150 millisecond time duration. The purpose of this stage is to supply enough overload current for a considerable time duration in order that high inrush current loads have sufficiently stabilized and second stage turn on does not result in nuisance trip outs. The second stage is not passively current limited and is the switch that handles load current for continuous operation. The dual stage switch configuration is shown in Figure 6. Both stages of the power switch circuit employ PNP transistors. This polarity allows for low saturation voltage across the power switch in the absence of dc/dc conversion.

Overload Sense and Power Switch Servo Drive Circuitry

Overload current sensing is accomplished in the second stage power switch by monitoring the voltage generated across a series .1 ohm resistor located in the emitter lead of the power switch. The voltage produced is the input to a differential amplifier. In turn, its output makes up one input to a differential integrator; the other input is obtained from the base drive circuit of the second stage switch. To close the loop, the differential integrator feeds a current source that supplies the correct amount of current necessary for the base drive circuit to hold the power switch in saturation at a forced gain of 35.

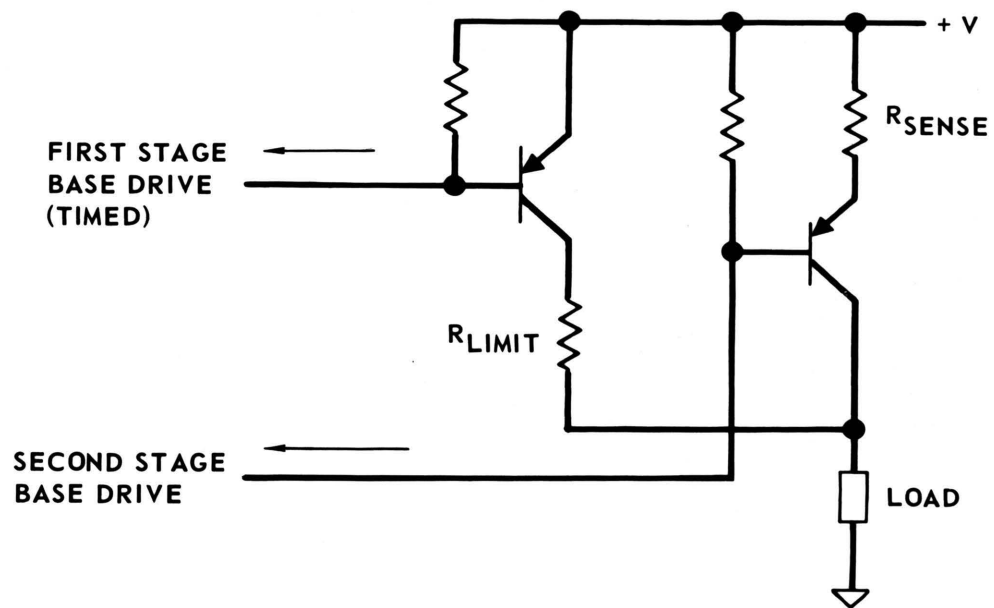


FIGURE 6 DUAL STAGE POWER SWITCH

The voltage output of the differential integrator establishes the desired base drive to closely track this gain for rated loads and larger. The differential integrator also provides stabilization for this closed loop servo.

Inverse Time Trip Out

The inverse time trip-out circuit generates electronically the trip-out function inherent in thermal circuit breakers. Trip-out curves for this controller over temperature are shown in Figure 7. This function is generated by the current sense differential amplifier charging a capacitor through a fixed resistor, but from higher source voltages as load current increases. An analog voltage comparator commands trip-out circuit response to all overloads of 150% to 700%.

Immediate Trip-Out

For loads greater than seven times rated, the immediate trip circuit causes power controller shutdown. Operation of this circuit is similar to the inverse time function in that the load current sense amplifier energizes this circuit by switching another voltage comparator when the amplifier output voltage exceeds a limit corresponding to 700% overload. The comparator then sets a latch which immediately removes the base drive from the power switch. This second voltage comparator bypasses the time delay involved in charging the inverse time capacitor. Thus, fast turn off plus a current limited base drive protects the power switch from drawing excessive currents for relatively long time durations. The trip-out latch is reset when the control command is again recycled.

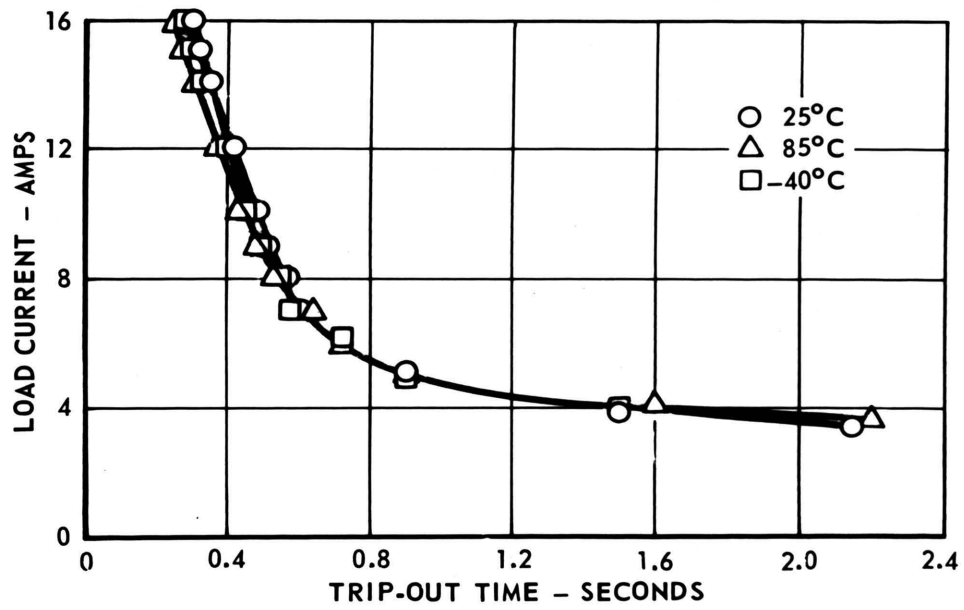


FIGURE 7 CONTROLLER TRIP-OUT CURVE

Soft Turn-Off

The soft turn-off function, like the turn-on function, is also generated open loop. This time, however, the second stage power switch is commanded from saturation to cutoff in one millisecond, minimum, at rated load. Turn off time increases with load due to a constant current rate of reduction in the switch.

Status Indication

The status of the 2.5 Ampere DC Power Controller is given by a five volt Boolean signal. When the controller is energized, the status signal is +5 volts, and capable of supplying 10 ma. When the controller is off or in the trip-out state, the signal is a low impedance to ground. The status indication will directly drive low power T²L (transistor-transistor logic).

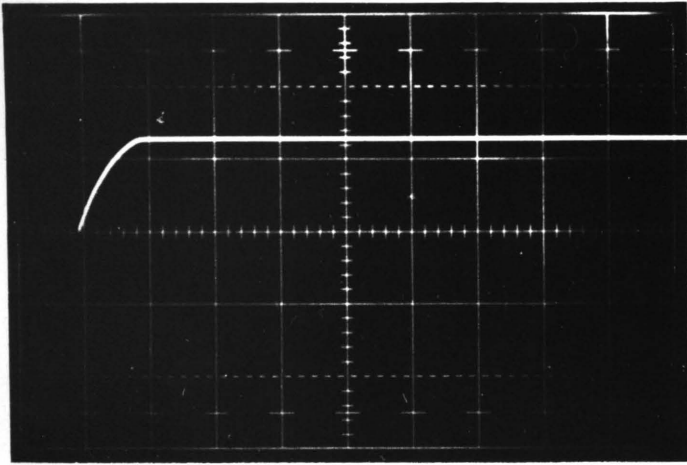
RESULTS

The 2.5 Ampere Remote Controlled DC Power Controller was tested over a temperature range of -40°C to $+85^{\circ}\text{C}$, and bus voltage variations of +10 to +80 volts. The rating of each component within the power controller equalled or exceeded the -55°C to $+125^{\circ}\text{C}$ operational temperature range. Furthermore, where applicable, each semiconductor could tolerate a continuous +80 volt bus surge. Normal controller operation was observed for continuous +10 VDC bus potential, and for +80 VDC bus potential in excess of 100 milliseconds (per MIL-STD-704A) over the -40°C to $+85^{\circ}\text{C}$ temperature range. Overload trip times were recorded at temperatures of -40°C , 25°C and 85°C and at a 28 VDC bus. These plots are shown in Figure 7.

Controller "off" power is 186 milliwatts for the conditions of 28 VDC bus voltage and 25°C . Most of this power is due to the continuously energized set/reset flip-flops within the controller. The controller efficiency at rated load 25°C , and 28 VDC was determined to be 95.3%.

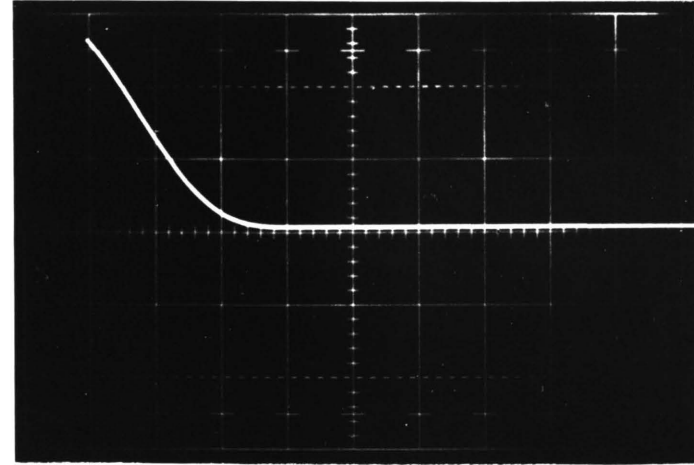
Typical capacitive, inductive, resistive, lamp and motor loads were energized by the power controller at the temperature settings of -40°C , 25°C and 85°C . Voltage and current waveforms were observed during turn-on and turn-off of these loads. The photographs shown in Figures 8 through 27 illustrate the effects of controlled turn on/off.

The voltage turn-on/off ramps respectively for a rated, 2.5 ampere, resistive load at 25°C are shown in Figures 8(a) and (b). Each ramp is smooth and free of oscillations. The first stage turn-on (at reduced



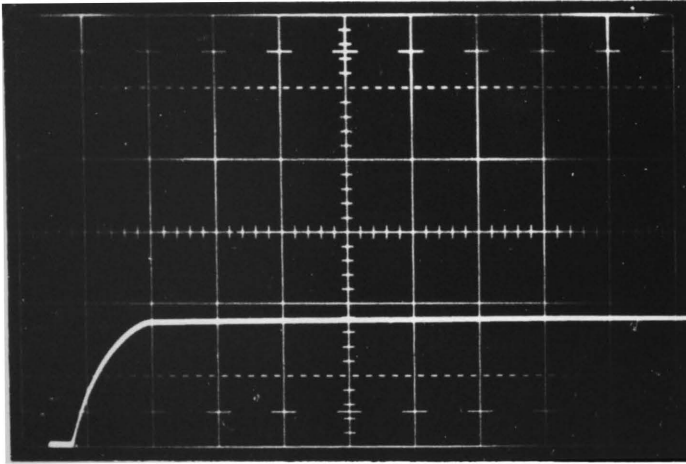
(A)

VERTICAL SCALE: 10 VOLTS DIV
HORIZONTAL SCALE: 1 MSEC DIV



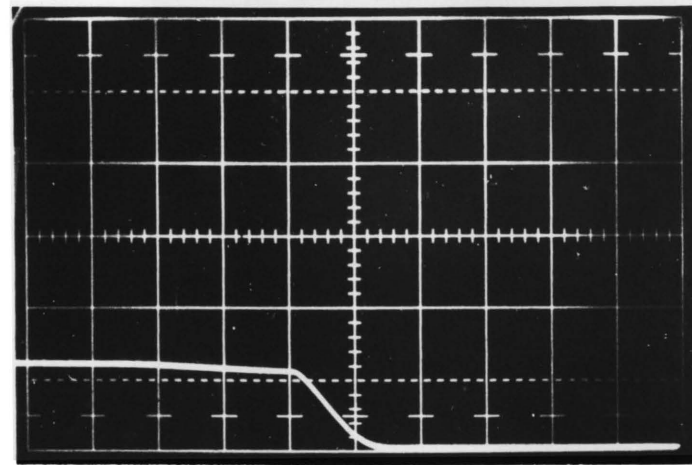
(B)

FIGURE 8 2.5 AMPERE RESISTIVE LOAD - VOLTAGE TURN ON/TURN OFF RAMPS 25°C



(A)

VERTICAL SCALE: 1.25 AMP DIV
HORIZONTAL SCALE: 1 MSEC DIV



(B)

VERTICAL SCALE: 2.5 AMP DIV.
HORIZONTAL SCALE: 2 MSEC DIV

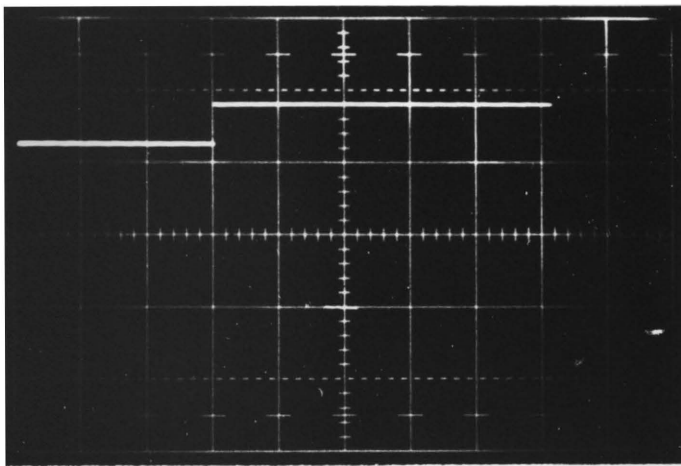
FIGURE 9 2.5 AMPERE RESISTIVE LOAD - CURRENT TURN ON/TURN OFF RAMPS 25°C

voltage) is observed in Figure 8(a). Figures 9(a) and (b) are the current waveforms, respectively, for the same resistive load.

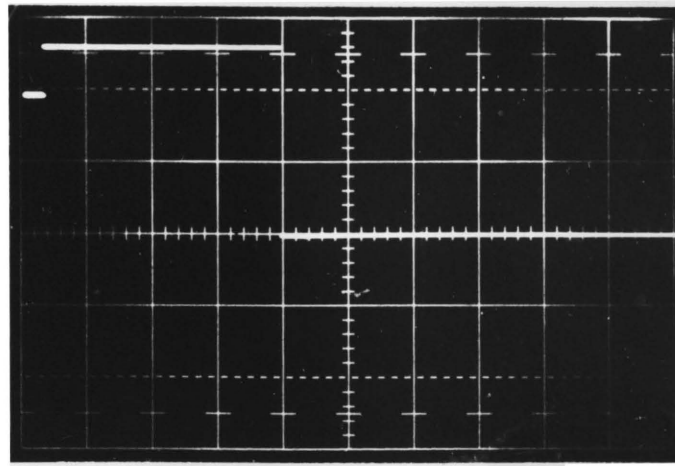
Figures 10(a) and (b) show the power switch output voltage for the dual stage turn-on and the 150% resistive overload trip-out, respectively, at 25°C. First stage turn-on is set at approximately 150 milliseconds; 150% overload trip-out time is set at the minimum of two seconds.

Figures 11(a) and (b) are the current waveforms for turn-on into a 500 μ f capacitor by means of a toggle switch (a) and the power controller (b), at 25°C. As expected, the capacitor draws enormous current for a short period of time when energized by the toggle switch. The power controller, on the other hand, limits this surge significantly by means of its one millisecond soft turn-on. Figures 12(a) and (b) illustrate the inrush current for a 2.5 ampere lamp load energized by a toggle switch and power controller, respectively, at 25°C. Inrush current for this lamp load is greater than six times rated when energized by the toggle switch. But, due to the soft turn-on and the first stage passive current limiting of the power controller, transient inrush current to the cold lamp filaments is significantly reduced. In fact, less than three times rated load current is drawn initially. Furthermore, second stage turn-on has been delayed sufficiently to cause very little current variation when energized, as also shown in Figure 12(b).

Current waveforms for toggle switch and controller turn-on of an unloaded 1/8 horsepower, DC brush-type, aircraft motor with brake

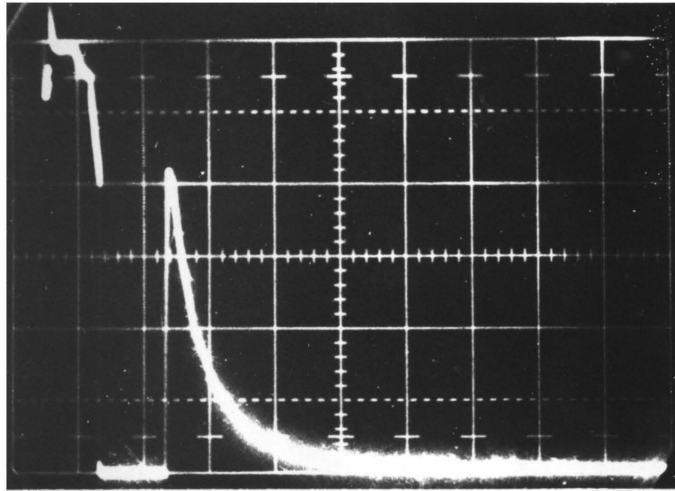


(A)
VERTICAL SCALE: 10 VOLTS DIV.
HORIZONTAL SCALE: 50 MSEC DIV.

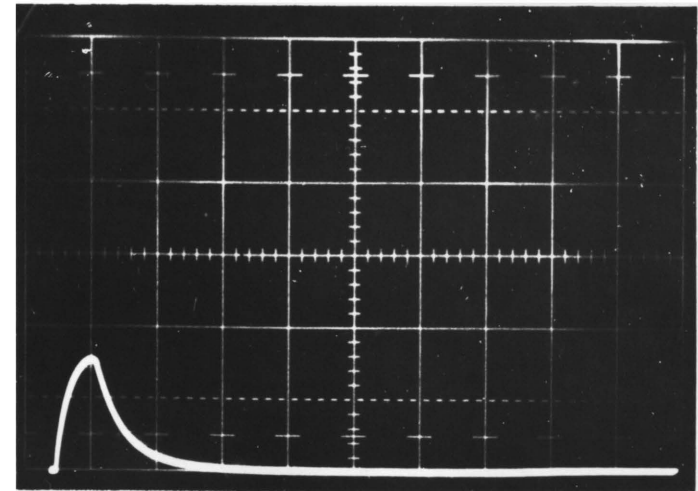


(B)
VERTICAL SCALE: 10 VOLTS DIV.
HORIZONTAL SCALE: .5 SEC DIV.

FIGURE 10 DUAL STAGE TURN ON, 150% TRIP OUT WAVEFORMS

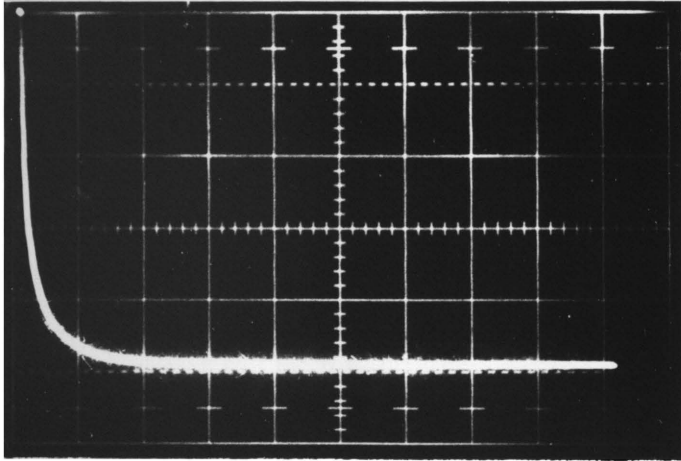


(A)
VERTICAL SCALE: 2.5 AMP DIV.
HORIZONTAL SCALE: 5 MSEC DIV.

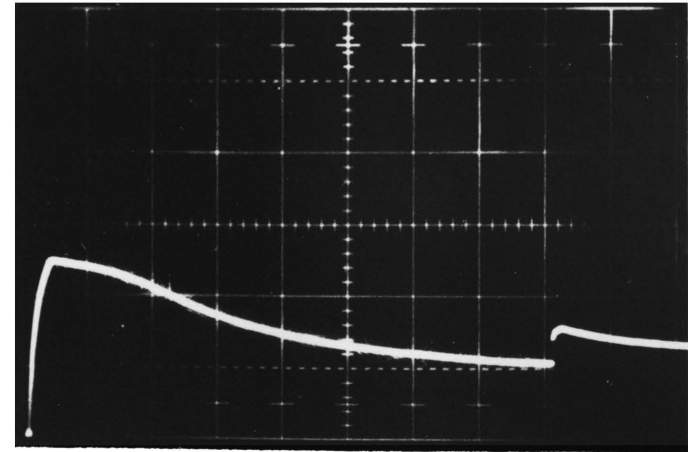


(B)
VERTICAL SCALE: 2.5 AMP DIV.
HORIZONTAL SCALE: 5 MSEC DIV.

FIGURE 11 CAPACITOR INRUSH CURRENT - TOGGLE SWITCH AND POWER CONTROLLER

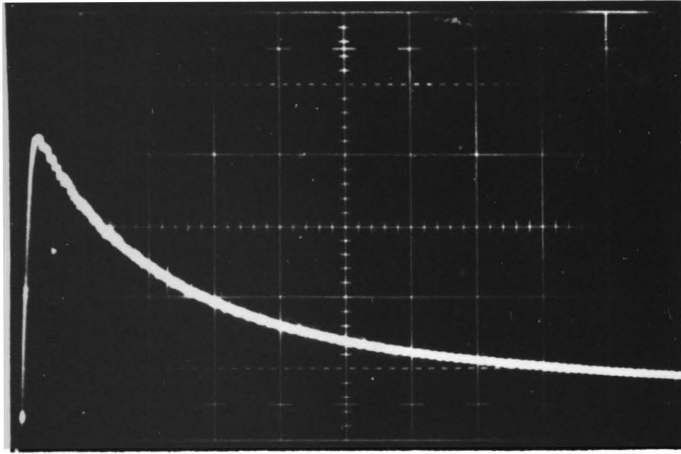


(A)
VERTICAL SCALE: 2.5 AMP/DIV.
HORIZONTAL SCALE: 50 MSEC/DIV.

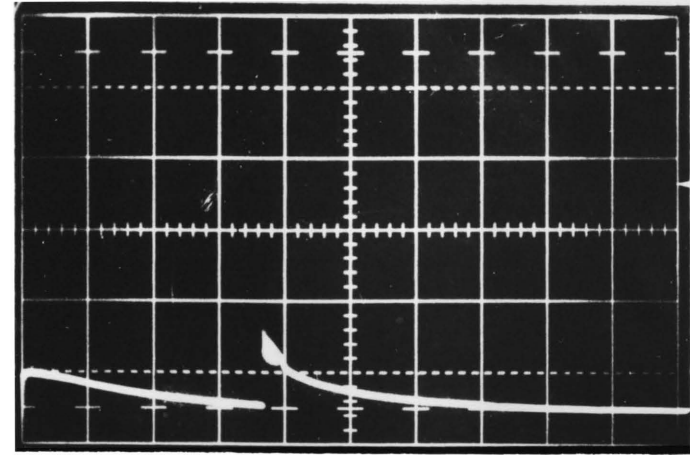


(B)
VERTICAL SCALE: 2.5 AMP/DIV.
HORIZONTAL SCALE: 20 MSEC/DIV.

FIGURE 12 LAMP INRUSH CURRENT - TOGGLE SWITCH AND POWER CONTROLLER



(A)
VERTICAL SCALE: 5 AMP DIV.
HORIZONTAL SCALE: 50 MS DIV.



(B)
VERTICAL SCALE: 5 AMP DIV.
HORIZONTAL SCALE: 500 MSEC DIV.

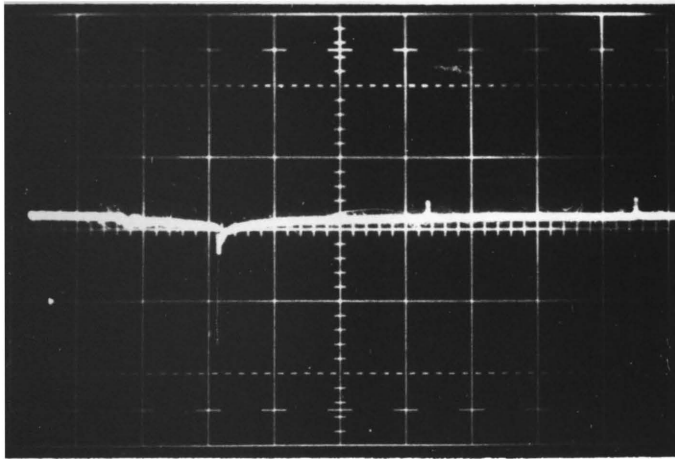
FIGURE 13 INRUSH MOTOR CURRENT - TOGGLE SWITCH AND POWER CONTROLLER

(AiResearch #32370-1), again at 25°C, are shown in Figures 13(a) and (b) respectively. Normal operating current is 2.5 amperes. Figure 13(a) shows that unlimited inrush current is 8.8 times rated (22 amps). However, the power controller turn-on (b) limits this peak to about seven amps. Note that the time duration of the 300% overload limited first stage had to increase from 150 milliseconds to 1.8 seconds to eliminate inverse time trip-out when the second stage was energized. The long time constant of the motor required this extension of operating time for the first stage.

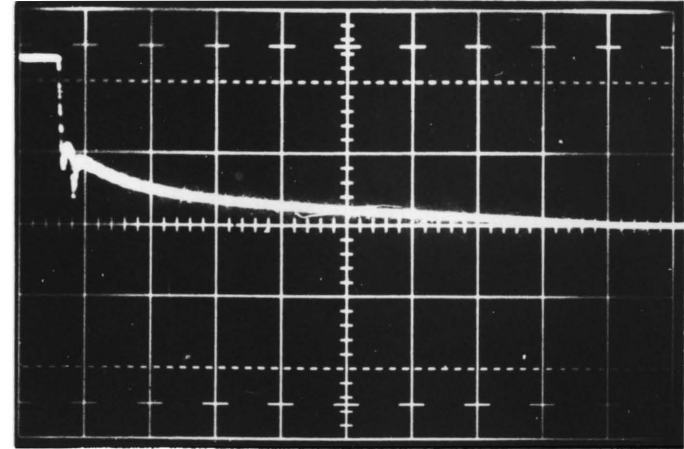
Figures 14(a) and (b) illustrate the voltage transient produced across the same motor when deenergized first by the toggle switch and then the power controller. The negative 160 VDC spike from toggle switch turn-off is not observed when turned off by the two millisecond current ramp of the power controller.

Figures 15(a) and (b) show the voltage transient due to the non-suppressed resistive-inductive load (a Potter and Brumfield KRF14D, 200 ma relay coil) when deenergized again by these two switches, at 25°C. Negative 700 to 800 volt transients are generated by toggle switch turn-off; only a negative 50 volt transient is generated by the soft turn-off of the power controller.

Finally, the response of the power controller to turn-on into a direct short circuit at 25°C is shown in Figure 16. Maximum current of about 32 amps is drawn for a 40 microsecond duration before the controller trips out. To achieve this, the base drive control was set for this power transistor so that maximum fault current is limited to a

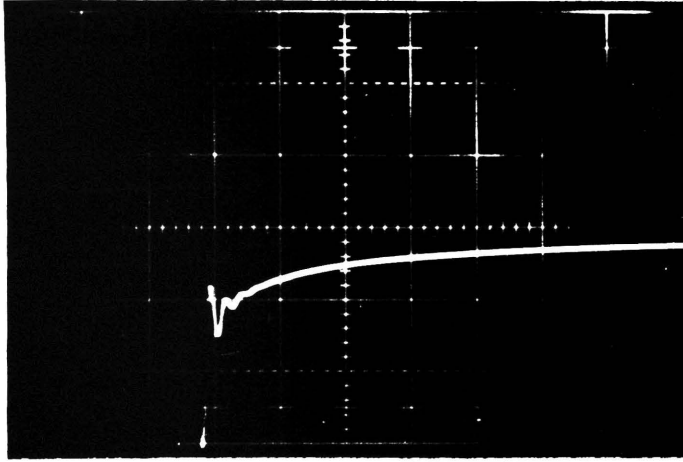


(A)
VERTICAL SCALE: 100 VOLTS DIV.
HORIZONTAL SCALE: .1 MSEC DIV.

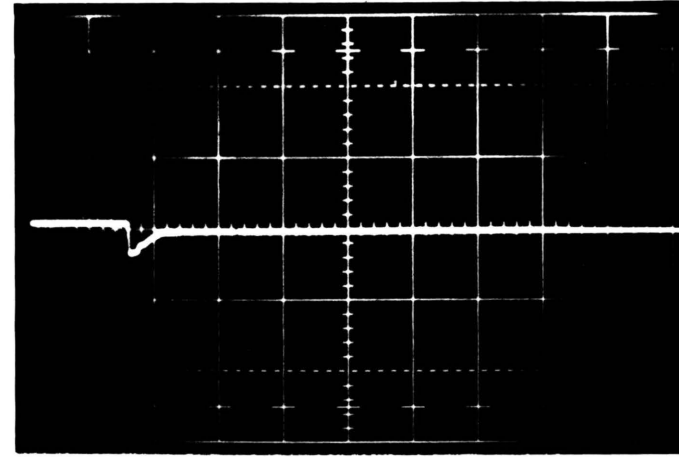


(B)
VERTICAL SCALE: 10 VOLTS DIV.
HORIZONTAL SCALE: 20 MSEC DIV.

FIGURE 14 MOTOR TURN OFF VOLTAGE - TOGGLE SWITCH AND POWER CONTROLLER

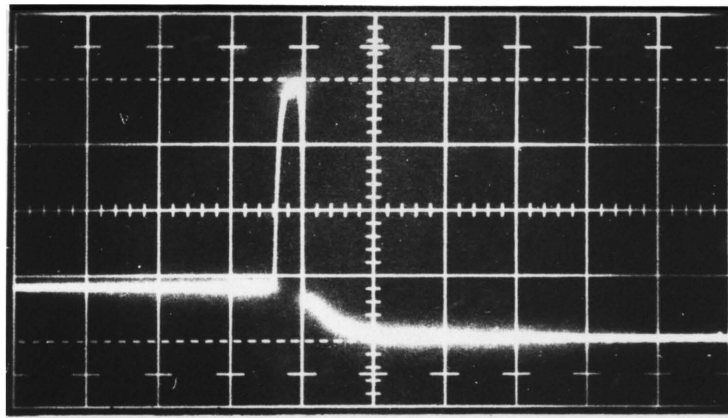


(A)
VERTICAL SCALE: 200 VOLTS/DIV.
HORIZONTAL SCALE: .1 MSEC/DIV.



(B)
VERTICAL SCALE: 200 VOLTS/DIV.
HORIZONTAL SCALE: 50 MSEC/DIV.

**FIGURE 15 INDUCTIVE VOLTAGE TURN OFF
TRANSIENT - TOGGLE SWITCH AND
POWER CONTROLLER**



VERTICAL SCALE: 8 AMP/DIV.
HORIZONTAL SCALE: 100 MSEC/DIV.

**FIGURE 16 POWER CONTROLLER RESPONSE TO
SHORT CIRCUIT TURN ON**

value that allowed safe power switch operation for the short period of time (40 microseconds) required to command the power switch immediately off. The transistor power switch helps to protect itself in short circuit conditions of excessive base drive is not supplied. For example, consider the power switch saturated at rated load and then the load is short circuited. If base control is allowed to increase and try to keep the power switch saturated, the fault current would destroy the switch within microseconds. But, if the base drive increased to some preset limit, the power transistor will pull out of saturation and consequently limit this fault current. This current limiting is due to the rapid decrease in transistor gain at high collector currents. A typical gain curve for this transistor power switch is shown in Figure 17(a). Short circuit protection then becomes a matter of choosing the current base drive limit corresponding to the finite time required to turn off the power switch with the immediate trip-out function. This combination allows the transistor to operate in its safe operating area (SOA). Figure 17(b) gives a typical SOA curve.

The soft turn-on/off voltage waveforms, the capacitive, lamp and motor starting current waveforms, and the inductive voltage turn-off for a nominal 28 VDC bus and +85^o ambient temperature are illustrated in Figure 18 through 22. Similar records for -40^oC ambient temperature operation are shown in Figure 23 through 27. The turn-on/turn-off voltage ramp slopes deviate somewhat from the 25^oC values. This variation is due to the small change of transistor gain over this temperature range. Nevertheless, the load response waveforms indicate that these variations are relatively insignificant.

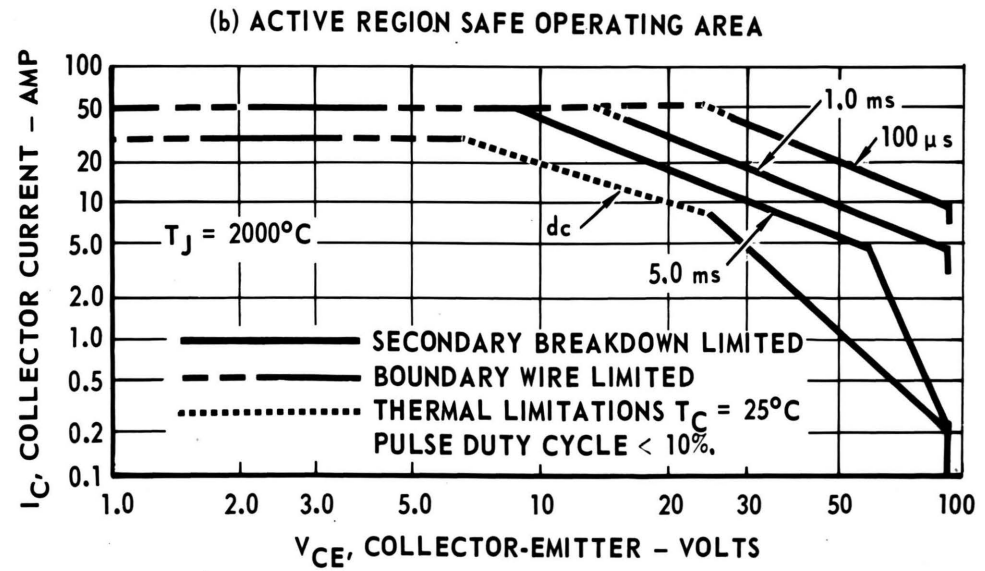
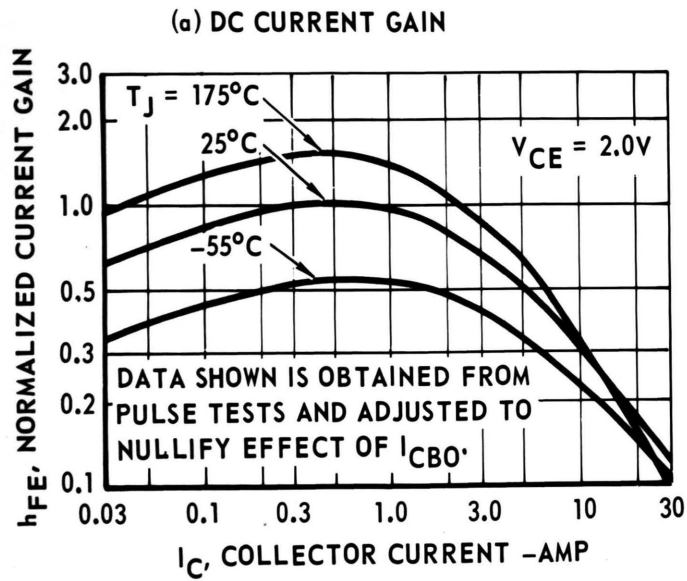
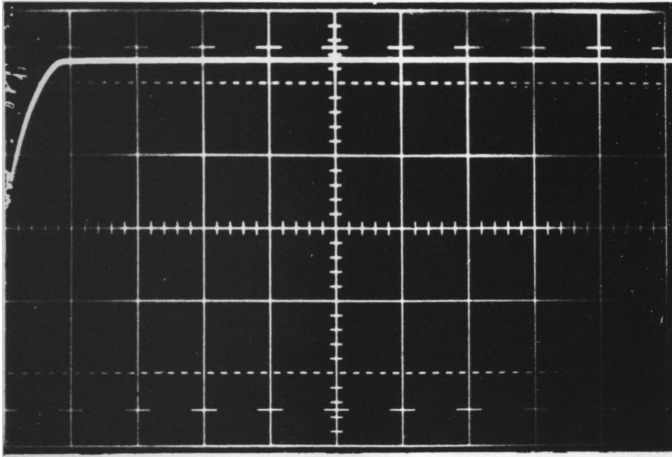
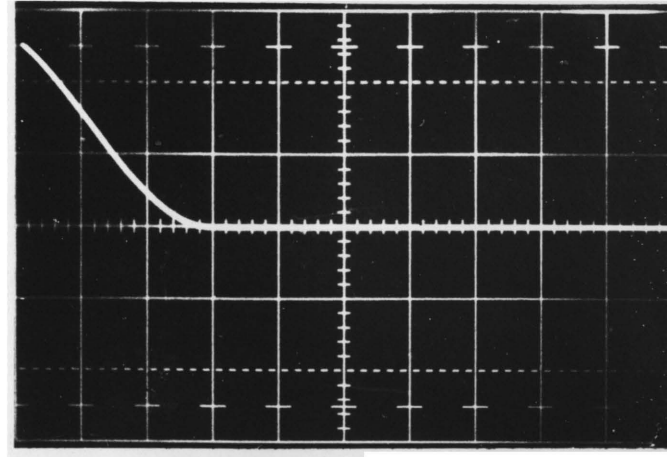


FIGURE 17 POWER SWITCH TRANSISTOR PARAMETERS



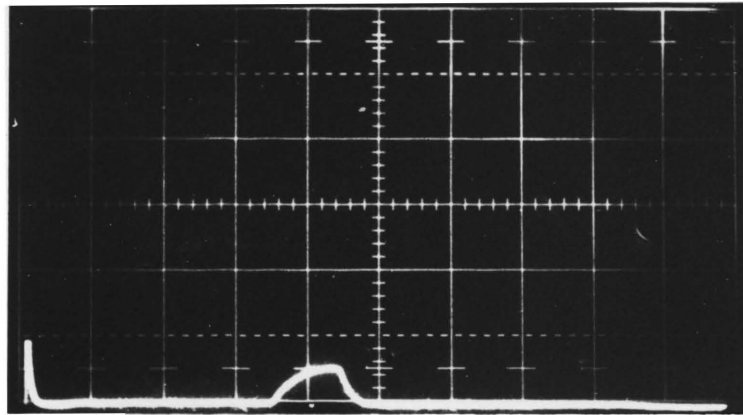
(A)

VERTICAL SCALE: 10 VOLTS DIV.
HORIZONTAL SCALE: 1 MSEC DIV.



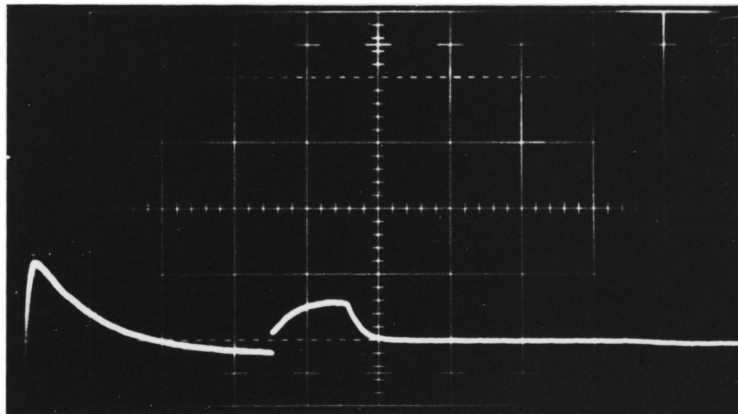
(B)

FIGURE 18 2.5 AMPERE RESISTIVE LOAD - VOLTAGE TURN ON/TURN OFF RAMPS 85°C



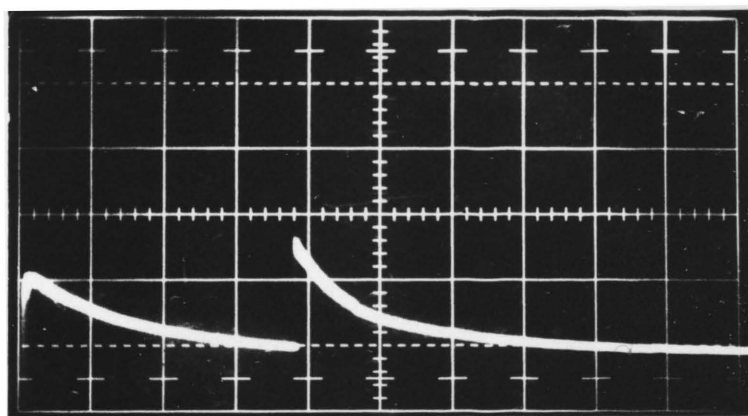
VERTICAL SCALE: 2.5 AMP DIV.
HORIZONTAL SCALE: 50 MSEC DIV.

**FIGURE 19 CAPACITOR INRUSH CURRENT - POWER
CONTROLLER 85°C**



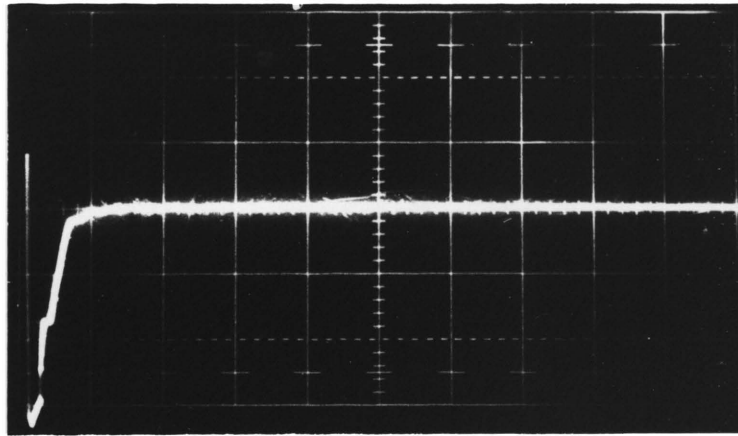
VERTICAL SCALE: 2.5 AMP/DIV.
HORIZONTAL SCALE: 50 MSEC/DIV.

**FIGURE 20 LAMP INRUSH CURRENT - POWER
CONTROLLER 85°C**



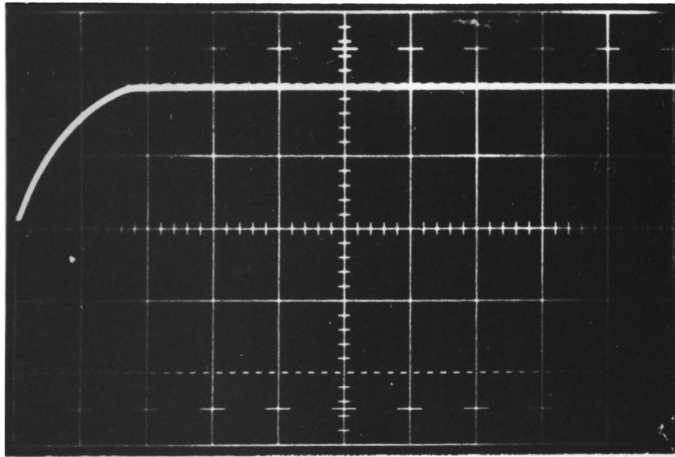
VERTICAL SCALE: 2.5 AMP/DIV.
HORIZONTAL SCALE: 500 MSEC/DIV.

**FIGURE 21 MOTOR INRUSH CURRENT - POWER
CONTROLLER 85°C**



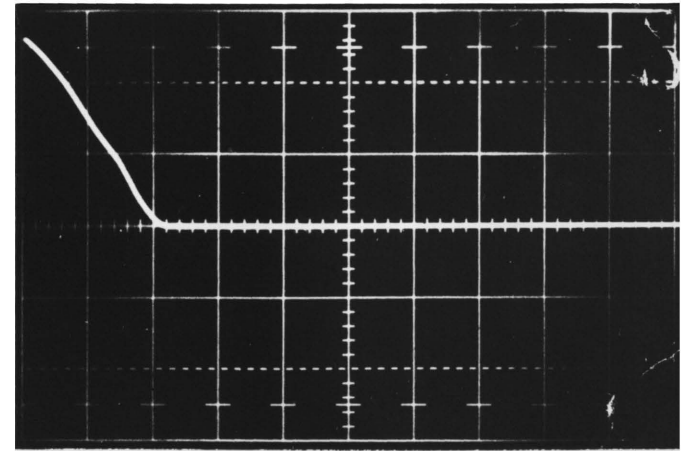
VERTICAL SCALE: 20 VOLTS/DIV.
HORIZONTAL SCALE: 10 MSEC/DIV.

**FIGURE 22 INDUCTIVE VOLTAGE TURN OFF
TRANSIENT - POWER CONTROLLER 85°C**



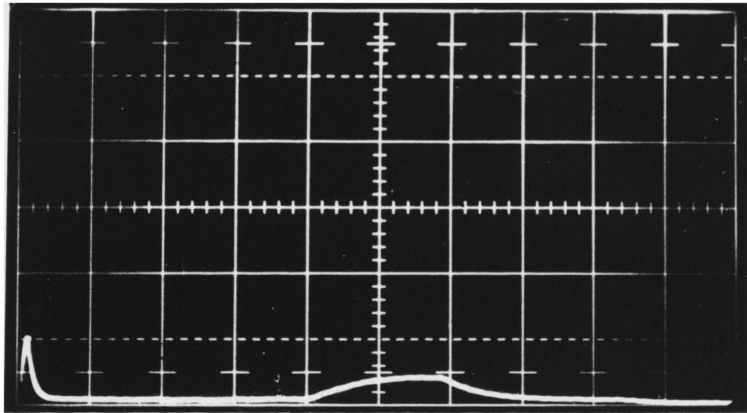
(A)

VERTICAL SCALE: 10 VOLTS DIV.
HORIZONTAL SCALE: 1 MSEC DIV.



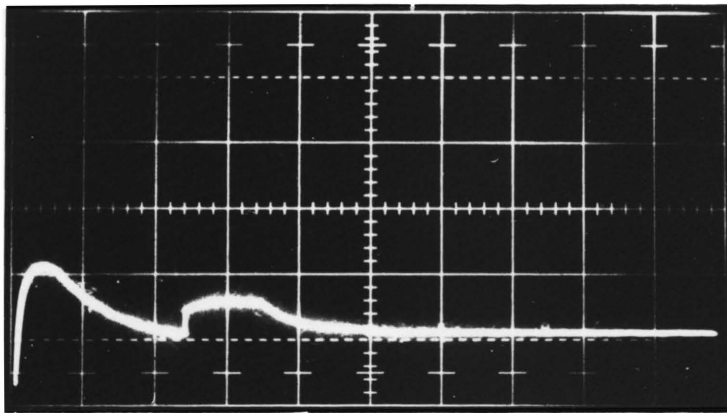
(B)

FIGURE 23 2.5 AMPERE RESISTIVE LOAD - VOLTAGE TURN ON/TURN OFF RAMPS -40°C



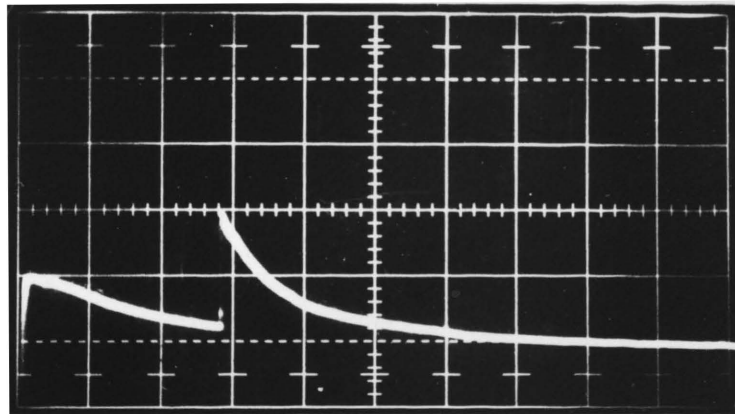
VERTICAL SCALE: 2.5 AMPS/DIV.
HORIZONTAL SCALE: 20 MSEC/DIV.

**FIGURE 24 CAPACITOR INRUSH CURRENT - POWER
CONTROLLER -40°C**



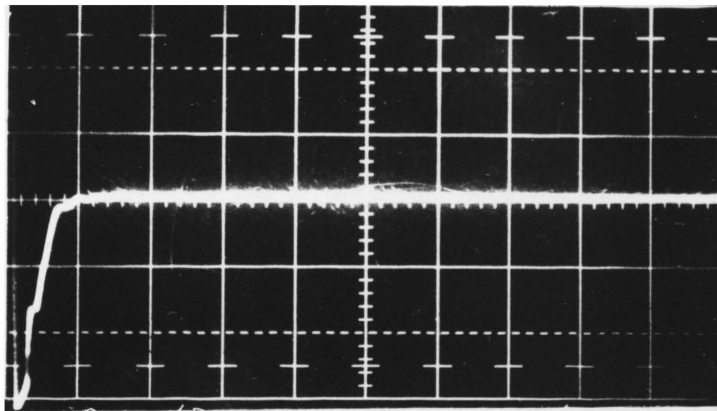
VERTICAL SCALE: 2.5 AMP / DIV.
HORIZONTAL SCALE: 50 MSEC / DIV.

**FIGURE 25 LAMP INRUSH CURRENT - POWER
CONTROLLER -40°C**



VERTICAL SCALE: 2.5 AMP DIV.
HORIZONTAL SCALE: 500 MSEC DIV.

FIGURE 26 MOTOR INRUSH CURRENT - POWER CONTROLLER -40°C



VERTICAL SCALE: 20 VOLTS/DIV.
HORIZONTAL SCALE: 10 MSEC/DIV.

FIGURE 27 INDUCTIVE VOLTAGE TURN OFF
TRANSIENT POWER CONTROLLER -40°C

CONCLUSIONS

From the previous section, it is obvious that the effects of the 2.5 Ampere DC Power Controller upon power quality is most beneficial. The detrimental response of high inrush current loads controlled by relays or mechanical switches is eliminated with the two stage and soft current turn-on of this solid state power controller. Similarly, the voltage transient due to current interruption of inductive loads is also reduced by the controlled di/dt rate of the soft turn-off function.

Unless precision is demanded, the open loop controlled method of soft current turn-on/turn-off is a simpler approach to reduce load switching transients. Precise prediction of voltage or current turn-on/turn-off ramps over a range of load and temperature may be desirable, but this requirement dictates a closed loop control system in which load current or voltage is controlled by tracking a fixed reference. In such a system, control of highly reactive loads (due to phase angle relationships) becomes critical for stable power controller operation. Thus, some limitation of current range and/or type of load controlled may be imposed on the power controller incorporating closed loop control.

The method of handling overcurrent and short circuit conditions is critical in both power controller and power system design. Some form of current limiting must be incorporated internal to the solid state power controller for its own protection. But current limiting at 150%-300% of rated current loads (followed by trip-out) is too restrictive, for example, when DC motors under load requiring up to ten times rated current for starting must be controlled. Thus, two switch requirements

must be met: (1) the power switch must be capable of handling in the range of seven to ten times rated load current (for short periods of time at least corresponding to the inverse time trip function) before going into current limiting. This forces the power rating of the transistor switch to greatly exceed rated conditions, or in other words, a 25 amp power switch must be used to control a 2.5 amp load. (2) The power switch must current limit at some preset level above this range, followed by immediate turn-off. This allows the transistor to stay within its safe operation region. The 2.5 Ampere Power Controller allows 700% rated current to flow before immediate trip-out commands shutdown. Furthermore, the maximum allowable power switch current, together with the response time of the immediate trip function, are set to fall within this transistor safe operating region.

The minimum contact voltage drop requirement plus the desire to switch the positive load lead tends to favor PNP over NPN power switches. Unfortunately, the availability of high current, high voltage and high gain PNP devices are limited. Power controller designs utilizing the more available NPN transistor, nevertheless, require dc/dc conversion in order to meet the .5 volt switch drop required for a 28 VDC system. This 2.5 Ampere Solid State Power Controller incorporates the PNP switch design. Higher current controllers can be achieved by paralleling PNP transistors, but this approach over the use of a single NPN transistor for high current controllers, however, needs further investigation.

One means of reducing solid state controller cost, size and complexity, while increasing operating efficiency is to make use of low

powered, multi-functioned, off-the-shelf, integrated circuits (CMOS, for example). However, these circuits cannot tolerate the voltage extremes of MIL-STD-704A. If these variations can be re-evaluated and possibly reduced or eliminated from the power system, solid state controller design would be greatly simplified.

Solid state power controllers can enhance power system design by improving overall power quality. They can also solve the problem of remote power control in a data multiplexed system. But maximum benefits from these devices require that power system designers become aware of the problem areas related to solid state controllers, designed to the antiquated and possibly superfluous requirements long set by past electromechanical systems. Similarly, designers of solid state power controllers must realize the problems associated with DC power systems and control of all types of electrical loads. This mutual investigation will provide optimum solid state power controller as well as power system distribution design.

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- 2 Boykin, J. C., and others. "Solid State Power Controllers," Proceedings of the Conference Held at NASA Manned Spacecraft Center, Houston, Texas, May 11-13, 1971. NASA TMX-58063, Vo. II., 105-131. Washington: National Aeronautical and Space Administration, 1971.
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- 5 Maus, L. G. and Williams, D. E. "Solid State DC Power Controller Design Philosophies and Their Evaluation," Proceedings of the 20th Relay Conference Held at Oklahoma State University, Stillwater, Oklahoma, April 18-20, 1972.
- 6 Trowbridge, W. A. and Freisen, T. H. "Solid State Power Controllers," Phase I and II reports prepared for NASA Marshall Space Flight Center by SCI Electronics, Inc., Prime Contract NAS 8-26092, August 1971.
- 7 Fordemwallt, J. N., (ed.). Integrated Circuits - Design Principles and Fabrication. New York: McGraw Hill, 1965.

APPENDIX A

LATCH PULSER

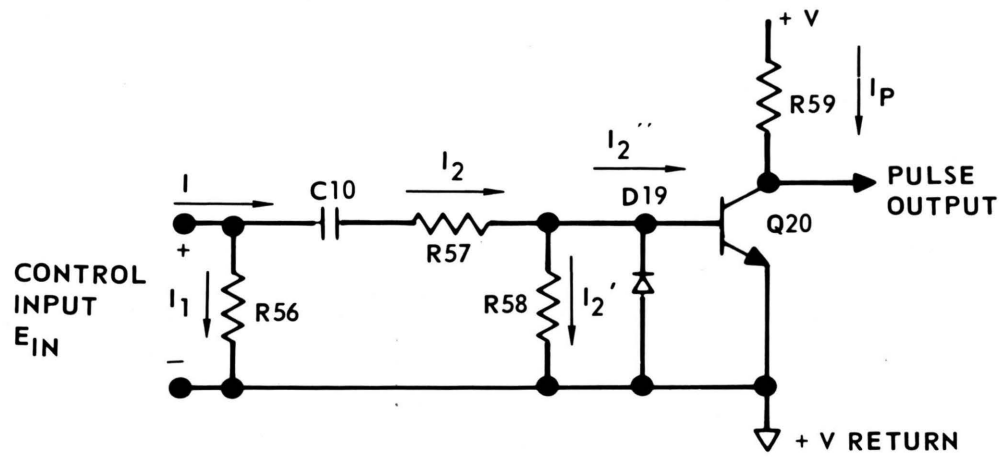


FIGURE A-1 LATCH PULSER

COMPONENT LIST

R56 = 27K Ω , 1/4W, 5%

R57 = 27K Ω , 1/4W, 5%

R58 = 27K Ω , 1/4W, 5%

R59 = 27K Ω , 1/4W, 5%

C10 = 100pf, 100 VDC, 10%

D19 = 1N914

Q20 = 2N3019, NPN

ASSUMPTIONS:

1. $\beta(h_{fe})$ of Q20 \geq over temperature range of -40°C to $+85^{\circ}\text{C}$ and 1 ma collector current.
2. V_{besat} (Q20) = .75 VDC.
3. V_{cesat} (Q20) = .2 VDC @ 1 ma collector current.
4. Leakage current for Q20, $I_{cbo} = 10 \mu\text{a}$ maximum.
5. $E_{IN} = 28 \text{ VDC}$ "ON"; 0 VDC "OFF"; step input.
6. $+V = 28 \text{ VDC}$.

ANALYSIS AND OPERATION:

$$I = I_1 + I_2$$

$$I_2 = I_2' + I_2''$$

$$I_1 = \frac{E_{IN}}{R56} = \frac{28\text{V}}{27\text{K}\Omega} = 1.04 \text{ ma}$$

$$E_{IN} = (R57 + R58) I_2 + \frac{I_2}{C10} \int_0^t E_{IN} dt + V_{C10} (0)^+$$

before Q20 saturates.

$$\text{If } C10 (0)^+ = 0 \text{ VDC}$$

Then

$$\frac{E_{IN}(s)}{I_2(s)} = (R57 + R58) + \frac{1}{(s)(C10)}$$

$$I_2(s) = \frac{E_{IN}(s)}{(R57 + R58)} + \frac{1}{(s)(C10)}$$

$$E_{IN}(s) = \frac{28}{s}$$

Therefore

$$i_2(t) = \frac{28}{(R57 + R58)} \left(e^{-\frac{t}{(R57 + R58)(C10)}} \right) = I_2(0)^-$$

Q20 will turn On when

$$[I_2'] [R58] \geq .75V \text{ (i.e., } V_{\text{besat}})$$

Since Q20 has a h_{fe} of ≥ 50

$$I_P = h_{fe} (I_2'')$$

$$I_2'' \text{ max} = \left(\frac{E_{IN} - .75}{R57} \right) - \left(\frac{.75}{R58} \right) = 1 \text{ ma}$$

$$I_P \text{ max} = \frac{+V - V_{\text{cesat}} (Q20)}{R59} = \frac{27.8V}{27K\Omega} = 1 \text{ ma}$$

at $t = 0+$

$$V_{R58} = 14.5 \text{ VDC if unloaded}$$

$$14.5 \text{ VDC} \gg V_{\text{besat}} (Q20)$$

Q20 will saturate immediately. Once Q20 saturates, then

$$i_2(t) = \frac{28 - .75}{R57} \left(e^{-\frac{t}{(R57)(C10)}} \right) \text{ Q20 will turn off when}$$

$$[I_2'] [R58] \leq .75 \text{ VDC}$$

$$I_2' = \frac{.75V}{27K\Omega} = .0278 \text{ ma}$$

Pulse time is

$$.0278 = \left(\frac{28 - .75}{R57} \right) \left(e^{-\frac{t}{(R51)(C10)}} \right)$$

$$.0278 = \left(\frac{27.25V}{27K\Omega} \right) \left(e^{-\frac{t}{2.7 \times 10^{-6}}} \right)$$

$$t = 10 \text{ } \mu\text{sec}$$

- NOTE:
1. Trailing edge of output pulse will exhibit a longer turn off fall time due to the (R57) (C10) time constant.
 2. D19 protects Q20 from the negative transients of C10 when commanded off.
 3. Q20 leakage current, (10 μ a) (R58) < .75 VDC to turn on Q20.
 4. Leakage current is only power drain on "off" mode.

ON POWER

$$\frac{E_{IN}^2}{27K\Omega} = \frac{28^2}{27K\Omega} = 29 \text{ mw}$$

APPENDIX B

CONTROL LATCH

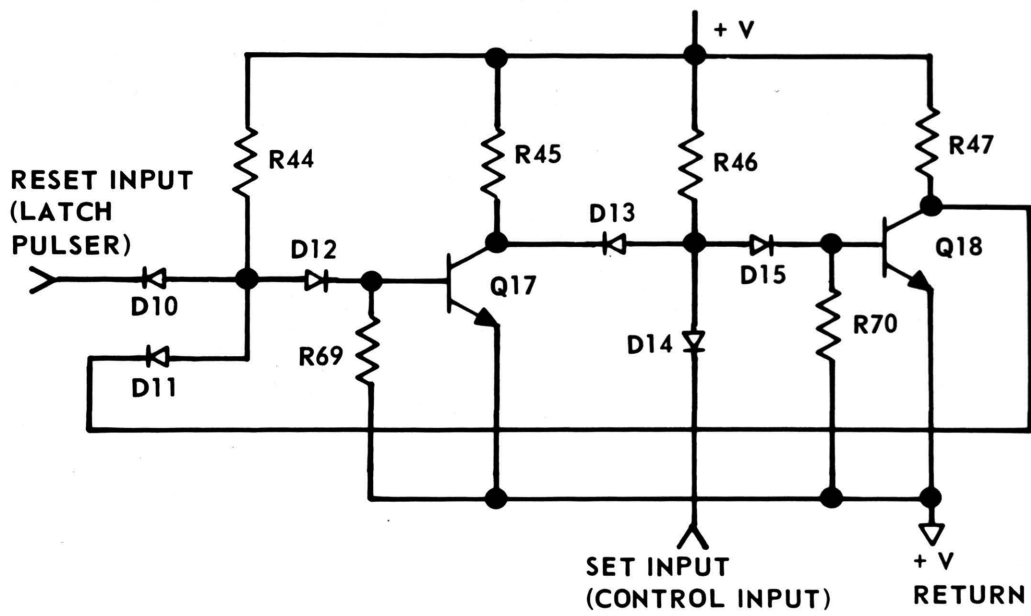


FIGURE B-1 CONTROL LATCH

COMPONENT LIST

R44 - 27K Ω , 1/4 W, 5%

R45 - 15K Ω , 1/4 W, 5%

R46 - 27K Ω , 1/4 W, 5%

R47 - 27K Ω , 1/4 W, 5%

R69 - 51K Ω , 1/4 W, 5%

R70 - 51K Ω , 1/4 W, 5%

D10 - 1N914

D11 - 1N914

D12 - 1N914

D13 - 1N914

D14 - 1N914

D15 - 1N914

Q17 - 2N3019, NPN

Q18 - 2N3019, NPN

ASSUMPTIONS:

1. All diodes forward voltage drop is .75 volt.
2. V_{besat} of Q17 and Q18 = .75 VDC.
3. V_{cesat} of Q17 and Q18 = .2 VDC.
4. h_{fe} of Q17 and Q18 \geq 50.
5. Q17 and Q18 Leakage current $I_{cbo} \leq 10\mu a$.
6. +V = 28 VDC.

ANALYSIS AND OPERATION:

Control Input to the SET input diode, D14, is normally low (i.e., at 0 VDC). Q18 is cut off because the forward drop of D14 and V_{be} is 1.5 VDC. It is this potential that must be exceeded to turn Q18 on. With Q18 off, D10 and D11 are both back biased. Base current $\frac{+V-1.5}{R44}$ forward biases D12 and V_{be} of Q17, driving Q17 into saturations. Collector current, $\frac{+V-V_{cesat}}{R45}$ flows in Q17, and since Q17 is overdriven, (as is Q18 in the reset mode) both Q17 and Q19 go from saturation to cut-off (and vice versa) rapidly.

The voltage V_{cesat} of Q17 is low enough to hold Q18 off even if D14 is open circuited. Transistion occurs when the control input goes positive (+28 VDC). D14 is back-biased while the Latch Pulser output forward biases D10, forcing $\frac{+V-.75}{R44}$ current to now flow in D10 instead of the base of Q17. Q17 thus turns off back-biasing D13. With D13 back-biased, $\frac{+V-1.5}{R46}$ current flows into the base of Q18, causing it to rapidly saturate. The low saturation voltage, V_{cesat} of Q18, is then fed back forward biasing D11. At this time, open-circuiting the control input causes no change in Latch status. The Control Latch is essentially a S-R Flip-Flop.

S-R Truth Table

S	R	Q	\bar{Q}
0	0	Q	\bar{Q}
0	1	0	1
1	0	1	0
1	1	U	U

U - Undetermined

Where

"0" is 0 VDC

"1" is 28 VDC

R69 and R70 are sized to hold Q17 and/or Q19 "off" at maximum I_{cbo}

$$(51K\Omega) (10\mu a) = .51 \text{ VDC} < .75 \text{ VDC}$$

OFF POWER:

$$\left[\frac{+V - V_{cesat}}{R45} \right]^2 (R45) + \left[\frac{+V - 1.5}{R44} \right]^2 (R44) + \left[\frac{+V - V_{cesat}}{R45} \right] (V_{cesat}) +$$

$$\left[\frac{+V - 1.5}{R44} \right] (1.5) + \left[\frac{+V - .75 - V_{cesat}}{R46} \right]^2 (R46) + \left[\frac{+V - .75 - V_{cesat}}{R46} \right] X$$

$$\left[.75 + V_{cesat} \right] = P_{off}$$

$$P_{off} = \left[\frac{(27.8)^2}{15} + \frac{(26.5)^2}{27} \right] X 10^{-3} + \left[\frac{27.8}{15} \right] \left[.2 X 10^{-3} \right] +$$

$$\left[\frac{26.5}{27 X 10^3} \right] \left[1.5 \right] + \left[\frac{(27.05)^2}{27 X 10^3} \right] + \left[\frac{27.05}{27 X 10^3} \right] \left[.95 \right]$$

$$= 107.3 \text{ mw}$$

ON POWER:

$$P_{on} = \left[\frac{(+V - V_{cesat})^2}{R47} \right]^2 \left[R47 \right] + \left[\frac{+V - 1.5}{R46} \right]^2 \left[R46 \right] +$$

$$\left[\frac{+V - V_{cesat}}{R47} \right] \left[V_{cesat} \right] + \left[\frac{+V - 1.5}{R46} \right] \left[1.5 \right] +$$

$$\begin{aligned}
& \left[\frac{+V - .75 - V_{\text{cesat}}}{R44} \right]^2 \left[R44 \right] + \left[\frac{+V - .75 - V_{\text{cesat}}}{R44} \right] \left[.75 + V_{\text{cesat}} \right] \\
= & \left[\frac{(27.8)^2}{27} + \frac{(26.5)^2}{27} \right] \times 10^{-3} + \left[\frac{27.8}{27} \right] \left[.2 \times 10^{-3} \right] + \left[\frac{26.5}{27} \right] \left[1.5 \times 10^{-3} \right] \\
& + \left[\frac{(27.05)^2}{27 \times 10^3} \right] + \left[\frac{27.05}{27K} \right] \left[.95 \right] \\
= & 84.36 \text{ mw}
\end{aligned}$$

NOTE: Power loss due to R69 and R70 is insignificant when Q17 and/or Q18 are "off" or "on".

APPENDIX C

INTEGRATED CIRCUIT POWER SUPPLY

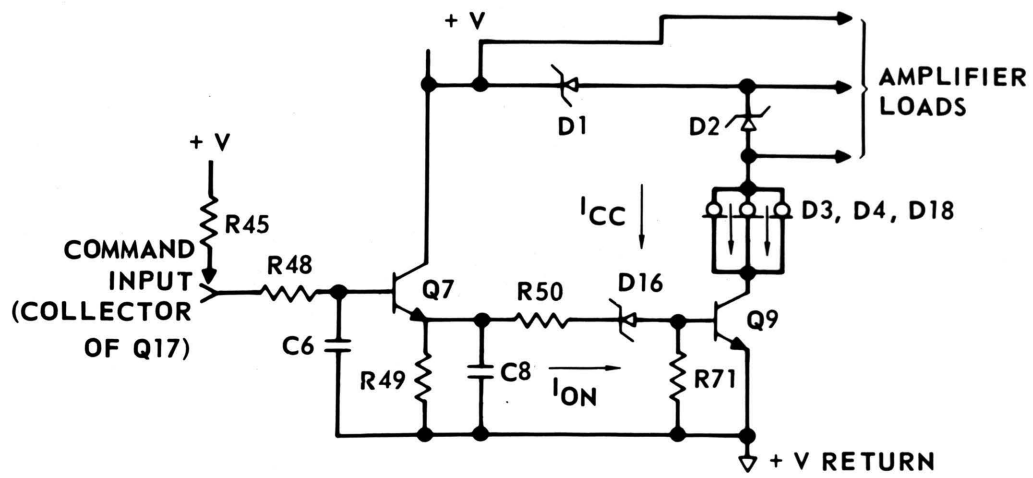


FIGURE C-1 INTEGRATED CIRCUIT POWER SUPPLY

COMPONENTS LIST

R48 - 27K Ω , 1/4 W, 5%
R49 - 100K Ω , 1/4 W, 5%
R50 - 10K Ω , 1/4 W, 5%
R71 - 51K Ω , 1/4 W, 5%
C6 - 2 μ f, 100 VDC, 10%
C8 - .01 μ f, 100 VDC, 10%
D1 - MZ4624, 4.7 VDC, 250 mw
D2 - MZ4624, 4.7 VDC, 250 mw
D3 - IN5314, 4.7ma, 600 mw
D4 - IN5314, 4.7ma, 600 mw
D18 - IN5314, 4.7ma, 600 mw
D16 - MZ4624, 4.7 VDC, 250 mw
Q7 - 2N3019, NPN
Q9 - 2N3019, NPN

ASSUMPTIONS:

1. $V_{cesat} = .2$ VDC for Q7 and Q9.
2. $V_{besat} = .75$ VDC for Q7 and Q9.
3. $h_{fe} \geq$ for Q7 and Q9.
4. Leakage current, $I_{cbo} = 10 \mu a$ max.
5. Q7 is an emitter follower to essentially unload C6 i.e. $(h_{fe}) \times (R49) \gg R45 + R48$.
6. Q7 is compensated by C8 for stability.
7. $+V = 28$ VDC.

ANALYSIS AND OPERATION:

1. From figure C-1

$$V_{C6} = 28 (1 - e^{-\frac{t}{(R45 + R48)(C6)}})$$

where $(R45 + R48)(C6) = (15K\Omega)(27K\Omega)(2\mu f) = 86$ ms

$$V_{R49} = 0 \text{ VDC before commanded turn on.}$$

@ $t = 0 +$, Turn on:

$$\begin{aligned} V_{R49} &= (+V - V_{besat}) (1 - e^{-\frac{t}{86 \times 10^{-3}}}) \\ &= 27.25 (1 - e^{-\frac{t}{86 \times 10^{-3}}}) \end{aligned}$$

Q9 will saturate when $V_{R49} > V_f(D16) + V_{besat} = 5.45$ VDC

R50 limits maximum base current to Q9 to $\frac{(27.25 - 5.45)}{10K\Omega} = 2.18$ ma = I_{on} .

Since $h_{fe} Q9 \geq 50$, Q9 will saturate rapidly with this base current.

The time it takes to saturate Q9 and thus energizing D1, D2, D3, D4 and D18 is

$$\begin{aligned} V_{R49} = 5.45 &= 27.25 (1 - e^{-\frac{t}{84 \times 10^{-3}}}) \\ \frac{(5.45 - 27.25)}{27.25} &= (e^{-\frac{t}{84 \times 10^{-3}}}) \end{aligned}$$

$$t = 18.7 \text{ msec.}$$

TURN OFF:

When commanded off, C6 discharges through R48 to V_{cesat} of Q7.

Discharge is governed by $V_{C6} = (28 V_{cesat}) \left(e^{-\frac{t}{(R48)(C6)}} \right)$

$$(R48)(C6) = 54 \text{ ms}$$

and Q9 will turn off when

$$V_{R49} < 5.45 \text{ VDC} \Rightarrow V_{C6} < (5.45 + .75) \text{ VDC}$$

$$6.2 = 28.2 \left(e^{-\frac{t}{54 \times 10^{-3}}} \right)$$

$$t = 81.5 \text{ msec.}, \text{ turn off time}$$

OFF POWER:

Leakage current accounts for the only quiescent power drawn, and it is considered insignificant.

ON POWER:

$$P_{on} = (3) (I_{cc}) (+V) + \left(\frac{+V_{besat} - V_{fD16} - V_{besat}}{R50} \right)^2 (R50) +$$

$$\left(V_{fD16} - V_{besat} \right) (I_{on}) + (I_{on}) (V_{ce(Q7)}) +$$

$$\left(\frac{(+V - V_{besat})}{R49} \right)^2 (R49) + \left(\frac{+V - V_{besat}}{h_{fe} (R49)} \right) (V_{besat})$$

$$P_{on} = (3) (4.7 \times 10^{-3}) (28) + \frac{(21.8)^2}{10} \times 10^{-3} + (5.45) (2.18 \times 10^{-3}) +$$

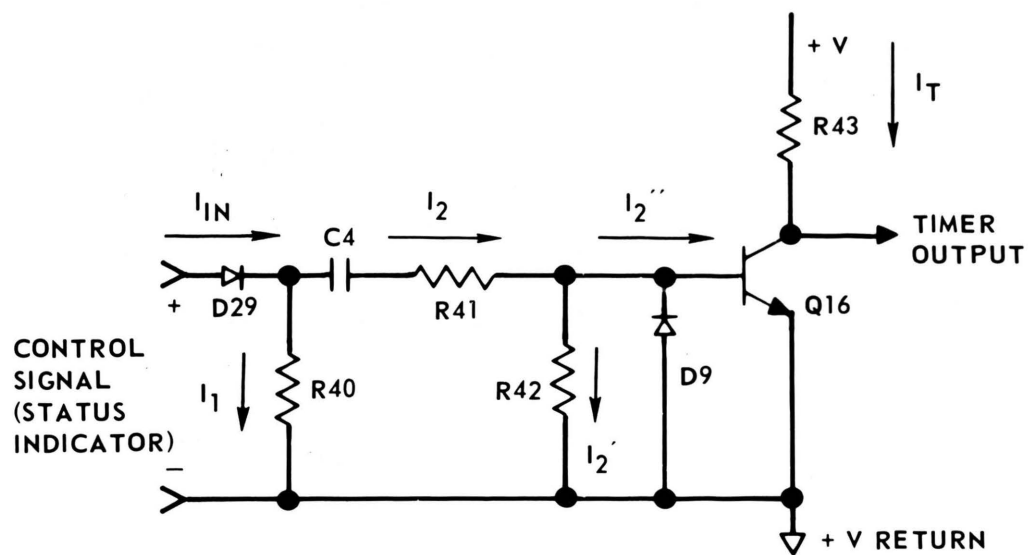
$$(2.18) (.75) \times 10^{-3} + \frac{(27.25)^2}{100} \times 10^{-3} + \frac{(27.25) (.25)}{500} \times 10^{-3}$$

$$= 462.4 \text{ mw}$$

NOTE: R71 holds Q9 from turning on due to I_{cbo} .

APPENDIX D

FIRST STAGE TIMER

**FIGURE D-1 FIRST STAGE TIMER**

COMPONENT LIST

R40 - 27K Ω , 1/4 W, 5%

R41 - 27K Ω , 1/4 W, 5%

R42 - 27K Ω , 1/4 W, 5%

R43 - 27K Ω , 1/4 W, 5%

C4 - 2 μ f, 100 VDC, 10%

D29 - 1N914

D9 - 1N914

Q16 - 2N3019, NPN

ASSUMPTIONS:

1. h_{fe} of Q16 ≥ 50 over temperatures of -40°C to 85°C .
2. V_{besat} , Q16 = .75 VDC = V_f of D9, D29.
3. V_{cesat} , Q16 = .2 VDC.
4. Leakage current for Q16, $I_{cbo} = 10 \mu\text{a}$ maximum.
5. E_{IN} is a 28 volt step input.

ANALYSIS AND OPERATION:

D29 keeps C4 from charging to a voltage above V_{besat} of Q16 during off mode of operation.

D9 protects the base-emitter junction of Q16 from the negative transient during turn off of C4.

Then,

$$I_{IN} = I_1 + I_2$$

$$I_2 = I_2' + I_2''$$

$$I_1 = \frac{+V - .75}{27\text{K}\Omega} = 1.0 \text{ ma}$$

$$E_{IN} = (R41 + R42)I_2 + \frac{I_2}{C4} \int_0^t E_{IN} dt + V_{C4}(0) \text{ before Q16 saturates}$$

$$V_{C4}(0) = 0 \text{ VDC}$$

Then,

$$I_2(s) = \frac{E_{IN}(s)}{(R41 + R42) + \frac{1}{s(C4)}}$$

$$E_{IN}(s) = \frac{28}{s}$$

Therefore,

$$i_2(t) = \frac{28}{(R41 + R42)(C4)} \left(e^{-\frac{t}{(R41 + R42)(C4)}} \right)$$

Q16 will turn on when,

$$(I_2')(R42) < .75 \text{ VDC}$$

Since Q16 has a $h_{fe} \geq 50$

$$I_T = h_{fe} (I_2'')$$

$$I_2'' = \frac{E_{IN} - .75}{R41} - \frac{.75}{R42} \cong 1 \text{ ma}$$

But $I_T \text{ max.} = \frac{+V - V_{cesat}}{R43}$ = also about 1 ma.

At $t = 0^+$

$$V_{R42} = E_{IN} \frac{(R42)}{(R41 + R42)} = 14.5 \text{ VDC if unloaded.}$$

Thus Q16 will saturate immediately!

Once Q16 saturates;

$$i_2(t) = \frac{28 - .75 - .75}{R41} \left(e^{-\frac{t}{(R41)(C4)}} \right)$$

And Q16 will turn off when

$$(I_2')(R42) < .75 \text{ VDC}$$

$$\text{and } I_2' = \frac{.75 \text{ VDC}}{27K\Omega} = .0278 \text{ ma}$$

Pulse time is then

$$.0278 = \frac{28 - .75}{27K\Omega} \left(e^{-\frac{t}{54 \times 10^{-3}}} \right)$$

$$t = 193 \text{ msec.}$$

- Note:
1. Trailing edge of output pulse will exhibit a longer turn off fall-time due to the (R41)(C4) time constant.
 2. D9 protects Q16 from the negative transient of C4 when commanded off.
 3. $(I_{cbo})(R42)$ is less than .75 VDC needed to turn on Q16.

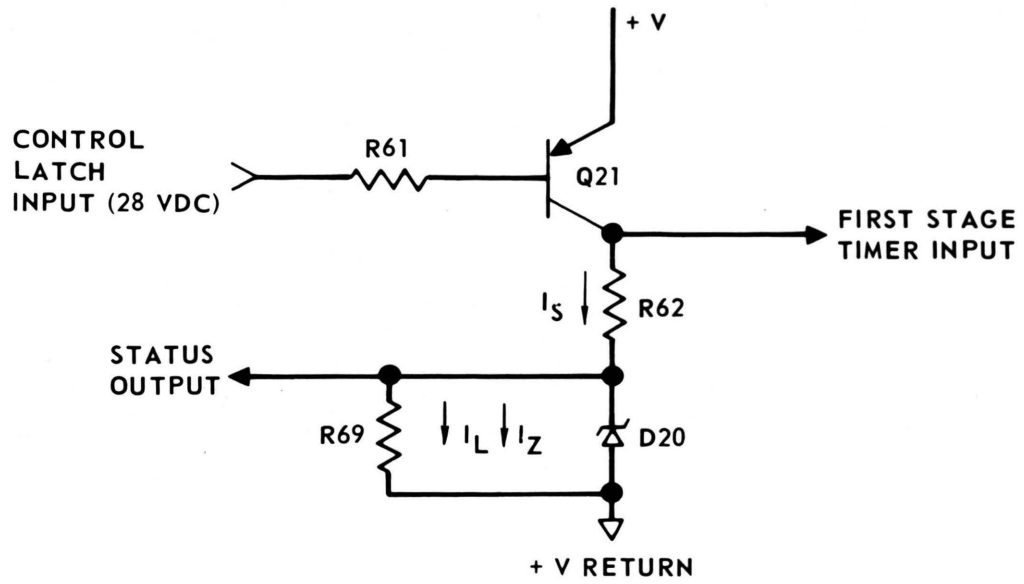
OFF POWER

Only leakage current contributes to off power drain.

ON POWER

$$\frac{E_{IN}^2}{R40} = \frac{28^2}{27 \times 10^3} = 29 \text{ mw}$$

APPENDIX E
STATUS INDICATOR

**FIGURE E-1 STATUS INDICATOR**

COMPONENT LIST

R61 - 27K Ω , 1/4 W, 5%

R62 - 27K Ω , 1/4 W, 5%

R69 - 10K Ω , 1/4 W, 5%

D20 - MZ4624, 4.7 VDC, 250 mW

Q21 - 2N4031, PNP

ASSUMPTIONS:

1. V_{besat} of Q21 = .75 VDC.
2. V_{cesat} of Q21 = .2 VDC.
3. R69 is a low impedance to TTL low level logic.
4. Q16, $h_{fe} \geq 50$.
5. +V = 28 VDC.

ANALYSIS AND OPERATION:

1. Q21 is off and its base-emitter junction is back-biased when the Control Latch is SET. Status indication is 0 VDC through a 10K Ω resistance to ground.
2. Q21 is energized when Control Latch RESETS. Q21 saturates immediately since h_{fe} is ≥ 50 .

Then,

$$V_{\text{CQ21}} = +V - V_{\text{cesat}} = 27.8 \text{ VDC}$$

$$I_{\text{s}} = \frac{V_{\text{CQ21}} - V_{\text{D20}}}{R62} = \frac{(27.8 - 4.7) \text{ VDC}}{15000 \ \Omega}$$

$$= 1.54 \text{ ma}$$

$$I_{\text{1}} = \frac{V_{\text{D20}}}{R69} = \frac{4.7 \text{ VDC}}{10000 \ \Omega} = .47 \text{ ma}$$

$$I_{\text{z}} = I_{\text{s}} - I_{\text{1}} = 1.07 \text{ ma}$$

Zener voltage, V_{D20} , is guaranteed @ 250 μa .

OFF POWER

Only an insignificant power loss due to the leakage current, I_{cbo} , is attributed to Q21. R69 will cause some power loss but is considered a loss to the "STATUS" power supply system.

ON POWER

$$\begin{aligned}
P_{\text{on}} &= \frac{(+V - V_{\text{besat}} - V_{\text{cesat}})^2}{R_{61}} + \frac{(+V - V_{\text{besat}} - V_{\text{cesat}})}{R_{61}} \times \\
&\quad (V_{\text{besat}} + V_{\text{cesat}}) + (V_{\text{cesat}})(I_s) + (I_s)^2(R_{62}) + \\
&\quad (V_{D20})(I_z) + (I_1)^2(R_{69}) \\
&= \frac{(27.05)^2}{27000} + \frac{(27.05)}{(27000)} (.95) + (.2)(1.54 \times 10^{-3}) + \\
&\quad (1.54 \times 10^{-3})^2(15000) + (4.7)(1.07 \times 10^{-3}) + \\
&\quad (.47 \times 10^{-3})^2(10000) \\
&= 70.12 \text{ mw}
\end{aligned}$$

APPENDIX F
SOFT TURN ON CIRCUIT

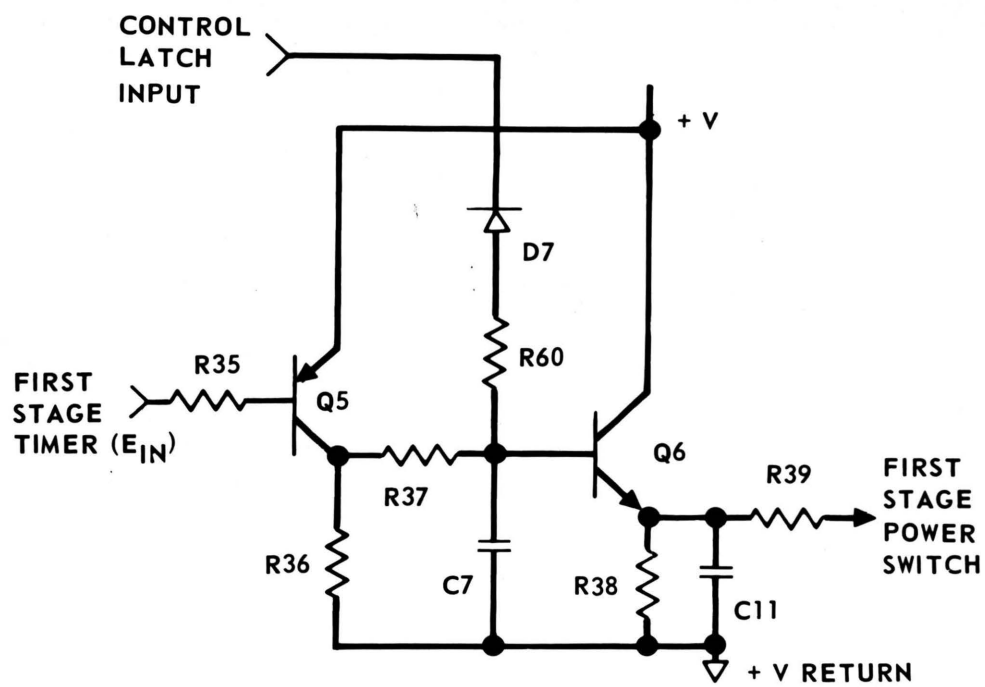


FIGURE F-1 SOFT TURN ON CIRCUIT

COMPONENT LIST

R35 - 27K Ω , 1/4 W, 5%

R36 - 10K Ω , 1/4 W, 5%

R37 - 82K Ω , 1/4 W, 5%

R38 - 5.1K Ω , 1/4 W, 5%

R39 - 2.7K Ω , 1/4 W, 5%

R60 - 200 Ω , 1/4 W, 5%

C7 - .1 μ f, 100 VDC, 10%

C11 - .01 μ f, 100 VDC, 10%

D7 - 1N914

Q5 - 2N4031, PNP

Q6 - 2N3019, NPN

ASSUMPTIONS:

1. V_{cesat} , Q5 and Q6 = .2 VDC.
2. V_{besat} , Q5 and Q6 = .75 VDC.
3. Minimum h_{fe} of Q6 = 90.
4. V_f of D7 = .75 VDC.
5. +V = 28 VDC.

ANALYSIS AND OPERATION:

1. D7 is forward biased by the RESET side of the Control Latch when off. Furthermore, D7 and R60 gives a low impedance path for C7 to discharge when Controller is commanded off. C7 will discharge at

$$V_{C7} = (+V - V_{cesat} - V_f - V_{cesatQ17}) \left(e^{-\frac{t}{(R60)(C7)}} \right)$$

The time constant is 20 μ sec.

Fast discharge of C7 is needed so that first stage power switch remains off during short circuit trip out. D7 is back biased when Controller is on.

2. C7 charge rate is:

$$V_{C7} = (+V - V_{cesat}) \left(1 - e^{-\frac{t}{(R37)(C7)}} \right)$$

if $(h_{feQ6})(10K\Omega) \gg R37$

and $900K\Omega \gg 82K\Omega$

$$\text{thus, } V_{C7} = (27.8) \left(1 - e^{-\frac{t}{8.2 \times 10^{-3}}} \right)$$

$$V_{R38} = V_{C7} - V_{besat}$$

$$V_{R38} = 27.05 \left(1 - e^{-\frac{t}{8.2 \times 10^{-3}}} \right)$$

$$V_{R38} \text{ @ 1 msec:}$$

$$V_{R38} = 3.12 \text{ VDC}$$

3. C11 shunts R38 since Q6 is a emitter follower, feedback amplifier.

OFF POWER

Only leakage current is drawn in the off mode of operation.

Power drain is insignificant.

ON POWER

Due to the dual stage power switch, turn on is a transient power drain.

Once the second stage power switch is energized, the soft turn on circuit draws insignificant power due to leakage current while C7 is allowed to discharge through R37 + R36. This discharge time constant is $(.1\mu\text{f})(92\text{K}\Omega) = 9.2 \text{ msec.}$

APPENDIX G
FIRST STAGE POWER SWITCH

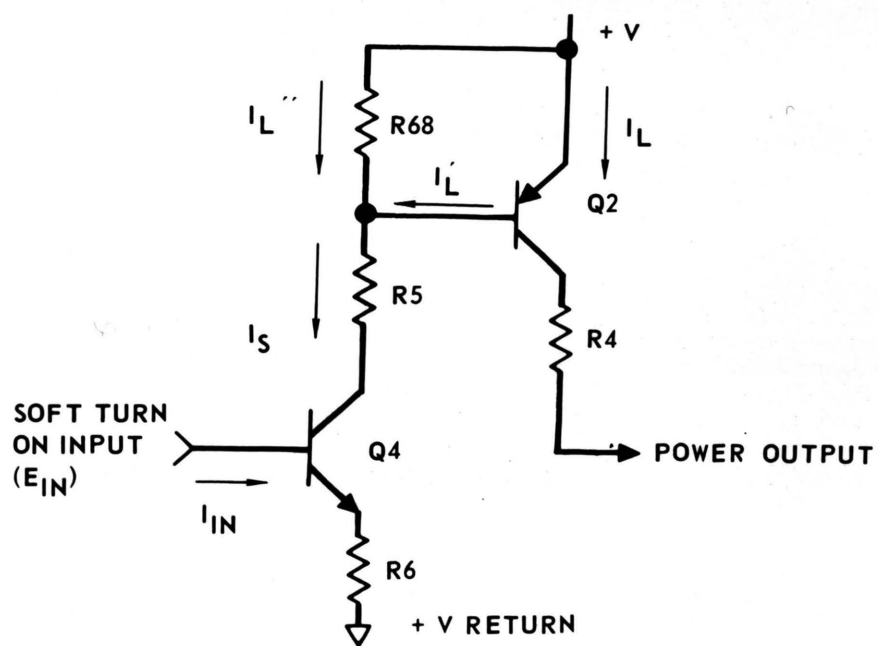


FIGURE G-1 FIRST STAGE POWER SWITCH

COMPONENT LIST

R4 - 3Ω , 1 W, 5%

R5 - 150Ω , 1/2 W, 5%

R6 - 150Ω , 1/2 W, 5%

R68 - $11K\Omega$, 1/4 W, 5%

Q4 - 2N3019, NPN

Q2 - MJ4502, PNP

ASSUMPTIONS:

1. V_{besat} , Q4 and Q2 = .75 VDC.
2. V_{cesat} , Q2 and Q4 = .2 VDC.
3. h_{fe} of Q2 \geq 25.
4. h_{fe} of Q4 \geq 90.
5. $+V = 28$ VDC.

ANALYSIS AND OPERATION:

$$I_{\text{IN}} = \frac{V_{\text{R38}}}{2.7\text{k}\Omega + (h_{\text{feQ4}} + 1)(150)}$$

$$V_{\text{R38}} = 27.05(1 - e^{-\frac{t}{8.2 \times 10^{-3}}})$$

$$V_{\text{R38}} = 3.12 \text{ VDC @ } 1 \text{ msec.}$$

$$\text{thus, } I_{\text{IN}} = \frac{3.12}{2700 + 13500} = .192 \text{ ma}$$

$$I_{\text{s max}} = (h_{\text{feQ4}})(I_{\text{IN}}) = .0173 \text{ AMPS.}$$

$$I_1' \gg I_1''$$

therefore,

$$I_{\text{s}} = I_1'$$

$$I_1' = 17.3 \text{ ma}$$

$$I_1 = (h_{\text{feQ2}})(I_1')$$

I_1 is the load current for a rated resistive load @ 25° C.

$$I_{\text{s}} = 17.3 \text{ ma}$$

If Q4 would saturate,

$$I_{\text{s max}} = \frac{+V - V_{\text{besat}}}{300\Omega} = \frac{27.25\text{V}}{300\Omega} = 91 \text{ ma}$$

$$91 \text{ ma} > 17.3 \text{ ma}$$

thus Q4 is operating in the active region, not saturated.

Rated resistive load is $\frac{(28 - .5) \text{ VDC}}{2.5 \text{ AMPS.}} = 11\Omega$

Q2 load is then

$$R4 + 11\Omega = 14\Omega$$

then,

$$I_1 = \frac{+V - V_{cesat}}{14\Omega} = 1.98 \text{ AMPS.}$$

I_1' is the base drive current to Q2, and

$$I_1 = (h_{feQ2})(I_1')$$

$$h_{feQ2} = \frac{1.98 \text{ AMPS.}}{17.3 \text{ ma}} = 115 @ 25^\circ \text{ C and } 28 \text{ VDC.}$$

From the general shape of the gain curves for the MJ4502 in Figure 17(a) this type of gain for 2 AMPS, 25° C and near saturation ($V_{ce} = 2.0 \text{ VDC}$), is feasible. However, from a system standpoint, a minimum gain for Q2 = 25 only means that turn on time is slightly longer, which is beneficial to the high inrush current loads being controlled. Lower gain in Q2 necessitates a higher voltage across R38 before Q2 saturates. Higher gain implies less voltage across R38 and shorter turn on time. In either case, the (R37)(C7) time constant in the Soft Turn On circuit can be adjusted to give the 1 millisecond turn on rise time for any h_{fe} of Q2.

As also pointed out from these curves, the higher temperature will yield a shorter turn on time while lower temperatures, a longer time. This effect is seen in the data, but the turn on variation is not drastic, less than 20%.

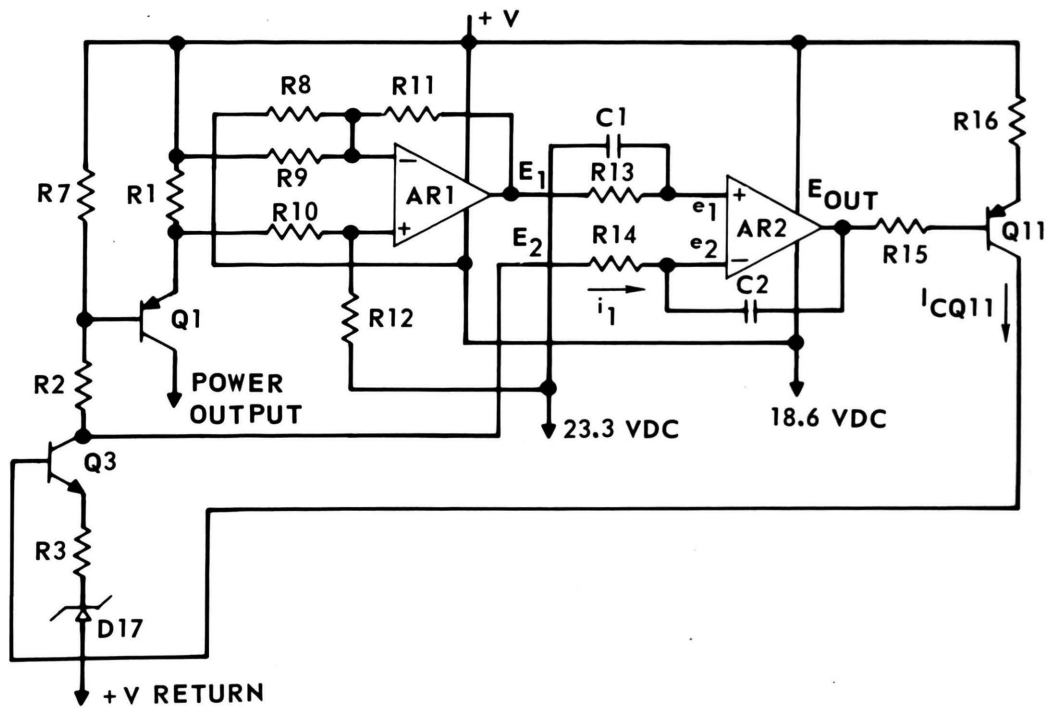
OFF POWER

The only power drain is the very small amount due to leakage current.

ON POWER

The First Stage Power Switch is a transient operation. It does not have a continuous on power drain.

APPENDIX H
CURRENT SENSOR AND SERVO BASE DRIVE
CONTROL CIRCUIT



**FIGURE H-1 CURRENT SENSOR AND SERVO
BASE DRIVE CONTROL CIRCUIT**

COMPONENT LIST

R1 - $.1\Omega$, 3 W, 1%
R2 - 6.6Ω , 1 W, 5%
R3 - 2Ω , 5 W, 1%
R8 - $208K\Omega$, 1/4 W, .1%
R9 - $50.5K\Omega$, 1/4 W, .1%
R10 - $50.5K\Omega$, 1/4 W, .1%
R11 - $184K\Omega$, 1/4 W, .1%
R12 - $97.6K\Omega$, 1/4 W, .1%
R13 - $101K\Omega$, 1/4 W, .1%
R14 - $101K\Omega$, 1/4 W, .1%
R15 - $5.1K\Omega$, 1/4 W, 5%
R16 - 51Ω , 1/4 W, 5%
C1 - $.12 \mu\text{f}$, 100 VDC, 10%
C2 - $.12 \mu\text{f}$, 100 VDC, 10%
D17 - 1N5343A, 7.5 VDC, 5W, 10%
Q1 - MJ4502, PNP
Q3 - 2N3716, NPN
Q11 - 2N4031, PNP
AR1 - S5556T, Operational Amplifier
AR2 - S5556T, Operational Amplifier

ASSUMPTIONS:

1. AR1 and AR2 operate between power supply limits of +28 to 18.6 VDC, a 9.4 volt differential.
2. These amplifiers can pull up or down to within a .6 VDC of either power supply.
3. The servo circuit controls a load current range of 2.5 AMPS. to 25 AMPS.
4. h_{fe} of Q11 = 80 @ 25°C.
5. V_{besat} = .75 VDC for Q11 and Q3.

ANALYSIS AND OPERATION:

For AR1:

$$(4.7 - .6) = -G(.25) + K \quad \text{for } I_1 = 2.5 \text{ AMPS.}$$

$$(-4.7 + .6) = -G(2.5) + K \quad \text{for } I_1 = 25 \text{ AMPS.}$$

Then,

$$2(4.1) = G(2.25)$$

$$G = 3.64$$

To obtain this range,

$$R11 = (G)R9 = (3.64)(50.5K\Omega) = 184K\Omega$$

To obtain the bias, solve for K

$$K = 5.0$$

K is positive; thus a negative voltage into the inverting input of

AR1 will give a positive K.

Therefore

$$K = 5.0 = -(R11/R8)(-4.7)$$

$$R8 = 173K\Omega$$

The value of R8 was tested and found to be too small, i.e., AR1 would not come into range from the positive power supply.

R8 was adjusted to a value of 208K Ω which alleviated this problem. This adjustment was probably due to the mismatch in the zener power supply diodes D1 and D2, to the unsymmetrical operational amplifier saturation voltage (i.e., positive saturation is greater than negative saturation), and the variation of bias current at this low supply voltage - 4.7 VDC. AR2 is constructed as a differential integrator. From figure H-1:

$$e_1 = \left[\frac{1}{\frac{(S)(C1)}{R13 + 1} + \frac{1}{S(C1)}} \right] E_1 = \frac{E_1}{T_1 S + 1}$$

$$T_1 = (R13)(C1)$$

$$E_2 - e_2 = i_1(R14)$$

$$e_2 - E_{out} = \frac{i_1}{(S)(C2)} \quad \text{if input impedance} = \infty$$

$$i_1 = \frac{E_2 - e_2}{R14} \quad \text{and} \quad i_1 = (E_2 - E_{out})(S)(C2)$$

Equating:

$$e_2 \left[\frac{1}{R14} + (S)(C2) \right] = (S)(C2)(E_{out}) + \frac{E_2}{R14}$$

But $e_1 = e_2$ if AR2 is a perfect operational amplifier

Therefore

$$\left[\frac{E_1}{T_1 S + 1} \right] \left[\frac{1}{R14} \right] + (S)(C2) = (S)(C2)(E_{out}) + \frac{E_2}{R14}$$

Let $T_2 = T_1 = T$ by letting $C1 = C2 = C$ and $R13 = R14 = R$

$$\left[\frac{E_1}{TS + 1} \right] \left[\frac{1 + TS}{R} \right] = (S) (C) (E_{out}) + \frac{E_2}{R}$$

$$\begin{aligned} E_{out} &= \frac{1}{SRC} (E_1 - E_2) \\ &= \frac{1}{RC} \int_{T_1}^{T_2} (E_1 - E_2) dt \end{aligned}$$

Operation:

As power supply diodes are energized, and no current flows through sensor R1, AR1 output is biased positive by R8. This positive output causes AR2 to slew negative since $E_2 > E_1$. This allows Q11 to feed base current into Q3. Q3 will turn on, and Q11 will supply just the right amount of base current to bring collector of Q3 to the same potential as E_1 , and thus completing the loop.

In order to allow for E_2 to track E_1 , Q11 must not saturate but rather appear like a voltage controlled variable resistor. For the nominal case, 25°C and 2.5 amperes of load current, h_{fe} of Q11 = 80, maximum collector current is:

$$I_{cQ11} \cong \frac{28 - V_{besat} - [(-V) + .6]}{R15 + (h_{fe})(R16)} \quad -V = 18.6 \text{ VDC}$$

$$= \frac{8.05 \text{ VDC}}{[5100 + (80)(51)]\Omega}$$

$\cong 70 \text{ ma}$ with Q11 saturated.

Even with a minimum gain of Q10 for Q1 (i.e., collector current of

Q3 $\cong 250 \text{ ma}$ Q3 gain must be

$$h_{feQ3} = \frac{250 \text{ ma}}{70 \text{ ma}} \cong 3.5$$

h_{feQ3} will always be greater than 3.5. Thus Q11 will never saturate at the nominal setting of 25°C and 2.5 amps load current.

Furthermore, such a small current gain is demanded from Q3, it is assumed Q3 never saturates, even up to maximum load -- seven times rated current.

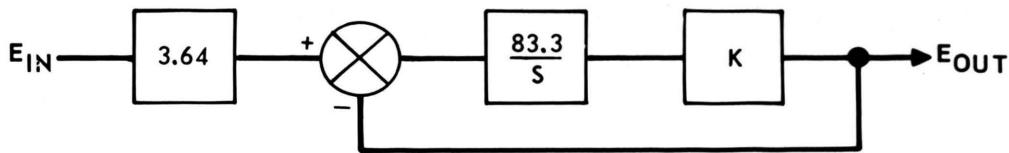


FIGURE H-2 BASE DRIVE SERVO MODEL

The frequency response of the components in the K gain stage is much greater than the integrator time constant. Thus, the K gain Block is considered a pure real number, greater than 1.

E_{IN} is a step function input.

$$\frac{E_{OUT}}{E_{IN}} = \frac{3.64(K)(83.3/S)}{1 + (1)(K)(83.3/S)} = \frac{3.64(K)(83.3)}{S + (K)(83.3)}$$

Since the only pole has a negative real root, the system is stable, independent of K.

OFF POWER

Only leakage current generates an insignificant power drain.

ON POWER

All power consumed by the operational amplifiers was accounted for in the Integrated Circuit Power Supply ON POWER.

APPENDIX I

SECOND STAGE POWER SWITCH

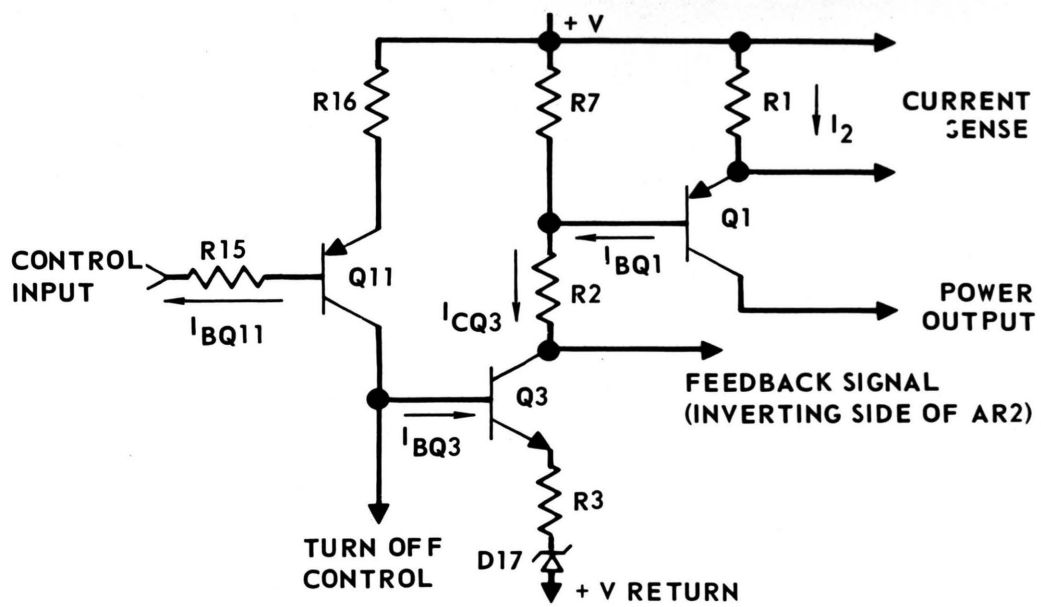


FIGURE I-1 SECOND STAGE POWER SWITCH

COMPONENT LIST

All components in this Appendix are found in the component list of Appendix H.

ASSUMPTIONS:

1. $h_{fe} Q11 = 80 @ 25^{\circ}C.$
2. $h_{fe} Q3 = 100 @ 25^{\circ}C.$
3. $V_{besat} Q3, Q11 = .75 \text{ VDC}.$
4. $V_{cesat} Q1 = .25 \text{ VDC @ } 2.5 \text{ AMPS}.$
5. $+V = 28 \text{ VDC}.$

ANALYSIS AND OPERATION:

From Appendix H,

$$V_{AR1} = (-3.64)(.25) + K @ 2.5 \text{ AMPS load current and w.r.t. } 23.2 \text{ VDC}$$

$$K = 4.15 \text{ VDC}$$

Therefore,

$$\begin{aligned} V_{AR1} &= (-3.64)(.25) + \frac{184 \times 10^3}{(208 \times 10^3)}(4.7) \\ &= 3.24 \text{ VDC} \end{aligned}$$

And

$$V_{AR1} \text{ w.r.t. } +V \text{ Return} = (3.24)(23.3) = 26.54 \text{ VDC}$$

Collector of Q3 will also be at this potential, due to the servo drive circuit. Thus the feedback voltage = 26.54 VDC @ 2.5 AMPS

Calculating h_{fe} of Q1:

$$\begin{aligned} I_{bQ1} &= \frac{+V - (I_1)(R1) - V_{besat} - V_{AR1}}{R2} \\ &= \frac{.46}{6.6} \cong 70 \text{ ma} \end{aligned}$$

$$h_{feQ1} = \frac{I_1}{I_{bQ1}} = \frac{2.5 \text{ AMPS}}{.07 \text{ AMPS}} = 35.6 @ 2.5 \text{ AMPS, load current}$$

At $I_1 = 25 \text{ AMPS}:$

$$\begin{aligned} V_{AR1} &= (-3.64)(2.5) + \frac{(184)}{(208)}(4.7) \\ &= -4.95 \text{ VDC} \end{aligned}$$

V_{AR1} w.r.t. +V Return = $23.3 - 4.95 = 18.35$ VDC. However minimum $V_{AR1} = 18.6 + .6 = 19.2$ VDC. Therefore, the use of the $208K\Omega$ resistor for R8 instead of the calculated $173K\Omega$ limits the range of AR1 to an equivalent load current of

$$-4.1 = (-3.64)(X) + 4.15$$

$$X = \frac{8.25}{3.64} \text{ where } X \text{ is maximum load current.}$$

$$X = 2.27 \text{ which corresponds to a } 22.7 \text{ AMP load current.}$$

Therefore,

$$I_{bQ1} @ 25 \text{ AMPS} = \frac{(28 - 1.7 - 2.27 - 19.2) \text{ VDC}}{6.6\Omega}$$

$$= .700 \text{ AMPS}$$

$$h_{feQ1} = \frac{22.7}{.7} = 32.4 @ 25 \text{ AMPS load current}$$

The forced gain of Q1 varies a small amount (35.6 -- 32.4) over almost a order of magnitude in load current -- 2.5 to 22.7 AMPS. Nevertheless, the power switch does not exhibit this high gain at large currents; and, it is the decrease in gain that actually saves the power switch from destruction during short circuit conditions. Calculating the base currents necessary from Q3 and Q11 @ 2.5 AMPS load current:

$$I_{bQ1} \approx I_{cQ3}$$

$$I_{cQ3} = (h_{feQ3})(I_{bQ3})$$

$$I_{bQ3} = \frac{70\text{ma}}{100} = .7\text{ma}$$

Similarly,

$$I_{bQ3} = I_{cQ11}$$

$$I_{bQ11} = \frac{I_{cQ11}}{h_{feQ11}} = \frac{.7\text{ma}}{80} = 8.75 \mu\text{a.}$$

Short Circuit Analysis

In order to protect the second stage power switch from catastrophic failure resulting from a short circuit, the power switch must be current limited to a value that gives sufficient transient time in which turn off can occur. The variation in transistor gain from transistor to transistor makes this task difficult but not impossible. From Figure 16, turn off transient is about 40 μ seconds after a short circuit was encountered. Figure 17(a) shows the variation of the switch gain curves over temperature, normalized to a minimum gain of 25 at 7.5 amperes and 25°C or a maximum gain 100 at the same point. Maximum gain must be used to calculate transient time before destruction.

With a maximum gain of 100 at 7.5 amperes and 25°C, the normalized value is 40. At 25 amperes, the normalized value is about 15 for all temperatures. Calculating h_{feQ1} at 25 amperes:

$$\frac{h_{feQ1}}{15} = \frac{100}{40}$$

$$h_{feQ1} = 37.5$$

At 30 amperes, normalized value is about 12. Similarly,

$$h_{feQ1} = \frac{1200}{40} = 30$$

As previously shown, the Servo Base Drive Circuit forces the gain of Q1 to a maximum of about 35 for load currents from 2.5 amperes to 25 amperes. With a maximum gain device, the second stage power transistor will not saturate above 25 amperes and therefore become current limited. Checking Figure 17(b) at 30 AMPS and 28 VDC, V_{ce} -- collector to emitter voltage -- is greater than 100 μ sec. Short circuit turn off time is

40 μ sec.

With a minimum gain device, current limiting will occur at a much lower collector current and thus give longer safe operating time during short conditions before turn off is necessary. R2 can be adjusted to compensate for a low gain device (i.e., in order to reach the 7 times rated current limit), but this adjustment will sacrifice efficiency.

Finally, D17 allows for fast turn off of Q3 during short circuit of extreme temperatures.

OFF POWER

Leakage current accounts for the only off power: it is considered insignificant.

ON POWER

At 2.5 amperes load current and 25°C:

$$\begin{aligned}
 P_{\text{on}} = & (I_1)^2 R1 + (V_{\text{cesatQ1}})(I_1) + (I_{\text{bQ1}})(V_{\text{besatQ1}}) + (I_{\text{cQ3}})^2 R2 \\
 & + (I_{\text{cQ3}})(V_{\text{AR1}}) + (I_{\text{bQ3}})^2 R3 + (I_{\text{bQ3}})(V_{\text{fD17}} + V_{\text{besatQ3}}) + \\
 & (I_{\text{bQ3}})(+V - V_{\text{bQ3}}) + (I_{\text{bQ11}})^2 R15 + (I_{\text{bQ11}})(V_{\text{besatQ11}}) + \\
 & \frac{(+V - V_{\text{bQ1}})^2}{R7}
 \end{aligned}$$

Substituting the assumed, calculated, and fixed values:

$$P_{\text{on}} = 3.1897 \text{ W}$$

APPENDIX J

IMMEDIATE TRIP OUT CIRCUIT

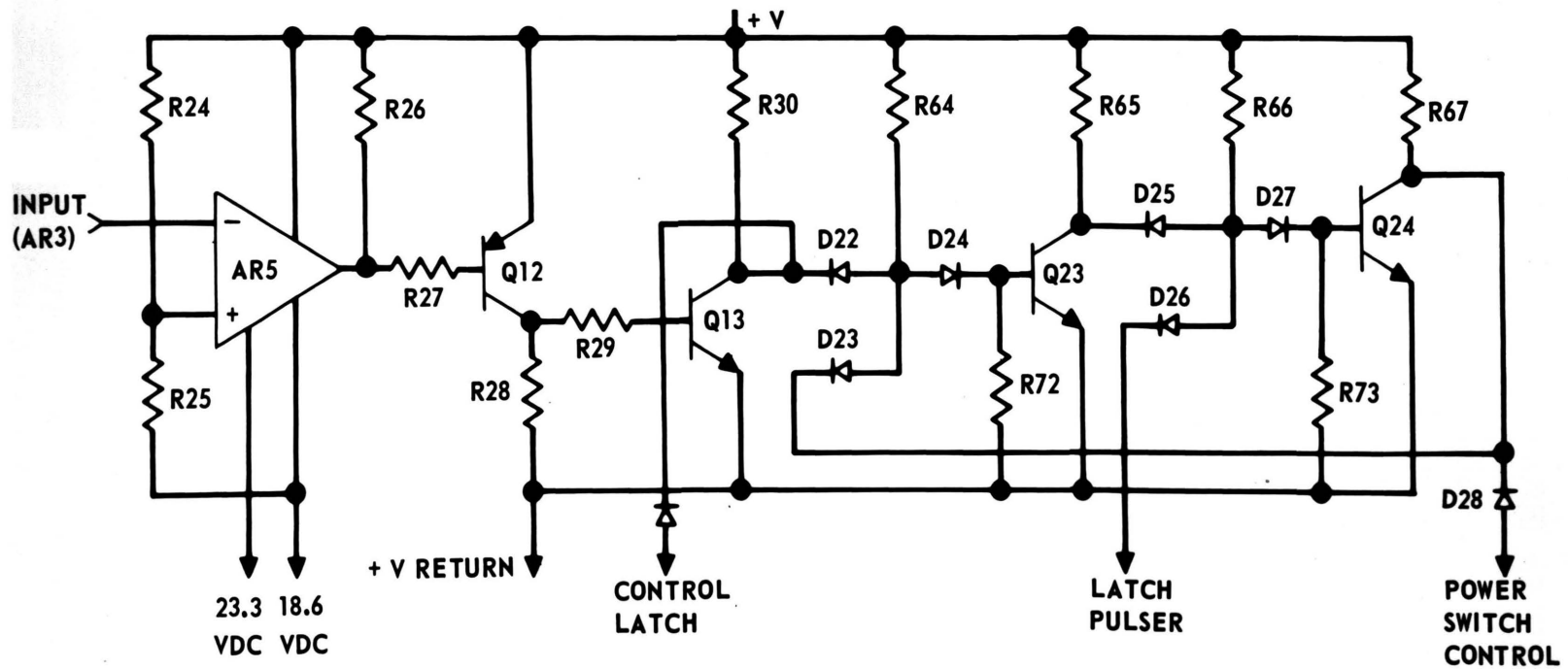


FIGURE J-1 IMMEDIATE TRIPOUT CIRCUIT

COMPONENT LIST

R24 - 27K Ω , 1/4 W, .1%
R25 - 130K Ω , 1/4 W, .1%
R26 - 12K Ω , 1/4 W, 5%
R27 - 10K Ω , 1/4 W, 5%
R28 - 15K Ω , 1/4 W, 5%
R29 - 15K Ω , 1/4 W, 5%
R30 - 15K Ω , 1/4 W, 5%
R64 - 27K Ω , 1/4 W, 5%
R65 - 27K Ω , 1/4 W, 5%
R66 - 27K Ω , 1/4 W, 5%
R67 - 27K Ω , 1/4 W, 5%
R72 - 51K Ω , 1/4 W, 5%
R73 - 51K Ω , 1/4 W, 5%
D6 - 1N914
D22-28 - 1N914
Q12 - 2N4031, PNP
Q13 - 2N3019, NPN
Q23 - 2N3019, NPN
Q24 - 2N3019, NPN
AR5 - LM111, Voltage Comparator

ASSUMPTIONS:

1. $V_{cesat} = .2$ VDC for Q12, Q13, Q23, Q24.
2. $V_{besat} = .75$ VDC for Q12, Q13, Q23, Q24.
3. $h_{fe} \geq 50$ for Q12, Q13, Q23, Q24.
4. $+V = 28$ VDC.

ANALYSIS AND OPERATION:

As the current in the sense resistor becomes excessive, the input to AR5 (from AR3) becomes more positive until the voltage V_{R25} is exceeded. AR5 switches from +28 VDC to +23.3 VDC causing Q12 and Q13 to turn on and saturate. When Q13 saturates, D22 is forward biased which eliminates the base current to Q23. This causes Q24 to latch low and Q23 to latch high, similar to the Control Latch operation. Q24 going low forward biases D28 which immediately removes all base drive from Q3 -- the transistor controlling the Second Stage Power Switch Q1. Q3 turns off immediately (due to D17) which in turn, deenergizes Q1. Q13 also resets the Control Latch. The Immediate Trip Out Circuit is reset only by the Latch Pulser Circuit.

AR5 is set to switch at:

$$V_{R25} = \left(\frac{R25}{R24 + R25} \right) +V - 18.6$$

$$= 7.9 \text{ VDC}$$

$$-V = 18.6 \text{ VDC (negative power supply)}$$

$$\text{Thus, } (18.6 + 7.9) \text{ VDC} = 26.5 \text{ VDC}$$

Retracing,

$$(26.5 - 23.3) \text{ VDC} = 3.2 \text{ VDC}$$

AR1 voltage output equation is then

$$-3.2 = -C(R1)(I_{load}) + 4.15$$

$$C = 3.64; R1 = .1\Omega$$

Then

$$I_{load} = 20.2 \text{ amperes}$$

This immediate trip point is above the 700% overload requirement but still provides for short circuit protection.

OFF POWER

The Off Power is due only to the latch circuit and is the same as the On Power for the Control Latch in Appendix B.

$$P_{off} = 84.36 \text{ mw}$$

ON POWER

$$P_{on} = P_{off} = 84.36 \text{ mw}$$

APPENDIX K
INVERSE TIME TRIP OUT CIRCUIT

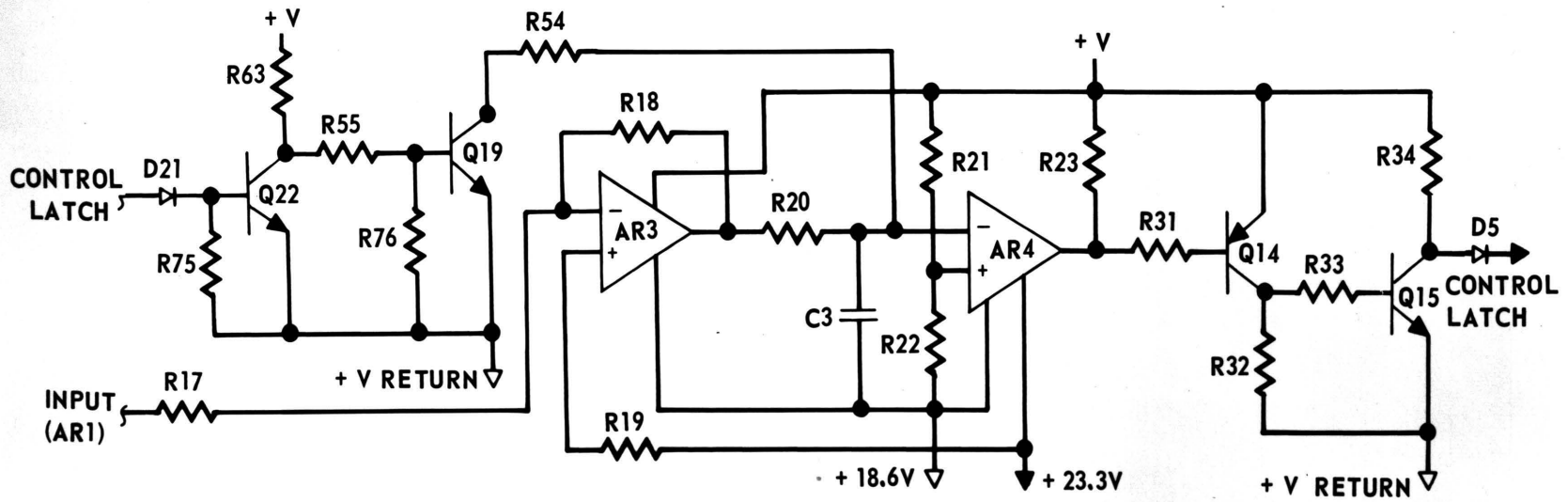


FIGURE K-1 INVERSE TIME TRIPOUT CIRCUIT

COMPONENT LIST

R17 - 101K Ω , 1/4 W, .1%
R18 - 101K Ω , 1/4 W, .1%
R19 - 50.5K Ω , 1/4 W, .1%
R20 - 11.3K Ω , 1/4 W, .1%
R21 - 50.5K Ω , 1/4 W, .1%
R22 - 11.3K Ω , 1/4 W, .1%
R23 - 12K Ω , 1/4 W, 5%
R31 - 10K Ω , 1/4 W, 5%
R32 - 15K Ω , 1/4 W, 5%
R33 - 15K Ω , 1/4 W, 5%
R34 - 15K Ω , 1/4 W, 5%
R54 - 27K Ω , 1/4 W, 5%
R55 - 15K Ω , 1/4 W, 5%
R63 - 27K Ω , 1/4 W, 5%
R75 - 51K Ω , 1/4 W, 5%
R76 - 51K Ω , 1/4 W, 5%
C3 - 47 μ f, 20 VDC, 10%
D5 - 1N914
D21 - 1N914
Q14 - 2N4031, PNP
Q15 - 2N3019, NPN
Q19 - 2N3019, NPN
Q22 - 2N3019, NPN
AR3 - S5556T, Operational Amplifier
AR4 - LM111, Voltage Comparator

ASSUMPTIONS:

1. $V_{besat} = .75$ VDC, for Q14, Q15, Q22, Q19.
2. $V_{cesat} = .2$ VDC, for Q14, Q15, Q22, Q19.
3. $h_{fe} \geq 50$ for Q14, Q15, Q22, Q19.
4. $+V = 28$ VDC.

ANALYSIS AND OPERATION:

The unity gain inverting amplifier, AR3, conditions the output voltage of AR1 to give a positive increasing voltage output with increasing load current. Capacitor C3 will charge to this positive voltage and energize the voltage comparator, AR4, if the load current exceeds 150% of rated load. AR4 then turn Q14 (and subsequently Q15) on, driving both into saturation, and presetting the Control Latch to deenergize the Second Stage Power Switch. The (R20)(C3) time constant, in conjunction with the R21, R22 voltage divider determines the shape of the inverse trip out response curve.

Once the Control Latch is SET, Q22 and Q19 turn on to provide a low impedance discharge path to C3.

From the Base Drive Servo analysis, Appendix H,

$$V_{AR1} = (-G)(R1)(I_1) + K$$

$$R1 = .1\Omega$$

$$G = 3.64$$

$$I_1 = \text{load current}$$

$$K = 4.15$$

At 150% Overload:

$$I_1 = 1.5(2.5\text{AMPS}) = 3.75 \text{ AMPS}$$

$$V_{AR1} = (-3.64)(.1)(3.75) + 4.15$$

$$V_{AR1} = 2.78$$

$$V_{AR1} \text{ w.r.t. +V return} = (23.2 + 2.78) = 26.08 \text{ VDC}$$

Then,

$$V_{AR3} \text{ w.r.t. +V return} = 23.3 - 2.78 = 20.52 \text{ VDC}$$

Therefore

$$V_{C3} = V_{AR3} (1 - e^{-\frac{t}{(R20)(C3)}}) + V_{C3}(0)$$

$$V_{C3}(0) = 0 \text{ VDC}$$

$$V_{C3} = V_{AR3} (1 - e^{-\frac{t}{(R20)(C3)}})$$

The input impedance to AR4 \approx infinity so that the equation for

V_{C3} holds.

AR4 will switch when:

$$V_{R22} = \frac{R22}{R21 + R22} (28 - 18.6) \text{ VDC is exceeded.}$$

Substituting,

$$V_{R22} = 1.72 \text{ VDC}$$

$$V_{R22} \text{ w.r.t. +V return} = (18.6 + 1.72) = 20.32 \text{ VDC}$$

Thus, trip out time for 150% overload is:

$$V_{C3} = (20.32 - 18.6) \text{ VDC} = (20.52 - 18.6) (1 - e^{-\frac{t}{.531}})$$

$$t = 1.22 \text{ sec.}$$

Considering the 130% overload:

$$V_{C3} = (20.32 - 18.6) = (2.033 - 18.6) = (20.33 - 18.6) (1 - e^{-\frac{t}{.531}})$$

$$t = 2.81 \text{ sec.}$$

Thus, the power controller trips out for the lower limit in less than the 3.0 seconds, the maximum time allowed in MIL-P-81653. However, R20 or R22 can be adjusted to change trip out time if longer or shorter time was required.

OFF POWER

$$P_{\text{off}} = \frac{(+V)^2}{R_{63} + R_{55}}$$
$$= 19 \text{ mw}$$

ON POWER

$$P_{\text{on}} = \frac{(+V)^2}{R_{63}}$$
$$= 29 \text{ mw}$$

APPENDIX L
SOFT TURN OFF CIRCUIT

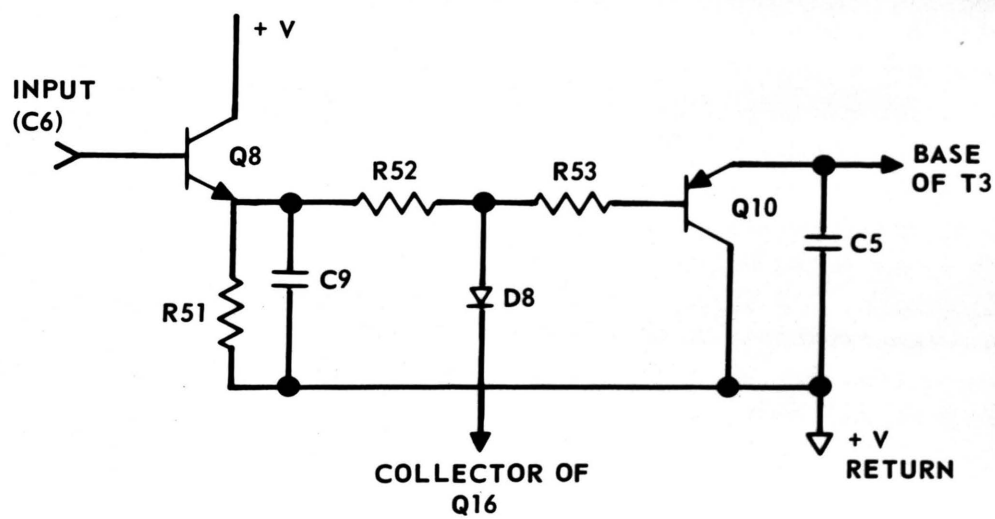


FIGURE L-1 SOFT TURN OFF CIRCUIT

COMPONENT LIST

R51 - 10K Ω , 1/4 W, 5%

R52 - 1K Ω , 1/4 W, 5%

R53 - 5.1K Ω , 1/4 W, 5%

C9 - .01 μ f, 100 VDC, 10%

C5 - .1 μ f, 100 VDC, 10%

D8 - 1N914

Q8 - 2N720A, NPN

Q10 - 2N4031, PNP

ASSUMPTIONS:

1. $V_{besat} = .75$ VDC for Q8, Q10; $V_{cesat} = .2$ VDC for Q8, Q10.
2. $h_{feQ10} \geq 80$; $h_{feQ8} \geq 20$.
3. $+V = 28$ VDC.
4. C9 shunts the emitter resistor of Q8 for stability.

ANALYSIS AND OPERATION:

1. Q16, the pulse circuit timer for the first stage power switch, goes low to forward bias D8 during first stage operation. Q10 turns on through R53 to supply a low impedance path for the base drive to Q3. Thus, Q3 is held off (and subsequently, the second stage power switch is held off) until the first stage timer back-biases D8. Then Q10 turns off immediately and all Q11 collector current (as justified on page 93) is routed through Q3. Activation of Q3 immediately saturates Q1 for second stage power switch operation. During the first stage operation V_{C9} has charged to a potential greater than V_{bQ3} , holding Q10 off until trip out or a turn off command is generated. When such a command is given, V_{C9} slowly decays - due to the (R48)(C6) time constant -- gradually pulling Q10 from cut off to saturation. The rate at which Q10 goes from off to on determines the rate of current reduction in Q3 and subsequently the speed at which Q1 goes from saturation to cut off. Q10 will sink this base current of Q3 until AR2 turns off Q11 and all base current is eliminated. Q8 is an emitter follower to essentially unload C6. However its impedance is approximately:

$$Z_{IN} = (h_{feQ8})(R51) = 200K\Omega$$

And

$$R45 = R48 = 27K\Omega$$

Thus, one has this equivalent circuit:

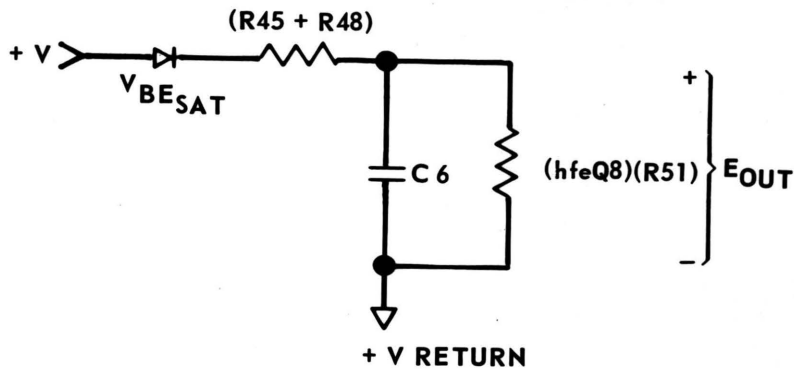


FIGURE L2 Q8 EQUIVALENT CIRCUIT

Let $R45 + R48 = R''$

$C6 = C$

$(h_{feQ8})(R51) = R'$

Then,

$$E_{OUT} = \left[\frac{\frac{(R') (1/SC)}{R' + 1/SC}}{R'' + \frac{(R') (1/SC)}{R' + 1/SC}} \right] (+V - .75)$$

$$= \left[\frac{\frac{R'}{(R'')(R')(C)}}{S + \frac{R'' + R'}{(C)(R'')(R')}} \right] (+V - .75)$$

Adding $+V(S) = \frac{28}{S}$ and simplifying:

$$E_{OUT} = \left[\frac{R'}{R' + R''} \right] \left[\frac{27.25 \left(\frac{1}{(R'')(C)} \right) \left(\frac{R'' + R'}{R'} \right)}{S \left(S + \frac{R'' + R'}{(C)(R'')(R')} \right)} \right]$$

Taking the Inverse Laplace Transform:

$$E_{OUT} = \left[\frac{R'}{R' + R''} \right] \left[(27.25) \left(1 - e^{-\frac{t}{\frac{(R'' + R')}{(C)(R'')(R')}}}} \right) \right]$$

At $t = 0$; $E_{OUT} = 0$

$$\text{At } t = \infty, E_{OUT} = \left(\frac{200K\Omega}{254K\Omega} \right) 27.25 \text{ VDC} = 21.2 \text{ VDC}$$

And,

$$\begin{aligned} \frac{R'' + R'}{(C)(R'')(R')} &= \frac{254 \times 10^3}{(2 \times 10^{-6})(200 \times 10^3)(54 \times 10^3)} \\ &= 117 \text{ msec.} \end{aligned}$$

From Appendix I, I_{bQ3} for a 2.5 ampere load current equalled about 7.0 ma.

Therefore,

$$\begin{aligned} V_{DQ3} &= V_{fD17} + V_{besat} + (7 \times 10^{-3})(100)(2) \\ &= 9.65 \text{ VDC} \end{aligned}$$

When D8 is forward biased, Q10 must sink the 7 ma originally feeding the base of Q3. Since $h_{feQ10} = 80$

$$\begin{aligned} I_{bQ10} &= \frac{I_{cQ10}}{h_{fe}} = \frac{7 \times 10^{-3}}{80} \\ &= .0875 \text{ ma, minimum} \end{aligned}$$

Thus,

$$\begin{aligned} V_{C5} &= V_{cesatQ16} + V_{fD8} + V_{besat} + (I_{bQ10})(R53) \\ &= 2.146 \text{ VDC} \end{aligned}$$

Therefore, $2.146 < 9.65$ volts needed to turn on Q3. Q3 will remain off when D8 is forward biased, and Q10 is on. After the first stage timer deenergizes, Q10 will turn off since:

$$\begin{aligned} V_{C9} &= 21.2(1 - e^{-1.3}) @ t = 155 \text{ msec. (first stage turn on time).} \\ &= 15.8 \text{ VDC} \end{aligned}$$

And $15.8 \text{ VDC} > 9.65 \text{ VDC}$ nominally needed to turn on Q3. Thus V_{beQ10} will be back biased at $t = 155 \text{ msec.}$ and D8 off. R52 allows for C9 to follow the $(R48)(C6)$ time constant (since $(R52)(C9)$ is greater than $(R48)(C6)$) even when D8 is forward biased.

Soft Turn Off Conditions

$$V_{bQ3} = 9.65 \text{ VDC @ } 2.5 \text{ AMPS load current and } 25^{\circ}\text{C}$$

Q10 is off

$$V_{C9} = 21.2 \text{ VDC}$$

D8 is back biased

$$R52 + R53 = 6.1\text{K}\Omega$$

Assume this model:

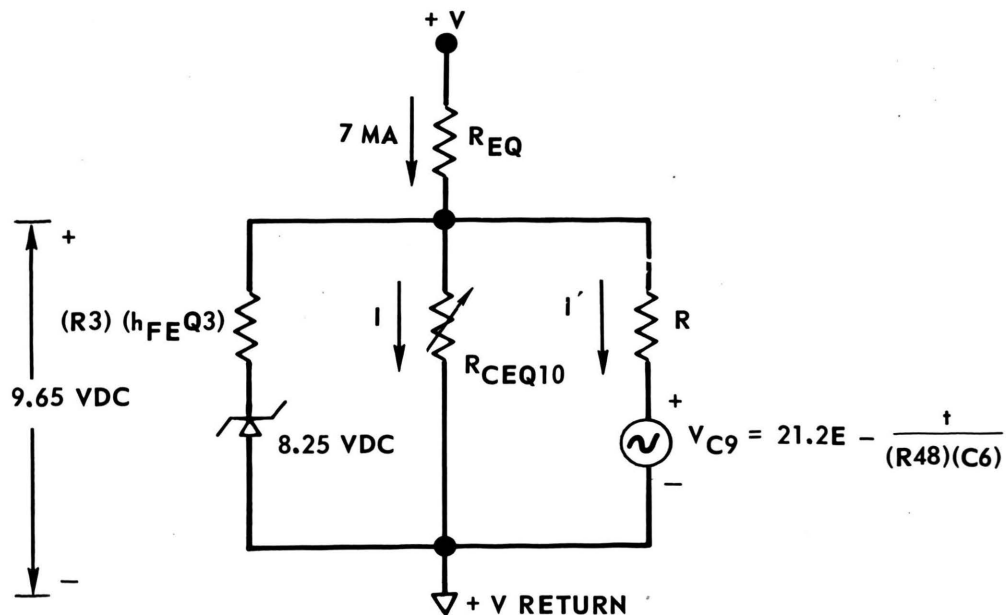


FIGURE L3 Q10 TURN OFF EQUIVALENT CIRCUIT

$$R_{EQ} = \frac{(28 - 9.65)V}{7 \text{ ma}} = 2.62K\Omega$$

$$(h_{feQ3})(R3) = (2)(100) = 200\Omega$$

$$R_{CEQ10} = 0 @ t = 0 \text{ to } V_{C9} = 9.65 \text{ VDC}$$

After a trip out command or a turn off command has been generated,

$$V_{C9} = 9.65 = 21.2 \left(e^{-\frac{t}{54 \times 10^{-3}}} \right)$$

$$t = 42.5 \text{ msec.}$$

Then I' becomes:

$$I' = \frac{9.65 - 21.2 \left(e^{-\frac{t}{54 \times 10^{-3}}} \right)}{6.1 \times 10^3}$$

Now

$$I = (h_{fe})(Q10)I'$$

$$I = \frac{80(9.65 - 21.2 e^{-\frac{t}{54 \times 10^{-3}}})}{6.1 \times 10^3}$$

If one assumes $R_{EQ} = 2.62K\Omega$ and constant, then Q3 will turn off when:

$$I = 7 \text{ ma, the normal base drive to Q3 @ 2.5 AMP load current.}$$

Solving for t in the above equation,

$$t = 44.7 \text{ msec.}$$

Q3 is calculated to turn off 2.7 msec after $V_{C9} = 9.65 \text{ VDC}$. Actual test data shows about 2.0 msec. This difference can be attributed to the tolerances of all related components and the R_{EQ} does not remain a constant during turn off. When the collector current in Q3 (and subsequently the load current in Q1) decreases, the voltage across current sensor R1 decreases causing AR2 to turn Q11 further and further off. R_{EQ} then increases from $2.62K\Omega$ to a very large impedance. This increase tends to decrease turn off time of Q1. C5 across Q10 will

tend to filter or "slow down" this effect and give a smooth fall time waveform.

OFF POWER

The only power drain is due to leakage current, and is considered insignificant.

ON POWER

$$P_{on} = \frac{(V_{C9})^2}{R51} + \frac{(+V - V_{C9})^2}{R51} + \frac{(+V - V_{C9} - V_{besat})^2}{R48 + R45 + (h_{feQ8})(R51)}$$

Substituting,

$$P_{on} = 79 \text{ mw}$$

APPENDIX M

2.5 AMPERE DC SOLID STATE POWER CONTROLLER

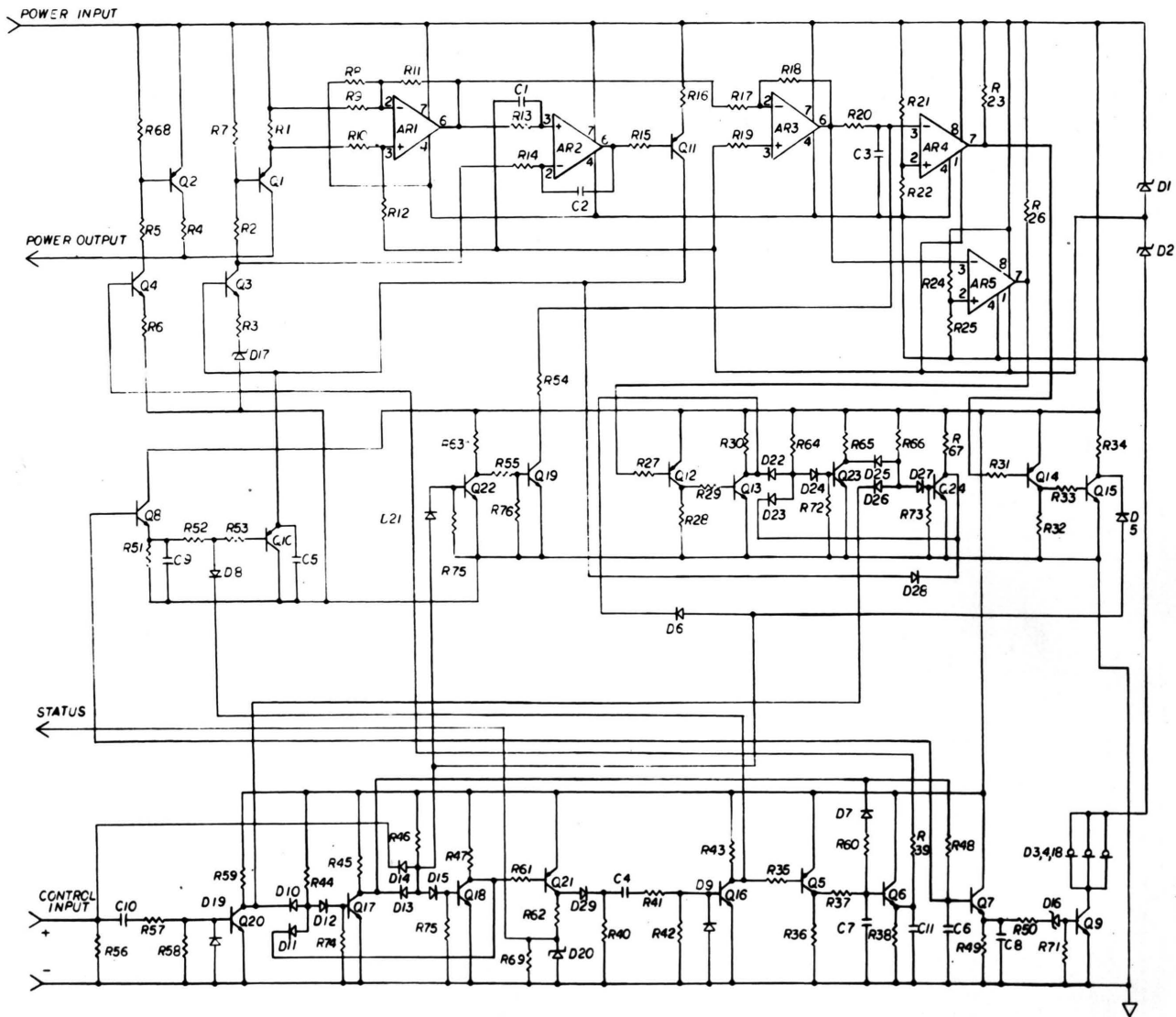


FIGURE M1 SCHEMATIC DIAGRAM OF 2.5 AMPERE DC POWER CONTROLLER

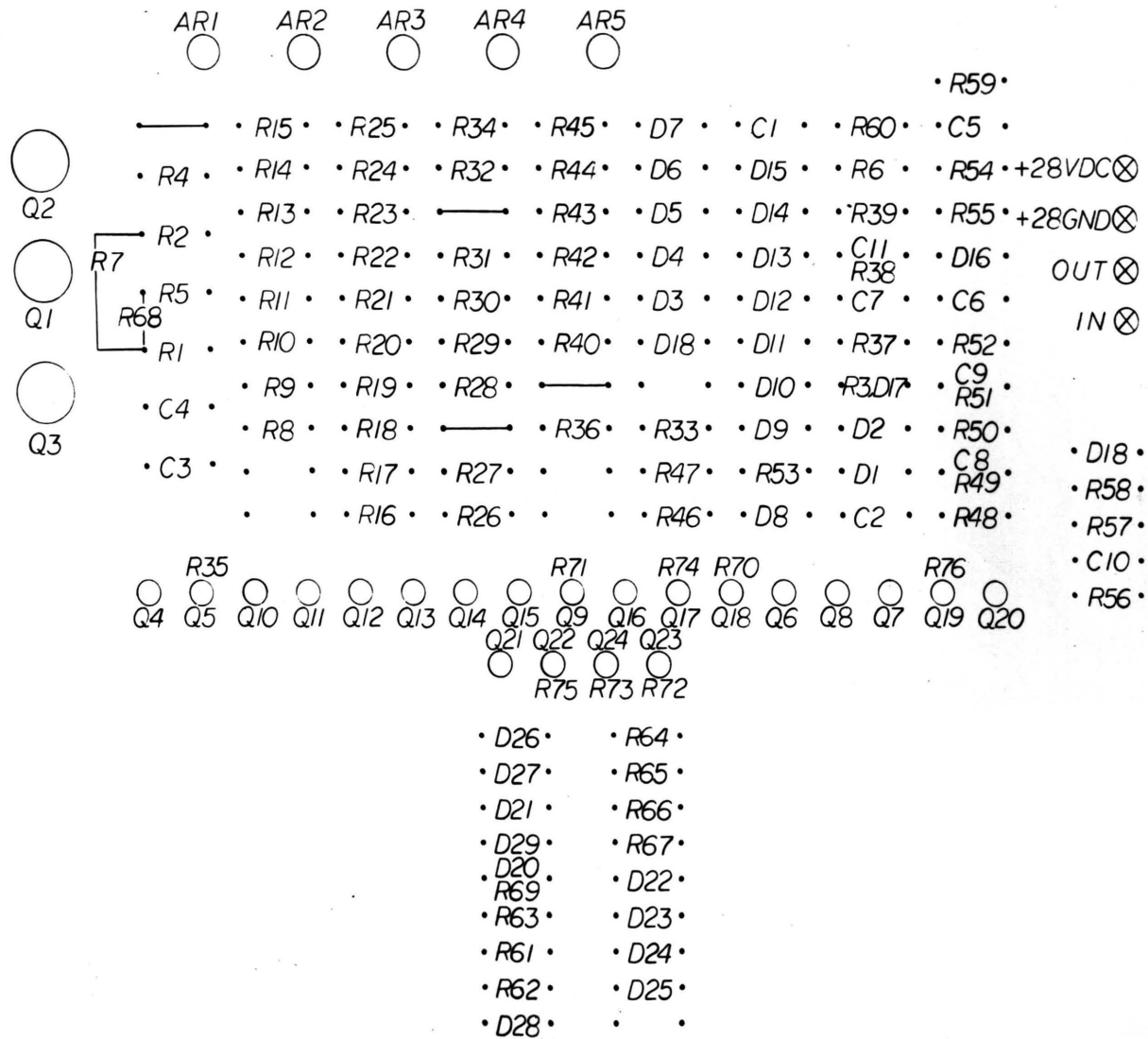


FIGURE M-2 MECHANICAL LAYOUT OF 2.5 AMPERE DC POWER CONTROLLER

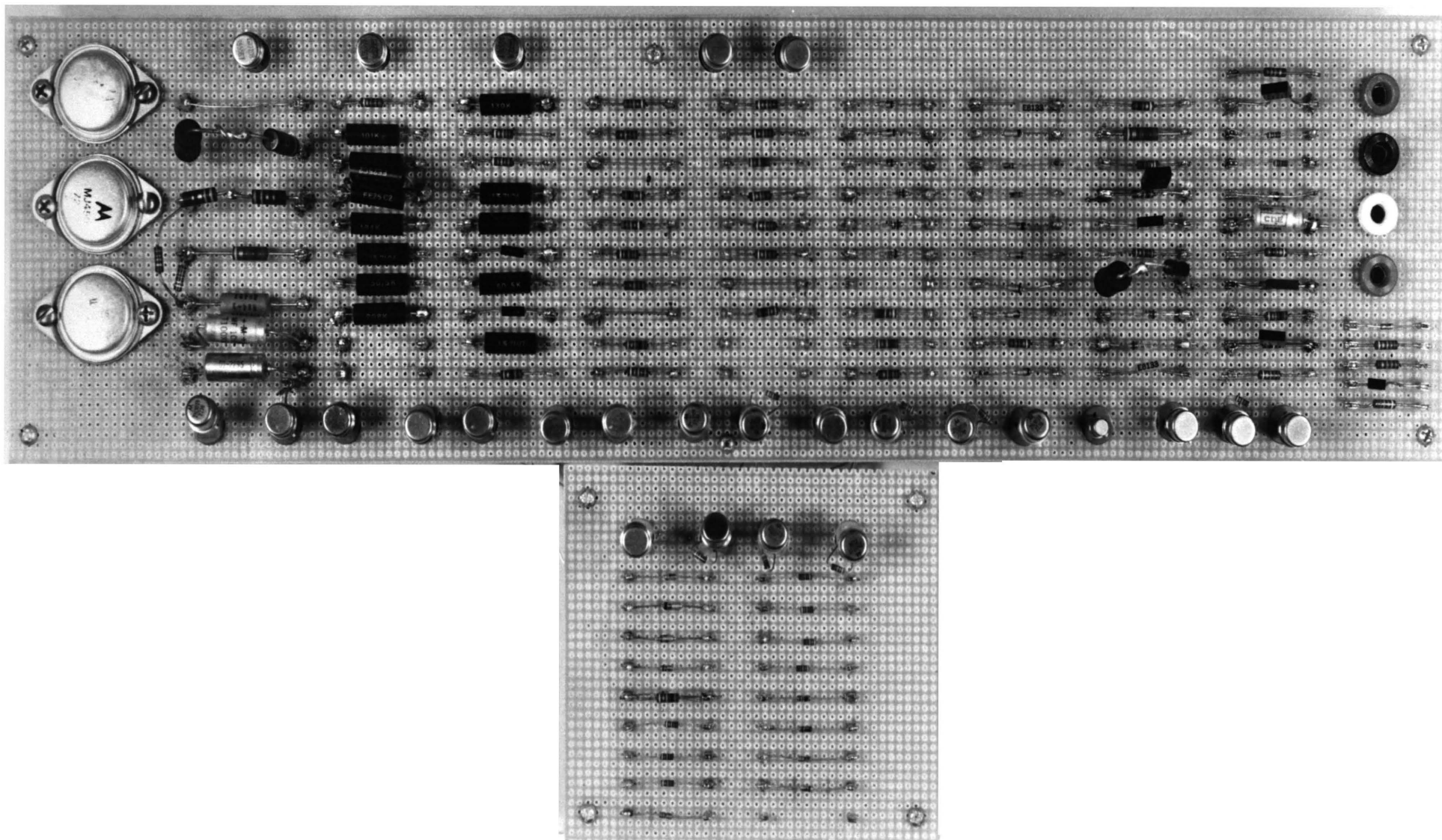


FIGURE M3 2.5 AMPERE DC POWER CONTROLLER

COMPONENT PARTS LIST

Integrated Circuits

1. AR1 -- S5556TV, Operational Amplifier
2. AR2 -- S5556TV, Operational Amplifier
3. AR3 -- S5556TV, Operational Amplifier
4. AR4 -- LM111, Analog Voltage Comparator
5. AR5 -- LM111, Analog Voltage Comparator

Transistors (Silicon)

6. Q1 -- MJ4502, PNP, 100 VDC, 30 AMP
7. Q2 -- MJ4502, PNP, 100 VDC, 30 AMP
8. Q3 -- 2N3716, NPN, 80 VDC, 10 AMP
9. Q4 -- 2N3019, NPN, 80 VDC, 1 AMP
10. Q5 -- 2N4031, PNP, 80 VDC, 1 AMP
11. Q6 -- 2N3019, NPN, 80 VDC, 1 AMP
12. Q7 -- 2N3019, NPN, 80 VDC, 1 AMP
13. Q8 -- 2N720A, NPN, 80 VDC, .15 AMP
14. Q9 -- 2N3019, NPN, 80 VDC, 1 AMP
15. Q10 -- 2N4031, PNP, 80 VDC, 1 AMP
16. Q11 -- 2N4031, PNP, 80 VDC, 1 AMP
17. Q12 -- 2N4031, PNP, 80 VDC, 1 AMP
18. Q13 -- 2N3019, NPN, 80 VDC, 1 AMP
19. Q14 -- 2N4031, PNP, 80 VDC, 1 AMP
20. Q15 -- 2N3019, NPN, 80 VDC, 1 AMP
21. Q16 -- 2N3019, NPN, 80 VDC, 1 AMP
22. Q17 -- 2N3019, NPN, 80 VDC, 1 AMP
23. Q18 -- 2N3019, NPN, 80 VDC, 1 AMP

- 24. Q19 -- 2N3019, NPN, 80 VDC, 1 AMP
- 25. Q20 -- 2N3019, NPN, 80 VDC, 1 AMP
- 26. Q21 -- 2N4031, PNP, 80 VDC, 1 AMP
- 27. Q22 -- 2N3019, NPN, 80 VDC, 1 AMP
- 28. Q23 -- 2N3019, NPN, 80 VDC, 1 AMP
- 29. Q24 -- 2N3019, NPN, 80 VDC, 1 AMP

Diodes (Signal, Zeners, Constant Current)

- 30. D1 -- MZ4624, 4.7 VDC, 250 mw
- 31. D2 -- MZ4624, 4.7 VDC, 250 mw
- 32. D3 -- 1N5314, 4.7 ma, 600 mw
- 33. D4 -- 1N5314, 4.7 ma, 600 mw
- 34. D5 -- 1N914, 100 VDC, 250 mw
- 35. D6 -- 1N914, 100 VDC, 250 mw
- 36. D7 -- 1N914, 100 VDC, 250 mw
- 37. D8 -- 1N914, 100 VDC, 250 mw
- 38. D9 -- 1N914, 100 VDC, 250 mw
- 39. D10 -- 1N914, 100 VDC, 250 mw
- 40. D11 -- 1N914, 100 VDC, 250 mw
- 41. D12 -- 1N914, 100 VDC, 250 mw
- 42. D13 -- 1N914, 100 VDC, 250 mw
- 43. D14 -- 1N914, 100 VDC, 250 mw
- 44. D15 -- 1N914, 100 VDC, 250 mw
- 45. D16 -- MZ4624, 4.7 VDC, 250 mw
- 46. D17 -- 1N5343A, 7.5 VDC, 5 w
- 47. D18 -- 1N5314, 4.7 ma, 600 mw
- 48. D19 -- 1N914, 100 VDC, 250 mw

- 49. D20 -- MZ4624, 4.7 VDC, 250 mw
- 50. D21 -- 1N914, 100 VDC, 250 mw
- 51. D22 -- 1N914, 100 VDC, 250 mw
- 52. D23 -- 1N914, 100 VDC, 250 mw
- 53. D24 -- 1N914, 100 VDC, 250 mw
- 54. D25 -- 1N914, 100 VDC, 250 mw
- 55. D26 -- 1N914, 100 VDC, 250 mw
- 56. D27 -- 1N914, 100 VDC, 250 mw
- 57. D28 -- 1N914, 100 VDC, 250 mw
- 58. D29 -- 1N914, 100 VDC, 250 mw

Capacitors

- 59. C1 -- .12 μ f, 100 VDC, 10%
- 60. C2 -- .12 μ f, 100 VDC, 10%
- 61. C3 -- 47 μ f, 20 VDC, 10%
- 62. C4 -- 2 μ f, 100 VDC, 10%
- 63. C5 -- .1 μ f, 100 VDC, 10%
- 64. C6 -- 2 μ f, 100 VDC, 10%
- 65. C7 -- .1 μ f, 100 VDC, 10%
- 66. C8 -- .01 μ f, 100 VDC, 10%
- 67. C9 -- .01 μ f, 100 VDC, 10%
- 68. C10 -- 100pf, 100 VDC, 10%
- 69. C11 -- .01 μ f, 100 VDC, 10%

Resistors (Carbon, unless otherwise stated)

- 70. R1 -- .1 Ω , 1%, 3 W (wirewound)
- 71. R2 -- 6.6 Ω , 5%, 1 W
- 72. R3 -- 2 Ω , 1%, 5 W (wirewound)

73.	R4 -- 3 Ω , 1%, 1 W	(wirewound)
74.	R5 -- 150 Ω , 5%, 1/2 W	
75.	R6 -- 150 Ω , 5%, 1/2 W	
76.	R7 -- 10K Ω , 5%, 1/4 W	
77.	R8 -- 208K Ω , .1%, 1/4 W	(metal film)
78.	R9 -- 50.5K Ω , .1%, 1/4 W	(metal film)
79.	R10 -- 50.5K Ω , .1%, 1/4 W	(metal film)
80.	R11 -- 184K Ω , .1%, 1/4 W	(metal film)
81.	R12 -- 97.6K Ω , .1%, 1/4 W	(metal film)
82.	R13 -- 101K Ω , .1%, 1/4 W	(metal film)
83.	R14 -- 101K Ω , .1%, 1/4 W	(metal film)
84.	R15 -- 5.1K Ω , 5%, 1/4 W	
85.	R16 -- 51 Ω , 5%, 1/4 W	
86.	R17 -- 101K Ω , .1%, 1/4 W	(metal film)
87.	R18 -- 101K Ω , .1%, 1/4 W	(metal film)
88.	R19 -- 50.5K Ω , .1%, 1/4 W	(metal film)
89.	R20 -- 11.3K Ω , .1%, 1/4 W	(metal film)
90.	R21 -- 50.5K Ω , .1%, 1/4 W	(metal film)
91.	R22 -- 11.3K Ω , .1%, 1/4 W	(metal film)
92.	R23 -- 12K Ω , 5%, 1/4 W	
93.	R24 -- 27K Ω , .1%, 1/4 W	(metal film)
94.	R25 -- 130K Ω , .1%, 1/4 W	(metal film)
95.	R26 -- 12K Ω , 5%, 1/4 W	
96.	R27 -- 10K Ω , 5%, 1/4 W	
97.	R28 -- 15K Ω , 5%, 1/4 W	
98.	R29 -- 15K Ω , 5%, 1/4 W	
99.	R30 -- 15K Ω , 5%, 1/4 W	

- 100. R31 -- $10\text{K}\Omega$, 5%, 1/4 W
- 101. R32 -- $15\text{K}\Omega$, 5%, 1/4 W
- 102. R33 -- $15\text{K}\Omega$, 5%, 1/4 W
- 103. R34 -- $15\text{K}\Omega$, 5%, 1/4 W
- 104. R35 -- $27\text{K}\Omega$, 5%, 1/4 W
- 105. R36 -- $10\text{K}\Omega$, 5%, 1/4 W
- 106. R37 -- $82\text{K}\Omega$, 5%, 1/4 W
- 107. R38 -- $10\text{K}\Omega$, 5%, 1/4 W
- 108. R39 -- $2.7\text{K}\Omega$, 5%, 1/2 W
- 109. R40 -- $27\text{K}\Omega$, 5%, 1/4 W
- 110. R41 -- $27\text{K}\Omega$, 5%, 1/4 W
- 111. R42 -- $27\text{K}\Omega$, 5%, 1/4 W
- 112. R43 -- $27\text{K}\Omega$, 5%, 1/4 W
- 113. R44 -- $27\text{K}\Omega$, 5%, 1/4 W
- 114. R45 -- $27\text{K}\Omega$, 5%, 1/4 W
- 115. R46 -- $27\text{K}\Omega$, 5%, 1/4 W
- 116. R47 -- $15\text{K}\Omega$, 5%, 1/4 W
- 117. R48 -- $15\text{K}\Omega$, 5%, 1/4 W
- 118. R49 -- $100\text{K}\Omega$, 5%, 1/4 W
- 119. R50 -- $10\text{K}\Omega$, 5%, 1/4 W
- 120. R51 -- $100\text{K}\Omega$, 5%, 1/4 W
- 121. R52 -- $1\text{K}\Omega$, 5%, 1/4 W
- 122. R53 -- $5.1\text{K}\Omega$, 5%, 1/4 W
- 123. R54 -- $27\text{K}\Omega$, 5%, 1/4 W
- 124. R55 -- $15\text{K}\Omega$, 5%, 1/4 W
- 125. R56 -- $27\text{K}\Omega$, 5%, 1/4 W

- 126. R57 -- $27\text{K}\Omega$, 5%, 1/4 W
- 127. R58 -- $27\text{K}\Omega$, 5%, 1/4 W
- 128. R59 -- $27\text{K}\Omega$, 5%, 1/4 W
- 129. R60 -- 200Ω , 5%, 1/4 W
- 130. R61 -- $27\text{K}\Omega$, 5%, 1/4 W
- 131. R62 -- $27\text{K}\Omega$, 5%, 1/4 W
- 132. R63 -- $27\text{K}\Omega$, 5%, 1/4 W
- 133. R64 -- $27\text{K}\Omega$, 5%, 1/4 W
- 134. R65 -- $27\text{K}\Omega$, 5%, 1/4 W
- 135. R66 -- $27\text{K}\Omega$, 5%, 1/4 W
- 136. R67 -- $27\text{K}\Omega$, 5%, 1/4 W
- 137. R68 -- $10\text{K}\Omega$, 5%, 1/4 W
- 138. R69 -- $10\text{K}\Omega$, 5%, 1/4 W
- 139. R70 -- $51\text{K}\Omega$, 5%, 1/4 W
- 140. R71 -- $51\text{K}\Omega$, 5%, 1/4 W
- 141. R72 -- $51\text{K}\Omega$, 5%, 1/4 W
- 142. R73 -- $51\text{K}\Omega$, 5%, 1/4 W
- 143. R74 -- $51\text{K}\Omega$, 5%, 1/4 W
- 144. R75 -- $51\text{K}\Omega$, 5%, 1/4 W
- 145. R76 -- $51\text{K}\Omega$, 5%, 1/4 W

OFF POWER

Calculated: 210.36 mw

Measured: 186.0 mw

ON POWER

Calculated: 3.986 W

Measured: 3.500 W

EFFICIENCY

(i.e., when operating in steady state conditions at 100% duty cycle)

$$\text{EFF.} = \frac{P_{\text{out}}}{P_{\text{in}}}$$

$$P_{\text{in}} = (I_{\text{rated}})(+V) = (2.5)(28) = 70 \text{ W}$$

$$P_{\text{out}} = P_{\text{in}} - P_{\text{loss}} = P_{\text{in}} - P_{\text{on}} = 70 - 3.986 - 66.94 \text{ W}$$

Calculated: 94.5%

Measured: 95.3%

VITA

John Anthony Gilbert was born on September 19, 1947, in St. Louis, Missouri. He received his primary and secondary education also in St. Louis. He attended St. Louis University where he graduated cum laude with a Bachelor of Science degree in Electrical Engineering on 1 June 1969.

He has been enrolled in the Graduate School of the University of Missouri--Rolla since late September, 1970. John is presently employed by the McDonnell Douglas Astronautics Company where he holds a position of Design Engineer in the Equipment and Electrical Subsystem Department. He is also a member of the Missouri Air National Guard, where he maintains a specialist rating in flight simulation.

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