# Totem-Pole Bridgeless Boost PFC Rectifier Using Series-Parallel Resonant Network 

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#### Abstract

A new series-parallel resonant bridgeless boost (SPBBR) power factor correction (PFC) rectifier is proposed in this paper. It is based on a totem-pole bridgeless boost (TPBLB) configuration which allows bi-directional current to flow during resonance to provide soft-switching for all semiconductor devices. Therefore, no additional active switch is needed. The resonant is produced by a resonant network which is placed before the output capacitor. A detailed analysis of the converter operation and control is presented. Design considerations and parameter values determination are also given. Simulation results is used to verify the theoretical analysis of the SPBBR.


Index Terms-Bridgeless Boost Rectifier (BBR); SeriesParallel Resonant; Totem-Pole; Zero Current Switching (ZCS).

## I. Introduction

The power factor correction (PFC) boost rectifier is the most popular topology amongst the rectifiers. It is a combination of a diode-bridge rectifier with a dc/dc boost rectifier. The circuit is simple and regulated output voltage and high power factor voltage can be easily achieved [1]-[3]. Figure 1 shows the typical circuit of continuous current mode (CCM) boost PFC converter with average current mode control [4]. Figure 2 shows the simulated waveforms of the circuit shown in Figure 1, where the inductor current follows the shape of the input voltage. The peak of the input current and the width of the pulse width modulation (PWM) signal are changed according to the input voltage.


Figure 1: Typical circuit of CCM boost PFC rectifier
However, the conduction losses are significantly high across the diode-bridge especially at a lower input voltage and higher output power [5]. The conduction losses caused by the diode-bridge rectifier is because two diodes need to be permanently active in the current path which causes conduction losses. Therefore, overall converter efficiency is
also decreased. The conduction losses caused by the conventional diode-bridge boost rectifier can be reduced further by reducing the number of device(s) in a current path. The number of device reduction topologies have been proposed by a number of researchers in past three decades [6]-[8]. The proposed device reduction converter is known as bridgeless converter where physically, the diode-bridge configuration is no longer exist in the converter.


Figure 2: Typical PFC boost rectifier in CCM related waveforms.
The bridgeless topology can also be configured as other dc/dc converter such as buck, cuk and buck-boost [9]-[11]. In bridgeless topologies, the number of devices in a current path is less than the number of devices in diode-bridge converter. There is no significant improvement for bridgeless topologies over the conventional diode-bridge converter in terms of the size of the passive component. However, the elimination of the diode-bridge means that the number of conducting devices in the current path is reduced. Hence, the efficiency will also increase.


Figure 3: Losses in between switching transition.

## II. BRidgeless Boost Rectifier with Soft-Switching

Bridgeless boost rectifiers (BBR) has the ability to achieve high power factor using a basic closed-loop control technique. Even though conduction losses are reduced in BBR topologies, the BBR topologies still suffer from switching losses which occur at every time the switch is on and off. The switching losses occur due to the BBR is switched by using the hard-switching technique. The hardswitching technique offers a simple control and switching circuit which means the overall cost and the complexity of the controller are reduced. However, the drawback of hardswitched BBR more dominant compared to their advantages such as higher device stress, higher switching loss and high rate of change of current and voltage over time as shown in Figure 3.
The switching losses can be reduced by applying the softswitching technique to the hard-switched BBR. The principal of the soft-switching is where the switch/device commutation occurs when its voltage or current is zero. This paper will discuss, analyse, and examine the effect of BBR when the soft-switching technique is applied.
Soft-switching technique may be divided into two categories, namely zero-current-switching, (ZCS) and zero voltage-switching, (ZVS). To achieved ZVS, the switch voltage must be forced to zero before the switch current starts flowing. A MOSFET body-diode or IGBT co-packed-diode will allow the current to flow in reverse direction through the switch. The current flow through the body-diode or co-packed-diode will clamp the voltage across the switch to a negligible voltage level such that turn-on switching losses are significantly reduced [1]. However, ZVS cannot be achieved during turn-off but the area of the switching transition can be reduced by adding a capacitor across the switch to bring down the voltage rising rate which is also called low-loss turnoff. In order to eliminate the capacitive losses during turn-on, ZVS is preferable due to MOSFETs have a larger drainsource capacitance ( $\mathrm{C}_{\mathrm{ds}}$ ) [12].
For ZCS, switch current must be zero before the gate voltage is increased by directing the current away from the switch. Negative voltage potential can also be imposed across the switch to direct the current away from the switch. However, ZCS cannot be achieved during the switch turn-on
transition due to an inductor is usually placed in series with a switch. Therefore, the ZCS can only be achieved during turnoff. The current rising rate of the switch could be reduced by the series inductance, hence, minimizing the overlapping between the current rise and voltage fall. This technique is suitable for an IGBT which known to have a tailing current problem [1].
In this paper, a ZCS BBR with high power factor is introduced. In order to achieve soft-switching operations, the proposed ZCS BBR combines a totem-pole bridgeless boost rectifier (TPBBR) topology [8] with passive L-C networks. The L-C resonant networks are placed before the output capacitor.


Figure 4: Resonant network configurations. (a) Series resonant network, (b) Parallel resonant network, and (c) Series-parallel resonant network.

The L-C resonant network is classified into three categories namely series resonant, parallel resonant and series-parallel resonant networks. The category is classified according to the connection of the resonant inductor and resonant capacitor as shown in Figure 4. Series resonant TPBBR and parallel resonant TPBBR have been proposed in [8] and [13] respectively. In this paper, TPBBR with series-parallel resonant network configurations (SPBBR) will be analysed.


Figure 5: A TPBBR topology with L-C resonant network.


Figure 6: (a) Proposed SPBBR converter topology (b) Equivalent circuit of the proposed SPBBR converter topology during steady-state.

## III. PROPOSED CONVERTER OPERATION

The concept of a BBR converter with soft-switching is by allowing the current to flow bi-directionally from high voltage point to low voltage point which occurs during the resonant. High voltage point is marked as A and low voltage point is marked as B as indicated in Figure 5. The bidirectional current flow can be realized by arranging $S_{1}$ on top of $S_{2}$ which also known as 'totem-pole' arrangement. The current flow from high voltage point to low voltage point through $S_{1}$ and $S_{2}$ when both switches are turned on and vice versa when both switches are turned off.
The proposed SPBBR converter circuit is shown in Figure 6(a) while the equivalent circuit of the converter during steady-state operation is shown in Figure 6(b). $L_{r}, C_{r 1}$ and $C_{r 2}$ network provides ZCS for $S_{1}$ and $S_{2}$ and causes both switches and diode $\mathrm{D}_{3}$ to turn-on softly. Only a slow recovery diode type is needed for $D_{1}$ and $D_{2}$. This is because the diodes are always conducted for half cycle line period. The SPBBR converter has a similar operation principle for each half cycle line period. Therefore, it is adequate to explain the circuit analysis during positive half cycle only. It will reflect the circuit analysis during the negative half cycle. The following assumptions have been made to further simplify the analysis.
i. SPBBR converter is operated in steady-state.
ii. $\quad L_{1}$ and $L_{2}$ are large. It is assumed as constant dc current source.
iii. $\mathrm{C}_{\mathrm{o}}$ is large. It is assumed as a constant dc voltage source.
iv. $\mathrm{D}_{2}$ is off during the positive half cycle.

Figure 7 illustrates the ideal key waveforms of the SPBBR converter, while Figure 8 shows the equivalent circuits of the SPBBR converter during the positive half cycle.


Figure 7: Ideal key waveforms of the proposed SPBBR converter.

## A. $\quad t_{0} \leq t \leq t_{l}$

It is assumed that $D_{1}, D_{3}$ and $D_{S 2}$ were conducting while $\mathrm{D}_{2}, \mathrm{~S}_{1}$, and $\mathrm{D}_{\mathrm{S} 1}$ were not conducting. $i_{\mathrm{Lr}}$ is increased to the level of the input current, $\mathrm{I}_{\mathrm{in}}$ while $v_{\mathrm{Cr} 1}$ and $v_{\mathrm{Cr} 2}$ are zero. At $t=t_{0}, S_{1}$ is turned on softly and body diode of $S_{2}$ is turned off at ZCS. $\mathrm{L}_{\mathrm{r}}$ is discharged from Iin through $\mathrm{D}_{3}-\mathrm{V}_{\mathrm{O}}-\mathrm{D}_{\mathrm{S} 2}-\mathrm{D}_{\mathrm{S} 1}$ to zero at $t=t_{1} . L_{r}$ causes $D_{3}$ to turn off at $Z C S$. The time interval can be described as:

$$
\begin{equation*}
t_{01}=t_{1}-t_{0}=\frac{I_{i n} L_{r}}{V_{O}} \tag{1}
\end{equation*}
$$

## B. $t_{1} \leq t \leq t_{2}$

In this interval, $\mathrm{I}_{\mathrm{in}}$ continues flowing through $\mathrm{D}_{1}$ and $\mathrm{S}_{1}$, while the other switches are off. $i_{\mathrm{Lr}}(\mathrm{t}), v_{\mathrm{Cr} 1}(\mathrm{t})$ and $v_{\mathrm{Cr} 2}(\mathrm{t})$ are zero. This interval will determine the shape of the input current waveform as described in Equation (2)

$$
\begin{equation*}
t_{12}=t_{2}-t_{1}=D T_{S}-t_{01} \tag{2}
\end{equation*}
$$

where $\mathrm{T}_{\mathrm{s}}$ is the switching period and D is the duty cycle.

## C. $t_{2} \leq t \leq t_{3}$

The resonance begins when $S_{2}$ is turned on. Iin continues flowing through $\mathrm{D}_{1}$ and $\mathrm{S}_{1}$, while $i_{\mathrm{Lr}}$ increases negatively through $S_{1}-S_{2}-C_{r 1}$ and reaches its peak. The peak voltage is determined by $\mathrm{V}_{\mathrm{o}}=\mathrm{Z}_{\mathrm{r}}$. At $t=t 3$, the peak voltage decreases to zero. $v_{\mathrm{Cr} 1}$, charges to its peak at $t=t_{3}$ while $v_{\mathrm{Cr} 2}$ discharges to $V_{0}$ through $L_{1}-S_{1}-S_{2}$. $V_{0}$ causes $D_{3}$ reverse-biased and opened. The time interval is determined as

$$
\begin{equation*}
t_{23}=t_{3}-t_{2}=\frac{\pi}{\omega_{r}} \tag{3}
\end{equation*}
$$

where

$$
\begin{gather*}
\omega_{r}=\frac{1}{\sqrt{L_{r}\left(C_{r 1}+C_{r 2}\right.}}  \tag{4}\\
Z_{r}=\sqrt{\frac{L_{r}}{C_{r 1}+C_{r 2}}} \tag{5}
\end{gather*}
$$

D. $t_{3} \leq t \leq t_{4}$

The resonance continues in this interval. The resonant continues to resonate for another half period through $\mathrm{L}_{\mathrm{r}}-\mathrm{C}_{\mathrm{r} 1}-$ $\mathrm{V}_{\mathrm{o}}-\mathrm{D}_{\mathrm{S} 2}-\mathrm{D}_{\mathrm{S} 1}$ until $t=t_{4}$. At this instant, $i_{\mathrm{Lr}}=\mathrm{I}_{\mathrm{in}}$, while $\mathrm{V}_{\mathrm{Cr} 1}$ is decreasing and $v_{\mathrm{Cr} 2}$ is increasing. The current that flows through $\mathrm{S}_{1}$ decreases sinusoidally until zero. The time interval can be described as

$$
\begin{equation*}
t_{34}=t_{4}-t_{3}=\frac{\sin ^{-1} \frac{I_{i n} Z_{r}}{V_{O}}}{\omega_{r}} \tag{6}
\end{equation*}
$$

## E. $t_{4} \leq t \leq t_{5}$

During this interval, $\mathrm{S}_{1}$ is turned off. The resonance continues resonating from the previous interval via $\mathrm{L}_{r}-\mathrm{C}_{\mathrm{r} 1}-$ $\mathrm{V}_{\mathrm{o}}-\mathrm{D}_{\mathrm{S} 2}-\mathrm{D}_{\mathrm{S} 1}$ while $\mathrm{I}_{\mathrm{in}}$ flows through $\mathrm{D}_{1}-\mathrm{L}_{\mathrm{r}}-\mathrm{C}_{\mathrm{r} 1}-\mathrm{V}_{\mathrm{o}}-\mathrm{D}_{\mathrm{S} 2}$ and back to the source. $\mathrm{C}_{\mathrm{r} 2}$ continues to discharge while resonating from the previous state. To achieve ZCS, the peak value for period $t_{45}$ must satisfy the condition in Equation (7):

$$
\begin{equation*}
\frac{V_{O}}{Z_{r}} \geq I_{i n} \tag{7}
\end{equation*}
$$

If the condition in Equation (7) is exceeded, more than double amount of the input current will flow through $\mathrm{S}_{1}$ during resonance. Hence, this will double the rating and cost of the component. To achieve ZCS with lower peak current through $S_{1}$, the ratio of $V_{0}=Z_{r}$ is required to be close as possible to $\mathrm{I}_{\mathrm{in}}$. Values of $\mathrm{C}_{\mathrm{r} 1}, \mathrm{C}_{\mathrm{r} 2}$ and $\mathrm{L}_{\mathrm{r}}$ can be obtained according to Equation (7) as long as $\mathrm{V}_{\mathrm{o}}$ is regulated. When the $\mathrm{I}_{\mathrm{S} 1}$ turns off with ZCS, this interval reached its end. The time interval is:

$$
\begin{equation*}
t_{45}=t_{5}-t_{4}=\frac{\pi-2 \sin ^{-1} \frac{I_{i n} Z_{r}}{V_{O}}}{\omega_{r}} \tag{8}
\end{equation*}
$$

F. $t_{5} \leq t \leq t_{6}$

Resonance process is stopped at $t=t_{5}$ when $i_{\mathrm{Lr}}=\mathrm{I}_{\mathrm{in}} . \mathrm{I}_{\mathrm{in}}$ flows through $\mathrm{D}_{1}-\mathrm{L}_{\mathrm{r}}-\mathrm{C}_{\mathrm{r} 1}-\mathrm{V}_{\mathrm{o}}-\mathrm{D}_{\mathrm{S} 2}$ and $\mathrm{D}_{1}-\mathrm{L}_{\mathrm{r}}-\mathrm{C}_{\mathrm{r} 2}-\mathrm{D}_{\mathrm{S} 2}$. All switches are off. Therefore, $\mathrm{v}_{\mathrm{Cr} 1}$ decreases linearly to zero and $\mathrm{v}_{\mathrm{Cr} 2}$ increases linearly to $\mathrm{V}_{\mathrm{o}}$ at $t=t_{6}$. During this time interval

$$
\begin{equation*}
t_{56}=t_{6}-t_{5}=\frac{2 V_{O}\left(C_{r 1}+C_{r 2}\right)}{I_{i n}} \cos \left[\pi-\sin ^{-1}\left(\frac{I_{i n} Z_{r}}{V_{O}}\right)\right] \tag{9}
\end{equation*}
$$

## G. $t_{6} \leq t \leq t_{0}$

At this interval, $v_{\mathrm{Cr} 1}$ is zero and $v_{\mathrm{C} 2}$ is fully charged to $\mathrm{V}_{\mathrm{o}}$. $\mathrm{D}_{3}$ starts to conduct. $\mathrm{I}_{\mathrm{in}}$ flows through $\mathrm{D}_{1}-\mathrm{L}_{r}-\mathrm{D}_{3}-\mathrm{V}_{\mathrm{o}}-\mathrm{D}_{\mathrm{S} 2}$. The same process repeated after it reaches $t=t_{0}$. process

$$
\begin{align*}
& t_{60}=t_{0}-t_{6}=T_{S}-D T_{S}-\left[\frac{2 \pi-\sin ^{-1}\left(\frac{I_{i n} Z_{r}}{V_{O}}\right)}{\omega_{r}}\right]+  \tag{10}\\
& \left.\frac{2 V_{O}\left(C_{r 1}+C_{r 2}\right)}{I_{i n}} \cos \left[-\sin ^{-1}\left(\frac{I_{i n} Z_{r}}{V_{O}}\right)\right]\right]
\end{align*}
$$

The functionality of the switches in SPBBR converter is fully utilized by exchanging the role of the switch at every half cycle. The resonant conduction time is determined by

$$
\begin{equation*}
T_{\text {res }}=t_{5}-t_{2}=\frac{2 \pi-\sin ^{-1}\left(\frac{I_{i n} Z_{r}}{V_{O}}\right)}{\omega_{r}} \tag{11}
\end{equation*}
$$

where $\mathrm{T}_{\text {res }}$ is resonance period between $\mathrm{t}_{25}$. The minimum value of $\mathrm{T}_{\text {res }}$ is $T_{\text {res }}=2$ and the maximum value of $\mathrm{T}_{\text {res }}$ is when $I_{\text {in }}$ is zero. It is suggested that set $T_{\text {res }}$ at $0.75 T_{\text {res }}$ when $I_{i n}=0$.

## IV. SPBBR PARAMETERS DETERMINATION

The specifications of SPBBR is shown in Table I. Based on the specifications, the parameters for the SPBBR can be determined.

Table 1
Proposed SPBBR Converter Specifications

| Parameters | Values |
| :--- | :--- |
| Output power, $\mathrm{P}_{\text {out }}$ | 400 W |
| Input Voltage, $v_{\text {in }}$ | $90-240 \mathrm{~V}_{\mathrm{rms}}$ |
| Input Current, $i_{\text {in }}$ | 4.44 A |
| Output voltage, $\mathrm{V}_{\text {out }}$ | $400 \mathrm{~V}_{\mathrm{dc}}$ |
| Input frequency, $\mathrm{f}_{\mathrm{in}}$ | 50 Hz |
| Switching frequency, $\mathrm{f}_{\mathrm{s}}$ | 45 kHz |


(a)

(c)

(e)

(b)

(d)

(f)


Figure 8: Equivalent circuit of the proposed TPBLB converter during positive half cycle (a) Interval 1 (b) Interval 2 (c) Interval 3 (d) Interval 4 (e) Interval 5 (f) Interval 6 (g) Interval 7.

## A. Determination of $L_{r}$ and $C_{r}$

In practice, resonance frequency, fr , is set to be higher than switching frequency by ten folds or higher [14]. Therefore, the characteristics of the boost converter output operated in CCM will not be affected. The condition as in Equation (7) will ensure that the ZCS and soft turn-on could be achieved. The limit of Lr needs to be set according to the (12).

$$
\begin{equation*}
L_{r} \leq \frac{I_{i n}}{2 \pi f_{r} V_{O}}=73.5 \times 10^{-6} \tag{12}
\end{equation*}
$$

By manipulating Equation (4) and satisfying Equation (7), $\mathrm{C}_{\mathrm{r} 1}$ and $\mathrm{C}_{\mathrm{r} 2}$ can be obtained.

$$
\begin{gather*}
\frac{1}{\sqrt{L_{r}\left(C_{r 1}+C_{r 2}\right)}}=\omega_{r}=2 \pi f_{r}=2 \pi 10 f_{s}=1.44 \times 10^{6}  \tag{13}\\
\sqrt{\frac{L_{r}}{\left(C_{r 1}+C_{r 2}\right)}} \leq \frac{V_{O}}{I_{i n}}=106.06 \tag{14}
\end{gather*}
$$

$\mathrm{L}_{\mathrm{r}}$ should be less than or equal to 73.5 H . Therefore, $\mathrm{Lr}=42 \mathrm{H}$ is chosen. The obtained $L_{r}$ is substituted into Equation (13) to obtain a total resonant capacitance $\left(\mathrm{C}_{\mathrm{r} 1}+\mathrm{C}_{\mathrm{r} 2}\right)$ equal to 12 nF . Therefore, $\mathrm{C}_{\mathrm{r} 1}=\mathrm{C}_{\mathrm{r} 2}=6 \mathrm{nF}$. Two 6.8 nF resonant capacitors are selected to produce a total resonant capacitance of 13.6 nF . $\mathrm{T}_{\text {res }}$ could be obtained by substituting $\mathrm{Z}_{\mathrm{r}}$ into Equation (11). The $L_{r}$ and $C_{r}$ rating are as follows:

$$
\begin{align*}
v_{C_{r}} & \geq 2 V_{O}  \tag{15}\\
i_{L_{r}} & \geq \frac{2 V_{O}}{Z} \tag{16}
\end{align*}
$$

Table 2
Proposed SPBBR Converter Parameters

| Parameters | Values/Model |
| :--- | :--- |
| Boost inductors, $\mathrm{L}_{1}$ and $\mathrm{L}_{2}$ | 1 mH |
| Resonant inductor, $\mathrm{L}_{\mathrm{r}}$ | 42 uH |
| Resonant capacitors, $\mathrm{C}_{\mathrm{r} 1}$ and $\mathrm{C}_{\mathrm{r} 2}$ | 6.8 nF |
| Output capacitors, $\mathrm{C}_{\mathrm{O}}$ | 680 uF |
| Output resistor, $\mathrm{R}_{\mathrm{O}}$ | $400-1.6 \mathrm{k} \Omega$ |

## V. Simulation results

PSIM® ${ }^{\circledR}$ is used to simulate the workability of the proposed SPBBR converter. Table 2 shows the parameters of the SPBBR. The gate signals for S1 and S2 are shown in Figure


Figure 9. The SPBBR simulation results at $240 \mathrm{Vin}_{\text {rms }}$ (a) Gate signal for S1. (b) Gate signal for S2. (c) $i_{\mathrm{Lr}}$. (d) Current through S1. (e) Voltage across S1. (f) Current through S2. (g) Voltage across S2. (h) Current through diode D3. (i) Voltage across resonant capacitor $\mathrm{C}_{\mathrm{r} 1} /$ diode D3 and (j) Voltage across resonant capacitor $\mathrm{C}_{\mathrm{r} 2}$.

9(a) and 9(b) respectively. The resonant network voltage and current waveforms are shown in Figure 9(c), 9(i) and 9(j) respectively, are similar as analysed in the SPBBR converter operations and confirmed that the analyses are valid. The soft switching for S1 and S2 are shown in Figure 9(d) until Figure 9(g). D3 is turned off at ZCS as shown in Figure 9(h) and 9(i). The input supply voltage, input supply current and it respective Fast Fourier Transform (FFT) are shown in Figure 10. It shows that the ability of SPBBR to achieve high power factor. The power factor and the FFT are improved when the power is increasing.

## VI. Conclusion

A new SPBBR converter topology has been presented. A detailed analysis of the converter operation under seriesparallel resonant network configuration has been described. The SPBBR has been analysed and the performance of the converter has been validated by using simulation. The performance of the converter has been evaluated by assessing the power factor and the total harmonic distortion of the input parameters. The SPBBR is able to work within different load condition. With the addition of the resonant networks, the input voltage and current are not affected. The THD of the SPBBR is within the acceptable limit.


Figure 10. Simulation results of input supply voltage, input supply current, and corresponding FFT for SPBBR at different loads

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