1965

The design and construction of a medium power, synchronous, electronic switch

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Department:

THE DESIGN AND CONSTRUCTION OF A MEDIUM POWER, SYNCHRONOUS, ELECTRONIC SWITCH

by

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A

THESIS

submitted to the faculty of the

UNIVERSITY OF MISSOURI AT ROLLA

in partial fulfillment of the requirements for the

Degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

Rolla, Missouri

1965

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ABSTRACT

This paper presents the design and construction of a medium power, synchronous, electronic switch and associated timing and control circuits.

The unit described is capable of controlling a 20 ampere resistive or inductive load from a 110/220 volt, 60 Hz excitation source. Thyristors are used as the active switching elements. The period of the on/off switching cycle may be varied from 1/60 second to 8 1/2 seconds. Turn-on and turn-off may occur at independently selected phase angles relative to the reference frequency source.

Higher power operation could be obtained easily with minor design changes.

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I. INTRODUCTION

A versatile, medium power switch was required in conduction studies of the magnetic behavior of ferromagnetic core materials. The requirements of the switch were stringent with regard to timing accuracy and current interruption capability.

It was necessary that the switch unit be capable of satisfying the following requirements:

A. It must be capable of controlling a 4.4 kVA resistive or inductive load, excited from a 220 volt, 60 Hz line.

B. It must be capable of effecting turn-on at any predetermined instant in time, regardless of load or source conditions.

C. It must be capable of continuous operation at load currents of up to 20 amperes.

D. It must be capable of effecting turn-off at any predetermined instant of time as long as the instantaneous load current at that time is not in excess of 25 amperes.

E. Turn-off must occur in as short a time period as possible. This entails high transient voltages in the case of inductive loads.

The timer, which controls the switch, must meet the following four specifications:

A. The timer shall cause turn-on to occur at any predetermined phase angle relative to the reference voltage.

B. The time duration of the "on" state shall be variable throughout the range of 5 milliseconds to 4 1/4 seconds.

C. The timer shall cause turn-off to occur at any predetermined phase angle relative to the reference voltage.

D. The time duration of the "off" state shall be variable throughout the range of 5 milliseconds to 4 1/4 seconds.

These four requirements are interdependent, with the result that the "on-off" cycle time must be an integral number of reference voltage cycles. With a 60 Hz reference voltage the timing cycle may have a period ranging from a minimum of 1/60 second, to a maximum of 8 1/2 seconds.

No commercial switching unit could be found capable of meeting the above requirements. The most common inadequacies of the existing units were their inability to extend the basic on-off cycle time to more than one reference voltage cycle, and/or their inability to withstand high transient voltages on turn-off. These inadequacies stem from the fact that commercial switches in the desired power range are designed for motor speed control and similar applications, where only the average power to the load is of significance. It also appeared that none of the commercially available devices could be modified to meet the necessary specifications at reasonable cost. This paper describes the design and development of a solid state switch and timer system to meet the need.

The switch design was divided into three areas; the timer, the basic switch, and the interface unit. A block diagram of the entire system is given in Fig. 1. The reference voltage and the ac power source may be independent; also, each voltage source may or may not have an earth ground at some point in the distribution system.

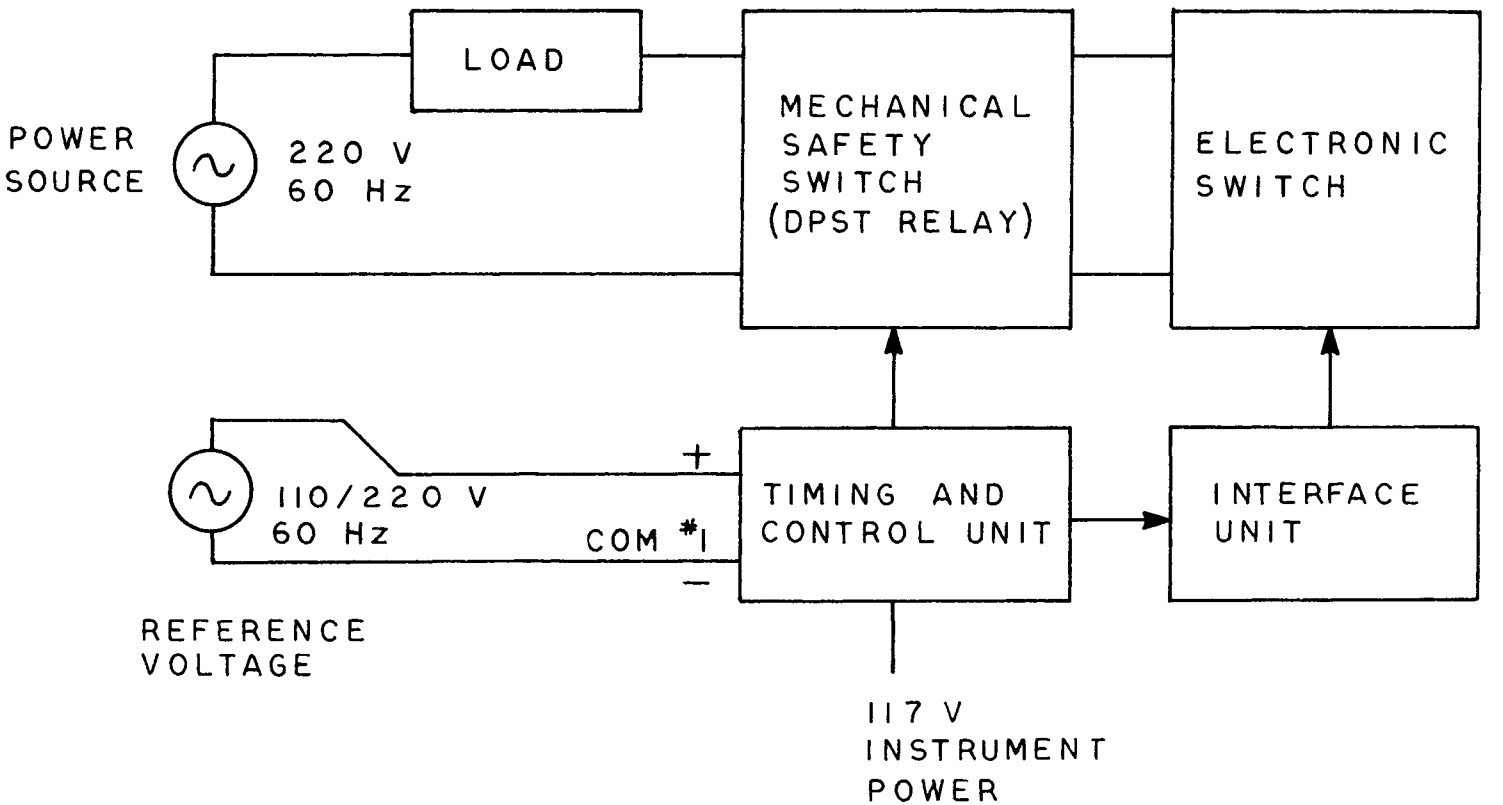

FIG 1 BLOCK DIAGRAM OF EXPERIMENTAL SYSTEM

II. THE TIMING UNIT

The basic timing circuit, presented in Fig. 2[1], consists of a flip-flop and two time delay elements. The circuit functions as a pulse train generator where the

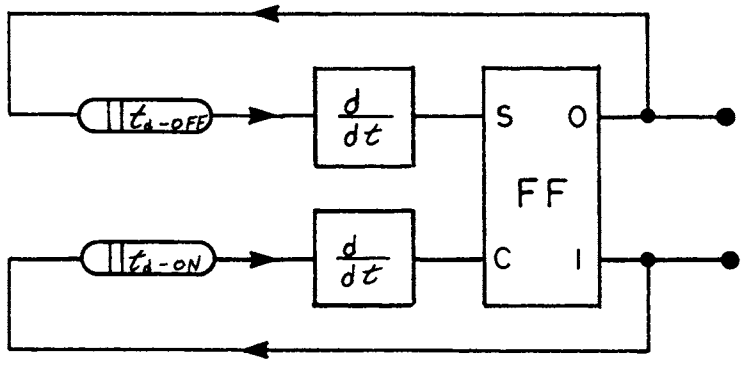

Fig. 2 Basic Timing Circuit

duration of the "on" pulse is determined by the $t_{d\text{-}ON}$ time delay element, and the time interval between pulses is determined by the $t_{d\text{-}OFF}$ time delay element. In order to meet timer specifications A and C, listed on page 1, the time delay elements must have some means of synchronizing with the desired phase angle of the reference voltage.

Two basic approaches to the design of the time delay elements were considered. The first method, often encountered in resistance welding units, is an analog method where the decaying charge on a timing capacitor determines the number of line cycles to be delayed, and a phase shifting network adjusts the output to the desired phase relationship with the reference voltage. Although this method is very simple, it was not used because of difficulties in maintaining the rigid timing specifications for delay periods of many cycles.

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[1]All symbols to be interpreted in accordance with Military Standard 806B.

The approach adopted, as presented in Fig. 3, is a digital technique, in which a cycle counter, and a "number recognition gate" control the delay period. This approach achieves a timing accuracy that is independent of the delay time, which may be any number of cycles. In addition, it uses on-off circuits, requiring less precision in establishing voltage levels in various parts of the circuits.

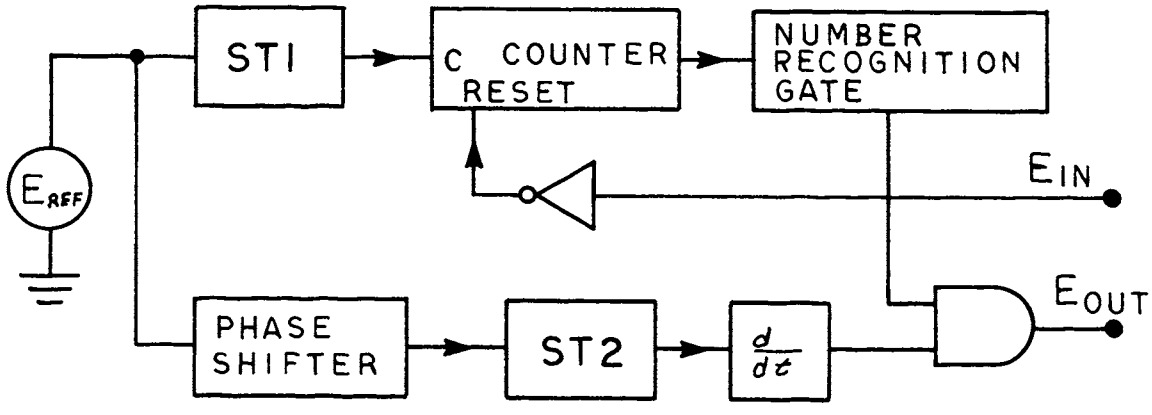


Fig. 3. Basic Block Diagram Of Digital Time Delay Scheme

Schmitt trigger ST1 is adjusted to produce a pulse to the counter input at each positive going, zero crossover point of the reference voltage. The counter, however, is disabled until the timer output flip-flop switches to the appropriate state. Once the counter is turned on, it begins to count the positive going zero crossovers of the reference voltage. The number recognition gate, which is a logical AND gate, gives a logical "one" output when the counter reaches a particular count. This is done by sensing the state of each flip-flop in the counter. By controlling the input to the AND gate, the operator can obtain a pulse output that is delayed any number of reference voltage cycles within the range of the counter. This pulse is of one cycle duration. The output of the number recognition gate thus identifies the reference cycle during which the delayed output should occur.

The correct phase angle within the cycle is identified by the phase shifter and Schmitt trigger ST2. The phase shifter is adjusted to approximately the desired phase angle and the threshold level of the Schmitt trigger is adjusted to advance or retard the output pulse as required to obtain the exact phase relationship between the Schmitt trigger output and the reference voltage. The output of the Schmitt trigger is differentiated to obtain a very short positive pulse which occurs at the desired phase point every cycle. The pulses from Schmitt trigger ST2 and the number recognition gate are fed to an AND gate. The output of this gate is the output of the time delay circuit and causes the output flip-flop to revert to the opposite state.

In the final timer design the same counter is used to determine both the "turn-on" and "turn-off" time interval. This, of course, necessitates changes in the counter reset circuits as indicated in the block diagram of the timing unit logic presented in Fig. 4. This circuit incorporates a buffer flip-flop which stores the pulse from the turn-on or turn-off gate (depending on the state the output flip-flop) and thus allows the counter to be reset as soon as the required number of cycles has been counted, instead of waiting until the output flip-flop changes state. The turn-on and turn-off gates of Fig. 4 correspond to the number recognition AND gate of Fig. 3. These gates are identical units, the schematic diagram of which appears in Fig. 5. The eight manual switches per gate permit the selection of the "on" and "off" time periods. Each gate also has two additional inputs, one of which disables the gate if the output flip-flop is not in the appropriate state, thus allowing only one gate to be in operation at any instant. The second additional input is connected to the complement of the counter reset line and disables the gate during the time interval during which the counter is reset to the zero state. This prevents spurious outputs from occuring during the counter reset process since the flip-flopsin the counter may not all clear at the same instant.

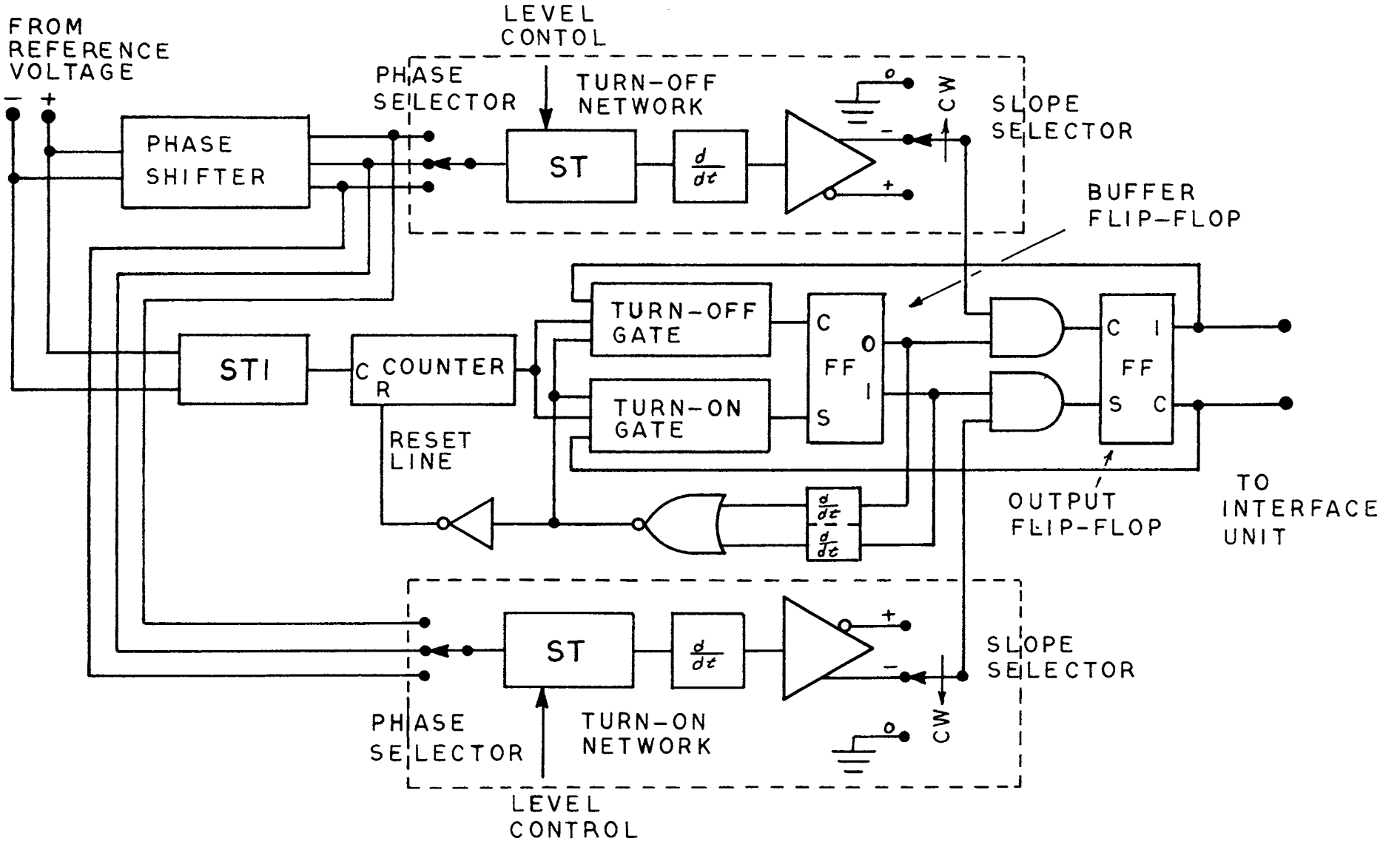
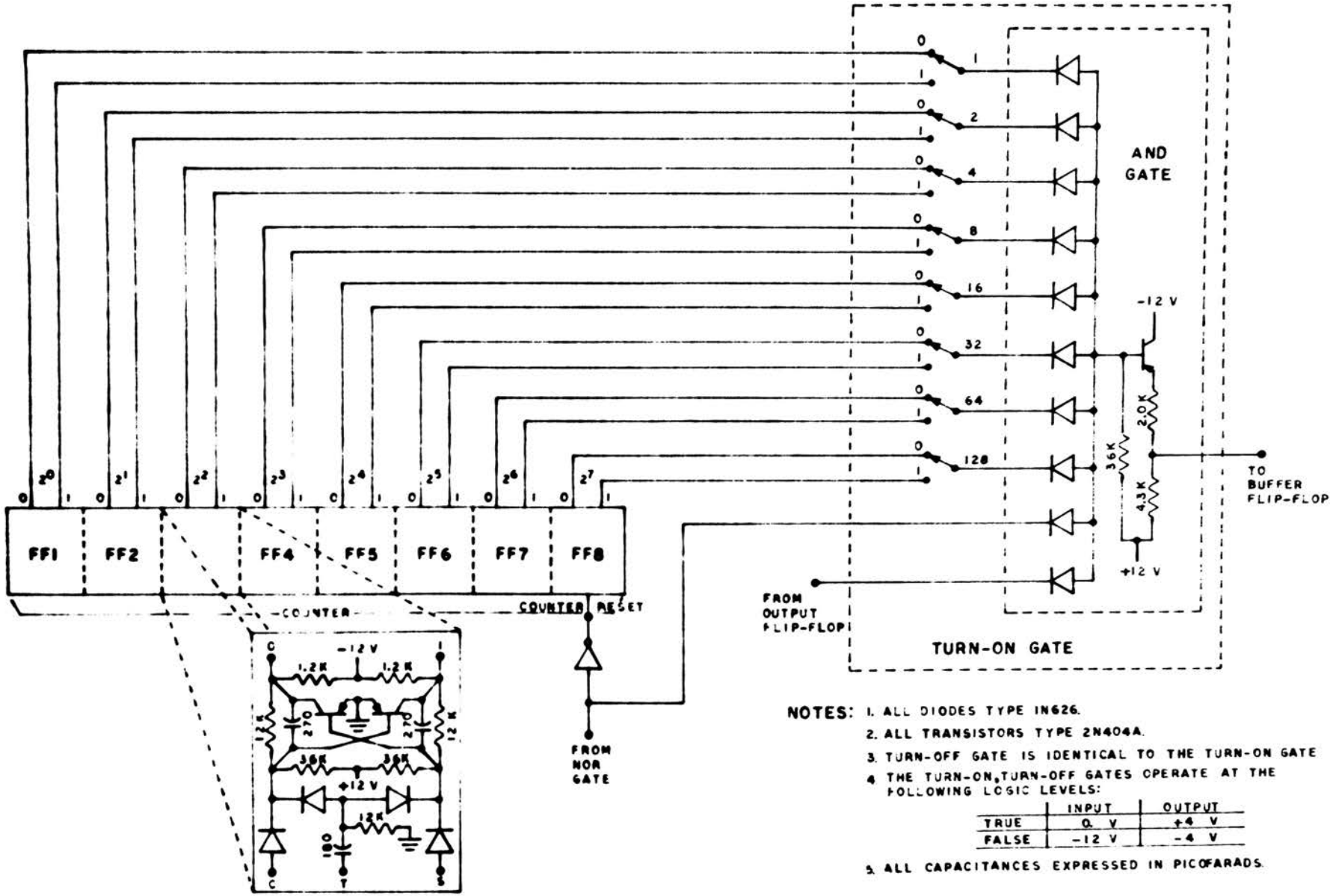


FIG. 4. LOGIC DIAGRAM OF TIMING UNIT



NOTES:
1. ALL DIODES TYPE IN626.
2. ALL TRANSISTORS TYPE 2N404A.
3. TURN-OFF GATE IS IDENTICAL TO THE TURN-ON GATE
4. THE TURN-ON, TURN-OFF GATES OPERATE AT THE FOLLOWING LOGIC LEVELS:

	INPUT	OUTPUT
TRUE	0 V	+4 V
FALSE	-12 V	-4 V

5. ALL CAPACITANCES EXPRESSED IN PICOFARADS.

FIG. 5 COUNTER AND ASSOCIATED LOGIC GATES

When the buffer flip-flop is switched to a new state at the end of the selected time delay period, the counter is reset to the zero state immediately. This resetting is accomplished by differentiating the outputs of the buffer flip-flop and applying the positive going output to the counter reset terminal via a logical NOR gate and an inverting driver amplifier.

The output of the buffer flip-flop is similar to that of the output flip-flop except that the switching transitions occur at the zero crossover point of the reference voltage. This characteristic is potentially useful in triggering the sweep of an oscilloscope. The output of the buffer flip-flop is made externally available for this purpose.

Determining Turn-On and Turn-Off Phase Angle - The turn-on and turn-off phase angle synchronizing networks differ from more familiar designs in that the phase shifter is not continuously variable. A precision R-C ladder type phase shifter provides three outputs with phase angles of -120^{o}, -180^{o}, and -240^{o} to both the turn-on and turn-off synchronizing networks. Each network has a PHASE SELECTOR which connects the appropriate phase to the input of a Schmitt trigger. The threshold level of the range of the level control is sufficient to cause the Schmitt trigger to fire at any point within $\pm 60^{o}$ of the zero crossover of the input voltage to the Schmitt trigger. This is shown graphically in Fig. 6, along with typical waveforms of the associated differentiator and buffer amplifiers.

There are two regions, relative to the Schmitt trigger input voltage, where a timing "spike" cannot be generated. However, the phase shifter has three outputs of different phase angles. The appropriate input for the Schmitt trigger is selected by means of the PHASE SELECTOR switch. The three operating regions will "overlap", extending the overall operating region an additional $\pm 60^{o}$ relative to the reference voltage.

By selecting the proper output of the buffer amplifier by means of the SLOPE SELECTOR, a positive going timing spike may thus be obtained at any point in the reference cycle, as indicated in Fig. 7.

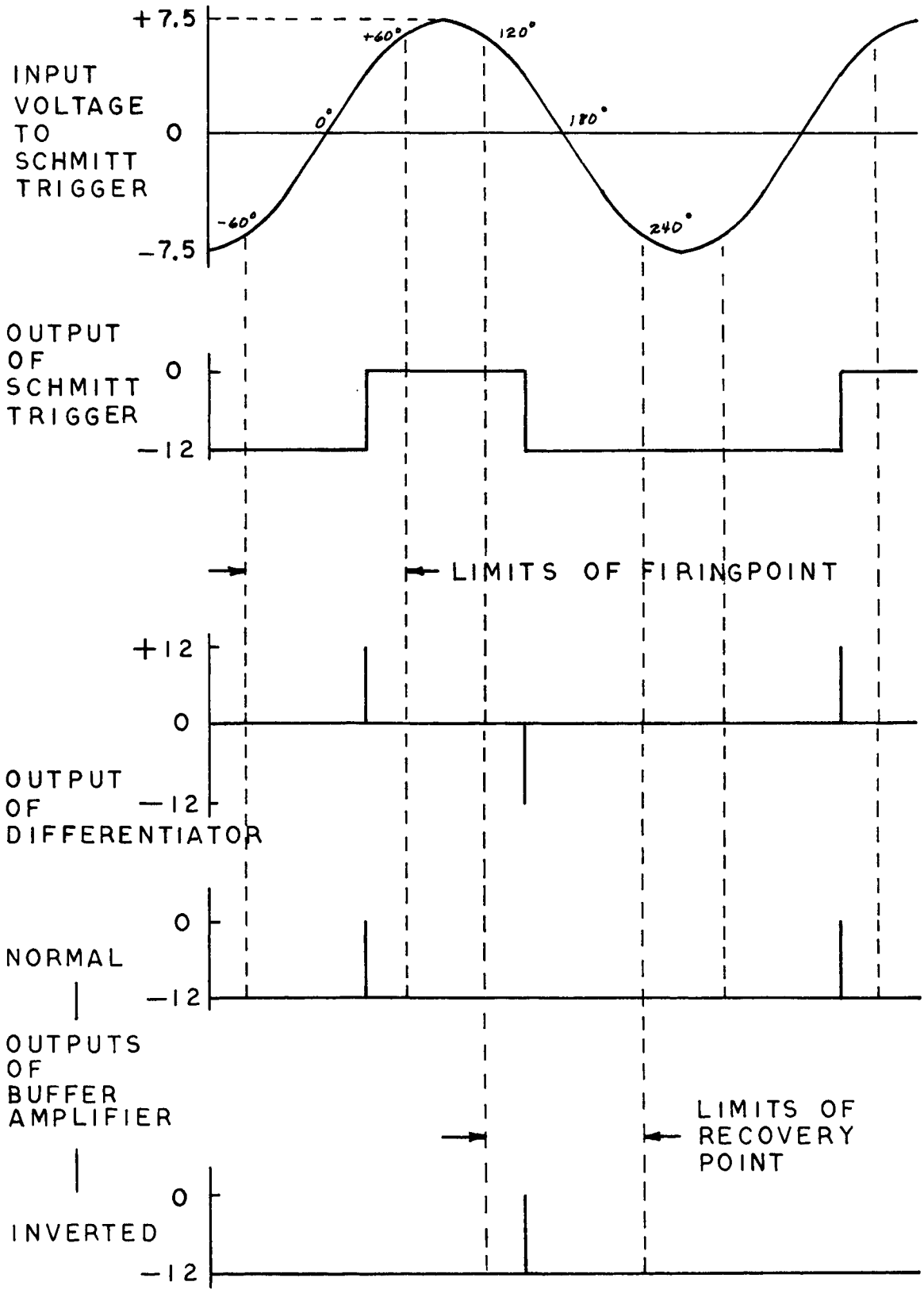


Fig. 6 Typical Waveforms Of A Turn-On or Turn-Off Network.

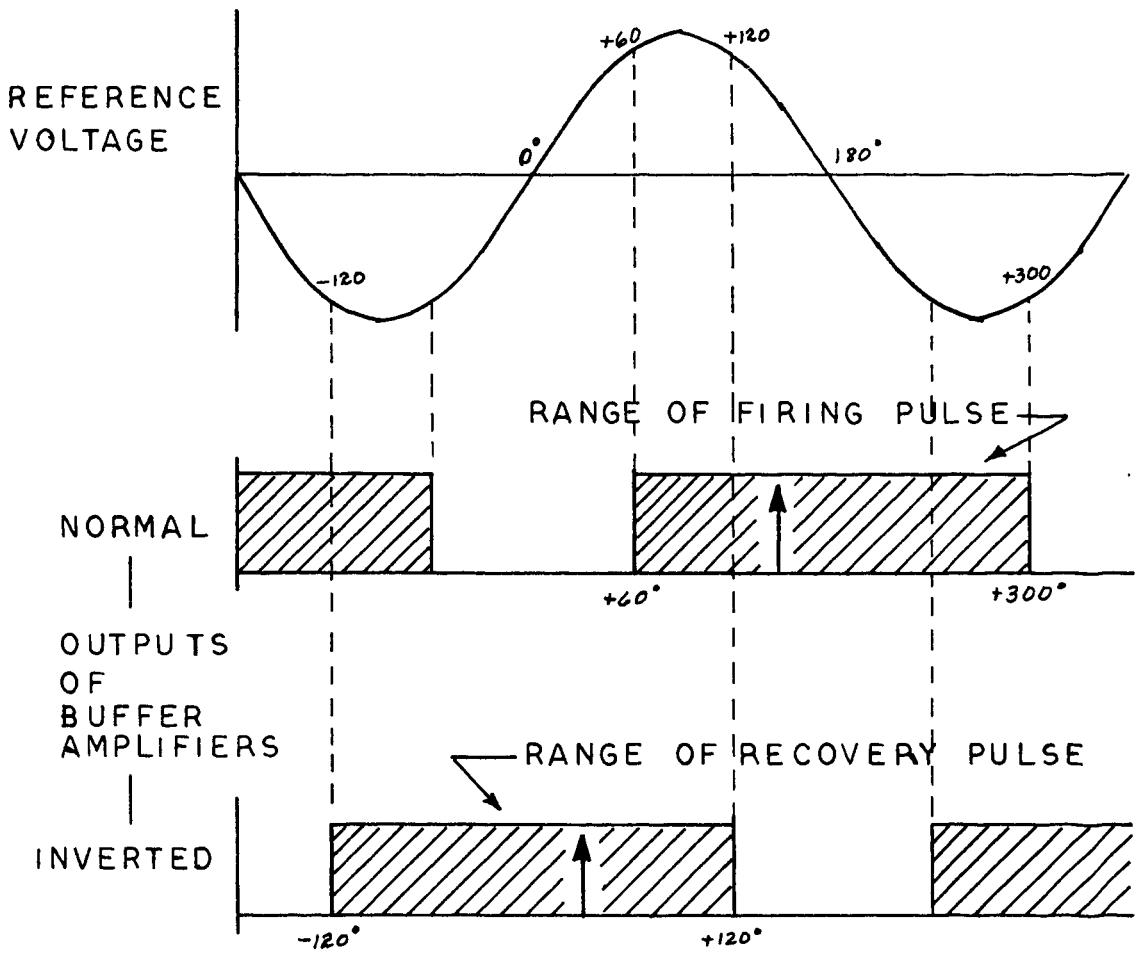
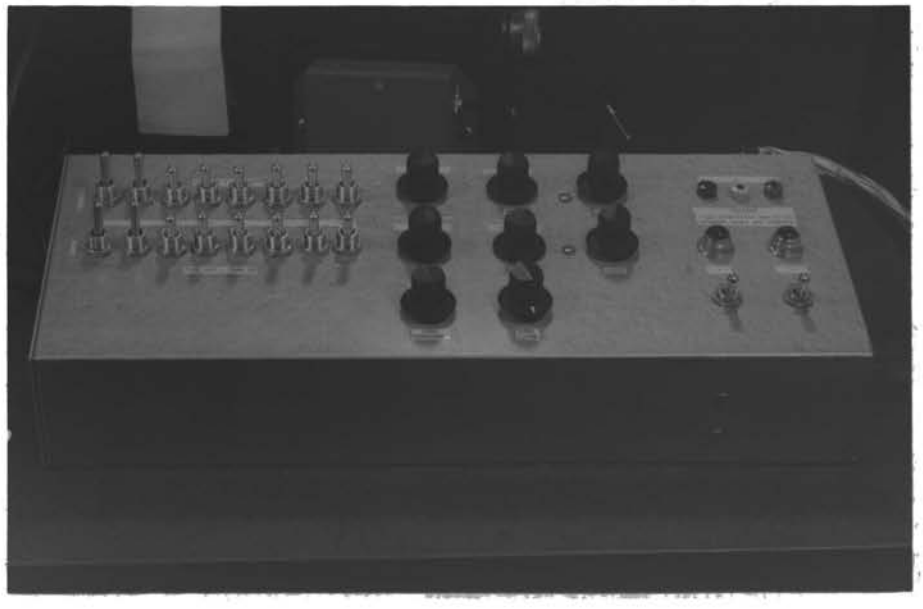


Fig. 7 Allowable Phase Angle Range Of Timing Pulses

The SLOPE SELECTOR has a third position which connects the output to a dc voltage, the level of which represents a logical "one". This allows the output flip-flop to change states at the same time as the buffer flip-flop. The switch transitions thus occur at the reference voltage zero crossover without further adjustment from the PHASE SELECTOR of LEVEL CONTROL.

Other controls of the TIMING AND CONTROL UNIT consists of an OPERATE switch which energizes the safety relay and the ZERO LEVEL controls. The ZERO LEVEL control adjusts the magnitude and polarity of a bias supply in order to shift the firing point of ST1 slightly ($\pm$ 3° maximum). This control is seldom, if ever, needed, but was included to allow very high precision in controlling to the zero crossover point if necessary.

The completed TIMING AND CONTROL unit is shown in Fig. 8.



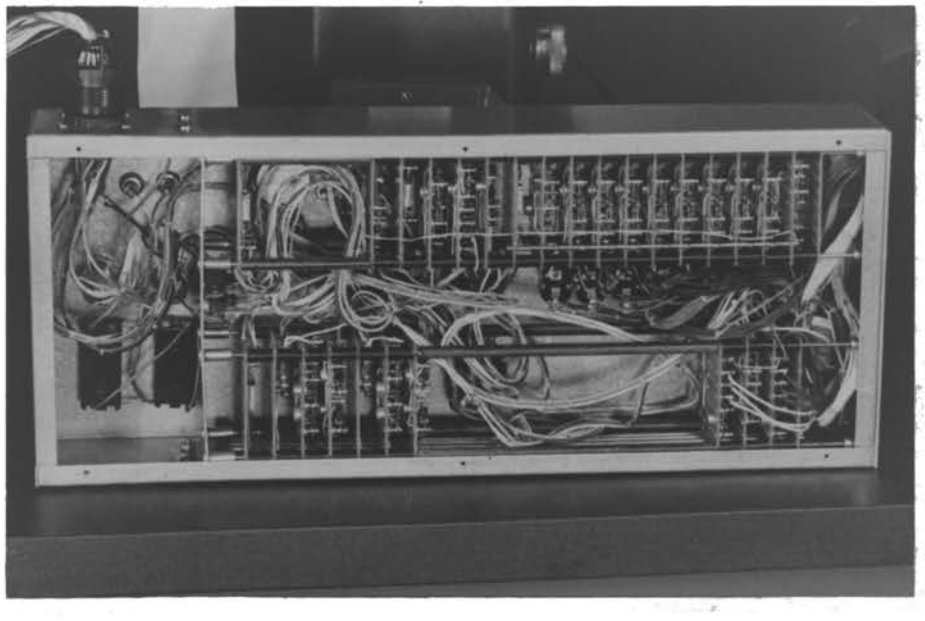


Fig. 8 Timing and Control Unit

III. THE SWITCH UNIT

Three basic types of switch elements were considered; electromechanical contactors, transistors, and silicon controlled rectifiers (thyristors).

The electromechanical approach was discarded because of problems of contact deterioration, contact bounce, speed of response, and general mechanical complexity.

The transistor approach was abandoned because no units were found which combined the ability to withstand high transient voltages, with high current ratings.

The silicon controlled rectifier, a thyristor device, is the most practical switch element as it is available in high current, high voltage units at moderate cost. A disadvantage of thyristors in the required power range is the lack of a convenient turn-off mechanism. The only way of returning a silicon controlled rectifier to the blocking state is to reduce the current through the device to zero for a period of time varying between 10 to 30 microseconds, depending on such factors as load current, device temperature, and gate bias conditions.

Having decided upon the silicon controlled rectifier as the basic switching element, different switch configurations and means of achieving turn-off were investigated. The capacitor discharge method was judged to be the simplest and least critical of the turn-off methods. The switch configuration of Fig. 9 was selected on the basis that the turn-off and interface circuitry would be less complicated than for other configurations.

In this circuit, thyristor A carries the full load current and is maintained in the conducting state by a dc gate current for the duration of the desired ON period. Also during the ON period, the commutating capacitor is given a charge of the polarity indicated, by external circuitry.

To achieve turn-off, the gate drive of thyristor A is reversed, and simultaneously a positive pulse is applied to the gate of thyristor B. Thyristor B switches to the conducting state, thereby shunting the load current away from thyristor A until the commutating capacitor is completely discharged. During this time thyristor A recovers to the blocking state. The load current then proceeds to charge the commutating capacitor to a high reverse voltage then recovers to the blocking state, completing the turn-off process.

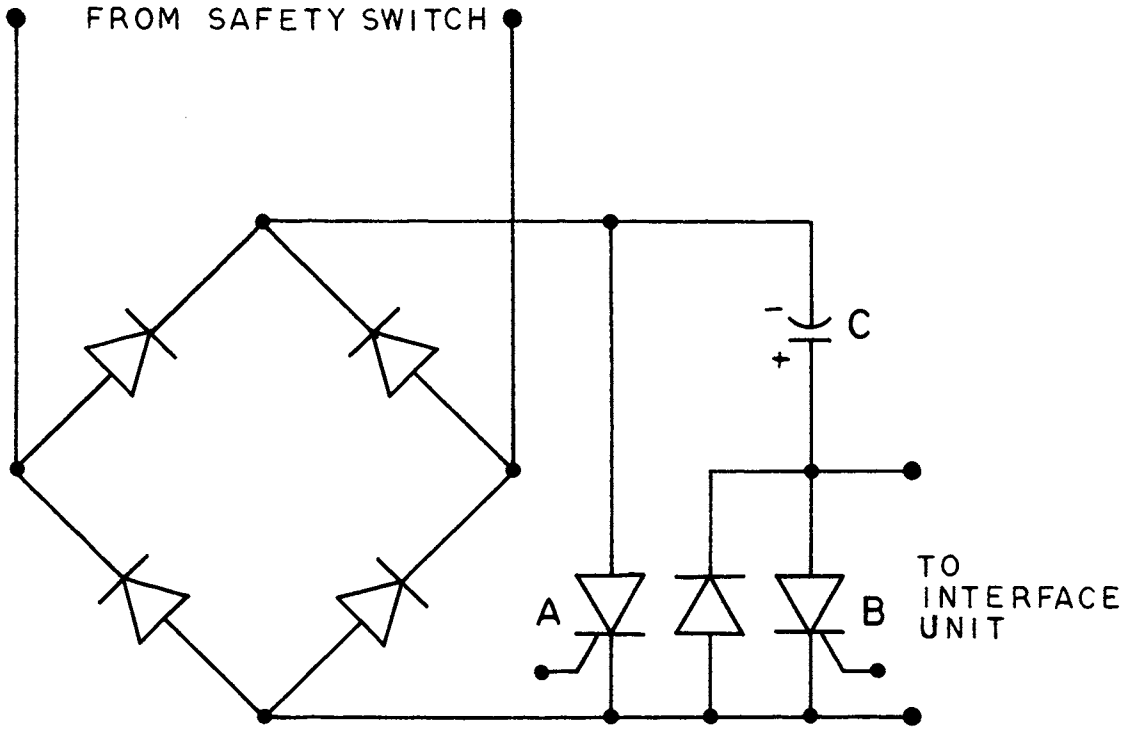


FIG 9 BASIC SWITCH CONFIGURATION

Selection of Semiconductor Devices - The specified current rating was 20 amperes which, in the chosen switch circuit, is conducted by the single thyristor. The transient voltage requirements were not specified directly, only that the load would be highly inductive and that turn-off should occur as quickly as possible. After surveying the blocking voltages of available silicon controlled rectifiers, the ability to withstand 600 volt operating transients and a maximum of 800 volts without damage, was taken to be a reasonable design goal.

Since semiconductor diodes with a reverse voltage rating of 800 volts are very expensive in designing the bridge circuit, two lower voltage units were connected in series. This complicates the circuitry and degrades the performance somewhat, because each diode must have a resistor and capacitor in parallel with it to insure that the reverse voltage is shared equally by each unit. Type 1N2159 diodes were selected; these diodes have a current rating of 25 amperes rms and a reverse voltage rating of 500 volts. The bridge circuit, when constructed using these diodes, is conservatively rated for 800 volt transients and a current rating of 50 amperes. The large current rating leaves a comfortable safety margin in the event of accidental overload.

Type 2N688 silicon controlled rectifiers were selected for the main switch element. The 2N688 has a minimum forward breakover voltage of 400 volts. This necessitates the use of two units in series. As with the diodes, a resistor and capacitor were connected in parallel with each thyristor to insure that the transient voltages are divided equally across the two units.

The current rating of the 2N688 is 25 amperes rms. This rating is adequate, but does not leave much of a safety margin for accidental overloads. Furthermore, since the turn-off time of a silicon controlled rectifier is dependent upon the temperature of the device and the current through the device immediately prior to turn-off, it was decided to operate two 2N688's in parallel to accelerate the turn-off process. A small resistor (0.085 ohm) is connected in series with each unit to insure that the current is shared equally between the parallel units.

For the commutating thyristor the type 2N1771 silicon controlled rectifier was selected. The commutating thyristor is not required to have a high rms current rating, only a high pulse current rating. Neither is a high, minimum forward breakover voltage rating required since the high voltage switching transients occur while it is in the conducting state. The unit must, however,

be capable of withstanding the 315 peak voltage of the 200 v rms power source. The 2N1771 has a minimum forward breakover voltage rating of 480 which is more than adequate.

The 2N1771 commutating thyristor is protected from reverse transient voltages by a type 1N255 diode connected across it. A schematic of the complete switch unit is presented in Fig. 10.

Transient Protection - Although the switch can withstand transient voltages approaching 800 volts, larger transients are a certainty when switching inductive loads, unless some type of transient surpressor is provided. No entirely satisfactory means of transient surpression was discovered. The following approach was considered to be an acceptable solution at moderate cost. Nine thyrector[1] diodes, type 6RS21SA3D3, were connected in three parallel branches, each branch consisting of three diodes in series. This arrangement will conduct 28 amperes at a terminal voltage between 575 and 700 volts as shown in Fig. 11. Thus as long as the instantaneous load does not exceed 28 amperes, the switching transient will not exceed 700 volts. As a fail-safe protection against larger transients, a series string of three 120 volt zenor diodes are connected from the anode to the gate of one 2N688 of each of the two parallel groups. Thus if the transient voltage across any 2N688 exceeds 360 volts the switch reverts to the conducting state until a current zero crossover occurs. The commutating thyristor is similarly protected. Thus, the switch fails to operate properly, but is not damaged by extreme transient voltages.

Heat Sinks - As all semiconductor types selected with the exception of the Thyrector diodes, are stud mounting units, a suitable heat sink is needed for each semiconductor. For uniformity, the required fin size was calculated for the device with the most stringent heat dissipation requirement and all semiconductors were mounted on fins of this size. The 2N688 required the largest fin area, as the stud temperature must not exceed 60° while dissipating 25 watts. A fin size of 12 inches (30 cm) by 9 inches (22.5 cm), was calculated to be a conservative fin area.

The semiconductors are mounted directly on fourteen fins of this size, the fins being insulated from each other by the supporting wood rack as shown in Fig. 12.

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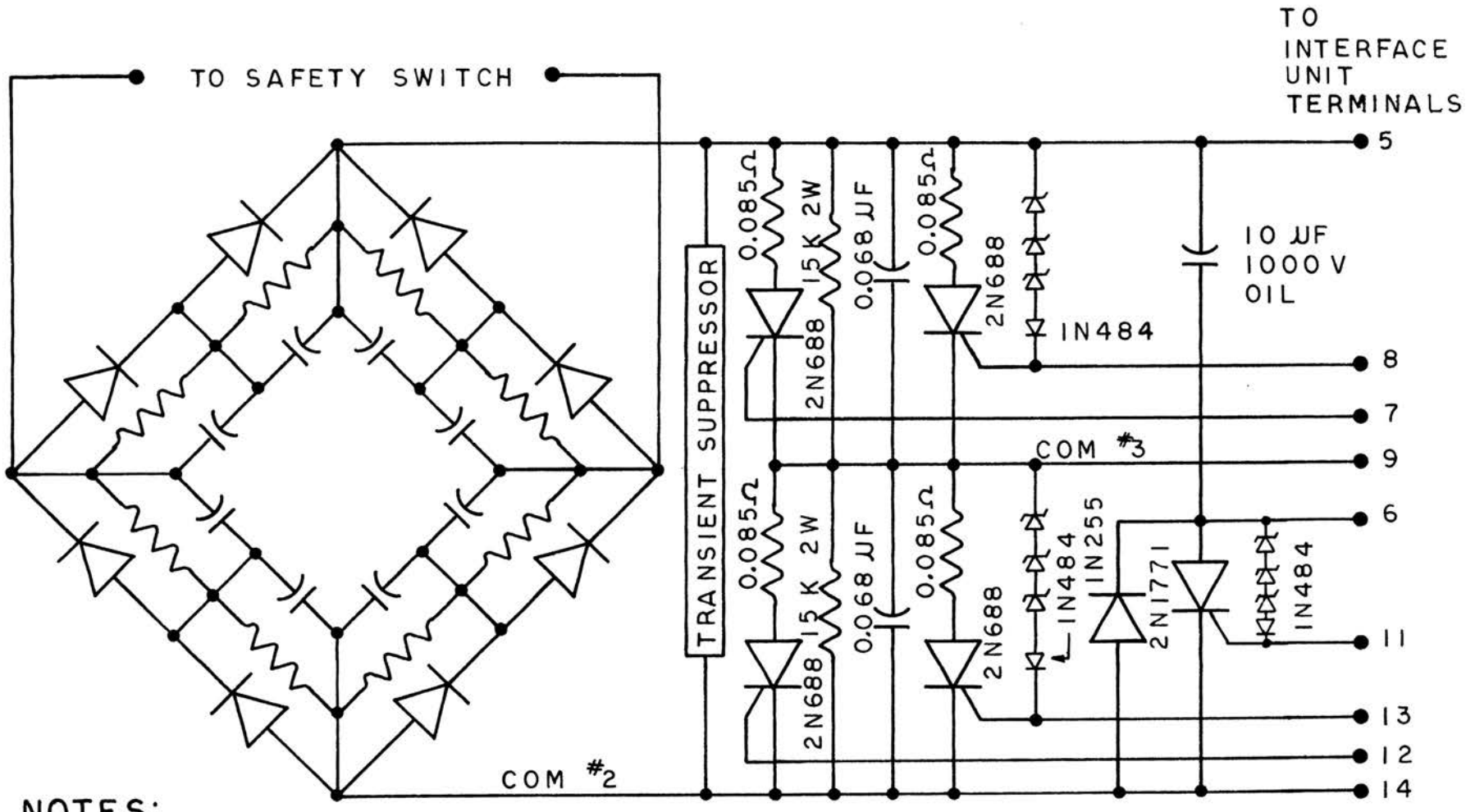
[1]Thyrector is a trademark of the General Electric Company.



NOTES:

1 ALL BRIDGEDIODES TYPE IN2159
2 ALL BRIDGE RESISTORS 51K 2W
3 ALL BRIDGE CAPACITORS 0.05 μF 600 V
4 ALL ZENOR DIODES TYPE IN3046

FIG. 10. SCHEMATIC DIAGRAM OF SWITCH UNIT

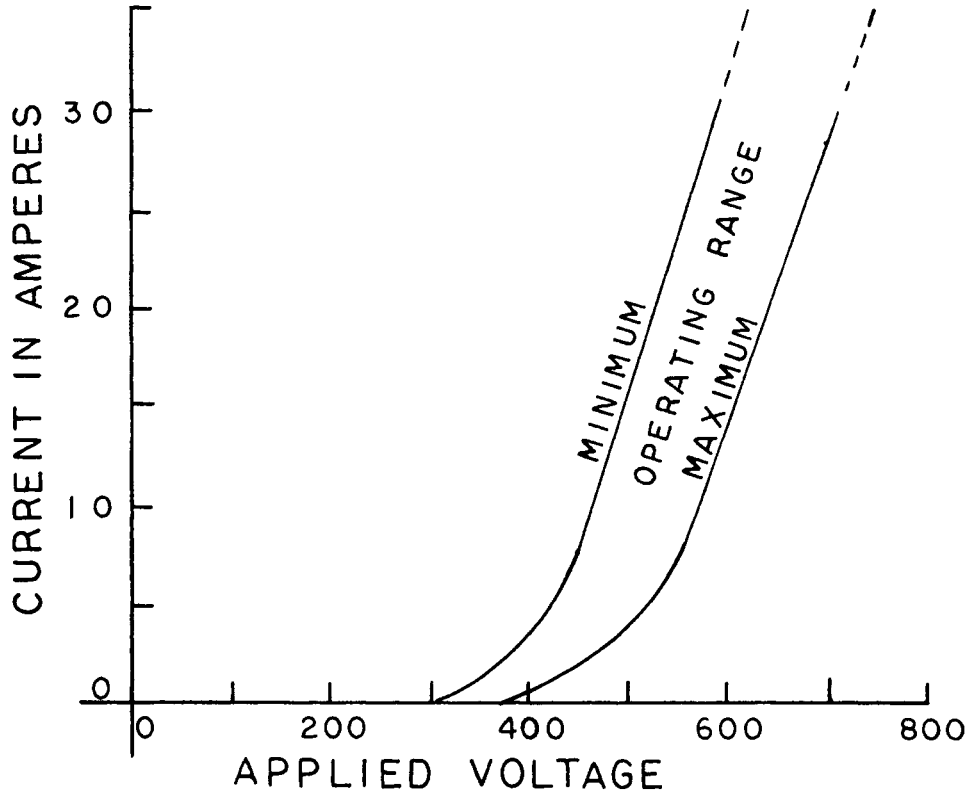


FIG. 11. VOLT–AMPERE CHARACTERISTICS OF TRANSIENT SUPPRESSOR

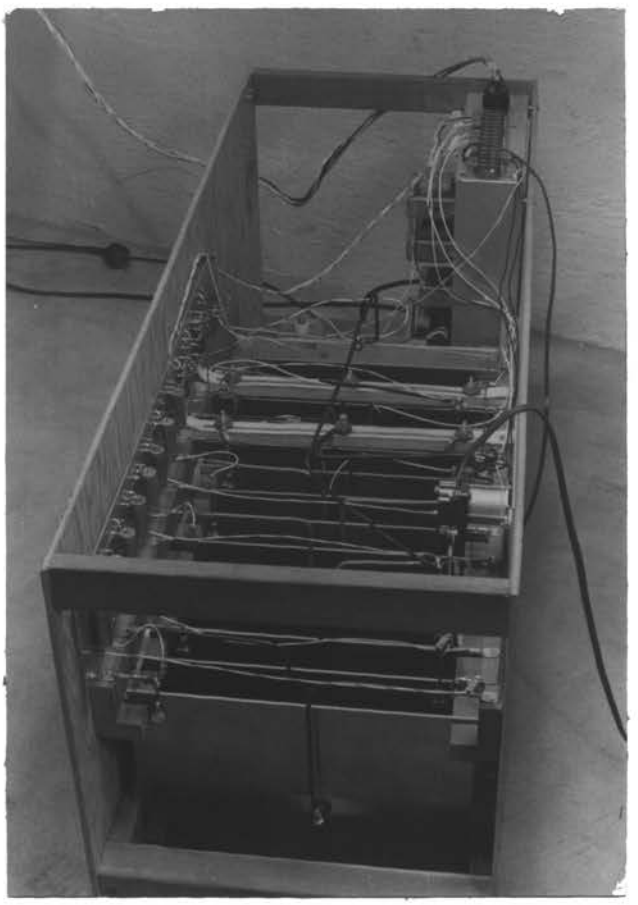


Fig. 12 Switch Unit

IV. INTERFACE UNIT

The block diagram of the interface unit is shown in Fig. 13. The 2N688 silicon controlled rectifiers are divided into two series groups. Separate, independent channels control each group since there will be large voltage transients between commons 1 and 2. Each channel consists of an electrically isolated power supply, a flip-flop memory, a pulse transformer to synchronize the memory flip-flop with the timing unit, and driver amplifiers to drive the thyristor gates. A low-impedance voltage source and electronic switch is also necessary to charge the commutating capacitor at the proper time.

Since high transient voltages occur between all signal commons, precautions were taken to prevent undesired coupling between the three signal systems. Special pulse transformers were designed to transfer the timing pulse from the timing unit to the memory flip-flops. Each pulse transformer consists of two diametrically opposed, center-tapped coils wound upon a torroidal core. The capacitance between the two windings was measured to be 10 pF. This low interwinding capacitance, plus the push-pull operation of both primary and secondary windings account, primarily, for the stability of operation during the high voltage transients.

The capacitor charging circuits prepare the commutating capacitor for the turn-off process. This is done by applying a +18 volt low impedance power supply to the commutating capacitor while the switch is in the conducting state. The minimum allowable ON time is determined by the time required to charge the commutating capacitor. This time is approximately 100 microseconds for the present circuits. The schematic diagram of the capacitor charging switch is given in Fig. 14.

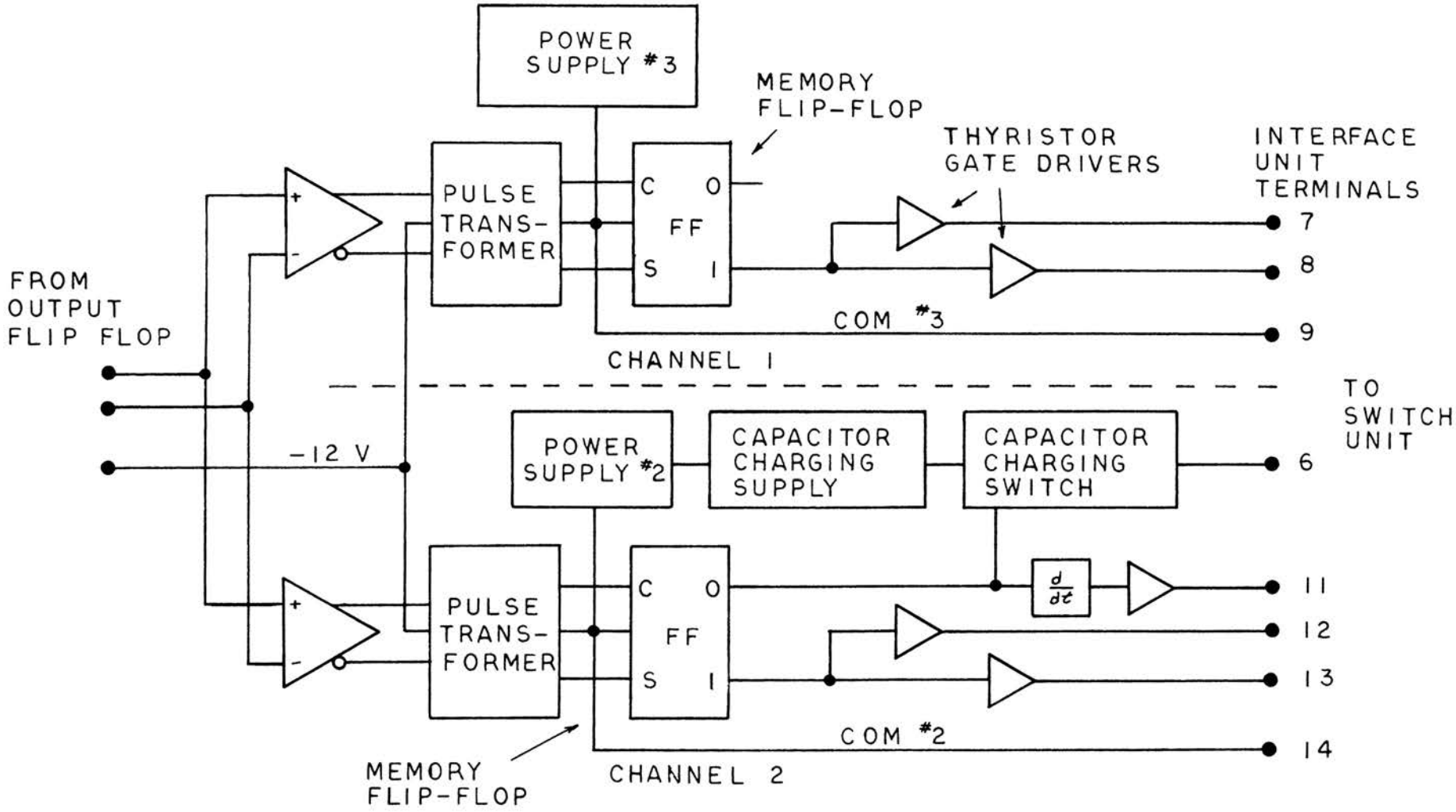


FIG. 13. BLOCK DIAGRAM OF INTERFACE UNIT

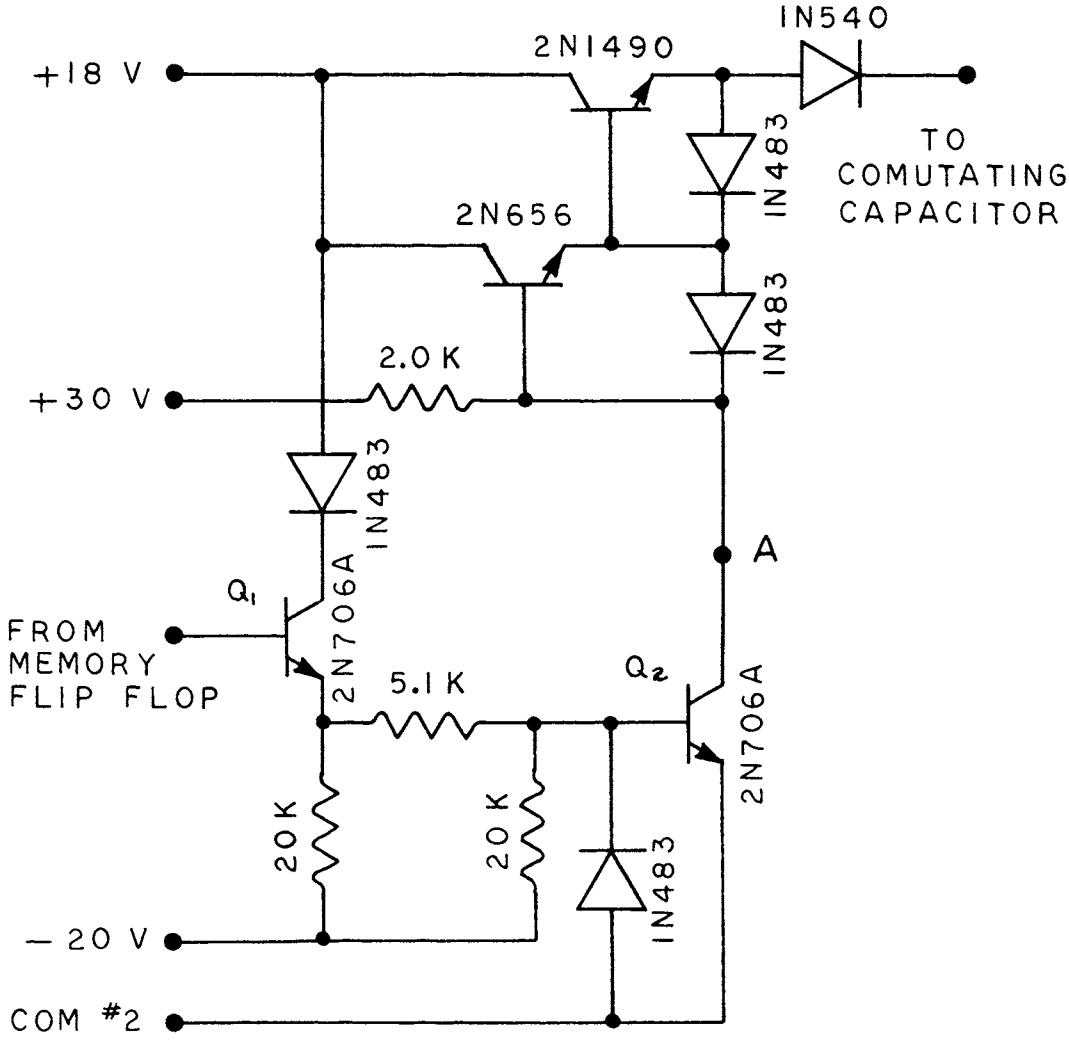


FIG. 14. SCHEMATIC DIAGRAM OF COMUTATING CAPACITOR CHARGING SWITCH

V. SWITCH PERFORMANCE

The completed switch met all design conditions with a slight modification of the allowable timing cycle, caused by the power ratings of the Thyrector diodes. Although the heat dissipation capacity of the Thyrector diodes is not given explicitly, calculations based upon the maximum recurrent pulse ratings indicate a value of approximately 13.5 watts per unit.

When switching inductive loads, the major portion of the magnetic energy is dissipated in the Thyrector diodes. Assuming an 20 ampere, purely inductive load, the minimum time between turn-off transitions should be greater than 0.085 seconds (5 cycles) to avoid overheating the Thyrector diodes.

Typical voltage and current waveforms for various loads are given in Fig. 15 and Fig. 16. The ringing of the transient voltage of Fig. 16 is caused by a resonance between the winding capacitance and the inductance of the load.

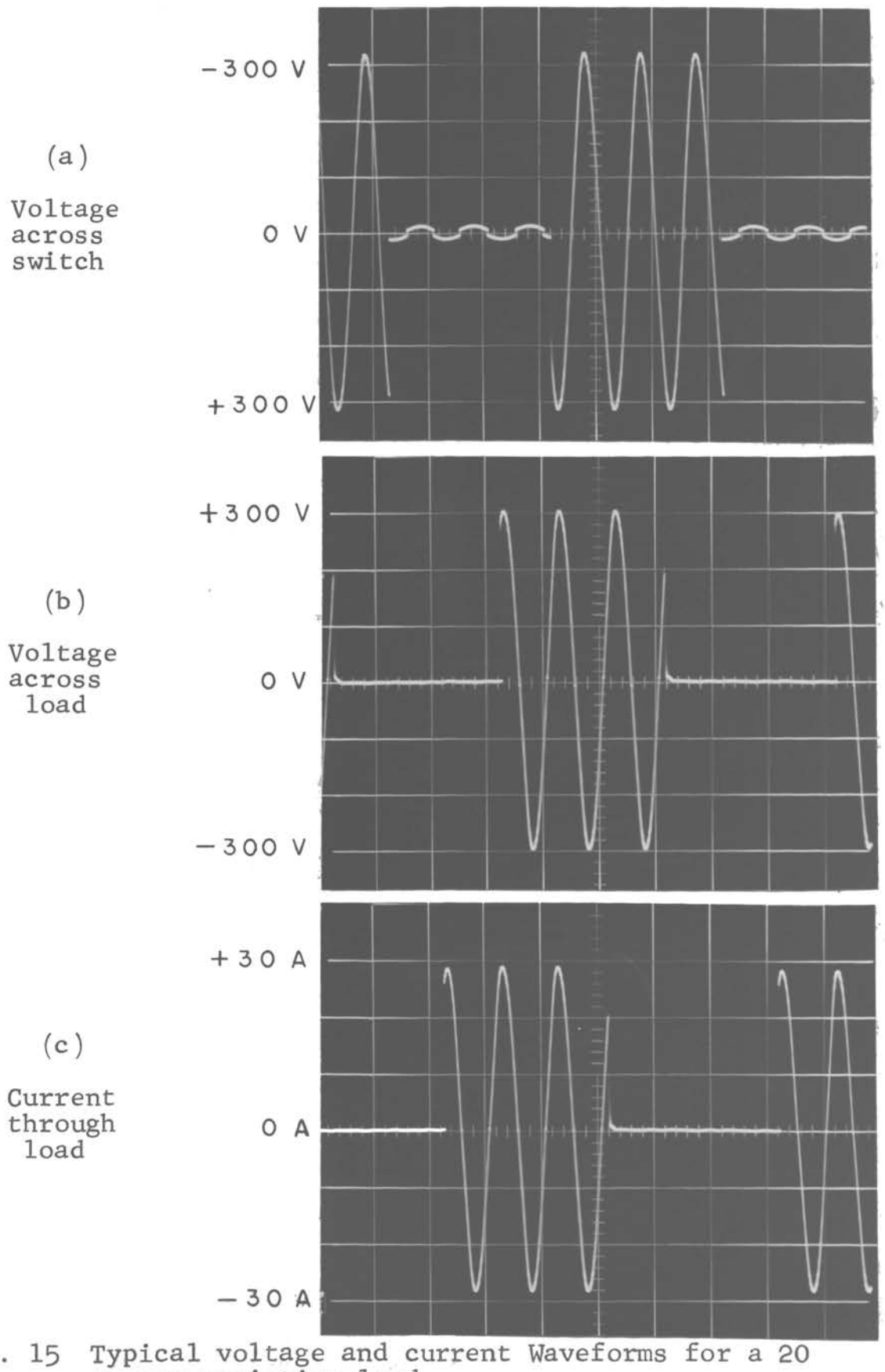


Fig. 15 Typical voltage and current Waveforms for a 20 ampere resistive load

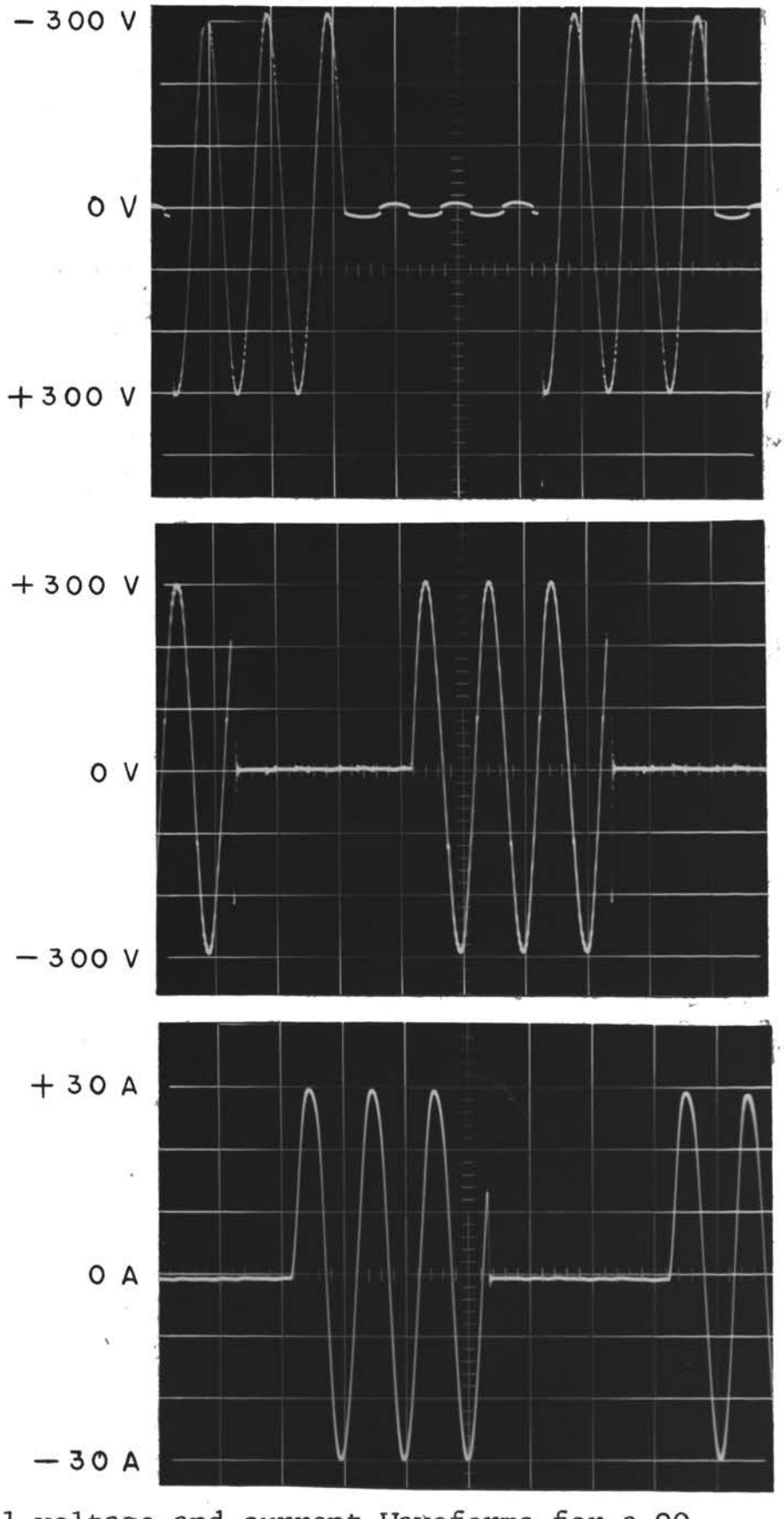


Fig. 16 Typical voltage and current Waveforms for a 20 ampere inductive load

IV. CONCLUSIONS

Switch operation was up to specifications, and no problems have been encountered in operating under fairly severe transient conditions. The only limit on complete flexibility of operation is the five cycles required between turn-offs with heavy inductive loads to prevent overheating of the transient surpressors.

No problems were encountered that would prevent the successful construction of much higher or lower power switches merely by redesigning the switch unit with suitable semiconductors and redesigning the gate drive circuits to accommodate the new gate drive requirements.

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APPENDIX A

Logic Symbols - The symbols used in this paper are to be interpreted in accordance with Military Standard 806B. The following figure defines the more common symbols.

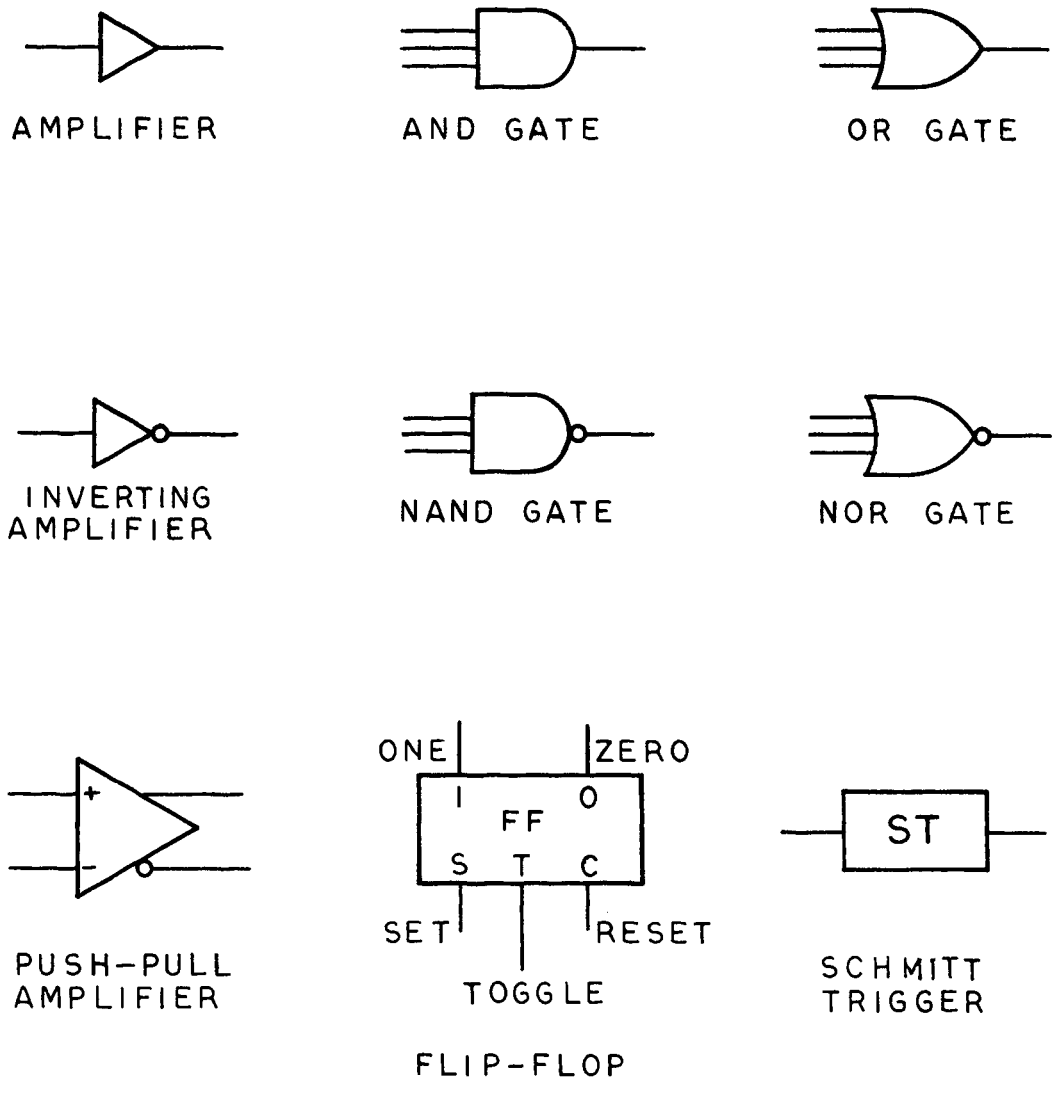


Fig. 17 Logic Symbols

APPENDIX B

Schematic Diagrams of Timing and Control Unit - There are three power supply systems in the synchronous switch, all of which are electrically isolated from earth ground and from each other. Therefore, the symbol ⏚ should be interpreted to mean signal ground and is the COMMON line of that power supply which energizes the circuits in question.

In appendix B the symbol ⏚ refers to COMMON #1 unless otherwise specified.

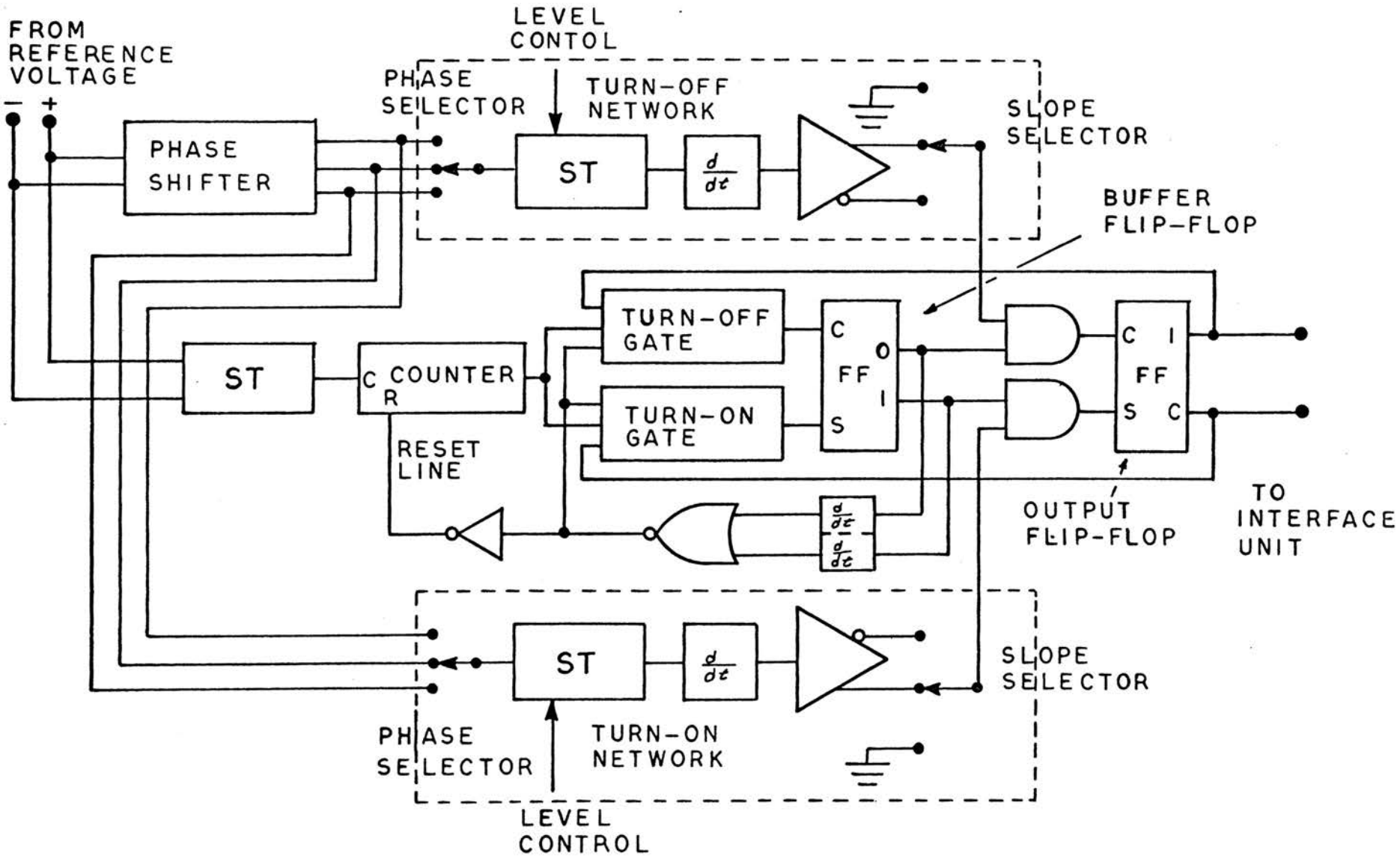


FIG. 18. LOGIC DIAGRAM OF TIMING UNIT

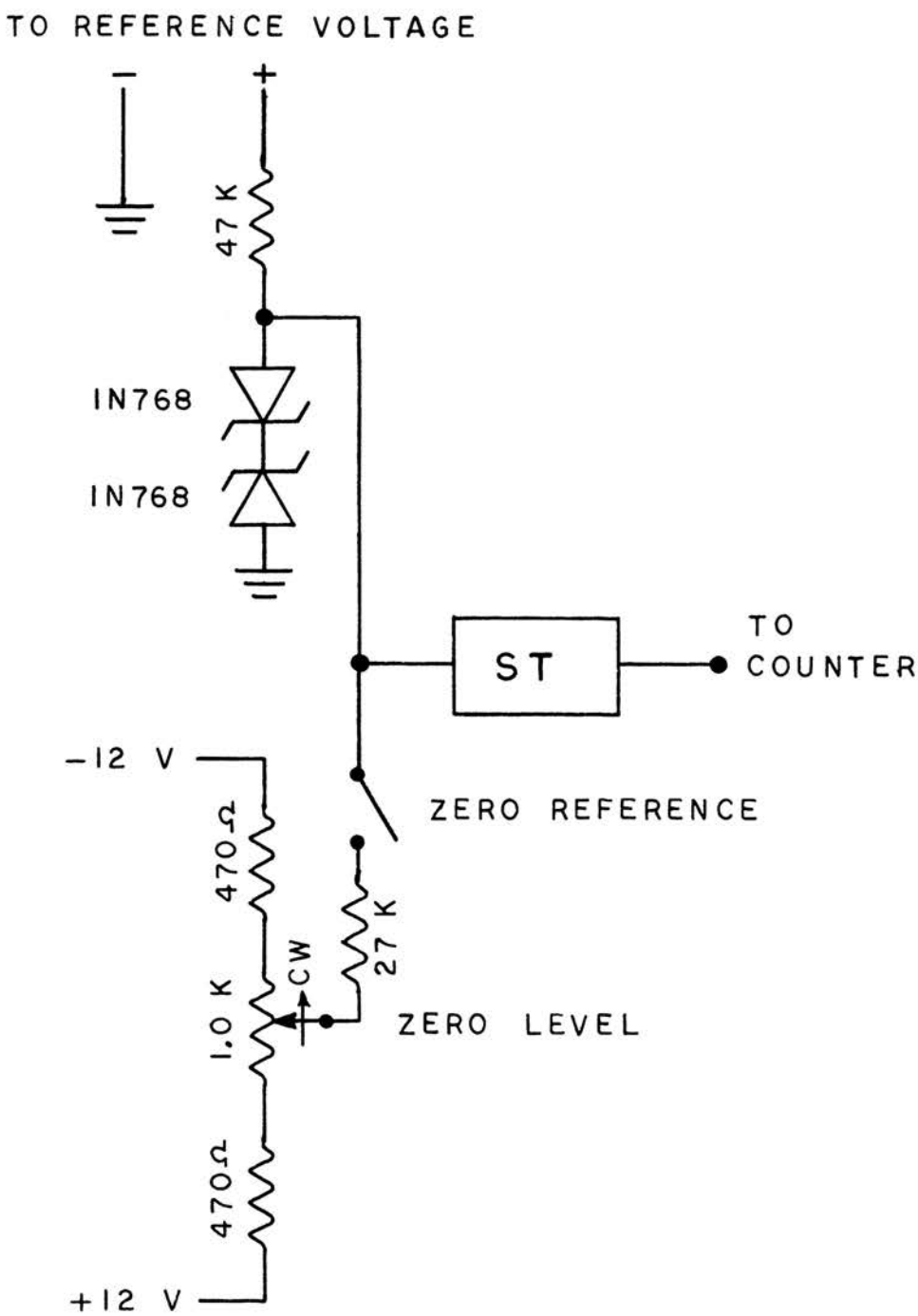


FIG. 19. SCHEMATIC DIAGRAM OF ZERO CROSSOVER DETECTOR

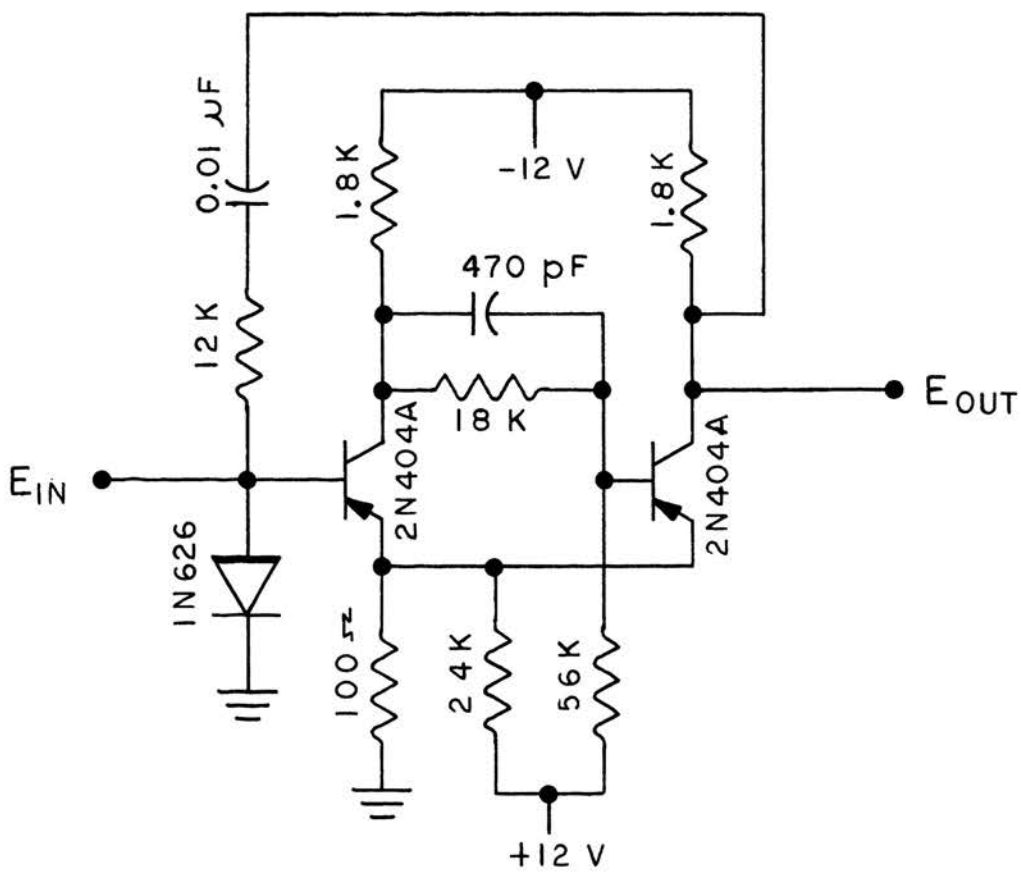


FIG. 20. SCHEMATIC DIAGRAM OF SCHMITT TRIGGER

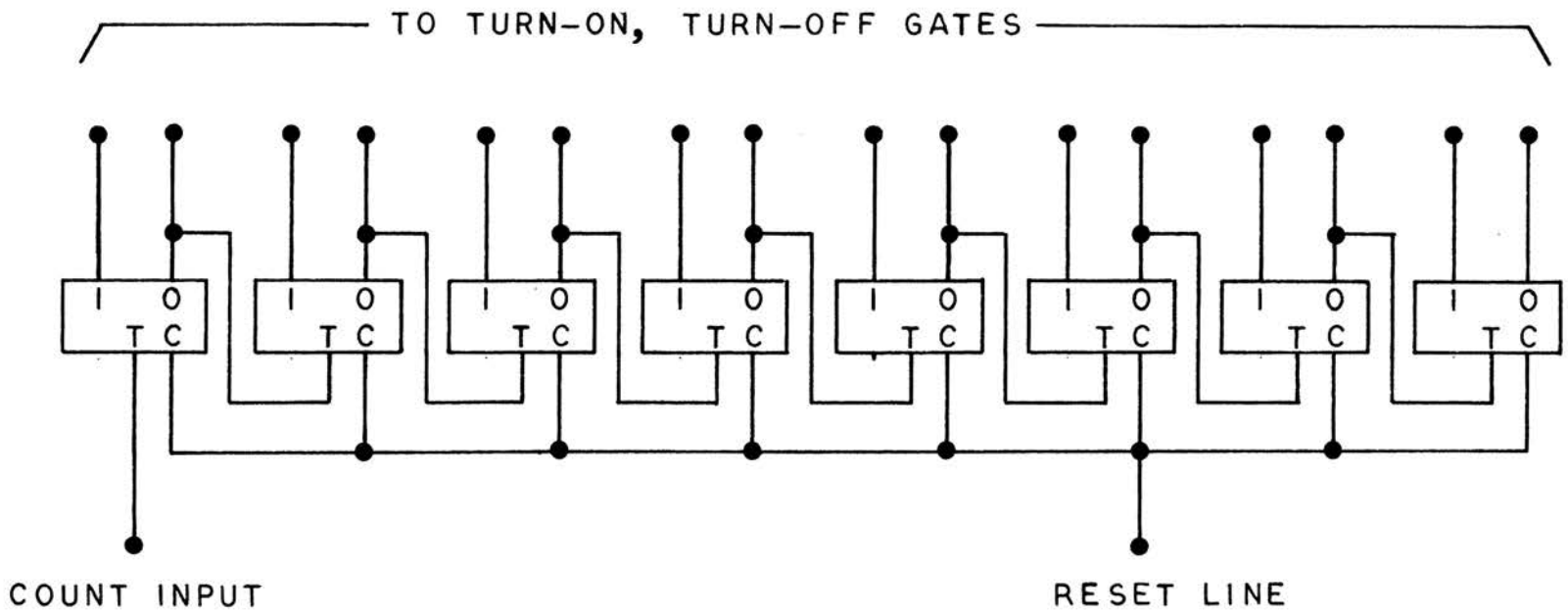


FIG. 21. BLOCK DIAGRAM OF COUNTER

LOGIC LEVELS

	INPUT	OUTPUT
TRUE	+4 V	0 V
FALSE	−4	−12 V

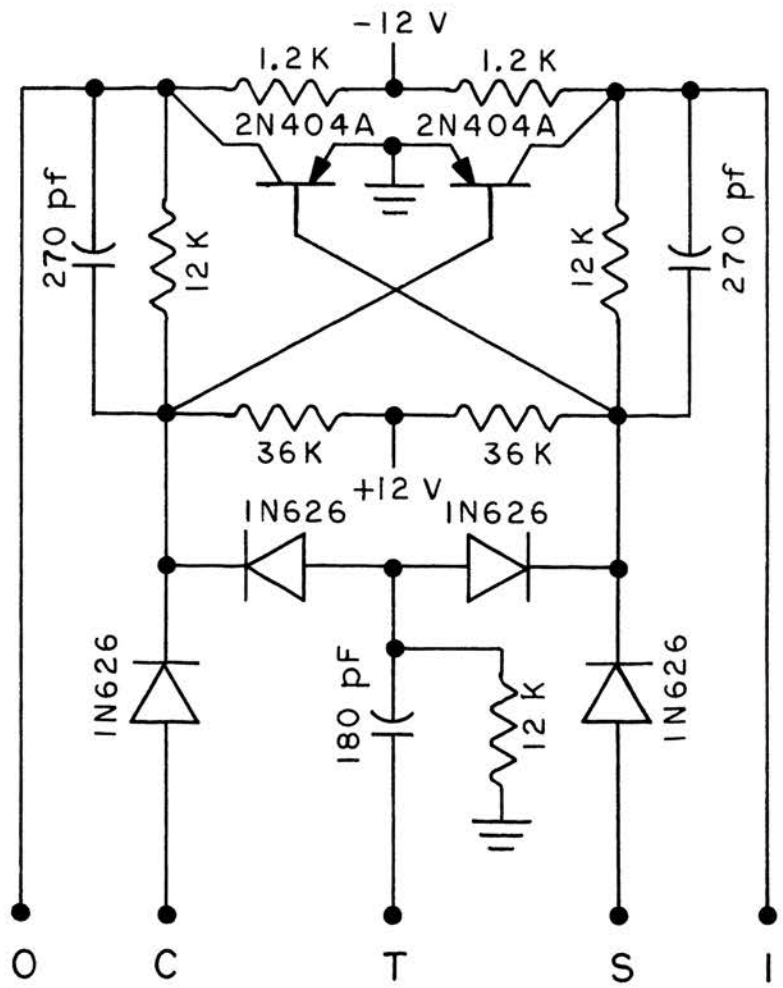


FIG. 22. SCHEMATIC DIAGRAM OF FLIP-FLOPS

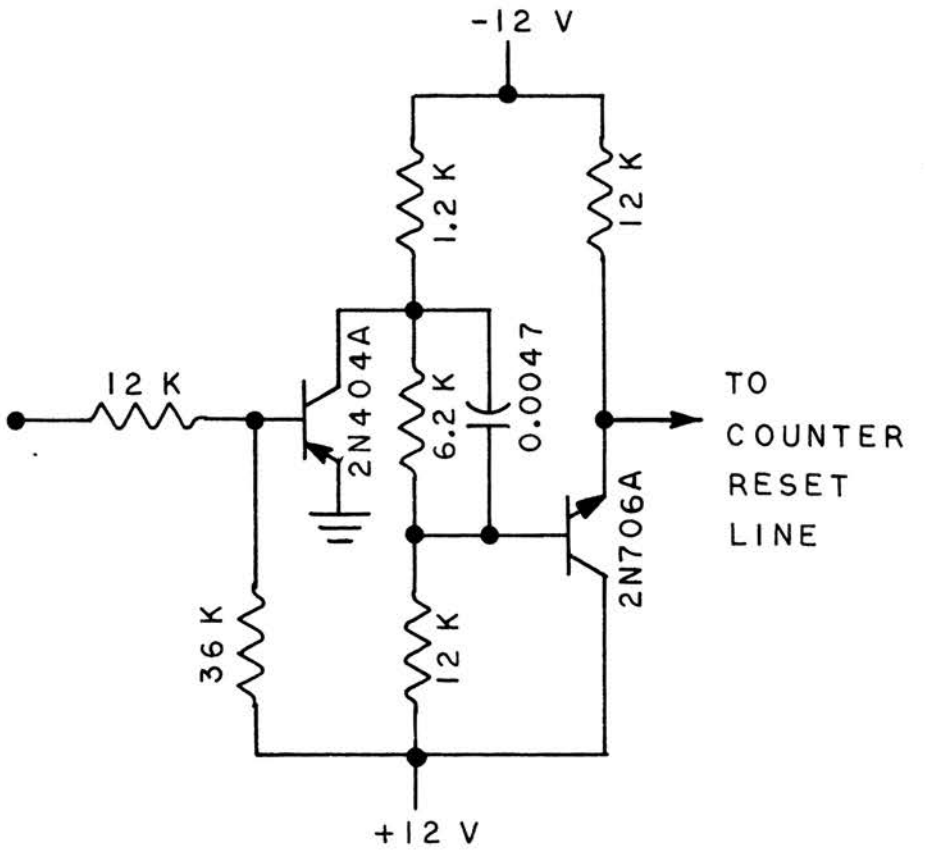


FIG. 23 SCHEMATIC DIAGRAM OF COUNTER RESET DRIVER

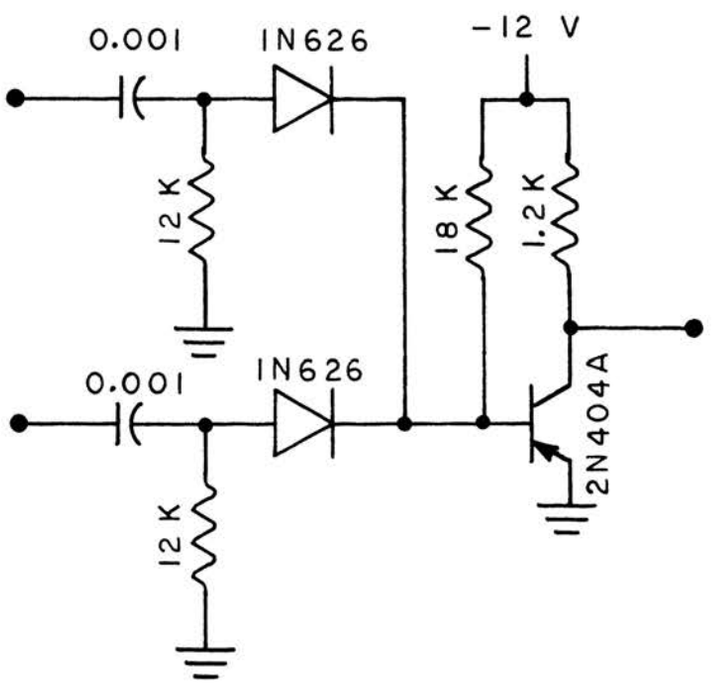


FIG. 24. SCHEMATIC DIAGRAM OF INTEGRATED DIFFERENTIATOR-NOR GATE

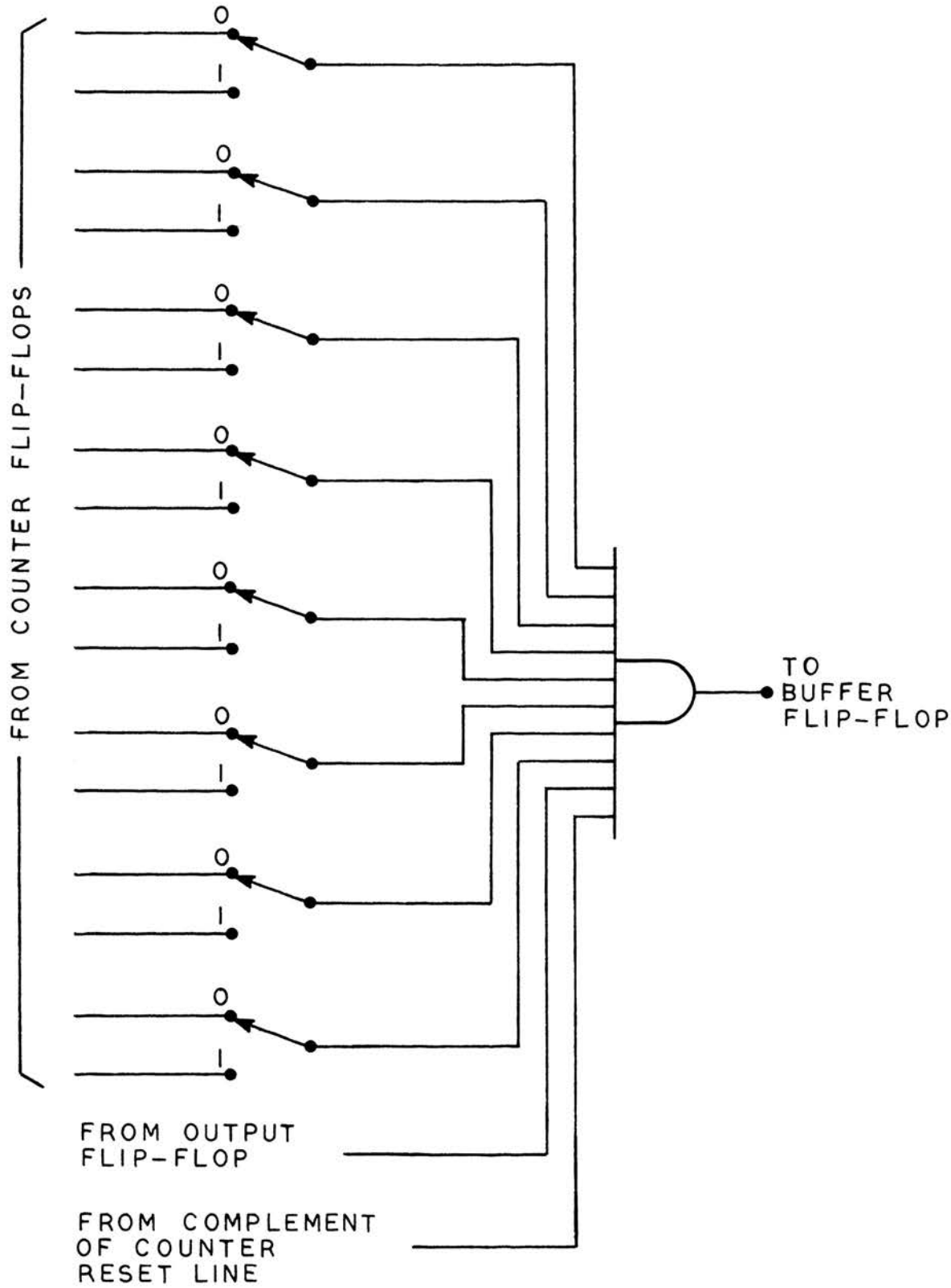
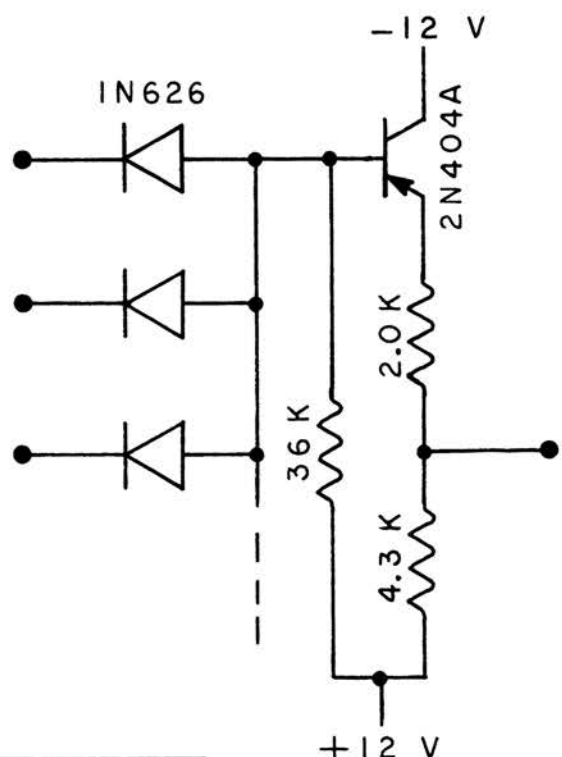


FIG. 25. BLOCK DIAGRAM OF TURN-ON, TURN-OFF GATES



LOGIC LEVELS

	INPUT	OUTPUT
TRUE	0 V	+4 V
FALSE	12 V	−4 V

FIG. 26. SCHEMATIC DIAGRAM OF LOGICAL AND GATE

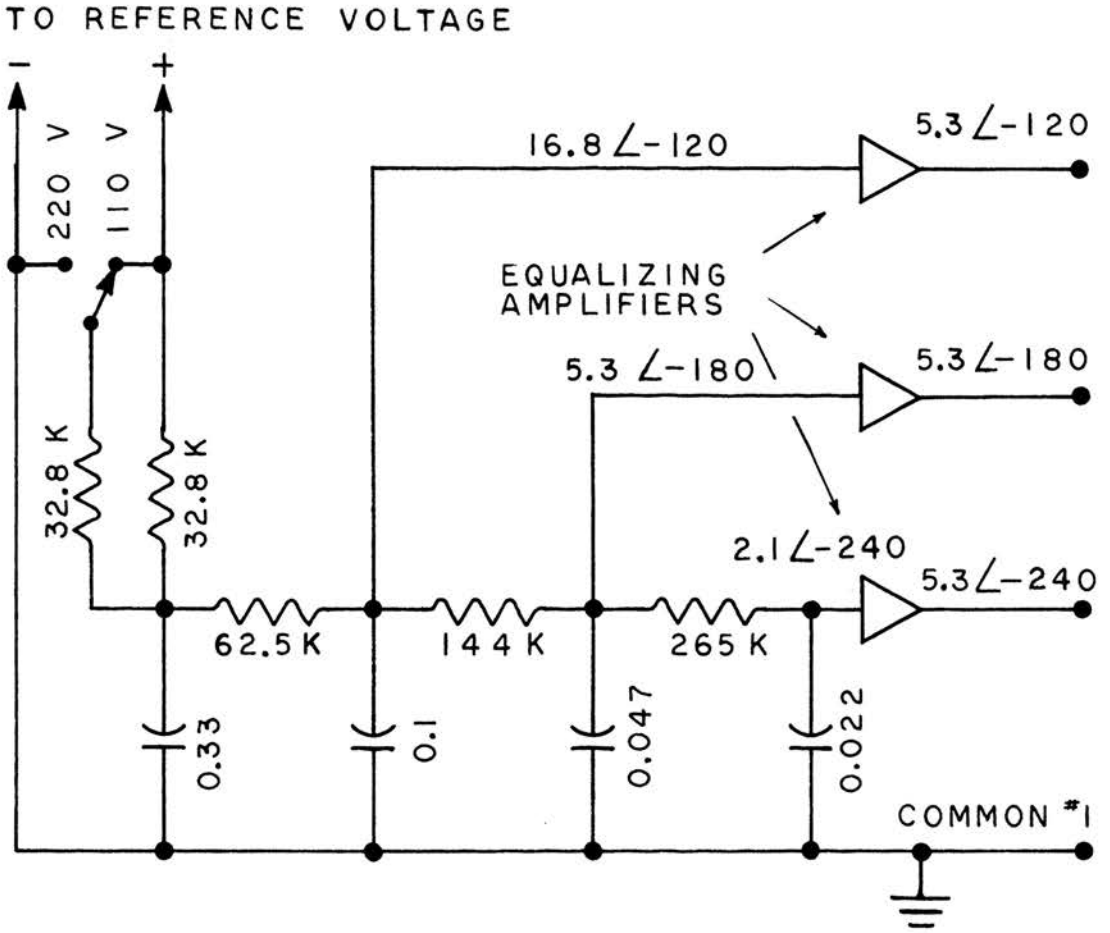
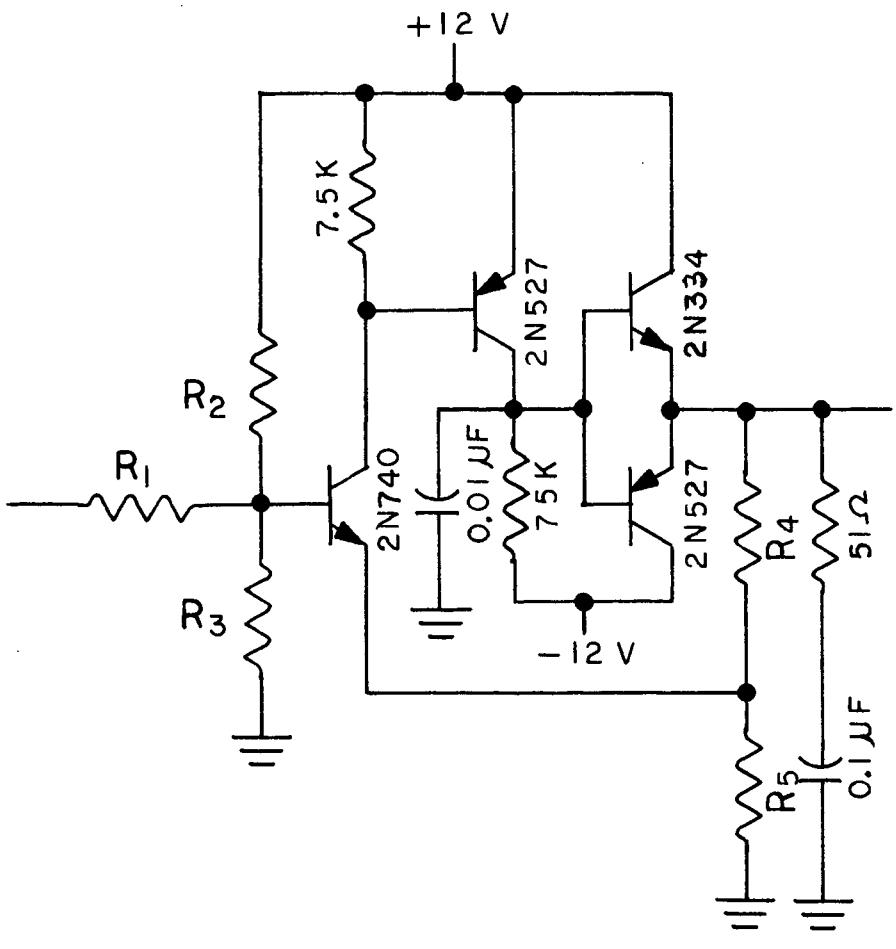


FIG. 27. SCHEMATIC DIAGRAM OF PHASE SHIFTER



RESISTORS $R_1 - R_5$ ARE SELECTED TO OBTAIN A 15 V P-P OUTPUT WITH NO DC COMPONENT AND AN INPUT IMPEDANCE OF ONE MEGOHM.

AMPLIFIER	R1	R2	R3	R4	R5
−120°	680K	∞	300K	0	3.6K
−180°	0	∞	1.1 MΩ	0	3.6K
−240°	0	6.8 MΩ	1.3 MΩ	2K	1.3K

FIG. 28. SCHEMATIC DIAGRAM OF PHASE-SHIFTER AMPLIFIERS

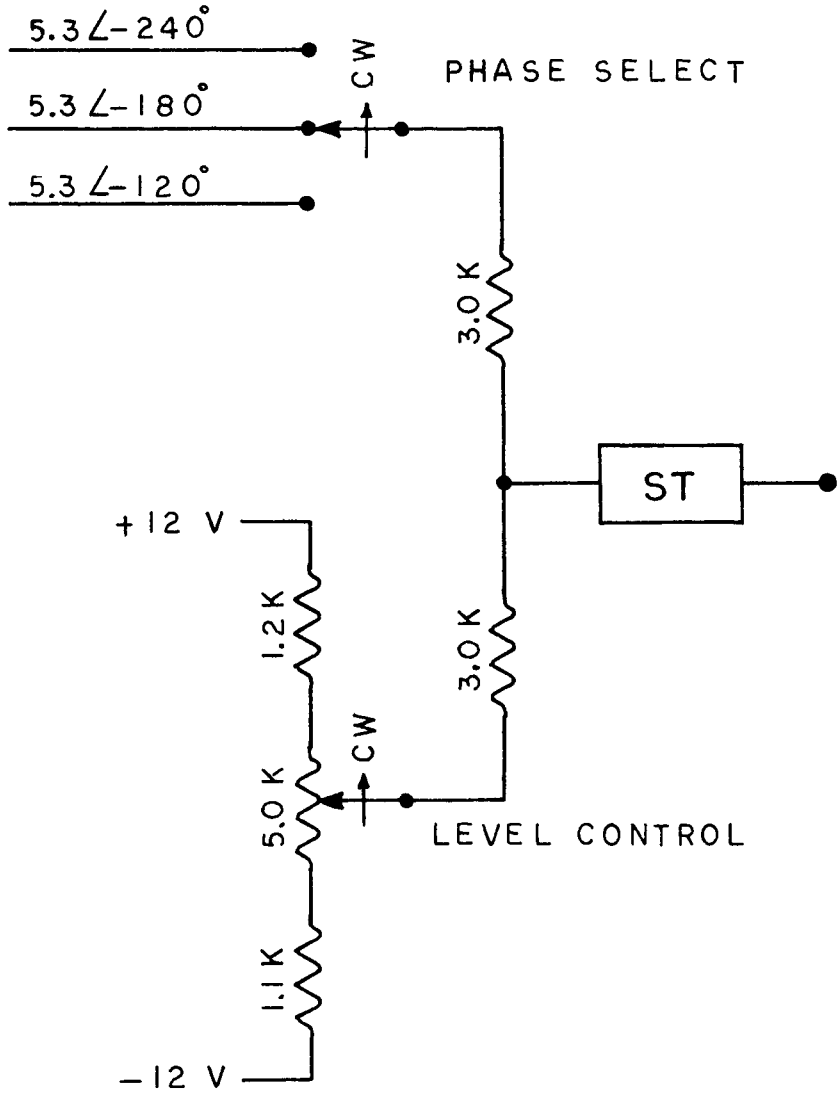


FIG. 29. SCHEMATIC DIAGRAM OF PHASE SELECT AND LEVEL CONTROLS

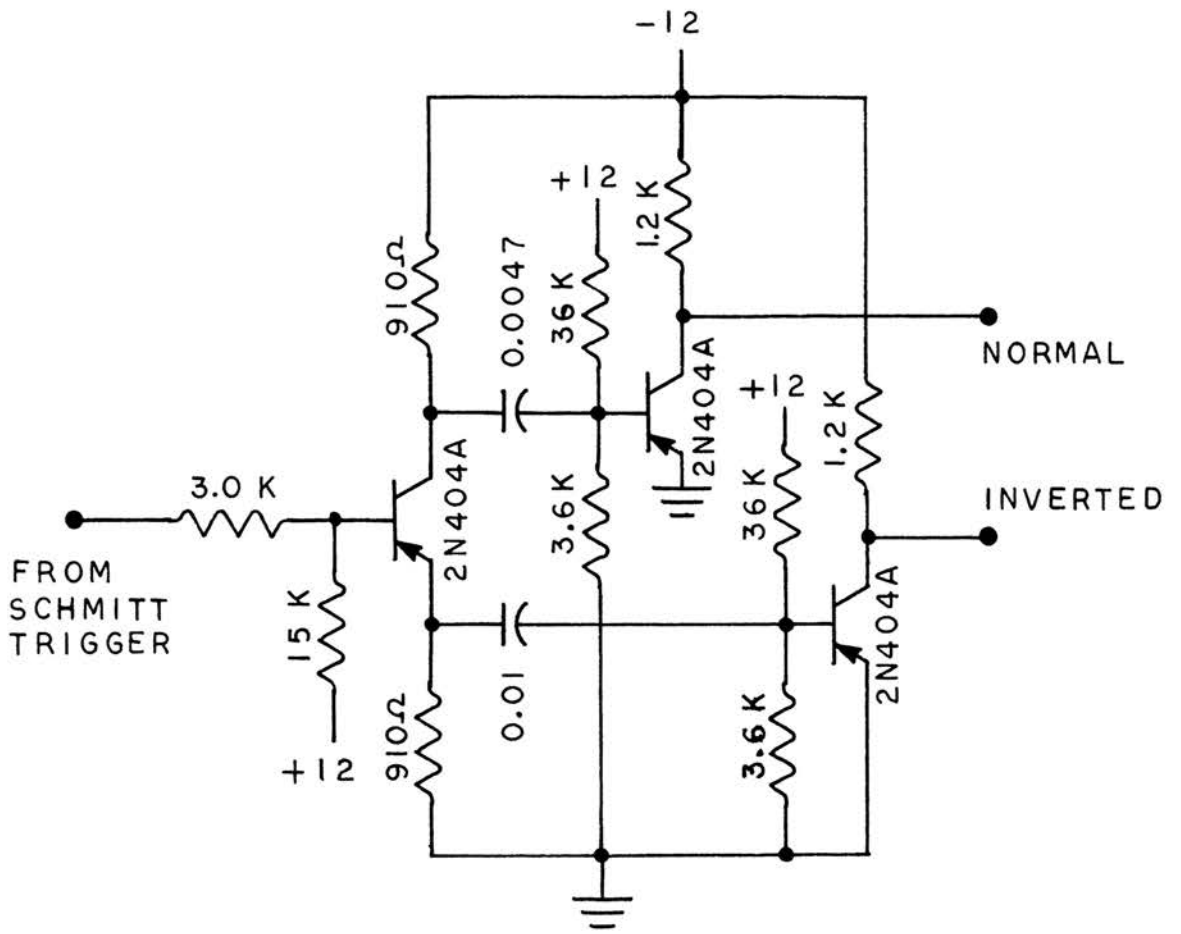


FIG. 30. SCHEMATIC DIAGRAM OF INTEGRATED DIFFERENTIATOR AND PHASE INVERTER

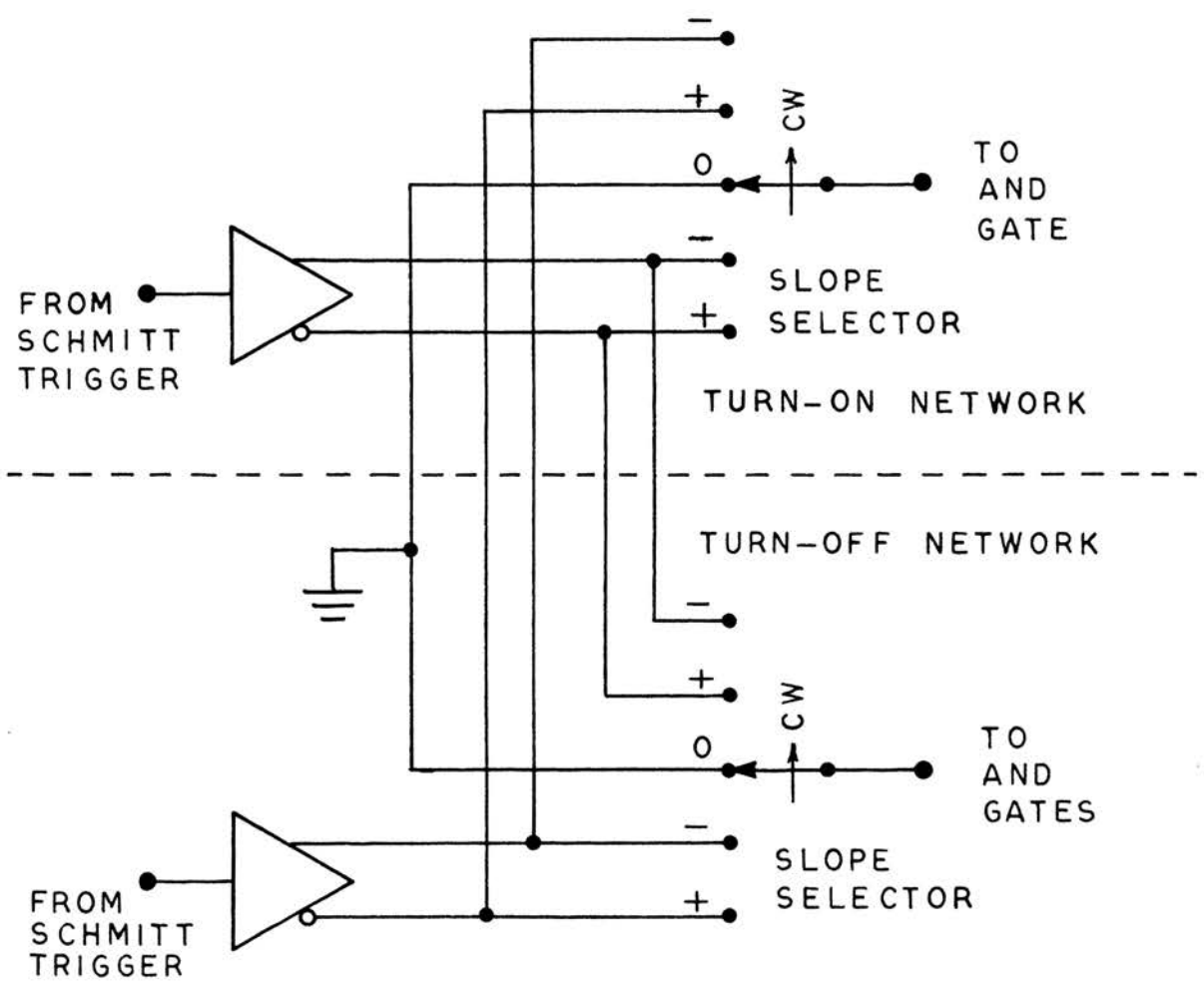


FIG. 31. SCHEMATIC DIAGRAM OF SLOPE SELECTORS

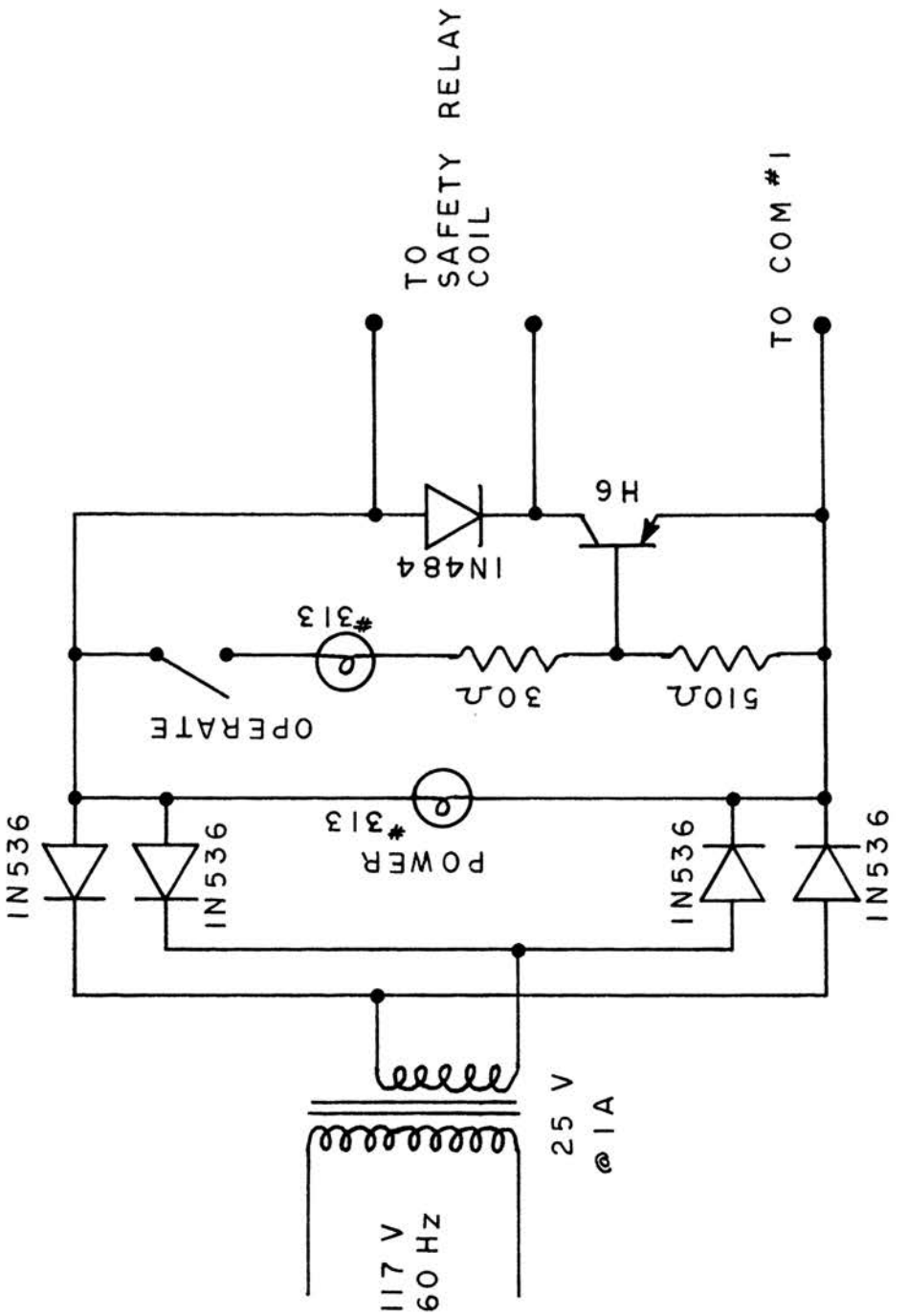


FIG. 32. SCHEMATIC DIAGRAM OF SAFETY RELAY ENERGIZER

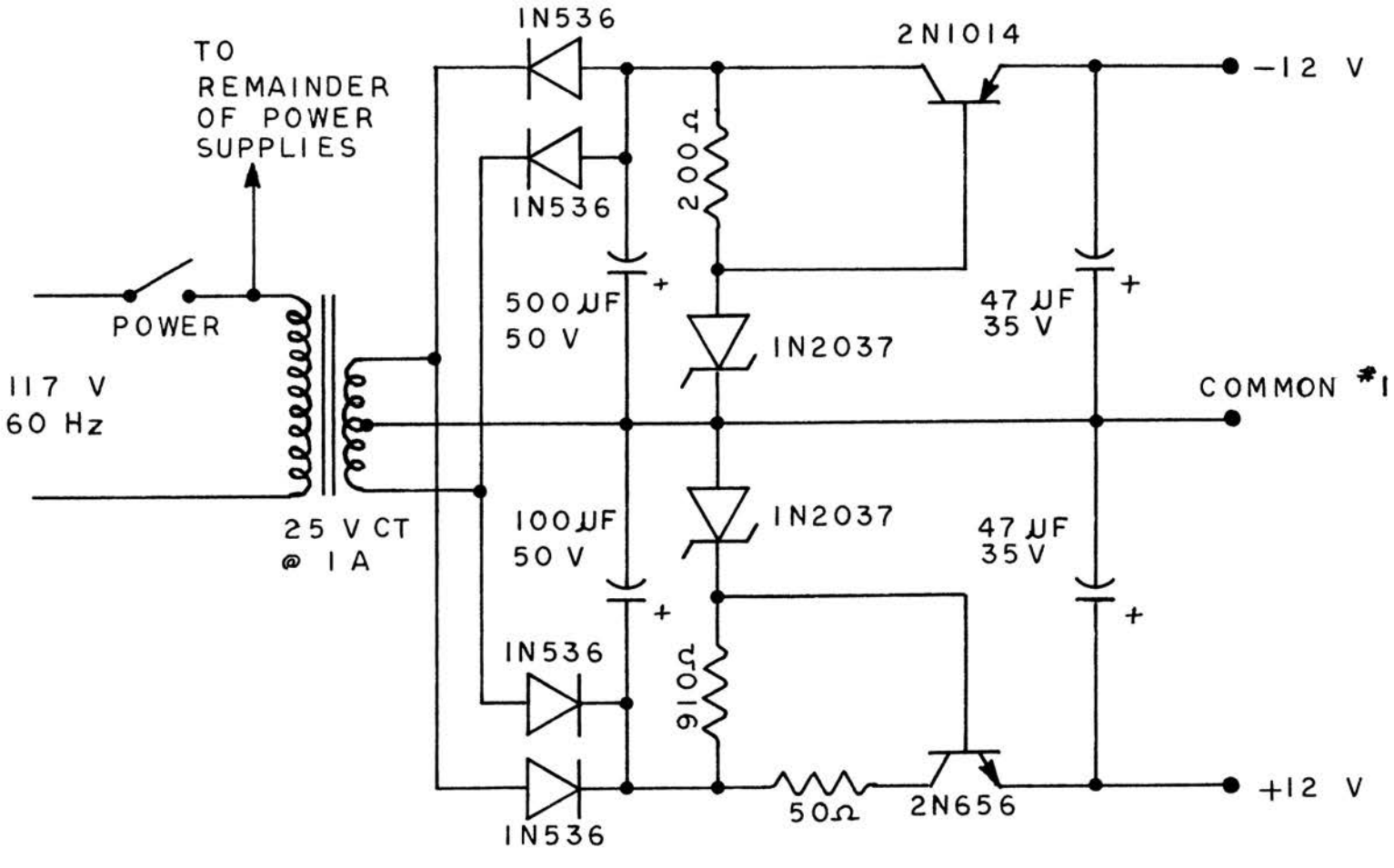


FIG. 33. SCHEMATIC DIAGRAM OF POWER SUPPLY NO. 1

APPENDIX C

Schematic Diagrams of Interface Unit - There are three power supply systems in the synchronous switch, all of which are electrically isolated from earth ground and from each other. Therefore, the symbol ⏚ shall be interpreted to mean signal ground and is the COMMON line of that power supply which energizes the circuits in question.

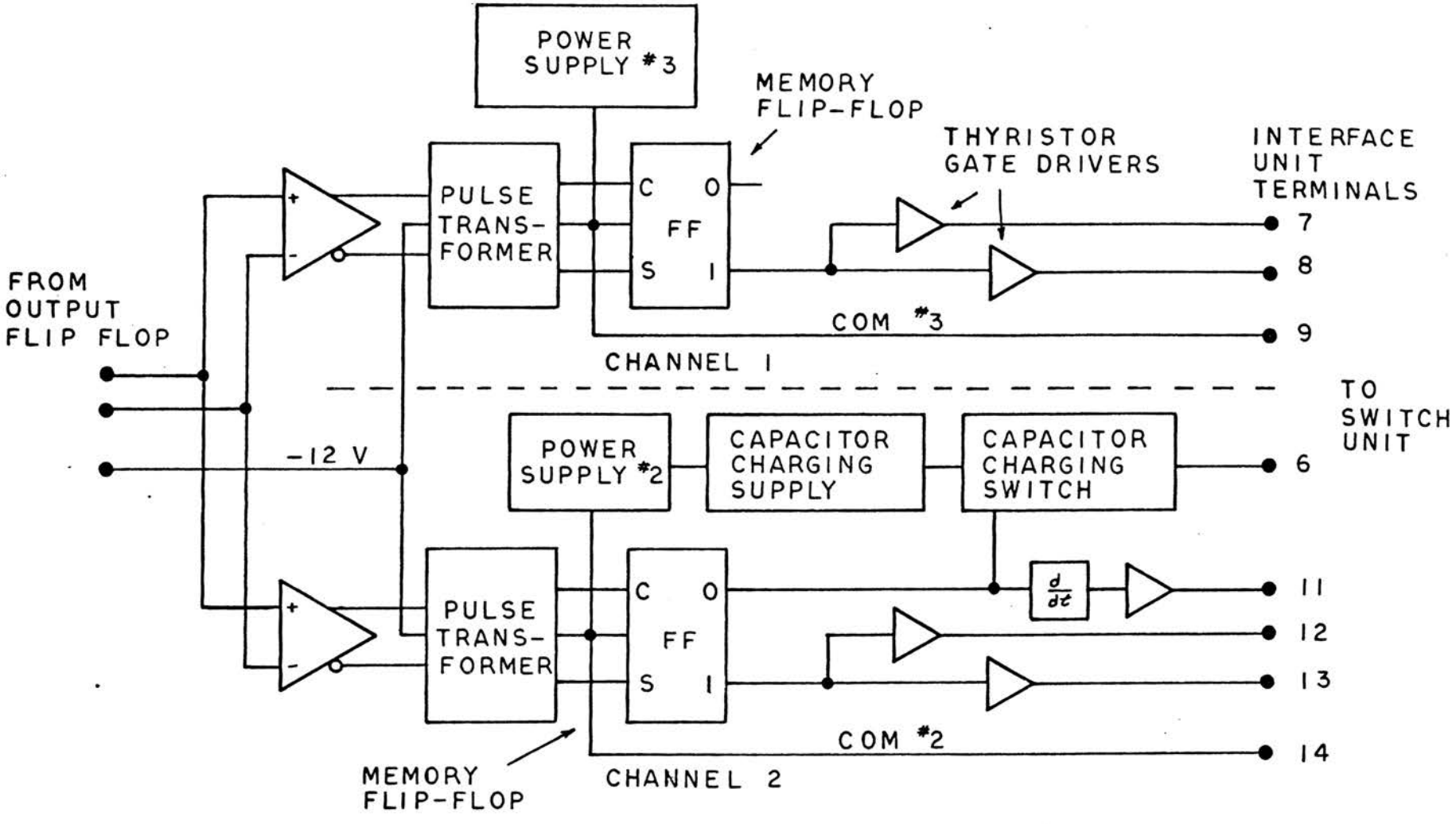
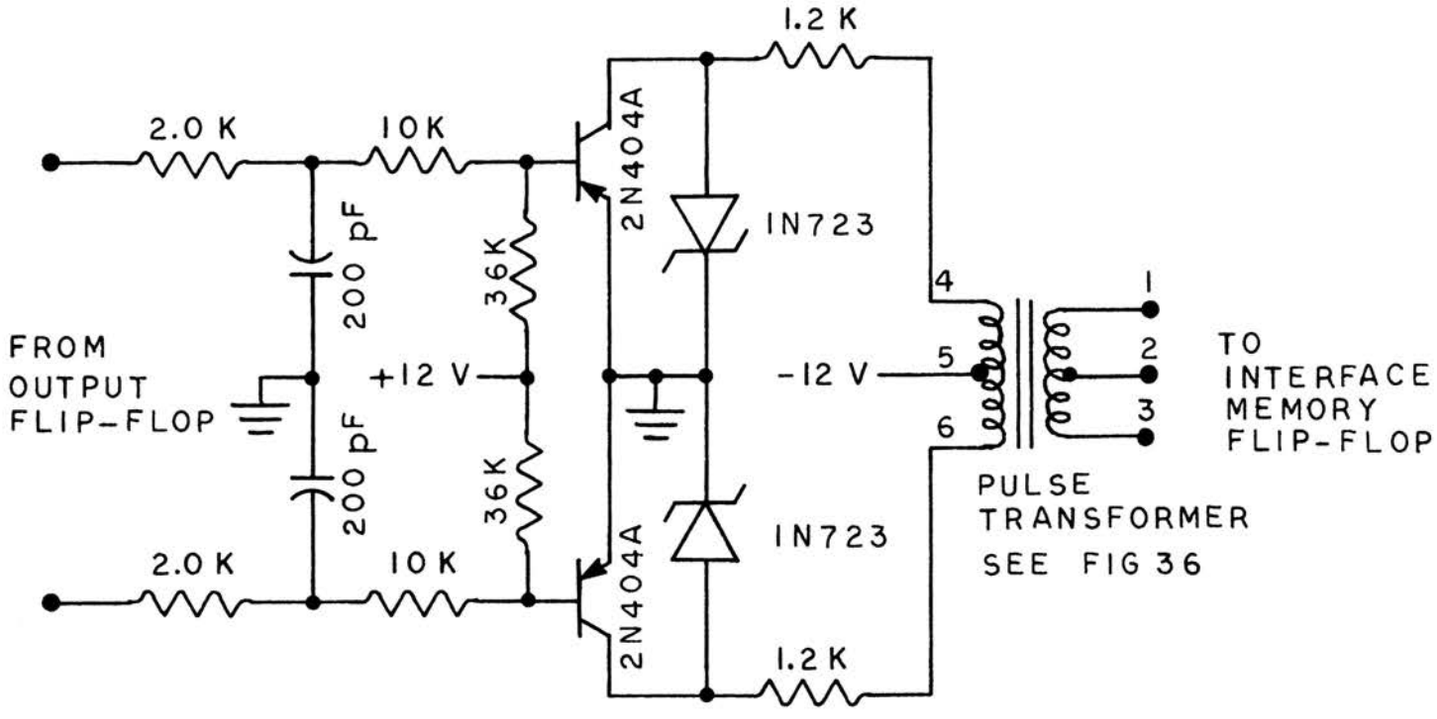
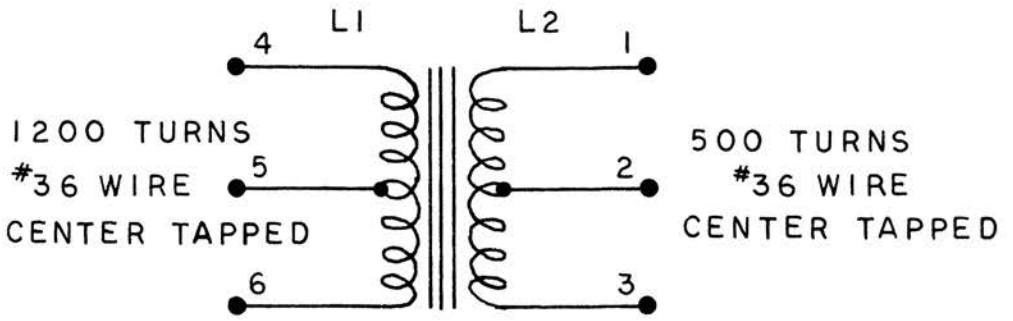


FIG. 34. BLOCK DIAGRAM OF INTERFACE UNIT



NOTE: THE SYMBOL ⏚ REFERS TO COMMON #1.

FIG. 35. SCHEMATIC DIAGRAM OF PULSE TRANSFORMER DRIVER



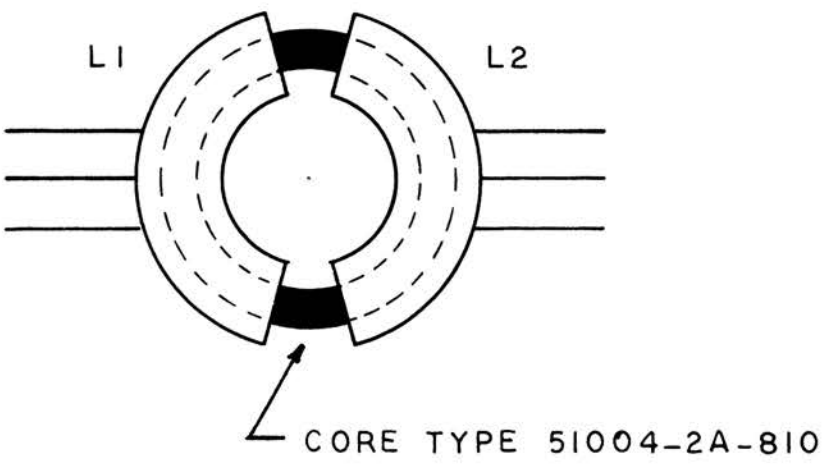


FIG. 36. DETAILS OF PULSE TRANSFORMERS

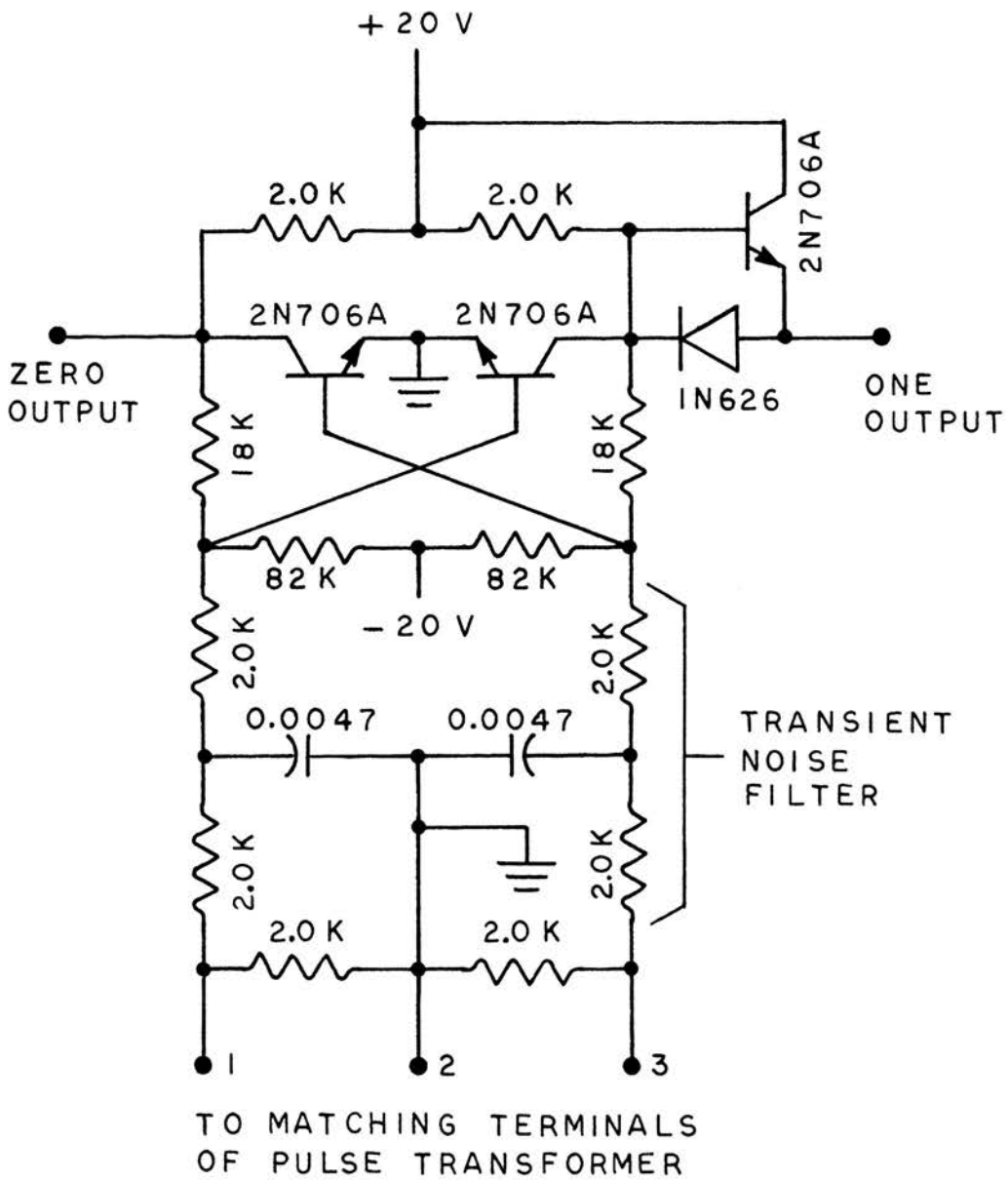


FIG. 37. SCHEMATIC DIAGRAM OF MEMORY FLIP-FLOP

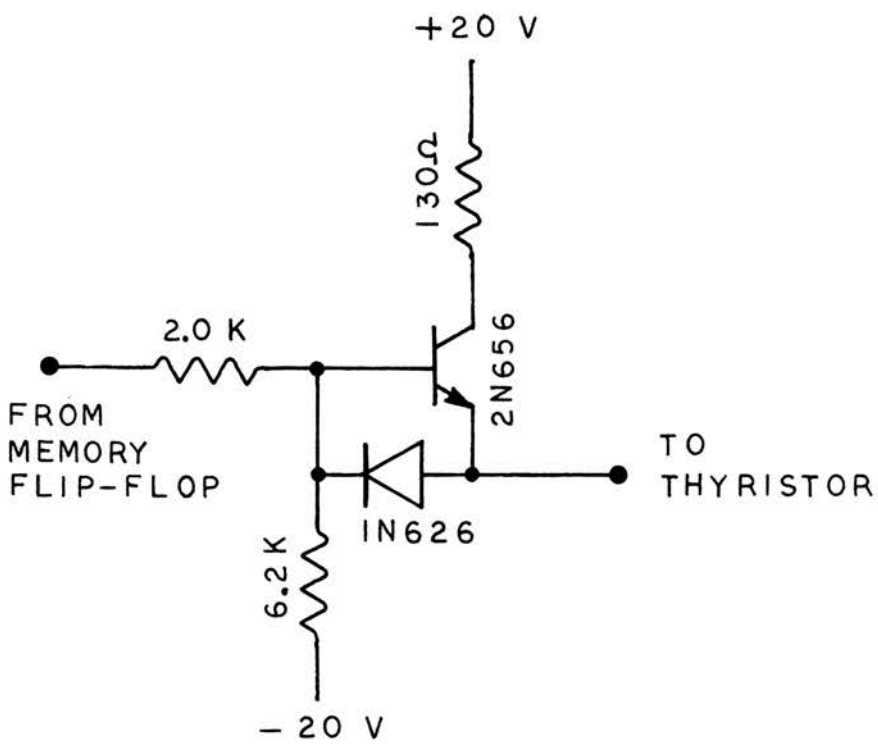


FIG. 38. SCHEMATIC DIAGRAM OF GATE DRIVER FOR THYRISTOR TYPE 2N688

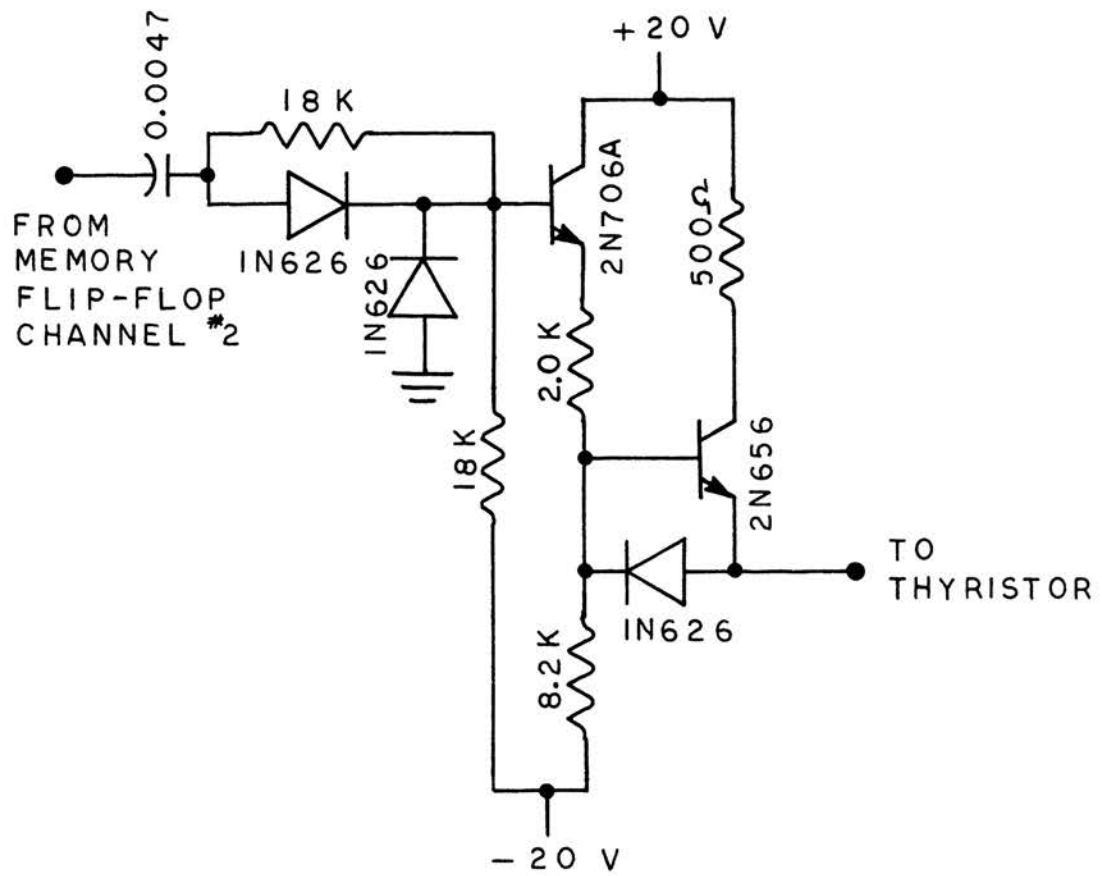


FIG. 39. SCHEMATIC DIAGRAM OF GATE DRIVER AND DIFFERENTIATOR FOR THYRISTOR 2N1771

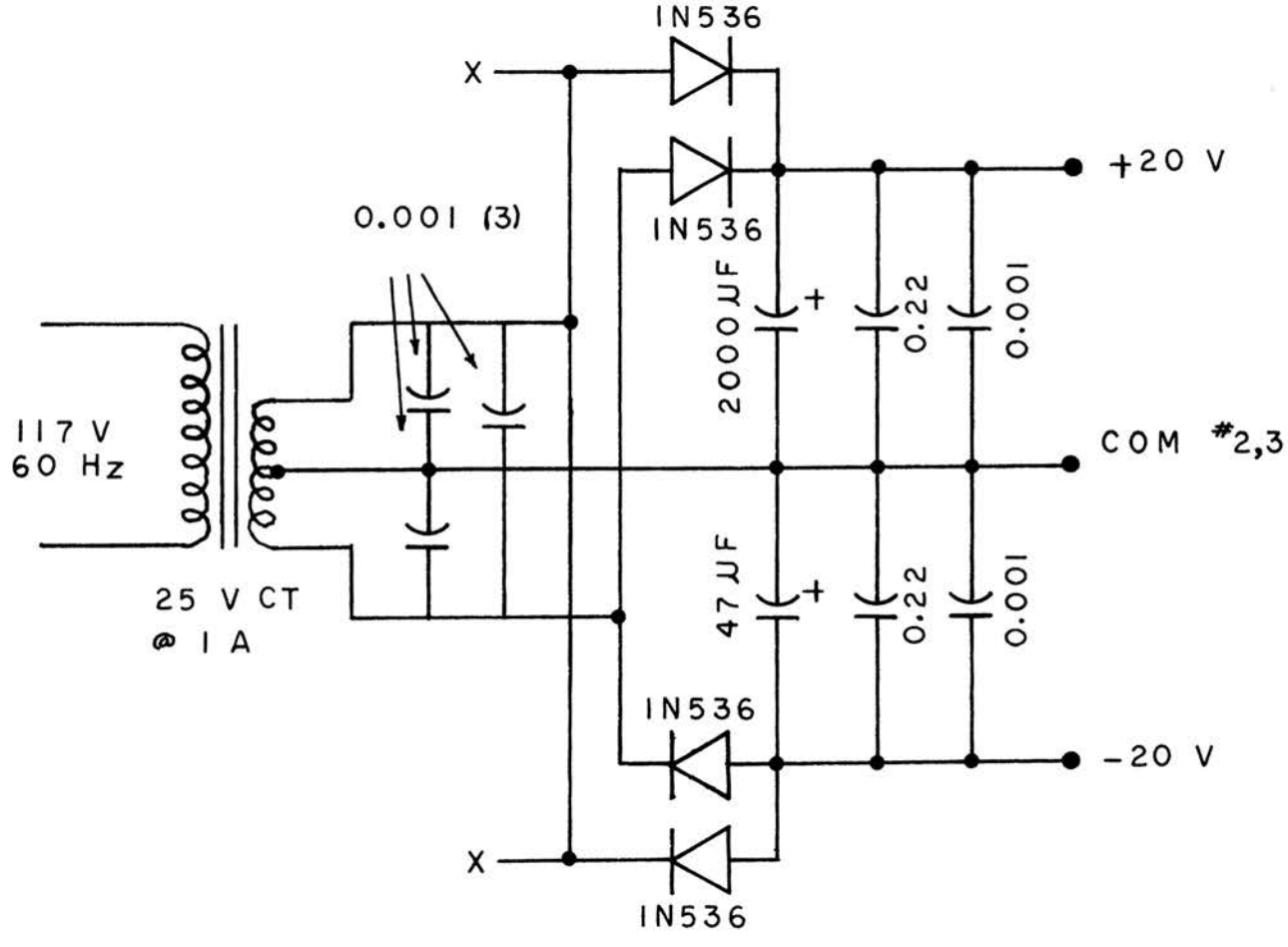


FIG. 40. SCHEMATIC DIAGRAM OF POWER SUPPLIES NO.'S 2 AND 3

APPENDIX D

Theory of Operation of Capacitor Charging Switch - Fig. 41 shows the circuit which charges the commutating capacitor in the thyristor switch circuit. The capacitor charging switch consists of a type 2N1490 transistor, the base of which is driven by a 2N656 transistor operated as an emitter follower. This results in low saturation voltage drop across the 2N1490, while maintaining reasonable input drive requirements.

The output of the memory flip-flop of Channel 2 indicates when the thyristors in the main switch circuit (Fig. 43) are conduction. The commutating capacitor is charged when these thyristors are in the conducting state. Thus, when the main switch is ON, a negative going signal is applied to the base of Q_2, by emitter follower Q_1, and Q_2 is switched off. The voltage at point A thus rises to +20 volts, causing 2N656 to conduct. The capacitor charging switch is then in the ON state.

A positive signal from the memory flip-flop causes Q_2 to saturate, the voltage at point A will be very close to zero. The 2N656 does not conduct under these conditions, and the capacitor charging switch is in the OFF state. Current is prevented from flowing back into the capacitor charging switch by the type 1N540 diode.

The type 1N483 diodes serve to protect the transistors from abnormal voltages.

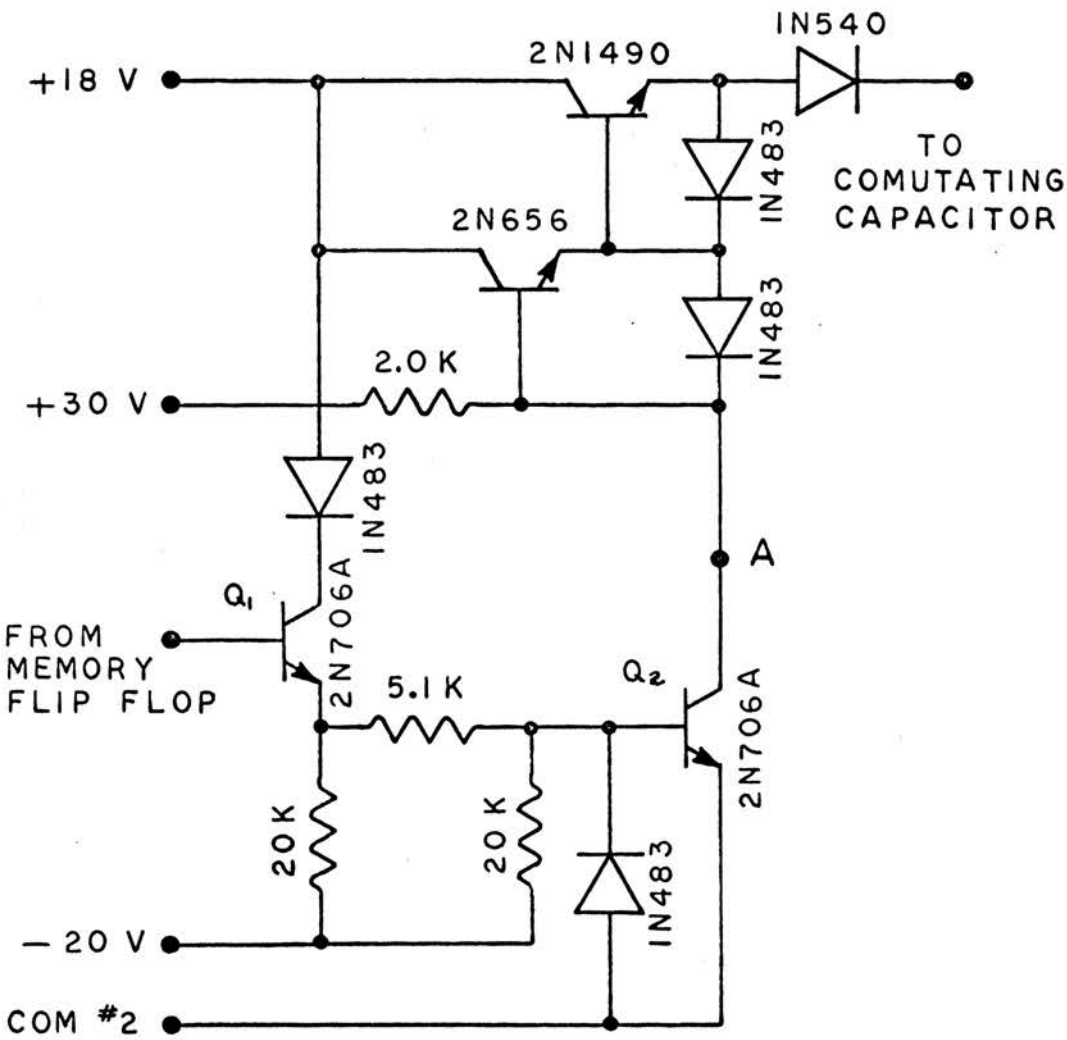


FIG. 41. SCHEMATIC DIAGRAM OF COMUTATING CAPACITOR CHARGING SWITCH

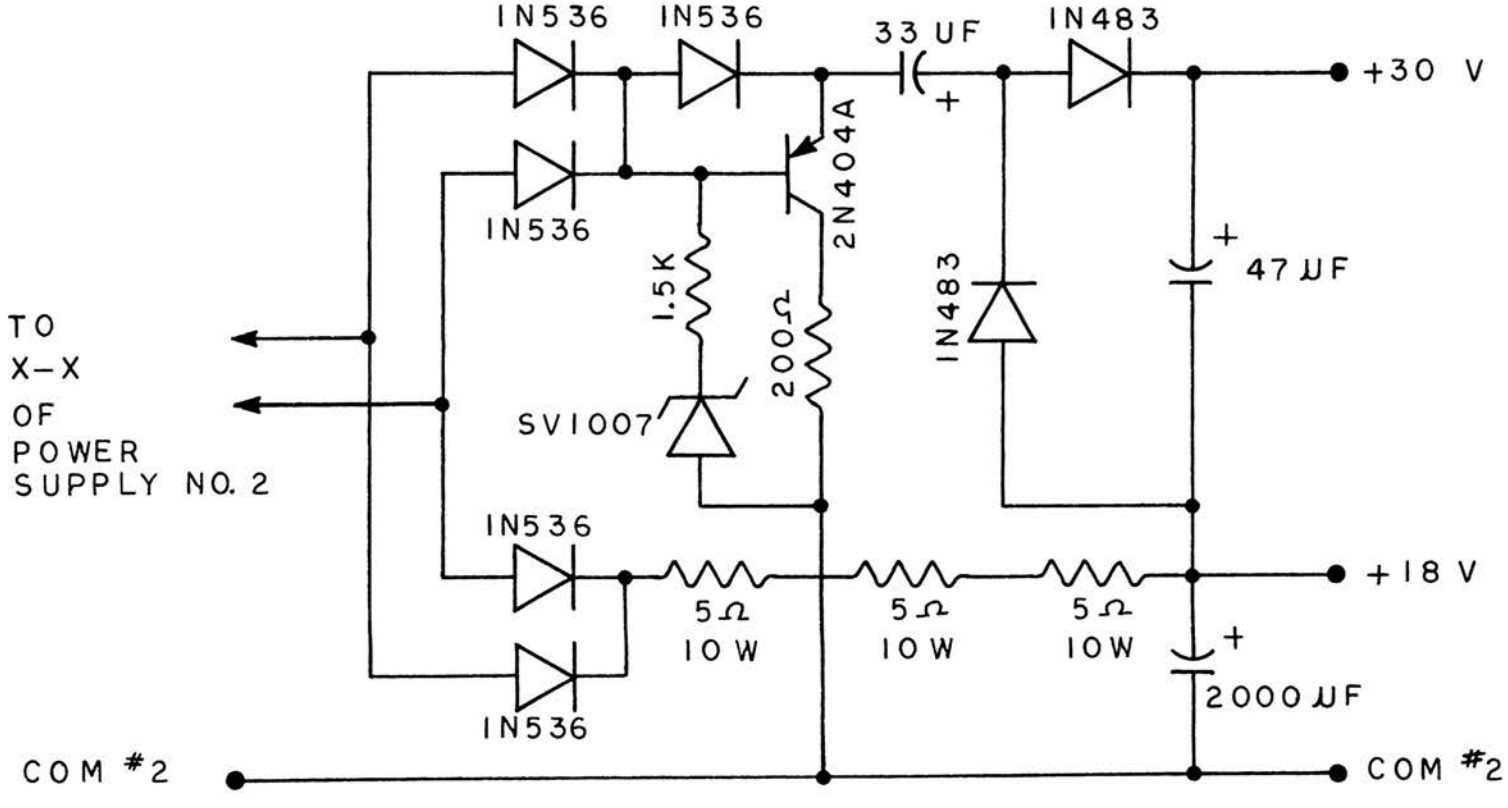
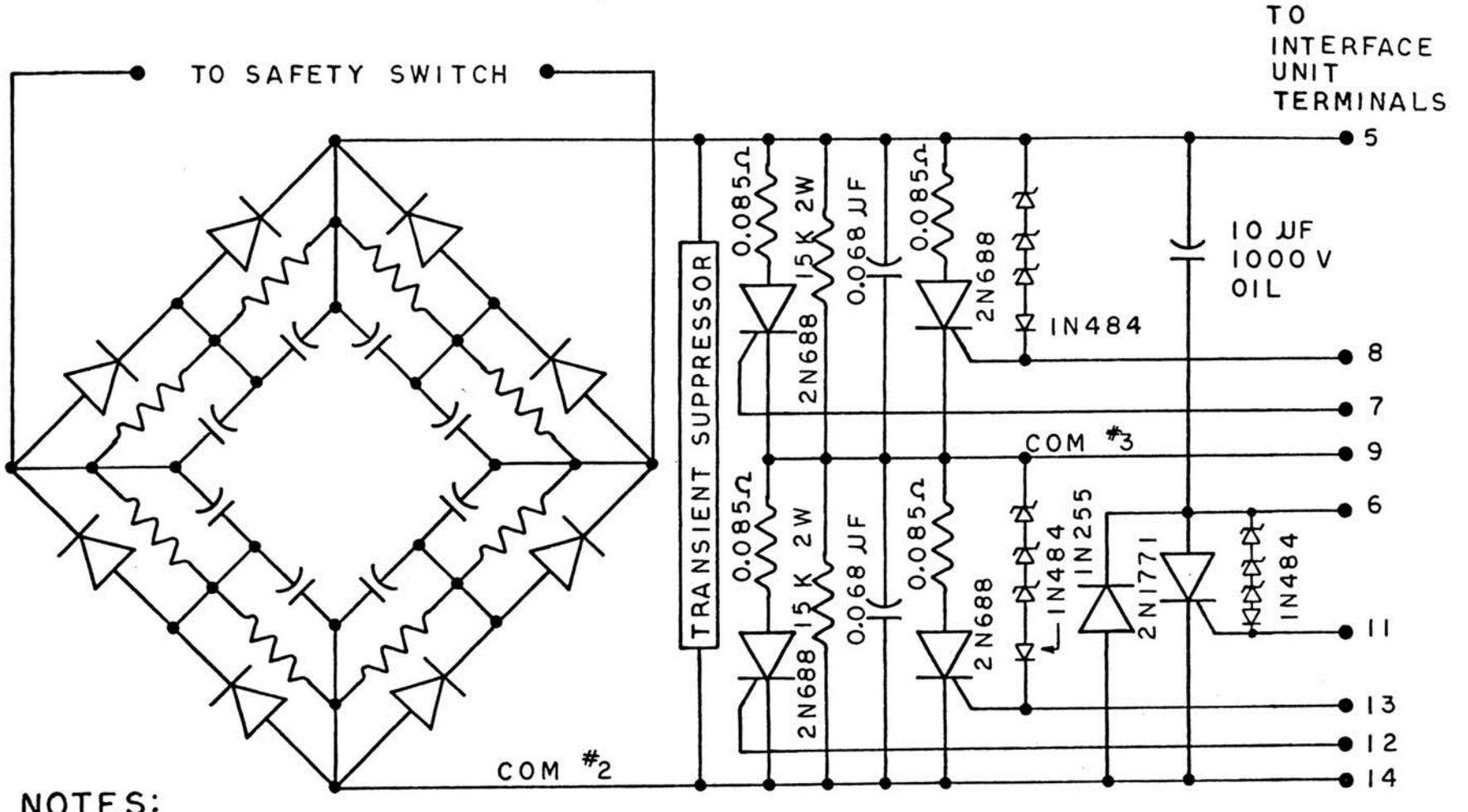


FIG. 42. SCHEMATIC DIAGRAM OF POWER SUPPLY FOR COMUTATING CAPACITOR CHARGING CIRCUIT

APPENDIX E

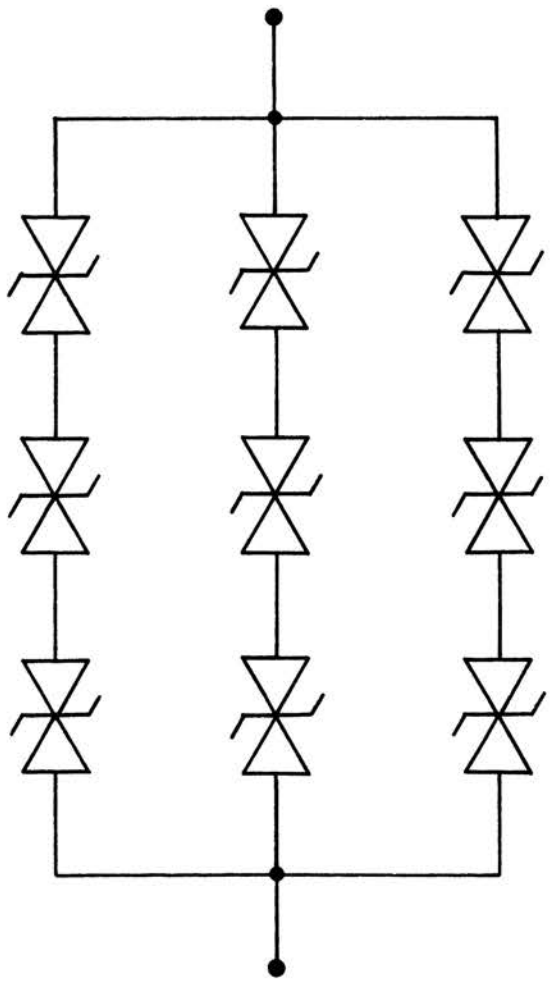
Schematic Diagrams of Switch Unit - There are three power supply systems in the synchronous switch, all of which are electrically isolated from earth ground and from each other. Therefore, the symbol ⏚ shall be interpreted to mean signal ground and is the COMMON line of that power supply which energizes the circuits in question.



NOTES:

1 ALL BRIDGEDIODES TYPE IN2159
2 ALL BRIDGE RESISTORS 51K 2W
3 ALL BRIDGE CAPACITORS 0.05 μF 600 V
4 ALL ZENOR DIODES TYPE IN3046

FIG. 43. SCHEMATIC DIAGRAM OF SWITCH UNIT



ALL UNITS THYRECTOR DIODES TYPE 6RS21SA3D3

FIG. 44. SCHEMATIC DIAGRAM OF TRANSIENT SUPPRESSOR

VITA

The author was born on December 13, 1941 in Nevada, Missouri. He graduated from Southeast High School of Kansas City, Missouri in 1959.

In the fall of that year he enrolled at the Missouri School of Mines and Metallurgy and received the Bachelor of Science degree in Electrical Engineering in the month of July, 1962.

Mr. Hall first registered as a graduate student in September, 1962 and completed the course work for a Master of Science degree in May, 1963. He has been employed by the U.S. Naval Ordnance Test Station since June, 1963.

The author is a member of Eta Kappa Nu, Kappa Mu Epsilon, and Phi Kappa Phi.