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Thin film techniques for the fabrication of nano-scale high energy density capacitors

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THIN FILM TECHNIQUES FOR THE FABRICATION OF NANO-SCALE HIGH ENERGY DENSITY CAPACITORS

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ABSTRACT

Dielectric thin films of either TiO_2 or $BaTiO_3$ were sputtered in O_2/Ar plasmas on Si wafers to thicknesses ranging from approximately 25 to 200 nm with patterned Ni or Pt electrodes sputtered in Ar plasmas at thicknesses from about 20 to 250 nm to form nano-capacitors. Statistical design of experiments (DOE) was used to determine the effects of the deposition power, plasma composition, and deposition temperature on the measured electrical properties of the nano-capacitors. Additional tests to determine the effects of the dielectric and electrode thickness on the measured dielectric responses of the devices were also undertaken. Characterization was performed with a combination of direct current (DC) and alternating current (AC) testing methods including AC impedance, coercive field and leakage current versus voltage, scanning electron microscopy, transmission electron microscopy (TEM), x-ray diffraction (XRD), x-ray photoelectron spectroscopy, focused ion beam microscopy, and atomic force microscopy.

The dielectric properties were found to depend on complex interactions of the process variables that could be modeled using statistical software. The permittivity was found to range from 100 to 10,000 with losses between 0.013 and 0.570. The resistance at 1 V DC varied from approximately 1.5 to 360 GΩ, and either a ferroelectric or paraelectric hysteretic response was observed for all specimens tested. Chemical analyses showed the films to be oxygen rich, while XRD and TEM data indicated the $BaTiO_3$ was amorphous. The electrical, chemical, and microstructural properties were found to depend on the sputtering conditions of the $BaTiO_3$, dielectric thickness, electrode material choice, and the electrode thickness. Collectively, the results indicated that the properties of nanometer thick dielectric and electrode materials have a significant impact on the measured electrical properties.

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Introduction

1. General Background

Of the three most common passive components in electronic circuitry, resistors, capacitors, and inductors, it is the capacitor that generally dominates the majority of components and printed circuit board space. As an example, the Nokia 6161 cell phone has a 40 cm^2 circuit board with 15 integrated circuits (ICs), 149 resistors, 24 inductors, and 232 capacitors [1]. The capacitors range in value from 1 to 10 nF. In addition to stand alone devices that are attached separately to complete a circuit board, capacitors are also integrated into standard IC fabrication procedures to produce gate circuitry [2-5], dynamic random access memory (DRAM) [6-10], microwave electronics [6-9, 11], and general integrated passives [12-14]. For DRAM chips at the 1 Gbit level, capacitors are needed with lateral dimensions in the 0.13 μm range with thicknesses between 5 and 30 nm [10]. On this front, Motorola, Inc. appears to be leading the commercial field with integrated resistors and capacitors in many of its newer cell phones [1]. Several Japanese companies are also continuing this trend, and are beginning to introduce products that take advantage of the integrated passives approach. In commercial research, DuPont is developing processes that show potential to produce integrated passives with over 100 nF/cm^2 capacitance, which would be high enough to replace many of the discrete capacitors that currently have to be soldered onto a circuit board [1, 15].

Driving this trend toward integrated passives is the continued development of thin ceramic films with thicknesses between 0.5 and 2 μm [9]. As these thicknesses are on the same scale as many microstructural characteristics such grain size, ferroelectric domains, and even the electrode interfaces [10, 15], it can become difficult to ensure property uniformity on a local scale when the device size also continues to decrease. The favored commercial fabrication technique of ceramic capacitors, tape-casting, has advanced over the past 10 years to allow the reliable fabrication of 0.8 μm thick dielectrics (0.5 μm thickness on research scales), but has not been able to definitively show that it will be capable of extending its use to thicknesses to 0.2 μm and below [16]. This limitation has opened the way for a variety of other thin film deposition methods to be introduced to the field of capacitor research and development.

As dielectric films continue to decrease in thickness due to advances in chemical vapor deposition, physical vapor deposition, and sol-gel processing it becomes increasingly important to control the microstructure to ensure property uniformity. As films become thinner both intrinsic (i.e. directional response of a single ferroelectric domain) and extrinsic (i.e. phase boundaries, defect densities, etc.) properties become more pronounced [10]. Intrinsic size effects result in a ferroelectric transition shift to lower temperatures, a broadening of the temperature dependence of the permittivity (e.g. the development of a Curie region as opposed to a Curie peak), and a drop in the peak permittivity. Extrinsic size effects have been observed to account for 60% to 70% of the dielectric property values in some of the common perovskite materials, and vary depending on the deposition method and chosen materials.

The current challenge for thin film capacitors is the fabrication of devices that exhibit high capacitance, possess high voltage capabilities, and have both high electrical stability and high temperature capability [9, 17] all while retaining a compact size and using materials and deposition techniques that are compatible with the materials and processes already in use in standard IC fabrication facilities [1]. For portable power devices (i.e. secondary power supplies, electric vehicles, or battery replacements), capacitors also need to exhibit long life cycles (>100,000 cycles), short charging times in ms to ns range, be safe for consumer handling (simple, robust design), and have a high power density [18]. For any capacitor technology to be accepted for commercial application it must exhibit:

1. High permittivity (maximized based on material to result in an associated high capacitance density) [17]
2. High breakdown strength (greater than $1x10^6$ V/cm for maximum power density) [17]
3. Low dielectric loss tangent ($\tan \delta = d$ needs to be at least less than 0.05) [16]
4. Low leakage current density (<1 $\mu A/cm^2$ at 10V) [17]
5. Low failure rates (2.4 failures or less in 10^9 component hours) [19]
6. Minimal temperature variance (± 15% or less between 55°C and 125°C) [19]

2. Thin Film Capacitors

2.1. Capacitor Designs

Three capacitor designs are currently used in the electronic industry: in-plane or single layer, electrolytic, and multi-layer capacitors (MLCs). Each design's capacitance can be calculated using:

$$C = \varepsilon_o \varepsilon_r \left({}^{A}/_{d}\right) \quad <1>$$

Where ε_o is the permittivity of free space ($8.854 \times 10^{-12}\ {}^{F}/_{m}$), ε_r is the permittivity of the dielectric material (also referred to as the dielectric constant, k), A is the interaction area of the electrodes (m^2), and d is the distance between the electrodes (m). In-plane capacitors attempt to maximize the capacitance by using large permittivity dielectrics, minimizing layer thicknesses, and increasing the electrode area by rolling the structure into a cylindrical configuration. This simple design allows easy manufacturing, but limits the maximum possible capacitance density by not taking advantage of a 3-dimensional construction methodology. Electrolytic devices maximize the capacitance by significantly increasing the electrode area with porous electrodes submerged within an electrolyte. The drawbacks to electrolytic capacitors are: [1)] the distance between the electrodes is set by the conductivity of the electrolyte and tends to be larger than is possible with a solid dielectric, and [2)] the use of a liquid electrolyte requires hermetic sealing of the capacitor which precludes the use as an integrated device [20].

MLCs maximize device capacitance by using high permittivity dielectrics (maximizing ε_r), minimizing the dielectric thickness (d), and increasing the electrode area (A) by alternating stacks of anode, dielectric, cathode, dielectric, anode, etc. Of the three designs discussed, MLCs are generally able to produce the highest capacitance density due to the use of a 3-dimensional structure that is not inherently limited by dielectric thickness [21]. As such, MLCs are the most popular for use in the electronics industry [19, 21, 22] with an estimated 10^{12} units made annually as of 2006 [16]. At present, most commercial MLCs are prepared by tape casting using dispersions of submicron ceramic powders with screen printed metal electrodes that are laminated, co-fired, and terminated with metallic paint [16]. Tape casting, however, has been found to be impractical and not

cost efficient for the fabrication of devices with layer thicknesses on the nano-meter scale [1, 16].

Thin film technology allows the optimization of the MLC design to be taken even further with the ability to reliably decrease the dielectric thicknesses into the nanometer range, thus surpassing traditional tape casting technology. As this thickness minimization occurs, multiple benefits in addition to an increase in capacitance are likely to be seen. Since the average AC current path is shorter with thinner films, a smaller series inductance is likely to be measured making a more efficient capacitor with a higher self-resonant frequency [14, 23]. A smaller active area also translates to shorter metal lengths, which in turn gives a lower series resistance, and subsequently lower power consumption/loss. On the other hand, as the device areas approach the same size scale as microstructural features (i.e. grain size and/or domain size), the devices are likely to be more susceptible to fractional variations in the measured capacitance [14].

Thin film technologies also allow the opportunity to create complex electrode patterns, such as micro-scale fractal patterns, that are not feasible with screen printing technology. By exploiting not only the vertical field components (e.g. minimizing the thickness) but also the lateral, or in-plane, electric field components it is possible to increase the capacitance density even further than with a standard MLC approach [14]. The capacitance of a device with patterned electrodes can be calculated as:

$$C_{total} = C_x + C_y + C_z \qquad <2>$$

$$= \varepsilon_o \varepsilon_r \left[\left(L_{x,min}(L_{x,min} + W_{x,min}) \right)^{-1} + \left(L_{y,min}(L_{y,min} + W_{y,min}) \right)^{-1} + \left(t_{ox}(t_{ox} + t_{metal}) \right)^{-1} \right]$$

where $L_{x,min}$ and $L_{y,min}$ are the minimum in-plane, lateral spacing between the electrodes, $W_{x,min}$ and $W_{y,min}$ are the in-plane widths of the metal electrodes, and t_{ox} and t_{metal} are the dielectric and metal thicknesses, respectively. Comparison of theoretical 3-dimensional structures to a standard MLC design has been done by Aparicio [14]. According to this work, with a dielectric and electrode thickness of 800 nm, the minimum feature sizes (L and W) needed to make complex electrodes more efficient than a standard parallel plate design is between 0.8 μm and 1.0 μm depending on the electrode design used. These feature sizes are well within the capability of standard micro-fabrication facilities, and

show promise for further increasing the maximum capacitance density achievable with thin film technologies.

2.2. Deposition Techniques

A wide variety of techniques have been investigated for the deposition of thin ceramic films including chemical vapor deposition (CVD), sol-gel, sputtering, pulsed laser deposition, among several others. Each process has a set of associated advantages and disadvantages, and any process must be chosen particularly with the disadvantages in mind. Observed size effects associated with varying the dielectric thickness are process dependent. Different deposition processes as well as different processing conditions within each process category are likely to result in different properties in the material adjacent to the electrodes, which in turn contributes to the scatter seen in the experimentally measured size effects on the dielectric properties [10]. This is in addition to the differences with the microstructure (e.g. density, grain size, morphology, etc.) of the deposited film from different processes. Based on the literature, it appears that the size effects are controlled more by processing rather than any intrinsic limits on material stability.

Table I gives a brief summary of the more popular thin film deposition techniques and some of the advantages and disadvantages of each. All of the processes have been utilized with success in multiple literature sources. Therefore, the choice in deposition technique must be made with a certain set of constraints. For this research a low deposition temperature was highly desirable due to the prevalence of temperature related issues resulting in cracking or delamination of films during cooling [24, 25]. A process was also desirable that exhibited a large degree of control over film stoichiometry, thickness, uniformity, and step coverage.

Of the above techniques the majority of research efforts have used CVD and sputtering technologies. CVD techniques, in particular metal-organic CVD (MOCVD), tend to provide excellent composition control with good potential for film homogeneity and conformal coatings of complicated topographies [26]. These benefits have resulted in CVD being regarded as producing the “highest quality” dielectric films [27, 28]. Unfortunately, CVD methodologies tend to require costly instrumentation and materials

and are known for complex process schedules [27, 28]. CVD is also typically performed in a batch process, making the technology less favored for mass production of devices.

Table I. Thin film deposition techniques with associated advantages and disadvantages

Deposition Technique	**Advantages**	**Disadvantages**
Sputtering	Controllable composition Thin, conformal coatings Low deposition temperatures	Many process parameters Requires vacuum Non-selective coating
Chemical Vapor Deposition	Selective coating Low temperatures possible Multiple assisted technologies	Exotic chemicals Thick, rough coatings Limited coating chemistries
Sol-Gel	Conformal coatings Ease of processing	High temperatures Multiple temperature cycles
Atomic Layer Deposition	Extremely thin layers Stoichiometric films Conformal coating	Slow deposition Expensive equipment

Comparatively, sputtering requires substantially more simplified equipment [27], and the process schedule is generally less complex [28]. The technique is also capable of producing thin ceramic films with comparable properties to those derived from CVD methods [27, 28] and are generally more reproducible [9, 11, 29]. The process variables of sputtering allow superior residual stress control by modifying the interaction of the energetic particles bombarding the surface of the substrate [11], which is effective for avoiding stress-induced mechanical peeling and thus increasing interlayer adhesion between the film and substrate as well as between individual layers of a stacked structure [11, 30]. Sputtering can also be performed at room temperature, potentially allowing the avoidance of high temperatures [3, 5, 31, 32]. Sputtering is commonly used in most IC

fabrication facilities resulting in a high potential for mass production, despite being a batch process, that is not seen with most of the other deposition techniques [11].

3. General Trends in the Literature for Sputtered Capacitors

All of the influences on electrical behavior can be modified and, ultimately, engineered using processing conditions. The processing parameters that can be readily altered during sputtering are the percent O_2 in the plasma, deposition temperature, plasma pressure, and RF power. In addition, the post deposition annealing temperature, if such an operation were found to be favorable, also directly impacts the electrical performance (Table II). By decreasing the percent O_2 in an Ar plasma during sputtering the literature shows a decrease in permittivity [12, 33, 34], increase in conductivity [3], increase in loss [12, 35], decrease in crystallinity [34], and a decrease in test temperature and test frequency sensitivities [33]. By decreasing the deposition temperature the crystallinity of the film in decreased [4, 5, 31, 32, 36], the permittivity is decreased [3, 5, 25, 31, 32, 37-40], the loss is decreased [31, 32, 37], and the breakdown strength is decreased [25]. Increasing the total pressure during sputtering leads to an increase in leakage current [41], can modify the crystallinity depending on the level of pressure (as previously discussed) [42], increase residual stress [11], increase stoichiometry of both the oxygen and metallic species in the deposited film [42], and decrease sensitivity to the target-to-substrate angle [42]. An increase in the RF power used during deposition increases the permittivity [43], decreases residual stress [44], and reduces leakage current [41]. An increasing annealing temperature tends to result in an increasing permittivity [9, 40, 43], increasing loss [9, 13, 44], and decreasing conductivity [9]. The effects of the annealing temperature have been related to the crystallization temperature by Thayer et al [13], who found that an annealing temperature well below that of the crystallization temperature only affected an increase in loss. Annealing between 50°C and 100°C below the crystallization temperature improved the interface characteristics, and annealing above the crystallization temperature gave no improvement over the lower temperature anneals.

Table II. Impact on capacitor electrical properties by process variables during sputtering

Process Variable	**Impact on Electrical Properties**
↓ $\%O_2$	↑ conductivity, loss
	↓ permittivity, crystallinity, temperature and frequency sensitivity
↓ T_{dep}	↑ residual stress
	↓ crystallinity, permittivity, loss, breakdown strength
↑ P_{total}	↑ leakage current, residual stress, stoichiometry
	↓ sensitivity to target to substrate angle
	(can modify crystallinity depending on pressure regime)
↑ RF Power	↑ permittivity
	↓ residual stress, leakage current
↑ T_{anneal}	↑ permittivity, loss
	↓ conductivity (related to crystallization temperature by Thayer et al [13])

In addition to processing variables, the electrical performance has also been linked to test conditions. Three of the most important testing factors in the literature have been temperature, testing frequency, and the atmosphere under which testing occurred. Most $BaTiO_3$ films in the literature have displayed a standard Curie-Weiss behavior with Curie-Weiss temperatures between 400K and 470K [10, 12, 34]. Shifts in the Curie-Weiss temperatures have been linked to a reduced polarizability due to Ti non-stoichiometry and the presence of biaxial mechanical stresses within the films [12, 34]. In addition to test temperature, the atmosphere in the immediate vicinity of the device under test has also been shown to affect the electrical performance. The two reported atmospheres that significantly degrade the electrical properties are reducing atmospheres (i.e. vacuum, pure Ar, etc.) and high humidity atmospheres. Long exposure to a reducing atmosphere at elevated temperatures results in a decreased resistivity and poor reliability throughout life testing [45]. Likewise, high levels of humidity degrade the electrical performance of thin films. The A sites in perovskite oxides, such as the Ba site in $BaTiO_3$, are susceptible to humidity [46]. At high humidity, liquid water will condense

in pinholes and allow electrolytic conduction to take place. The results of Agarwal et al [46] with (Ba,Sr)TiO_3 show that increasing the relative humidity both decreases the permittivity (by as much as a factor of 10) and resistance (by two orders of magnitude) of the films.

4. Chosen Research Directions

Based on the above discussions and the available literature, it was decided that sputtering would be used to deposit MLCs. Given the controllability of sputtering, this deposition technique is the most likely candidate capable of resulting in the desired dielectric chemistry with the microstructural and morphological characteristics necessary to make viable MLC devices. Barium titanate was chosen as the dielectric material due to its potential for high permittivity (greater than 5,000 possible) and low loss values (less than 0.05), as well as its prevalence in the literature showing it to be a favored material for passive devices. In order to prepare for the use of a complex ternary system, TiO_2 was first studied to gain a basic understanding of the effect of various processing parameters due to its prevalence in the literature, and the dielectric properties being extremely sensitive to oxygen stoichiometry. The electrode materials chosen were Pt, due its chemical inertness and acceptance in industry as a standard electrode material, and Ni, due to its increasing popularity as a base metal electrode and as a cheaper alternative to Pt.

After gaining some basic proficiency with the deposition of TiO_2 (Paper 1), efforts were transitioned to the use of $BaTiO_3$ using either Pt or Ni electrodes. An in depth understanding of the effects of the sputter processing parameters on the development of the AC and DC dielectric properties was investigated with a statistical design of experiments (Papers 2 and 3). Using the information gained from that analysis, studies were conducted on the effects of varying the dielectric thickness (Paper 4) and electrode thickness (Paper 5). Chemical and microstructural characterization of the sputtered $BaTiO_3$ films was conducted to understand the effects of these features on the measured dielectric properties (Paper 6).

5. Equipment and Materials

5.1. Deposition Equipment

Deposition was conducted with a Denton Discovery-18 Sputter Deposition System with 3 sputter cathodes (Figure 1). Two of the three heads are connected to a DC power supply capable of operation at 100 to 600 W in 100 W increments. The third is operated through a RF power supply with an attached matching network and is capable of powers up to 600 W in 1 W increments. All cathodes are equipped with magnets behind the targets to allow magnetron sputtering to occur, and are at a fixed angle of 60° from vertical. The head assemblies hold 3 inch diameter targets with a thickness of up to 0.25 inches. The deposition chamber is equipped with a variable speed rotation assembly to ensure uniformity of film deposition. Rotation was kept at a constant speed of approximately 30 revolutions per minuteduring this research. Gas composition in the chamber is controlled with 2 mass flow controllers connected to lab grade purity Ar and O_2 tanks. For this research, 99.9% pure metallic targets of Ti, Ni, and Pt were used on the DC heads, and a custom made $BaTiO_3$ target with bonded head assembly was attached to the RF head.

Figure 1 – Photograph of Denton Discovery-18 Sputter Deposition System used for this research.

Masking of the electrode and dielectric layers was carried out with physical masks (a.k.a. shadow masks) machined out of brass sheet or thin molybdenum sheet. The brass masks (Figure 2) were machined in-house with a CNC mini-mill. The electrode mask (left) is a series of 1.6 mm wide by 3.2 cm long channels arranged in an array of 5 parallel lines per quarter of the 4 inch diameter mask. This mask was limited to use in the preliminary TiO_2 studies. The dielectric mask contains four large openings (2.7 cm by 2.7 cm) to allow a blanket coating of the thin film dielectric over the previous layer(s).

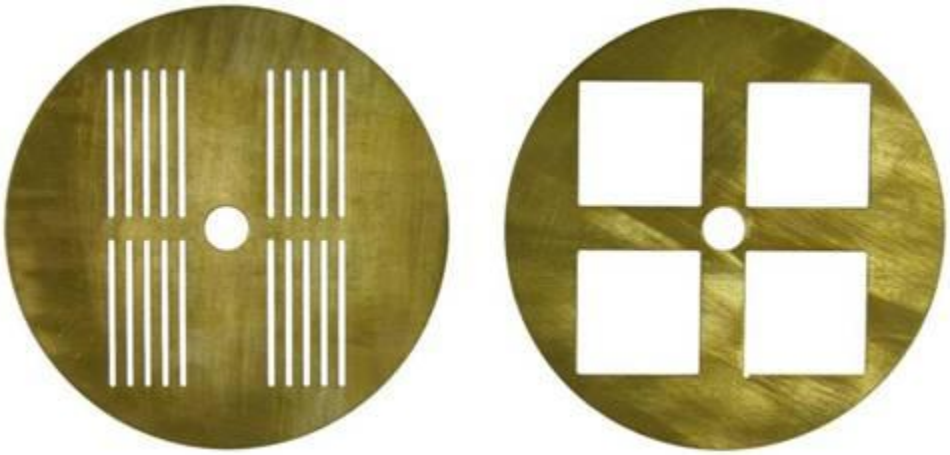

Figure 2 – Machined brass shadow masks for electrode (left) and dielectric (right) patterning. The use of the electrode mask results in a capacitor area of 2.56×10^{-2} cm^2.

A second electrode mask was machined via CNC laser ablation at Missouri State University in Springfield, MO. The channels on this mask are 73.7 μm wide (minimum beam width of the laser used for machining) and 2.4 cm long, with 2 mm diameter test pads at both ends to facilitate electronic testing (Figure 3). Similar to the machined brass mask, these channels are arrayed in 11 parallel lines in each quarter of the 4 inch square mask. The purpose of this mask was to create a smaller capacitor area (2.56×10^{-2} cm^2 with larger mask, 5.43×10^{-5} cm^2 with small) to minimize the measurement of macro-defects within the dielectric films. An additional benefit of the smaller device area is the increased number of data points per wafer (100 with large mask, 484 with small mask), improving statistical analysis. This mask was used extensively throughout the series of $BaTiO_3$ characterizations.

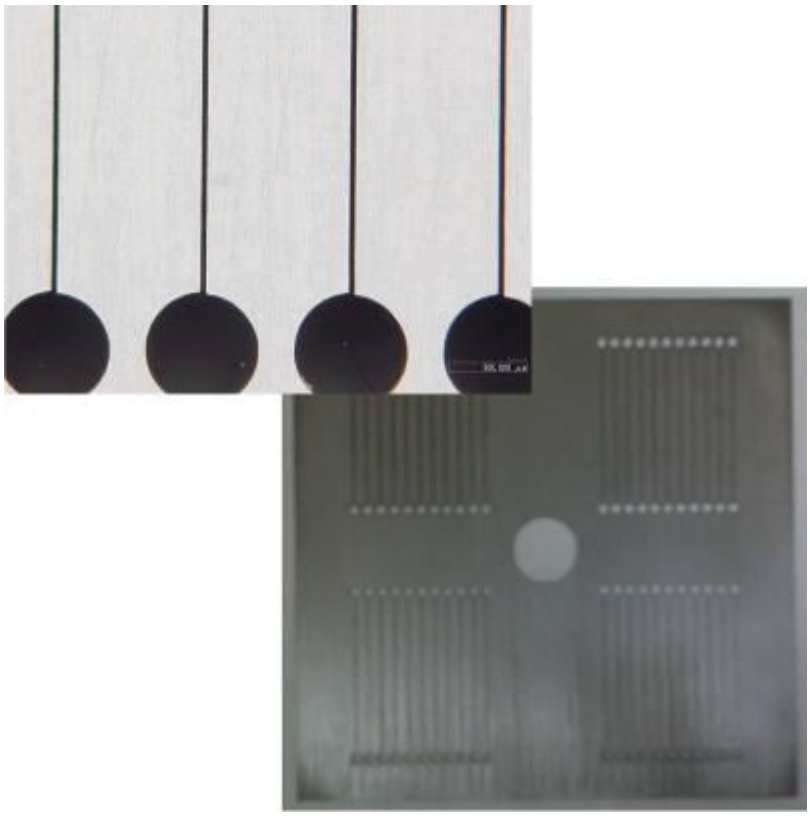

Figure 3 – Laser machined molybdenum mask for the fabrication of small capacitor area devices. This mask results in a capacitor area of 5.43×10^{-5} cm^2.

5.2. Electrical Test Equipment

Electrical testing was performed in two stages, direct current (DC) and alternating current (AC). Basic, initial DC testing was conducted with a Wavetek Meterman 10XL multimeter to determine device yield per wafer. The Wavetek could measure a maximum of 20 MΩ, and was found to be a suitable initial test of the sputtered devices. More in-depth DC analysis was conducted using an HP 4140 pA Meter (Figure 4) to obtain current-voltage (I-V) plots between 0.1 and 100 V in both positive and negative polarities. Hysteresis plots were acquired through the use of a Radiant Technologies RT6000HVS (Figure 5) from 1 to 19 V (being largest whole number potential at which measurements could be performed in the low voltage mode).

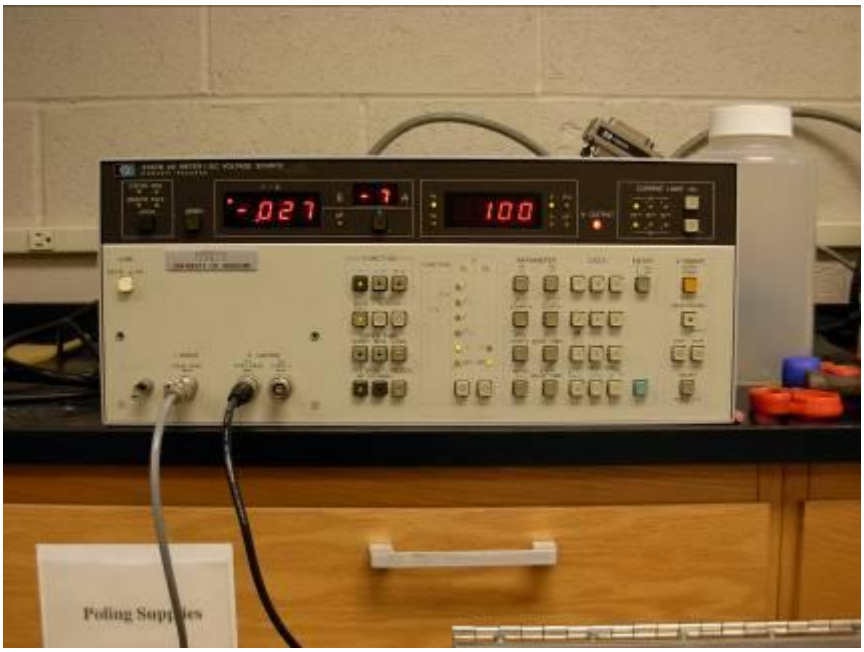

Figure 4 – The HP 4140 pA Meter used for the acquisition of I-V plots from the sputtered $BaTiO_3$ capacitors with either Ni or Pt electrodes.

Figure 5 – The Radiant Technologies RT6000HVS used for the acquisition of hysteresis loops for the sputtered $BaTiO_3$ capacitors.

Alternating current (AC) testing was conducted with two pieces of equipment. The first was a Leader LCR-745-01 set to measure at 1 kHz (Figure 6). The system measures at a V_{rms} or 1 V, and was used with 0 V DC bias. The second piece of AC test equipment was an HP 4194 (Figure 7) at 1 V_{rms} with 0 V DC bias from 500 Hz to 200,000 Hz.

Figure 6 – The Leader LCR-745-01 test bridge used for initial AC investigations at 1 kHz, 1 V_{rms}, and 0 V DC bias.

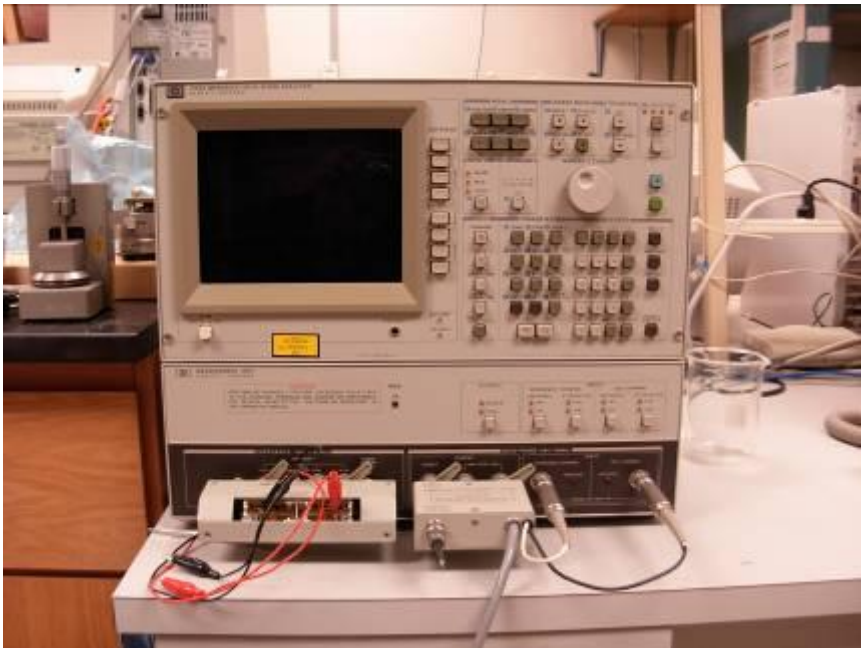

Figure 7 – The HP 4194 used for more in depth AC characterization at 1 Vrms with 0 V DC bias at frequencies between 500 and 200,000 Hz.

Testing on the HP 4140B, HP 4194, and RT6000HVS was conducted in a specially fabricated Faraday cage made of solid Al with two coaxial and two triaxial

throughputs for electrical connections (Figure 8). The image also shows the micro-positioning needles used to make contact with the anode and cathode of all devices during electrical testing. The combined use of the Faraday cage with micro-positioning needles allowed precise measurements of the dielectric properties of the sputtered $BaTiO_3$ devices at temperatures between 20°C and 300°C (hot plate also pictured in Figure 8) with minimal external electrical interference.

Figure 8 – Image of the specially made, solid Al Faraday cage used for a portion of the electrical testing.

5.3. Chemical and Microstructural Characterization Equipment

A variety of chemical and microstructural characterization techniques were used throughout the investigation of the sputtered nano-capacitors. X-ray diffraction (XRD) was conducted using a Philips X-Pert system at 2θ values between 5° and 90° with 0.03° incremental steps at a rate of 1.5 sec/step using Cu Kα radiation with a wavelength of 1.54 Å. A Kratos Analytical Axis 165 with a Mg source was used for all x-ray photoelectron spectroscopy (XPS) work. Scanning electron microscopy (SEM) was performed on both a Hitachi S-4700 FESEM and Helios Nanolab 600 FIB-SEM.

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PAPER I

Electrical and Statistical Characterization of Reactively Sputtered TiO_x Capacitors with Nickel Electrodes

by

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Abstract

Thin film capacitors were sputtered on Si wafers with Ni electrodes in order to determine the dielectric properties of reactively sputtered TiO_x with a base metal electrode system. The use of Ni electrodes gave electrically responsive devices with low frequency resistances of 350 to 9100 Ω, permittivities from 250 to 1500, and losses between 0.300 and 0.750. The large loss values have been attributed to the semi-conductive nature of sub-stoichiometric TiO_x. The decreased resistance is subsequently responsible for the elevated permittivities. Dielectric data was able to analyzed by a full factorial design of experiments analysis, and has be related to the activity of oxygen in the plasma during deposition. XPS characterization confirmed the proposed effects of oxygen both in and on the film during deposition.

1. Introduction

Thin films of TiO_2 have found significant use in optical and chemical sensor applications [1-3], as well as for low to moderate permittivity dielectric materials [4-6]. Bulk rutile TiO_2 has a permittivity of 170 parallel to the c-axis and 89 perpendicular to

the c-axis [2]. The anatase form of TiO_2 has been reported to have a permittivity as high as 76 for 60 nm thick films [7]. Literature on amorphous TiO_2 as well as the rutile, anatase, and metastable structures of polycrystalline TiO_2 thin films show a range of permittivities from as low as 3 to above 800, depending on deposition technique and process conditions [8-11]. Lower permittivities have generally been observed with lower losses [5, 8, 9]. The high leakage currents and loss values observed in thin film TiO_2 dielectrics compared to other metal oxides has severely limited the use of TiO_2 as a capacitor [1]. The most influential variable on the electrical response of TiO_2 thin films is the defect chemistry, which is significantly dependent on the processing technique used and the associated parameter levels. Sputtering is a thin film deposition technique that allows the defect chemistry to be modified through a variety of process parameters (e.g. deposition power, oxygen content of plasma, deposition temperature, etc.).

The most significant defects in the TiO_2 system are oxygen vacancies and titanium interstitials [12, 13]. The concentration of these defects is affected by the oxygen concentration during sputter deposition, and can be indirectly measured by the electrical responses of the resulting film. Films sputtered at low oxygen concentrations typically have higher permittivities and corresponding higher losses than films made at higher oxygen concentrations [5]. Room temperature depositions require an oxygen concentration between 10% and 50% in the plasma to obtain acceptable permittivities and loss values. Similar trends were observed for the conductivity of sputter deposited TiO_2 films [14, 15].

Another factor that has been observed to impact electrical performance of the TiO_2 thin films has been microstructure. The crystallinity, nature of phases (anatase, rutile, etc.), and porosity (both macro- and micro-porosity) are known to, at least in part, control the dielectric properties of these films. Lower film crystallinity, which has been suspected to be due to film stress, results in a lower permittivity film [7]. Other work indicated that films sputtered at temperatures below 500°C were found to be amorphous, and also showed increased permittivity values [8, 9]. Furthermore, deposition across a range of 200° to 500°C showed a lack of dependence on deposition temperature in regards to electrical response [8], suggesting that if the material is amorphous deposition temperature does not play as major a role in film development as it does with crystalline

films. Post-deposition annealing, however, has been shown to crystallize the films to form coexisting anatase and rutile structures at annealing temperatures of 300°C [8], and a single phase of rutile at 800°C [16]. In both cases, the dielectric properties of the films were observed to improve over the amorphous, as-deposited materials. These results suggest that the as-deposited films were oxygen deficient, and that a subsequent annealing, even at as low a temperature as 300°C, in an oxygen containing atmosphere supplies enough thermal energy to begin crystallization of the film as well as enough oxygen to minimize oxygen vacancy concentration [16].

The present work was conducted to gain a more in-depth understanding of the behavior of the dielectric properties of reactively sputtered TiO_x thin films with Ni electrodes using statistical design and analysis. The electrical properties of the films will also be correlated with the O:Ti ratios in the resultant films, and ultimately linked with the activity of the oxygen in both molecular and ionic form in the deposition chamber during sputtering.

2. Procedure

All samples were fabricated on 4 inch, <111>, p-type Si wafers with 1 μm thermal oxide for electrical insulation. The wafers were cleaned in a series of acetone, methanol, and DI water with subsequent spin drying and a dehydration bake at 200°C. The bottom Ni electrodes were patterned with a physical mask consisting of 5 parallel lines per quarter wafer measuring 1.6 mm wide by 3.2 cm long at a thickness of 100 nm using a Denton Discovery-18 sputter deposition system (Fig. 1.a). The dielectric was then patterned using another physical mask with 1 square-shaped opening per quarter wafer measuring 2.7 cm per side to a thickness of ~175 nm using a Ti target at DC powers between 100 and 300 W in a reactive atmosphere of between 50 and 75% O_2 in Ar (Fig. 1.b). The top electrode was then patterned by rotating the electrode mask 90º in relation to the bottom electrodes, resulting in 25 capacitor structures per quarter wafer with active device areas of 2.6×10^{-2} cm^2 (Fig. 1.c). An image of a quarter wafer of a completed sample after deposition of all three layers is shown in Fig. 2. Plasma composition was controlled via two mass flow controllers connected to Ar and O_2 cylinders. The thickness of each of the three layers was measured using a Tencor Alpha-Step 200 profilometer.

Initial DC resistance was measured using a handheld multimeter (Wavetek Meterman 10XL) to test for electrical discontinuity; with any location on the wafer measuring a resistance < 1 MΩ considered a non-testable device. The percentage of devices with measurable dielectric properties was then calculated based on the ratio of devices with resistance < 1 MΩ to the total number of locations per wafer (e.g. 5 locations with < 1 MΩ resistance gives 95 electrically measurable devices per 100 locations on the wafer, resulting in a percent of testable devices of 95%). Low frequency measurements were then made with a Leader LCR-745-01 test bridge at 1 kHz in ambient air at room temperature to measure capacitance, loss, and resistance. Based on the measured capacitance and thickness values, the effective permittivity of the sputtered TiO_x films were calculated.

To gain an understanding of the effects of the sputtering process variables on the dielectric properties of these devices, a 2-level full factorial design of experiments (DOE) matrix with 3 variables was created using Design Expert 7.1 statistical software packages. The variables and their corresponding levels are given in Table I. In addition to the prescribed 8 tests for the DOE, 2 center point samples were run at 62.5% O_2 and 160°C deposition temperature at both 100 W and 300 W to test for curvature within the system. All samples were fabricated and electrically tested as described above, and statistically analyzed using the statistical software.

3. Results and Discussion

The results of the DOE were analyzed in several parts. First, the percentage of testable devices was calculated as a measure of fabrication reliability. Next the dielectric response properties (e.g. resistance, permittivity, and loss) were analyzed to determine the effect of the sputtering process parameters on the electrical response of the TiO_x films. Lastly, all of responses were related to the oxygen-based phenomenon occurring in the deposition chamber during sputtering.

3.1. Percentage Testable Devices

The DOE did not show any statistically significant pattern in the yield data at a standard confidence level, α, of 5%. Plotting the percentage of testable devices versus

deposition temperature, however, shows a general increasing in yield with increasing temperature (Fig. 3). Given the standard deviations associated with each temperature, it can be seen that the statistical variance was interpreted as noise by the DOE software. Whereas a specific numerical model cannot be determined, the general trend of increasing testable devices (both the averages and associated standard deviations) with increasing deposition temperature is an important finding in itself. This behavior suggests that the increased energy present in the system due to the elevated temperature is aiding in the fabrication of less defective dielectric films, and was the first indication that an elevated temperature may result in more devices with good electrical properties.

3.2. Resistance

The room temperature resistance values of individual devices as measured by an LCR meter ranged from 350 to 9140 Ω depending on processing conditions, and were capable of being modeled by the DOE software (wafer averages given Table II). These values are within the bounds of reported resistances in the literature, which range from 300 Ω to over 100 MΩ [10, 15, 17, 18]. The TiO_x system showed a complex 3-way interaction with the process variables as all three factors interacted with one another to create complex inter-relationships between the factors and the measured resistance (Fig. 4). It was observed that an elevated temperature appears to flatten the resistance curve versus oxygen content and power at the upper end of the measured resistances (between 5500 and 7000 Ω). This is likely due to the added thermal energy allowing the atoms to reposition themselves into more regular, short range structures, which translates to better electrical performance. Elevated temperatures may also be creating a more uniform oxygen entrapment in the films, resulting in a more uniform resistance profile across a wide range of oxygen concentrations and deposition powers. The resistance was also observed to decrease at higher oxygen contents, regardless of deposition temperature. This behavior may be due to the increased bombardment of negatively charged oxygen ions against the surface of the depositing films [6, 19, 20]. This bombardment creates additional film defects, resulting in a film with lower resistance. This can be seen in XPS data obtained from 20ºC depositions across various oxygen contents and power levels (Table III). At 100 W, the O:Ti ratio was observed to decrease from 1.60 at 50% to 1.49

and then 1.40 at 60% and 70%, respectively. The decreasing O:Ti ratio with increasing oxygen content in the plasma was also found at the 300 W deposition, with a O:Ti ratio of 1.66 at 50% O_2 and decreasing to 1.54 and 1.52 for 60% and 70% O_2, respectively. The same phenomenon may be occurring with respect to power, as the resistance is found to decrease with increasing power. As the power is increased, the negatively charged oxygen ions gain more energy as they are propelled toward the substrate surface, again resulting in the addition of more film defects. This trend does not directly match with the XPS data as the O:Ti ratio was observed to increase with increasing power. However, as the O^{2-} ions impact the film surface with more energy at 300 W than at 100 W, it is reasonable to assume that more of these ions may become trapped in the film after disrupting the surface order of the developing film. Thus more damage is imparted to the film, despite the added O content. The higher energy O^{2-} ions may be re-sputtering the Ti atoms from the surface of the developing film, thus effectively increasing the O:Ti ratio thus counteracting the increased film damage.

3.3. Permittivity

The calculated permittivity ranged between 245 and 1495 (wafer averages in Table II), and fits within the wide range of permittivities observed in the literature from 5 [1] to greater than 2000 [21, 22]. As with the resistance, a complex 3-way interaction was observed within the statistical analysis of the data (Fig. 5). Similar trends are observed for the effective permittivity as were seen with the resistance. Higher deposition temperatures resulted in less appreciable changes in the calculated permittivity and display a more flat surface. At 20°C, an increase in the oxygen content in the plasma resulted in a decreased permittivity, and is more pronounced at a 300 W deposition power. This behavior again fits the pattern of increased oxygen ion activity in the plasma interacting with the substrate surface during deposition, resulting in film damage as discussed above. The power trends are observed to depend on the deposition temperature as well. At 20°C an increase in power results in an increased permittivity; whereas at 300°C, an increase in power corresponded to a slight decrease in permittivity. The 20 °C permittivity showed pronounced sensitivity to deposition power at 50% oxygen in the plasma, where the permittivity was observed to decrease from over 1150 to less than 350

with power decreasing from 300 W to 100 W. This is in contrast to the rising resistance occurring simultaneously. This contradiction is not supported by the oxygen ion activity theory proposed for the resistance, and may be related to the increased oxygen atomic concentration found in the final film (Table III). As the permittivity of TiO_x is based on the polar nature of the O atom in a Ti tetrahedral interstitial site [12, 18, 23], an increase in the absolute O concentration in the film should result in an increased permittivity.

3.4. Loss

The loss was also found to be involved in a 3-way interaction with the process variables. The measured values ranged from 0.300 to 0.748 (wafer averages in Table II). The high loss values of these films are due to the n-type semi-conductive nature of sub-stoichiometric TiO_x ceramics [12, 13]. In most respects, the loss trends mirror those observed for resistance; where the resistance is maximum the loss is minimum (Fig. 6). This same trend has been observed in other sources [9, 18]. Regardless of the deposition temperature, a decrease in oxygen content in the plasma results in a lower loss. This observation is consistent with the proposed activity of the negatively charged oxygen ions in the plasma and the increased atomic percent in the film. The power trends depend on deposition temperature with a low sensitivity to power at 20°C, and variable sensitivity at temperatures approaching 300°C with an increase in power resulting in an increased loss to varying degrees depending on percent O_2 in the plasma. The 300°C response, while not observed for the resistance or permittivity, still matches with the oxygen ion theory, as an increased power will result in more energetic oxygen ions striking the substrate surface. At 100 W, an increase in oxygen content significantly raises the loss and decreases the resistance. As the loss is a measure of non-90° current flow as a result of a continuous flow of current passing through the device, this behavioral match between the loss and resistance was expected. Similarly, at 50% oxygen an increase in power results in an increased loss, with a corresponding decrease in resistance, due to the added energy imparted to the oxygen ions by the increased power creating a higher defect concentration in the film.

3.5. Discussion

Final observation of all three responses as a whole shows a complete picture of how the activity of the oxygen in the plasma is affecting the chemical and electrical natures of the TiO_x thin films. As the percent O_2 is increased in the plasma, the concentration of O^{2-} ions increases. This results in more damage to the film resulting in an increased loss, decreased resistance, and decreased permittivity. Likewise, as the power is increased the resistance decreases and the loss increases due to the same mechanism. The permittivity, however, is observed to increase, possibly due to the increased O:Ti ratio resulting from the added oxygen entrapment and/or the re-sputtering of Ti from the film surface as a consequence of the increased energy in the O^{2-} ions. Lastly, in both the resistance and permittivity the increasing of deposition temperature had the effect of flattening the surface models, and lessening the response sensitivities to both percent O_2 and deposition power. In the case of the loss models, an increased temperature increased the sensitivity to power, potentially due to the scale of the loss value and the method of measurement. All of these factors combine to present a complex yet predictable system.

4. Summary

Dielectric testing of TiO_x devices with Ni electrodes resulted in the development of statistically based models that can be used to analyze the resistance (350 to 9140 Ω), permittivity (245 to 1495), and loss (0.300 to 0.748) of devices with similar thicknesses of TiO_x dielectric (175 nm) and Ni electrodes (100 nm). Dielectric properties appear to vary based on the activity of oxygen ions within the plasma at various oxygen and power combinations ranging from 50% to 75% and 100 to 300 W, respectively, over a wide range of temperatures between 20°C and 300°C. XPS data has confirmed the observed trends with an O:Ti ratio of 1.60 at 100 W and 1.66 at 300 W at 50% O_2 decreasing to 1.40 and 1.52, respectively, at 70% O_2. These results lead to a more complete, self-consistent understanding of the development of these devices during sputter deposition. In addition, the models appear to be self-consistent with the loss increasing as the resistance is decreasing, with similar trends in permittivity as was observed in the

resistance. Additionally, all measured dielectric property values fit within the range of those reported by other authors.

5. Acknowledgements

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Figures

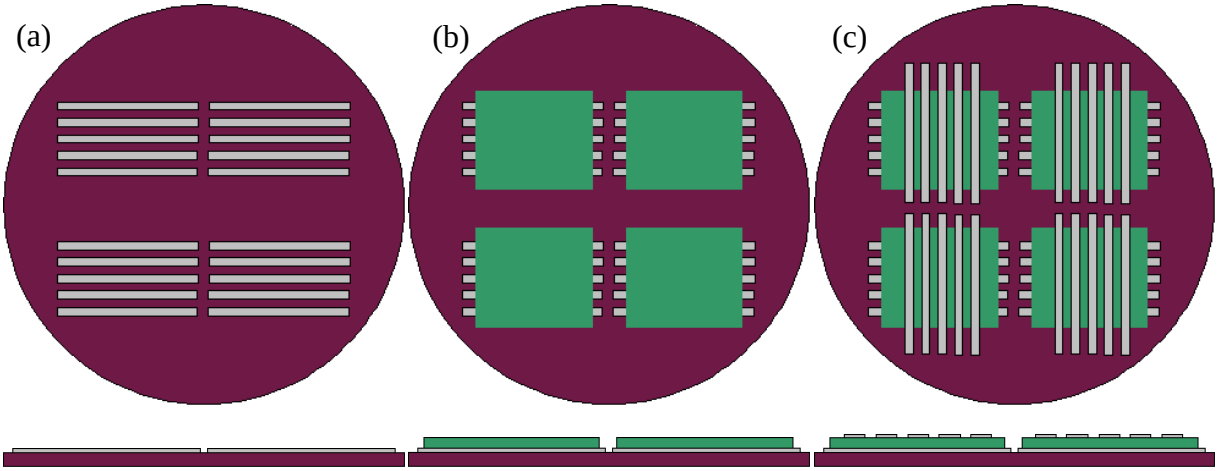


Fig. 1 – Process sequence followed for the patterned deposition of a single dielectric layer capacitor. 1st electrode layer (a), dielectric (b), and 2nd electrode layer (c). Vacuum was broken between layers to allow the exchanging of physical masks between depositions.

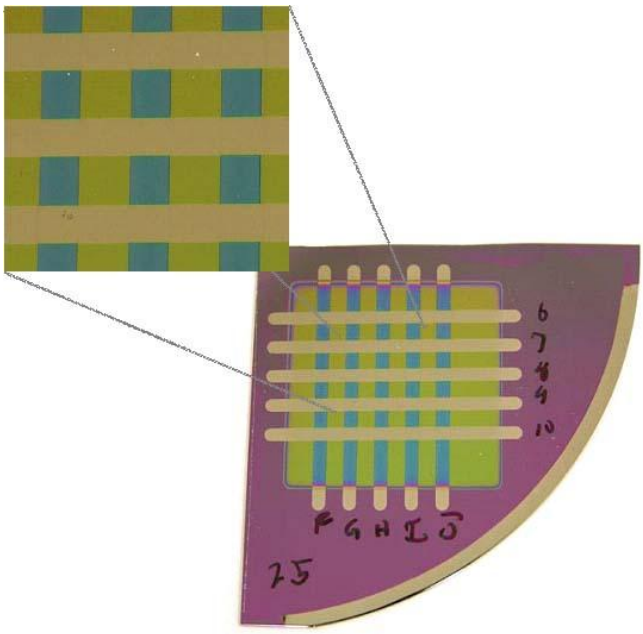


Fig. 2 – Images of a TiO_x specimen with Ni electrodes. Upper left image is a close up view of the electrode cross over areas.

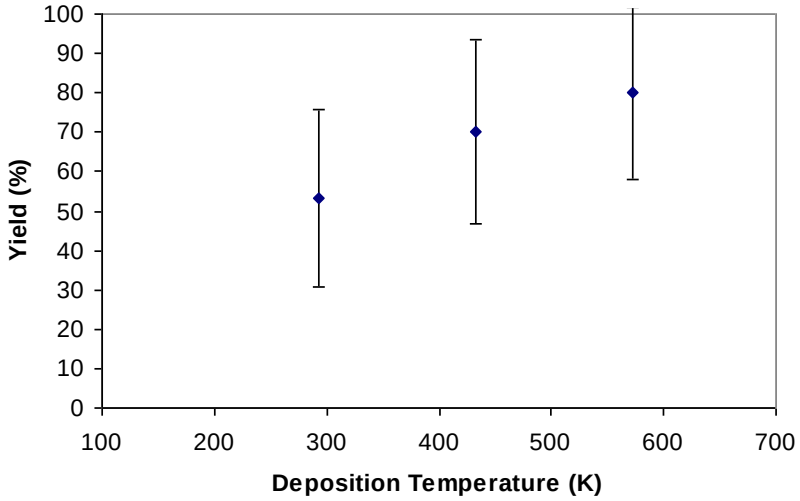
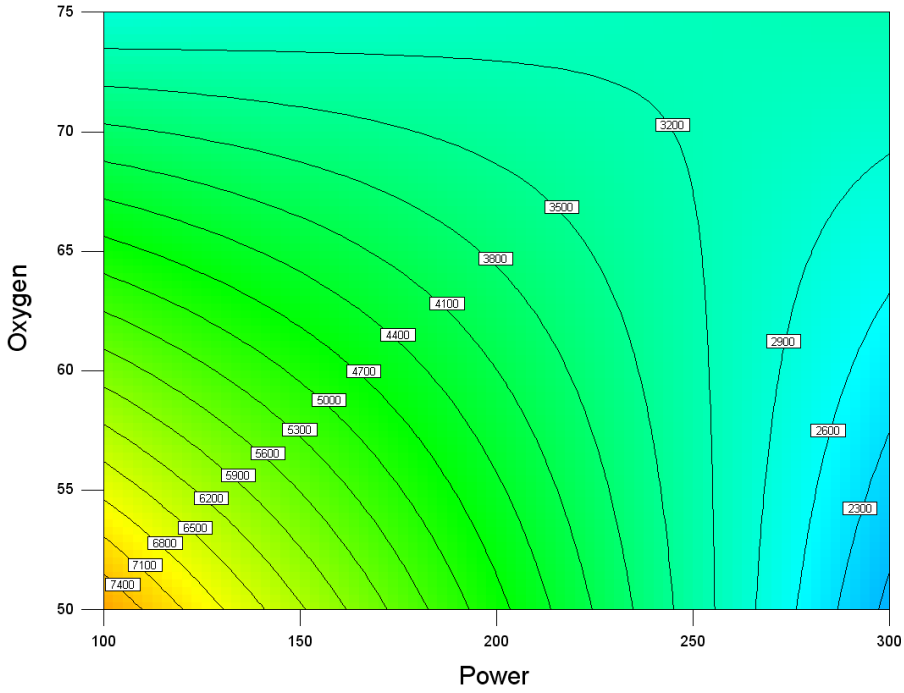


Fig. 3 – Percentage devices with measurable dielectric properties versus deposition temperature for the TiO_x DOE shows a positive temperature correlation.

(a)



(b)

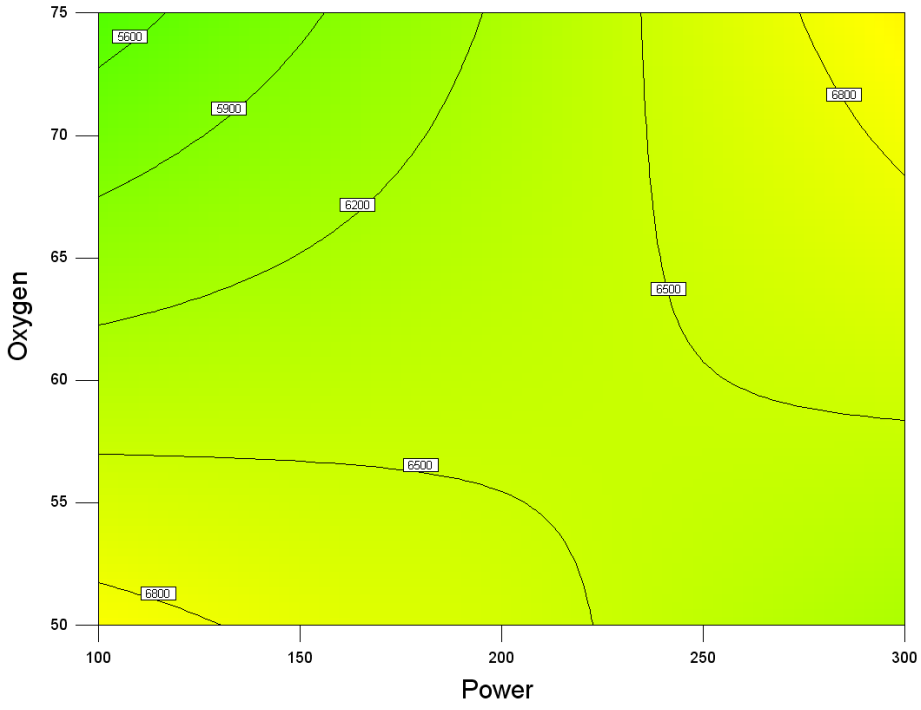
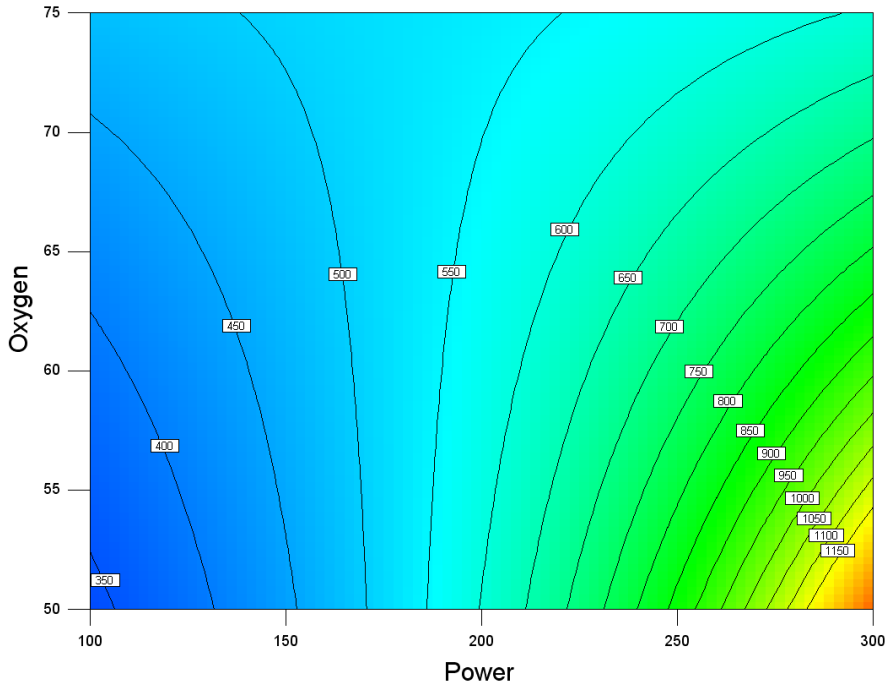


Fig. 4 – Contour plots of the predicted room temperature resistance of reactively sputtered TiO_x with Ni electrodes at 20°C (a) and 300°C (b).

(a)



(b)

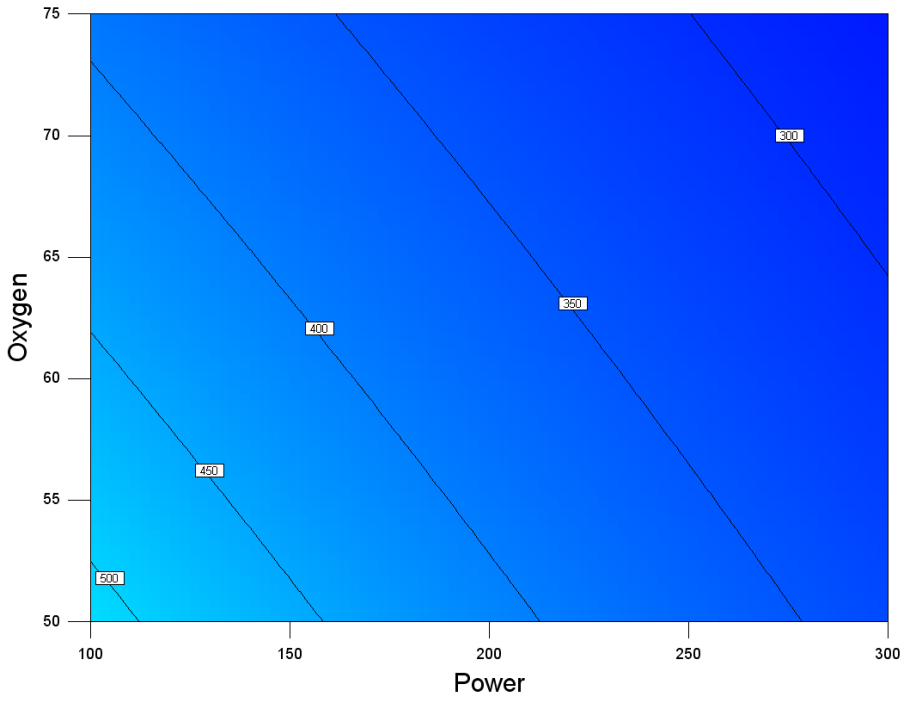
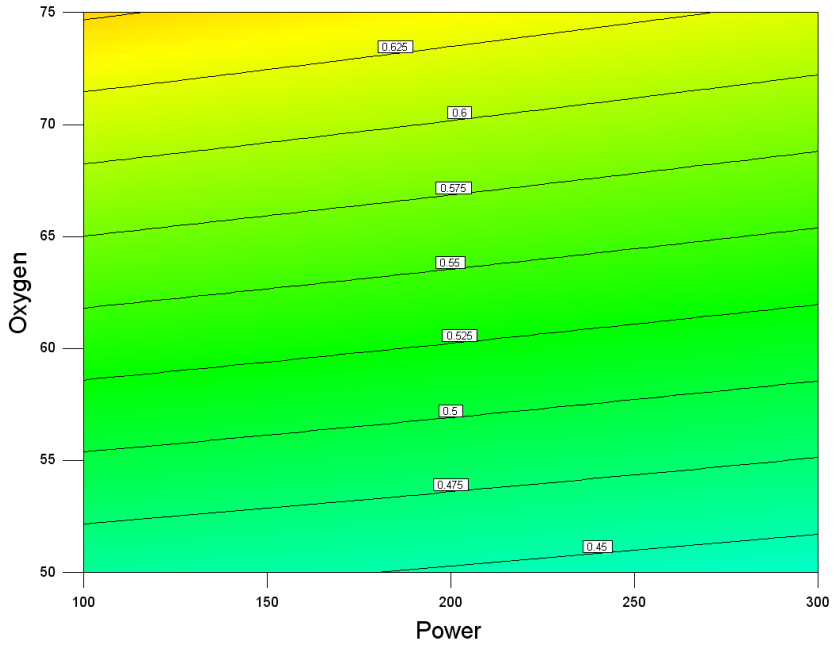


Fig. 5 – Contour plots of the predicted room temperature permittivity of reactively sputtered TiO_x with Ni electrodes at 20°C (a) and 300°C (b).

(a)



(b)

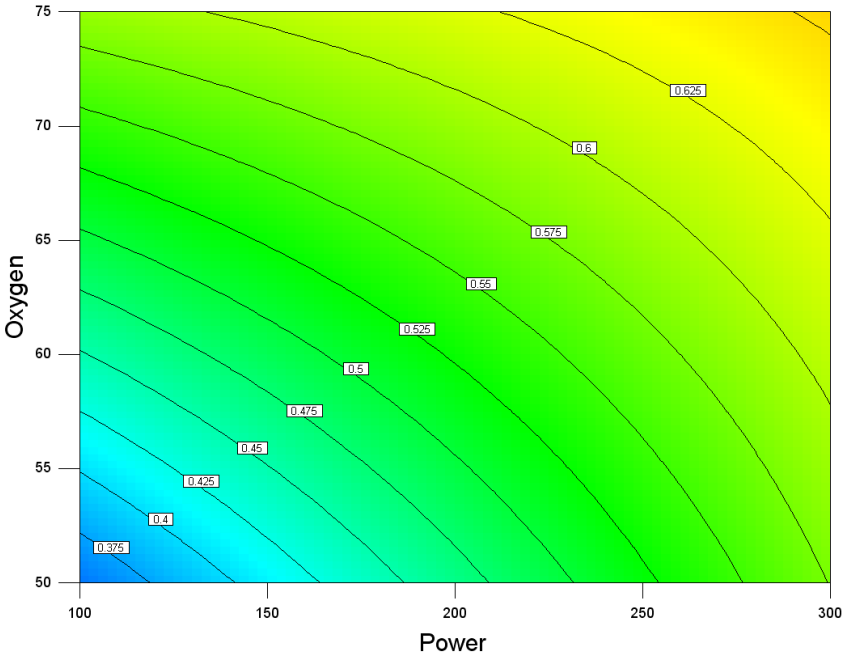


Fig. 6 – Contour plots of the predicted room temperature loss of reactively sputtered TiO_x with Ni electrodes at 20°C (a) and 300°C (b).

Tables

Table I. DOE parameters for the characterization of TiO_x sputter deposition

	Low	**High**
Power (W)	100	300
Percent O_2 (%) [balance Ar]	50	75
Deposition Temperature (°C)	20	300

Table II. Average and standard deviations of measured dielectric properties for the TiO_x DOE specimens with Ni electrodes

Run #	**Power (W)**	**O_2 Conc. (%)**	**Dep. Temp. (K)**	**Resistance (Ω)**	**Permittivity**	**Loss**
1	100	50	20	7700 ± 520	340 ± 12	0.458 ± 0.04
2	100	75	20	3300 ± 2300	480 ± 120	0.645 ± 0.05
3	300	50	20	20000 ± 770	1200 ± 220	0.495 ± 0.09
4	300	75	20	3200 ± 240	610 ± 72	0.608 ± 0.08
5	100	50	300	6700 ± 1500	520 ± 28	0.352 ± 0.04
6	100	75	300	5200 ± 1000	400 ± 59	0.627 ± 0.09
7	300	50	300	6200 ± 1000	340 ± 36	0.585 ± 0.07
8	300	75	300	6900 ± 700	280 ± 20	0.663 ± 0.06

Table III. Calculated O:Ti ratios based on XPS data for samples TiO_x deposited at 20°C

20°C		**Power**	
		100 W	**300 W**
$\%O_2$	**50**	1.60	1.66
	60	1.50	1.54
	70	1.40	1.52

PAPER II

Analysis of RF-sputtered $BaTiO_3$ thin film capacitors with Ni electrodes using a statistical design of experiments
Part 1 – AC Analysis

by

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Abstract

Nano-scale $BaTiO_3$ thin film capacitors with Ni electrodes were RF-magnetron sputtered onto Si wafers. A design of experiments regimen was performed to gain an understanding of the process variable interactions during deposition of Ni-$BaTiO_3$ devices with 100 nm thick $BaTiO_3$ and 20 nm thick Ni without any post-deposition heat treatments. RF powers between 100 and 200 W with plasmas containing between 10% and 50% O_2 at deposition temperatures between 20°C and 300°C resulted in calculated permittivities from approximately 150 to 1100 with losses between 0.016 to 0.371. Resistances were > 20 MΩ with device yields averaging > 95%. Statistical models were fit to the permittivity and loss data with R^2 values of 0.99 and 0.91, respectively. Model predictions based on the design of experiments results tested at 150W and 30% O_2 at 20°C showed a deviation of predicted versus actual values of 7.1% for permittivity and 19.0% for loss. Variations in the dielectric response were related to the activity of oxygen both in the plasma and in the film during sputter deposition.

1. Introduction

Thin film dielectrics with high permittivity and low loss have many applications in the electronics industry. One of the most commonly used dielectric materials for capacitors is $BaTiO_3$ [1]. Applications for these thin films include dynamic random access memory (DRAM) [2-5], tunable microwave devices [5-8], as well as in more traditional discreet, solderable capacitors [1, 4, 6, 7]. In order to achieve higher capacitance in a smaller area for high-end electronic devices, the fabrication of capacitive components using tape-casting technology becomes a limiting factor in achieving thin dielectric layers [9, 10]. This limitation requires the use of techniques designed specifically for the deposition of thin films not based on powder processing.

One of the major issues involved with any thin film technique used for the fabrication of thin film capacitors is the necessity of creating uniform, nanometer scale layers capable of performing up to the standards of the electronics industry. As these thicknesses are on the same scale as many microstructural characteristics, such as grain size, ferroelectric domains, and even the electrode interfaces [11, 12], it can be difficult to ensure property uniformity on a local scale when the device size also continues to decrease. As a result, both intrinsic (i.e. appropriate directional response of a single ferroelectric domain) and extrinsic (i.e. phase boundaries, defect densities, etc.) properties become more pronounced [11]. Intrinsic size effects are expected to be seen as a ferroelectric transition shift to lower temperatures, a broadening of the temperature dependence of the permittivity, and a drop in the peak permittivity. Extrinsic size effects have been observed to account for 60% to 70% of the dielectric property values in some of the common perovskite materials [11], and are seen to vary depending on the deposition method and chosen materials.

There are a variety of techniques that have been researched to deposit thin films of $BaTiO_3$ dielectric, including sol-gel [2, 13] and various methods of chemical vapor deposition (CVD) [14, 15]. Sputtering has been reported as having the capability to produce films with quality as good as that achievable with CVD [16, 17] and are more reproducible [5, 18] with high mass production potential [6]. During sputtering, the electrical behavior can be modified and, ultimately, engineered using processing conditions. The processing parameters that can be readily controlled during $BaTiO_3$

sputtering are the percent O_2 in the plasma, deposition temperature, plasma pressure, and RF power (Table I). A decrease in the percent O_2 in a plasma during $BaTiO_3$ sputtering results in a decrease in permittivity [2, 19, 20], increase in conductivity [21], increase in loss [2, 22], decrease in crystallinity [20], and a decrease in sensitivities to test temperature and test frequency [19]. By decreasing the deposition temperature the crystallinity of the film in reduced [23-27], the permittivity is decreased [21, 24, 26-32], the loss is lowered [26-28], and the breakdown strength drops [30, 31]. Increasing the total pressure during sputtering leads to an increase in leakage current [33], increased residual stress [6], more stoichiometric films (i.e. Ba:Ti:O approaches 1:1:3) [34], and decreased sensitivity on the target-to-substrate angle [34]. An increase in the RF power used during deposition increases the permittivity [35], decreases residual stress [36], and reduces leakage current [33]. Each of these factors represents a portion of the overall factors determining the properties and performance of the dielectric film. To date, an in depth characterization of the process parameters and the corresponding effects on the dielectric properties, which is required to readily develop the most robust fabrication philosophy for thin film capacitors, has not been conducted. The present work aims to give a detailed look into the effects of the sputtering parameters on the dielectric properties using statistical design and analysis, and attempts to relate the measured properties to physical phenomena occurring during the deposition process.

2. Procedure

Silicon <111>, p-type wafers, 4 inches in diameter with 1 μm thermal oxide for electrical insulation were used as the substrates for all experiments. The wafers were cleaned using a series of acetone, methanol, and DI water with a subsequent spin drying and dehydration bake at 200°C. For the purpose of statistical analysis and future post-deposition processing, the wafer was patterned with a grid of 11 x 11 capacitors for each quadrant of the wafer. The bottom Ni electrodes were patterned with a physical mask consisting of 11 parallel lines per quarter wafer measuring approximately 75 μm wide by 2.4 cm long to a thickness of ~20 nm (Fig. 1.a) using a Denton Discovery-18 sputter deposition system. The dielectric was patterned using another physical mask with 1 opening per quarter wafer measuring 2.7 cm square to a thickness of ~125 nm (Fig. 1.b).

The electrode mask was then rotated 90° from the bottom electrode layers, and the top Ni electrodes were deposited to a thickness of ~20 nm (Fig. 1.c). This process resulted in 121 capacitors per quarter wafer with active device areas of 5.43×10^{-5} cm^2. The plasma composition for all depositions was controlled with two mass flow controllers attached to Ar and O_2 cylinders. The thickness of each of the three layers was measured using a Tencor Alpha-Step 200 profilometer.

Initial DC resistance was then measured using a handheld multimeter (Wavetek Meterman 10XL); with any location on the wafer measuring a resistance < 20 MΩ (approximately < 5×10^8 Ω-m) considered a non-functional device. The yield was then calculated based on the ratio of functional devices to the total number of locations per wafer. Low frequency measurements were then made with a Leader LCR-745-01 test bridge at 1 kHz to measure capacitance, loss, and resistance at room temperature. Based on the measured capacitance and thickness values, the effective permittivity of the sputtered $BaTiO_3$ films were calculated. The effective permittivity and loss values were analyzed using Design Expert 7.1 statistical software package.

3. Design of Experiments Setup

A Box-Behnken design of experiments (DOE) was used to better understand the effects of processing parameters on the electrical properties. The variables investigated were deposition temperature, RF power, and percent oxygen in the plasma (Table II). The resulting 13 samples were tested for dielectric properties following the procedure outlined above in the as-deposited state (i.e. no annealing). The levels of RF power (100, 150, and 200 W) and O_2 concentrations (10%, 30%, and 50%) are based on trends seen in the literature as being the preferred range of values for sputtered $BaTiO_3$ with acceptable dielectric properties. The deposition temperatures were set at 20ºC, 160ºC, and 300ºC due to the desire to have a low, medium, and high value, with 300ºC being the upper limit of the deposition chamber.

4. Results and Discussion

All samples from the DOE were electrically tested for resistance, capacitance, and loss at 1 kHz. A statistical model was fit to the permittivity and loss data with R^2 values

> 0.90. The room temperature resistance of the testable devices, however, was observed to be too high for measurement with the LCR meter used for these experiments. Assuming a resistivity of $BaTiO_3$ between 20 and 40 MΩ-cm [37], the resistance of a 100 nm thick film with an area of 5.43×10^{-5} cm^2 is expected to be on the order of 3.7 to 7.4 MΩ. This could be readily measured with the LCR meter, but it is possible that the added resistance of the electrodes in conjunction with the signal losses associated with unshielded test fixtures may have increased the observed resistance of these devices.

Device yield was calculated based on multimeter readings of all 484 test locations on each wafer. The number of high resistance devices (e.g. resistance > 20 MΩ on multimeter) divided by the total number of possible devices (484) resulted in a percentage yield per wafer. At $BaTiO_3$ thicknesses of 100 to 125 nm yields were seen between 99.4% and 100% (0 to 3 failed devices per wafer), with an average of 99.9 ± 0.2%. Since all but two of the preparation conditions resulted in 100% yield, no statistical modeling was done on the yield data.

4.1. Dielectric Measurements

The samples had effective permittivities ranging from approximately 180 to 1100 and loss values of 0.016 to 0.371 for individual devices, depending on deposition conditions (averages given in Table III). The models for the predicted room temperature permittivity are shown in Figure 2. For both deposition temperatures, at 50% O_2 there was a maximum in permittivity observed at 150 W, with the permittivity decreasing at lower and higher power values. At low deposition temperatures (below 160°C), this parabolic trend continued as the concentration of O_2 decreased until it was between 10% and 20%, at which point the permittivity leveled off, and became nearly constant at approximately 840. At 300°C the initial parabolic relationship at 50% O_2 was inverted at 10% O_2, with a minimum around 175 W and the permittivity increasing as power increased or decreased from that value. Again, as was observed at 20°C, a constant 100 W deposition power showed the permittivity increasing with decreasing O_2 content in the plasma at 300°C, but with significantly less sensitivity to oxygen content than at 20°C.

The maximum permittivity for all temperatures was observed to be at approximately 50% O_2 and 150 W, and interestingly the values were approximately the

same: 1033 ± 75 at 20°C and 938 ± 69 at 300°C. This suggests that despite all of the processing parameters during deposition, there exists a constant permittivity at 50% O_2 and 150 W regardless of deposition temperature.

Figure 3 displays the models for the predicted room temperature loss. Both temperature models show loss values of less than 10% for all process variable combinations, with the majority of values being less than 7%. These loss values fit well with those found in the literature for other sputtered $BaTiO_3$ films, which ranged from 0.2% to over 100% [2, 19, 25, 29, 35, 38]. It should be noted, however, that the thickness of the $BaTiO_3$ films in this study are approximately 5 times thinner than the thinnest film studied by that group of authors. It was also observed that the behavioral trends of the models inverted from 20ºC to 300ºC, with the 20ºC max of 0.066 at ~35% O_2 and 150 W being the minimum of 0.008 at 300ºC. The minimum loss at 20ºC was seen at 10% O_2 and both 100 W and 200 W with a value of 0.015 whereas the maximum loss at 300°C was observed to be 0.086 and 0.100 at 50% O_2 and 100 W and 200 W, respectively.

4.2. Dielectric Response in Relation to Processing Conditions

In order to better understand the physical phenomenon behind the observed trends in the dielectric models, it is necessary to examine the individual forces acting on the film during deposition, and how these forces respond to changes in process parameters. Of particular interest is the activity of negatively charged oxygen ions in the plasma, and the oxidation/reduction potential of the dielectric film. Both of these factors are readily altered by the process parameters investigated by the DOE, and can be related to the measured dielectric properties.

Oxygen ion activity has been noted in the literature to impart damage to developing oxide films [1, 23, 34]. These negatively charged ions are propelled by the plasma sheath voltage surrounding the target toward the substrate, and can result in film damage such as oxygen vacancies and resputtering of the film (e.g. film removal) [1, 34]. Given the difference in sputter rates between Ba and Ti atoms, unequal material removal is likely to occur due to the lower energy state of the O^{2-} ions versus the Ar^{+} radicals responsible for primary removal of atomic species from the surface of the target. Both the oxygen vacancies and material removal will result in a decreased resistance and

increased loss due to the increased number of electronic charge carriers in the dielectric. Assuming a stoichiometric film was originally deposited, the added O^{2-} vacancies and non-stoichiometric material removal would result in a lower permittivity [33, 39, 40]. If the deposited $BaTiO_3$ film is non-stoichiometric prior to O^{2-} bombardment dielectric constant could increase or decrease depending on other processing conditions.

The concentration of O^{2-} ions striking the surface of the substrate is related to the process conditions in which the sputtering is conducted. The simplest factor to control is the amount of O_2 gas added to the plasma with an increase in O_2 content raising the concentration of the negatively charged ions [41]. An increase in sputter power should result in an increased O^{2-} concentration due to the increased potential moving through the plasma [33, 42], as well give the ions more momentum from the increased electronic repulsion between the increased voltage on the target and the inherent negative charge on the oxygen ions [33]. An increase in temperature will also result in an increase in O^{2-} activity. Basic thermodynamic principles suggest that the increased thermal energy will decrease the electric potential required to ionize the O_2 gas. The thermal energy will also increase the molecular motion of all gaseous species, thereby increasing the O^{2-} motion within the chamber. To minimize the activity of O^{2-} ions it is necessary to minimize the percent O_2 in the plasma, as well as minimize the deposition power and temperature.

At the same time, however, the sputter deposition of oxide films requires an oxygen source to offset oxygen loss during processing [21, 23]. The preferred method to accomplish this is to add O_2 gas to the plasma during deposition, which as stated above results in the detrimental addition of O^{2-} ions. In addition to increasing the partial pressure of O_2 in the plasma, a decreased deposition power and increased temperature, at the same percentage oxygen, will result in more film oxidation due to the increased kinetics from the thermal energy, and added reaction time given by the decreased deposition rate from the lower power. An oxygen deficient dielectric will result in an increased loss [2, 19], decreased resistance [17, 21], and either a decrease [2, 22] or increase [19, 20] in permittivity.

In addition to the competition of the oxygen ions and the oxidation of the dielectric, the process parameters also relate to other phenomenon that will affect the quality of the dielectric film. As Ba and Ti sputter at different rates due to their

difference in density of states, conductivity, and bonding energies within the $BaTiO_3$ matrix of the target, a condition arises where the composition of the deposited film will likely be Ti rich (due to its higher sputter rate compared to Ba). The extent of excess Ti is related to the deposition power, as an increased power will result in more Ba being removed from the surface of the target, thereby bringing the deposited film closer to stoichiometry [35]. At some point the rates of both Ba and Ti will equalize, and the deposition will be as close to stoichiometry as is possible for the other given process conditions [35]. In addition to adjusting the deposition power, a modification of the oxygen content in the plasma can also affect this equilibrium point. Assuming the sputter pressure is kept constant, as was the case with these experiments, the number of Ar^+ radicals striking the surface of the target per unit time is decreased for a given power due to the removal Ar gas from the plasma to allow for the addition of the extra O_2. Thus, as the O_2 content is increased, the power required to reach the equilibrium of Ba and Ti sputter rates must increase by some extent to account for the decrease in the Ar^+ available.

Table IV summarizes the effects of the three process variables that were examined in the above DOE analysis. These factors and the associated effects on the dielectric responses of the $BaTiO_3$ film show the complex nature of the 3-way interactions that were expressed in the statistical models developed by the DOE. These cause and effect relationships can be used to better understand the behaviors developed at the various process combinations displayed in the DOE models.

Consider the 25°C models of permittivity and loss first. At a constant concentration of O_2 in the plasma, the loss and permittivity are observed to experience a maximum at approximately 150 W. The initial behavior of rising loss and permittivity is linked to the increasing concentration of oxygen ions in the plasma. As the power is increased above 150 W, this behavior gives way to a combination of increased oxidation and a more equal sputtering of Ba and Ti atoms from the target. This change in behavior may be due to a saturation of oxygen ions in the plasma at 150 W, thereby allowing the other factors to be more influential.

At a constant power the loss is observed to have a maximum at approximately 30% O_2. The relative influence of the O_2 was similar to the observed influence for the

constant O_2 case. Namely, between 10% and 30% O_2 there is a rise in the concentration of O^{2-} ions in plasma due to the added O_2, resulting in an increased loss. At 30% O_2, the plasma appears to become saturated with the oxygen ions for that power, which allows the increased oxidation effects of the added O_2 in the plasma to take effect and lower the loss. Under the same constant power condition, the permittivity is found to increase with increasing O_2 concentration at powers between 130 W and 175 W, but decrease with rising O_2 concentration at the powers below 130 W and again above 175 W. It should be noted that this increasing permittivity portion of the model occurs in the power ranges associated with increased loss. As such, the increasing permittivity is likely to be due to the increased concentration of oxygen ions as the percentage of O_2 is increased. The decreasing permittivity, associated with decreasing loss values, is likely due to the increased oxidation associated with an increase in O_2 content.

The above trends have been displayed graphically in Figure 4. The bottom two rows contain schematic representations of the loss and permittivity models, respectively. The second column shows the case of constant power, and the third column the constant percent O_2 case. The schematics display the model trends with solid lines, and denote any transition points (i.e. a transition from domination by O^{2-} concentration to increased film oxidation) using dashed lines. Presented in this form, it can be observed that each area where the model indicates an increase in either permittivity or loss is a region dominated by the concentration of O^{2-} ions, and that for the decreasing regions the dominate influence is attributed to increased oxidation of the film. It is also easier to observe the self-consistent nature of the DOE models: where the loss is decreasing, so too is the permittivity [5, 19, 22, 29].

Similar trends are observed in the 300°C models, the schematic representations of which are given in Figure 5. Here, again, a decrease in response is attributed to increased oxidation of the dielectric, and an increase to the rising concentration of O^{2-} ions. Also consistent with the 20°C models, the 300°C responses are self-consistent with each other. The primary difference in the temperature models is the increased thermal energy in the system causing a change in the factor influences of a given region. For example, at 20°C the increase in $\%O_2$ from 10% to 30% resulted in an increased concentration of O^{2-} ions, and a subsequent increase in permittivity due to the induced film damage. At 300°C,

however, the increased thermal energy has increased the oxidation of the film resulting in a subsequent decrease in permittivity.

4.3. Model Verification

Based on the initial results of the $BaTiO_3$ work, a specimen was fabricated using 30% O_2 with an RF power of 150 W at a deposition temperature of 20°C, which was not one of the parameter sets previously investigated (Table II). This factor combination was predicted by the statistical models for the as-deposited condition to have a permittivity of 831 ± 8.4 with a loss of 0.127 ± 0.003. Table V gives the predicted values for the $BaTiO_3$ deposition versus the actual measured dielectric properties, namely a permittivity of 828 ± 9.9 and loss of 0.081 ± 0.045. The only average that falls outside of the bounds of the predicted value is that of the measured loss which was predicted to be higher than was measured. When the standard deviation of the measured loss is taken into consideration, however, it is reasonable to assume that the differences in averages are due to noise. The predicted permittivity, however, matched well with the measured value. The close correlation between the predicted and measured values suggests the models are able to accurately predict the dielectric properties of sputtered $BaTiO_3$ within the design space examined by this DOE. The accuracy of the models suggests that it is possible to engineer the dielectric properties for a chosen application of nano-scale $BaTiO_3$ films that has not been previously reported in the available literature.

4.4 Discussion

Following the above analysis, it becomes clear how there could exist contradictory information within the available literature. The general behavioral trend of increasing permittivity and simultaneously increasing loss [5, 22, 25, 29] has been in direct contrast with other work [2, 10] and in some cases within the same source [19]. More specific trends, such as the effect of increasing O_2 during deposition, have been reported to result in an increase in permittivity [2, 19] and an increase in loss [19] while others have found the opposite trends for both a decreasing permittivity [22] and a decreasing loss [2, 22]. Similar trends can be found in thickness dependencies [10, 19, 25, 29, 43]. At face value, these contradictions may call to question the validity of one

testing method over another, or perhaps the need for more standardized testing regimens. Based on the premise of competing factors detailed above, however, it is suggested that these contradictions may instead be due to the chosen process parameters for the given source. Given the complexity of the sputtered $BaTiO_3$ system across a wide range of processing variables, the results presented in Figure 5 are an attempt at explaining and unifying the data found in multiple sources [2, 19, 22, 25, 26, 35]. There are some sources where the proposed trends do not match the presented data [29, 33], but this is attributed to differences in reporting methods and/or a lack of pertinent information given regarding the sputtering parameters.

5. Summary

The deposition of $BaTiO_3$ sputtered under various RF powers, O_2 concentrations, and temperatures resulted in an accurate statistical model for the prediction of permittivity and loss of approximately 125 nm thick $BaTiO_3$ films with 20 nm thick Ni electrodes. The models fit the measured data with R^2 values of 0.9912 (permittivity) and 0.9068 (loss), showing a good correlation of the data to mathematical models. The model behaviors have been related to physical phenomenon known to occur during sputtering, and present a basic theory for understanding the development of sputtered $BaTiO_3$ in relation to the film's dielectric properties. The proposed theory states that there exists a competition between the inherent concentration of O^{2-} ions due to the presence on O_2 in the plasma attacking the surface of the depositing film, and the increased oxidation of the film due to the presence of non-ionized O_2 molecules within the chamber. The balance of these factors can be controlled by the deposition power, fraction of O_2 added to the plasma, and the deposition temperature. A test of the DOE models was carried out at a power of 150W in 30% O_2 at a deposition temperature of 20°C, and the predicted values were observed to be within less than 1% of the calculated permittivity and approximately 36% of the measured loss (actual value lower than predicted value). The DOE results were then related to the dielectric values available in the literature, and an explanation offered to explain the apparent contradictions in observed trends due to the chosen test parameter ranges examined.

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Figures

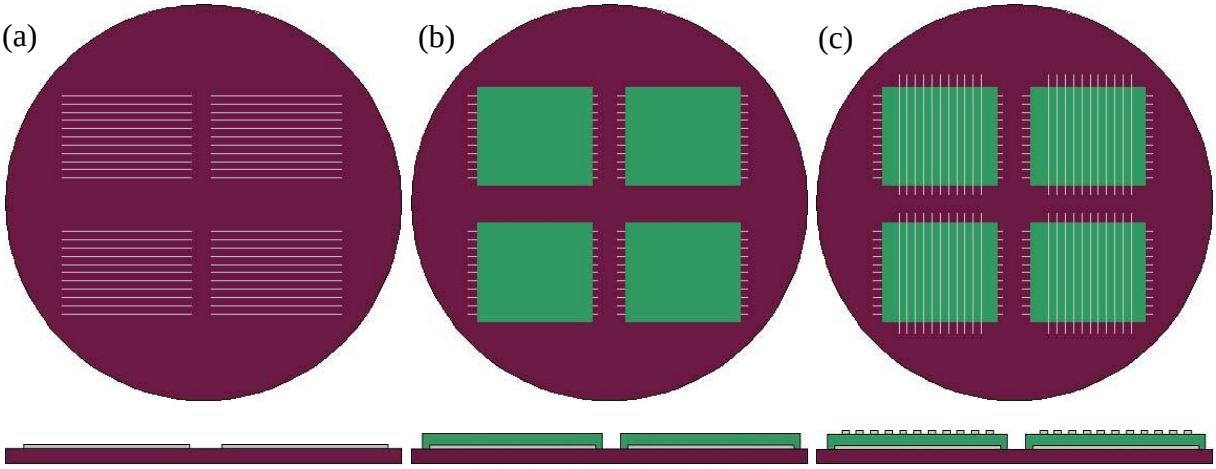


Fig. 1 – Process sequence followed for the patterned deposition of a single dielectric layer capacitor. 1st electrode layer (a), dielectric (b), and 2nd electrode layer (c). Top images are plan view looking at surface of substrate, and bottom images are cross sections. Vacuum was broken between layers to allow the exchanging of physical masks between depositions.

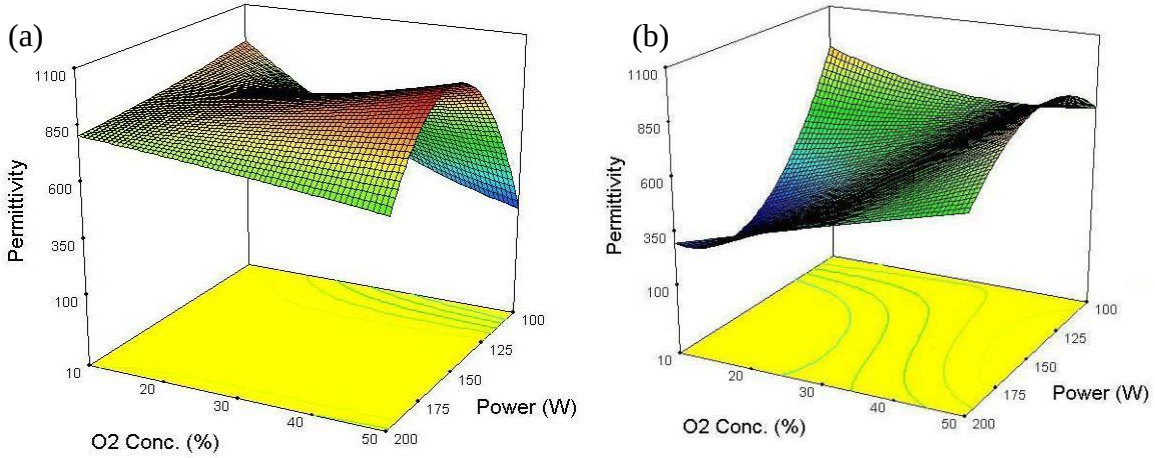


Fig. 2 – Model graphs of the predicted room temperature permittivity of sputtered $BaTiO_3$ at 20°C (a) and 300°C (b) in the as-deposited condition.

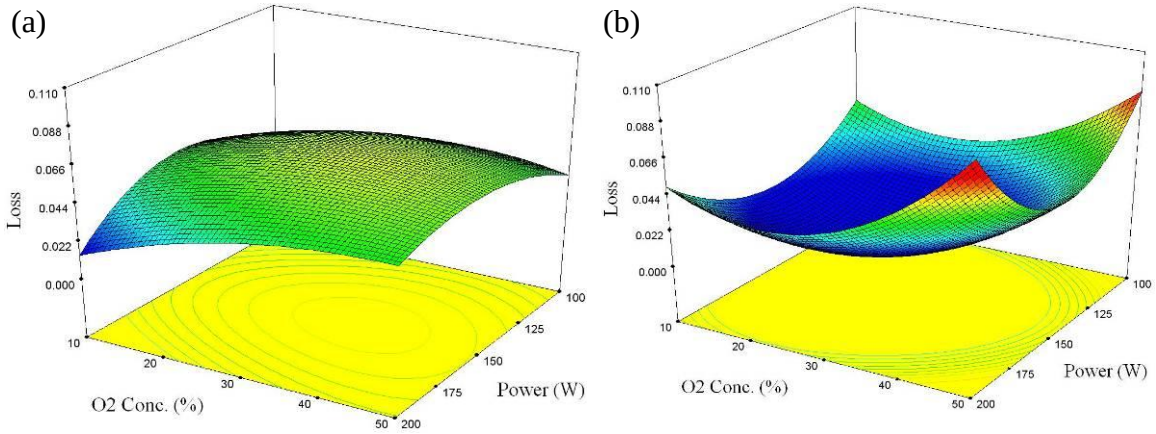


Fig. 3 – Model graphs of the predicted room temperature loss of sputtered $BaTiO_3$ at 20°C (left) and 300°C (right) in the as-deposited condition.

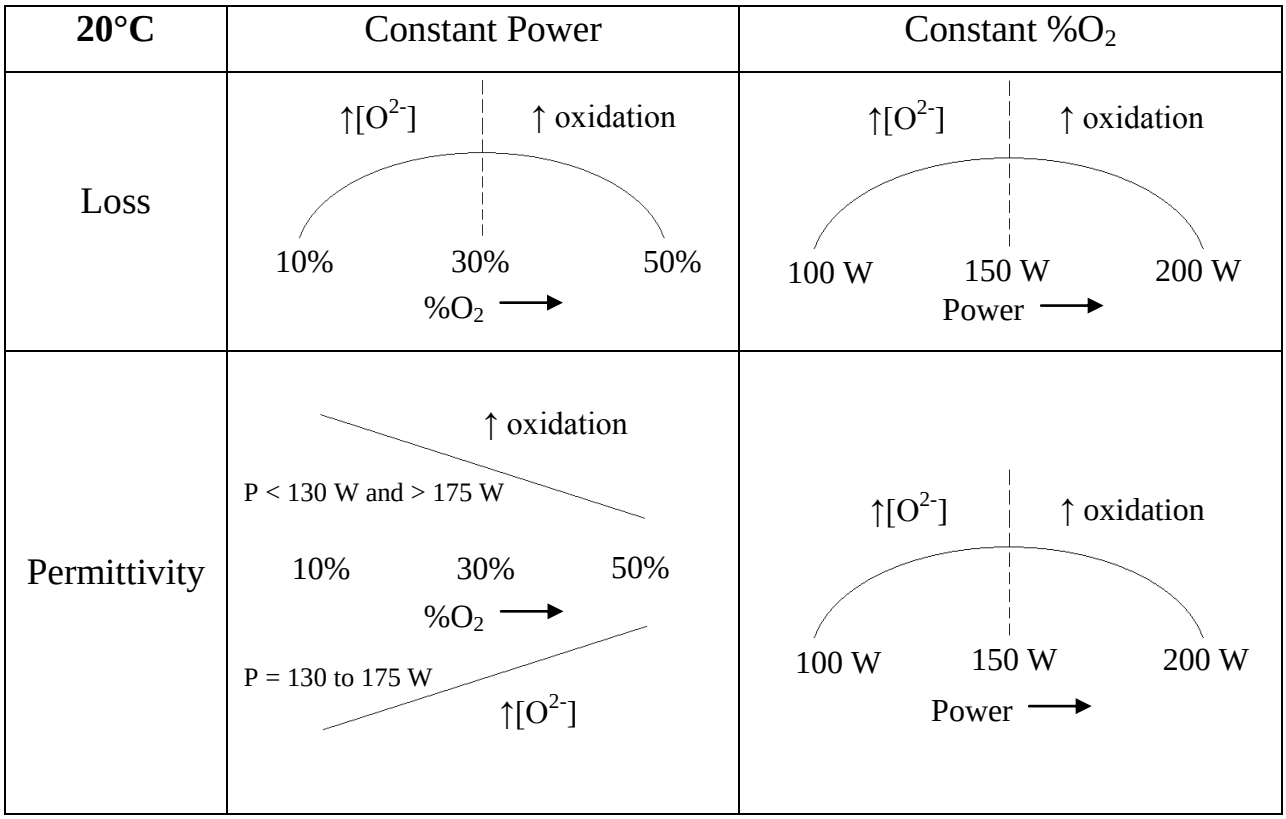


Fig. 4 – Schematic diagrams detailing the physical phenomena responsible for the loss and permittivity behaviors observed from the DOE models for 20°C condition. Solid lines and curves represent observed model behavior. The dashed lines indicate a change in dominating factors.

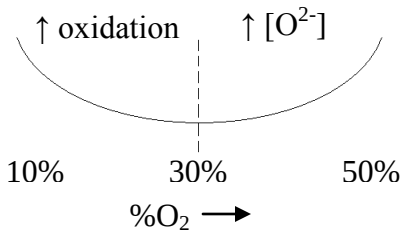
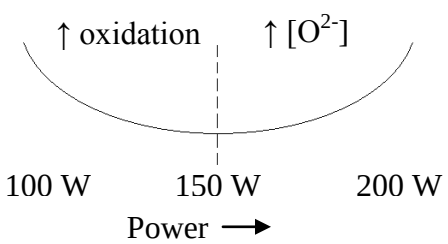
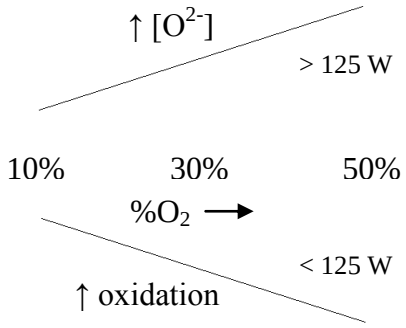
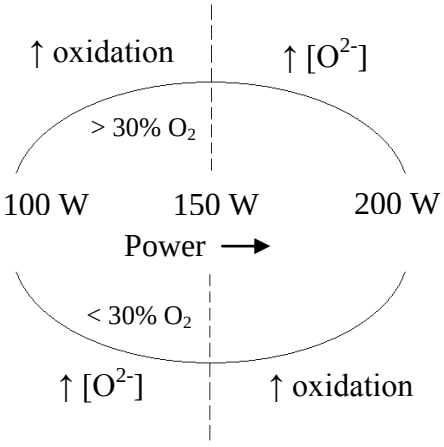
300°C	Constant Power	Constant $\%O_2$
Loss		
Permittivity		

Fig. 5 – Schematic diagrams detailing the physical phenomena responsible for the loss and permittivity behaviors observed from the DOE models for 300°C condition. Solid lines and curves represent observed model behavior. The dashed lines indicate a change in dominating factors.

Tables

Table I. Impact on electrical properties by process variables during sputtering

Process Variable	**Impact on Electrical Properties**
$\%O_2$	↑ $\%O_2$: ↑ permittivity, crystallinity, sensitivity to temp and frequency
	↓ $\%O_2$: ↑ conductivity, loss
T_{dep}	↑ T_{dep} : ↑ crystallinity, permittivity, loss, breakdown strength
	↓ T_{dep} : ↑ amorphorsity, residual stress
P_{total}	↑ P_{total} : ↑ leakage current, residual stress, stoichiometry
	↓ P_{total} : ↑ sensitivity to target-substrate angle and placement
RF Power	↑ Power : ↑ permittivity
	↓ Power : ↑ residual stress, leakage current

Table II. Variable levels for Box-Behnken design of experiments

	Low	**Mid**	**Hi**
RF Power (W)	100	150	200
%O_2 [balance Ar]	10	30	50
Deposition Temperature (°C)	20	160	300

Table III. Compilation of dielectric property measurements for the Ni-$BaTiO_3$ DOE specimens

Run #	**Power (W)**	**O2 Conc. (%)**	**Dep. Temp. (K)**	**Average Permittivity**	**Average Loss**
1	200	50	433	580 ± 27	0.092 ± 0.023
2	100	30	293	500 ± 18	0.042 ± 0.010
3	150	10	293	800 ± 40	0.046 ± 0.005
4	150	50	293	1000 ± 75	0.059 ± 0.005
5	100	10	433	840 ± 80	0.039 ± 0.019
6	150	50	573	940 ± 69	0.045 ± 0.003
7	150	10	573	280 ± 79	0.023 ± 0.007
8	150	30	433	640 ± 98	0.041 ± 0.018
9	100	30	573	720 ± 24	0.038 ± 0.003
10	200	30	293	710 ± 27	0.042 ± 0.006
11	200	30	573	480 ± 16	0.042 ± 0.011
12	200	10	433	460 ± 15	0.033 ± 0.002
13	100	50	433	450 ± 16	0.062 ± 0.006

Table IV. Effects of processing variables on the physical development and electrical properties of sputtered $BaTiO_3$ films

	Physical Effects Responsible for Given Property Change	Adjustment of Parameters Needed to Achieve Physical Response		
		$\%O_2$	Power	T_{dep}
$\uparrow \varepsilon_r$	Increased oxidation	↑	↓	↑
	Decreased $[O^{2-}]$	↓	↓	↓
$\downarrow \tan \delta$	Increased oxidation	↑	↓	↑
	Decreased $[O^{2-}]$	↓	↓	↓

Table V. Validation of $BaTiO_3$ DOE at 30% O_2, 150 W, and 20°C

	Predicted Permittivity	**Actual Permittivity**	**Predicted Loss**	**Actual Loss**
Measured Value	831 ± 8.4	828 ± 9.9	0.127 ± 0.003	0.081 ± 0.045
Percent Error	-----	0.36%	-----	35.7%

PAPER III

Analysis of RF-sputtered $BaTiO_3$ thin film capacitors with Ni electrodes using a statistical design of experiments
Part 2 – DC Analysis

by

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Abstract

Investigation of nano-scale $BaTiO_3$ thin film capacitors with Ni electrodes deposited by RF-magnetron sputtering using design of experiments and DC test methods was conducted. The devices were approximately 125 nm thick $BaTiO_3$ sputtered under varying RF powers (100-200 W), plasma compositions (10%-50% O_2 balance Ar), and deposition temperatures (20°C to 300°C) with approximately 25 nm thick Ni electrodes. Current voltage (I-V) plots indicated highly insulating films with resistances at 1 V between 16 and 270 GΩ. Hysteresis loops indicated a mix of paraelectric and ferroelectric films depending on the deposition conditions, with permittivities ranging from 170 to 10,000. Electrical testing at temperatures between 25°C and 300°C showed increasing conductivity as the temperature increased with activation energies ranging from 0.3 to 0.9 eV for conduction, along with limited amounts of remnant ferroelectric behavior. Statistical analysis of the data resulted in mathematical surface response models with R^2 values of 0.90 to 0.99, but complex higher order interactions resulted in the models incorrectly estimating the predicted values.

1. Introduction

One of the most commonly used dielectric materials for commercial capacitors is $BaTiO_3$ [1]. Applications for this material as a thin film include dynamic random access memory (DRAM) [2-5], tunable microwave devices [5-8], and discreet capacitors [1, 4, 6, 7]. In order to achieve higher capacitance density for high-end electronics, the fabrication of these devices with sub-micron thicknesses using tape-casting technology becomes impractical due to the necessity of powder precursors [8, 9]. This inherent limitation of the traditional capacitor fabrication technologies requires the use of techniques designed specifically for the deposition of thin films not based on powder processing.

Sputtering has been reported as having the capability to produce thin films of equal quality to that achievable with CVD [11, 12] that are more reproducible [5, 13] with high mass production potential [6]. The processing parameters that can be readily controlled during $BaTiO_3$ sputtering are the percent O_2 in the plasma, deposition temperature, plasma pressure, and RF power; each of which has been shown to impact the dielectric properties of the resulting film [2, 10-14]. The effects imposed by these parameter changes has been addressed previously [15]. Each of these factors represents a portion of the overall factors determining the properties and performance of the dielectric film. To date, an in depth characterization of the process parameters and the corresponding effects on the dielectric properties, which is required to readily develop the most robust fabrication philosophy for thin film capacitors, has not been reported. The present series of work aims to give a detailed look into the effects of the sputtering parameters on the dielectric properties using statistical design and analysis, and attempts to relate the measured properties to physical phenomena occurring during the deposition process. The AC responses were previously reported [15] and determined to be related to the competing effects of film oxidation and oxygen ion activity in the plasma during deposition. This work continues the analysis of these devices under an applied DC field, and determines the validity of the oxygen activity effects on the measured DC properties.

2. Procedure

Silicon <111>, p-type wafers, 4 inches in diameter with 1 μm thermal oxide for electrical insulation were used as the substrates for all experiments. The wafers were cleaned using a series of acetone, methanol, and DI water with a subsequent spin drying and dehydration bake at 200°C. To ensure the validity of the statistical analysis and allow for future post-deposition processing, the wafer was patterned with a grid of 11 x 11 capacitors for each quadrant of the wafer. The bottom Ni electrodes were patterned with a physical mask consisting of 11 parallel lines per quarter of a wafer measuring approximately 75 μm wide by 2.4 cm long to a thickness of ~25 nm using a Denton Discovery-18 sputter deposition system (Fig. 1.a). The dielectric was patterned using another physical mask with one opening per quarter wafer measuring 2.7 cm square to a thickness of ~125 nm (Fig. 1.b). The electrode mask was then rotated 90° from the bottom electrode layers, and the top Ni electrodes were deposited to a thickness of ~25 nm (Fig. 1.c). This process resulted in 121 capacitors per quarter of a wafer with active device areas of 5.43×10^{-5} cm^2 each. Plasma composition for all depositions was controlled with two mass flow controllers attached to Ar and O_2 cylinders and was monitored with a capacitance monometer in the sputter chamber. The thickness of each of the three layers was estimated using a Tencor Alpha-Step 200 profilometer on patterned glass slides placed near the wafer during each of the depositions, and confirmed by cross-sectional focused ion beam.

Following the AC testing previously reported [15], DC testing was initiated with current-voltage (I-V) plots from 0.1 to 100 V using an HP 4140B pA meter. The resistances of the devices were calculated assuming an ohmic relationship between the voltage and current at a constant voltage (e.g. V=IR). Following I-V measurement, hysteresis loops were taken for each of the specimens at incrementing voltages from 1 V to the system's low voltage maximum of 19 V using a Radiant Technologies RT6000HVS system set to low voltage. Determination of the permittivity was calculated based on the initial slope of the hysteresis loops, and remnant polarizations were recorded directly from the loop. The permittivity, remnant polarization, and resistances from 3 randomly chosen locations per wafer were analyzed using Design Expert 7.1 statistical software package.

3. Design of Experiments Setup

As previously described [15], a Box-Behnken design of experiments (DOE) was used to better understand the effects of processing parameters on the electrical properties. The variables of the DOE were set as deposition temperature (20°C, 160°C, and 300°C), RF power (100, 150, and 300 W), and percent oxygen in the plasma (10%, 30%, and 50% O_2 balance Ar). Table I gives the process schedules for the deposition of the different $BaTiO_3$ films. These levels were selected based on trends in the literature and equipment limitations, and allowed a broad range of the design space to be examined. The resulting 13 samples were tested for dielectric properties following the procedure outlined above in the as-deposited state (i.e. no annealing).

4. Results and Discussion

The AC properties and their dependencies on process conditions has been addressed previously [15]. In conjunction with AC behavior, the DC responses provide an overall understanding of how a given material will behave in a chosen application. As such, current-voltage (I-V) and hysteresis plots were measured and subsequently analyzed statistically to gain a more complete understanding of sputtered $BaTiO_3$ thin films with a thickness of approximately 100 nm.

4.1. I-V Behavior

Current-voltage plots can give significant amounts of information regarding a material's conduction mechanisms, breakdown strength, and the overall symmetry of the capacitive device. I-V plots were taken for all 13 specimens as defined by the original DOE. Figure 2 shows a typical I-V plot observed for these specimens. The relative symmetry between the positive and negative voltage regions indicates an overall symmetry in the device. This information primarily relates to the fact that the interfaces between the electrodes and $BaTiO_3$ are nearly identical on both sides of the dielectric. This symmetry was observed for 7 of the 13 specimens. The 6 specimens that showed asymmetrical response between measured positive and negative potentials prior to breakdown were generally symmetrical to ±10-25 V (Fig. 3), suggesting the asymmetry

may been due to the interaction of the defects within the film at high fields (10V is approximately 1 MV/cm). Table II lists the voltage at which the specimens became asymmetrical along with a compilation of the data obtained from the I-V analysis.

The resistance of the specimens was calculated at 1 V assuming an ohmic relationship between the applied voltage and measured leakage current (Table II). The insulation resistances ranged from approximately 16 to 270 GΩ, indicating that even at 125 nm these films were excellent insulators. Statistical analysis of the resistance data resulted in a predictive model for the resistance at 1 V with an R^2 value of 0.90 (Figure 4). The analysis showed that resistance of these devices was greatly affected by interactions between the sputter power with both the percent O_2 in the plasma and the deposition temperature. The low temperature model shows an inverse parabolic relationship with power where the resistance is maximized at approximately 150 W, with the value observed to decrease as the power is raised or lowered to another value. The relationship with the percent oxygen in the plasma is more complicated. At 100 and 200 W there is an inverse parabolic relationship with a maximum at approximately 20% O_2, that transitions to a parabolic trend at 150 W with a minimum at 10% O_2. Increasing the temperature to 300°C resulted in more stable responses across the power and $\%O_2$ ranges examined. A general parabolic trend with power was observed, the minimum of which was found to shift from approximately 130 W at 10 $\%O_2$ to around 200 W at 50 $\%O_2$. An inverse parabolic trend at 200 W with a maximum at 10 $\%O_2$ was found to transition to a parabolic behavior at 100 W with a minimum observed at 30 $\%O_2$.

The I-V plots were also used to determine the conduction mechanisms occurring in an insulating material over a range of applied voltages. All of the specimens consistently showed 2 regions of conductivity, the first of which was ohmic at voltages between ±1 V with the second non-ohmic mechanism occurring at voltages of above 1 V and below -1 V. The second mechanism was generally seen to be in effect until either the material experienced breakdown, or the maximum test voltage of 100 V for the pA meter was reached. Analysis of the low voltage region (±1 V) of the data sets showed a near linear behavior between the voltage and leakage current. This was determined by assuming that:

$$I = C*V^{n} \quad <1>$$

where I is the measured leakage current (A), V the applied voltage (V), C a standard coefficient, and n the power exponent. A power exponent, n, of ~1 indicates a linear (i.e. ohmic) behavior, and a value of 2 or more indicating a space-charge-trap limited conduction mechanism [16]. Using equation 1, the ln(I) was plotted against the ln(V) and a linear regression of the data was obtained (Figure 5). This procedure resulted in exponents of approximately 1 for all but 3 of the 13 specimens, indicating that the majority of the specimens were following a traditional ohmic behavior at low voltages between ±1 V (Table II). Of the three specimens with exponents not approaching unity, two showed an exponent of 0.3 and 0.4 (R6 and R4, respectively), and may be an indication of potentially misleading data taken for these two specimens. The third non-unity exponent was observed for R3 which had a value of 1.71, potentially indicating the presence of a space-charge-trap limited condition for this specimen.

At voltages above 1 V and below -1 V, the conduction mechanism was found to transition to a non-ohmic behavior. Two of the more common conduction mechanisms found in the literature relating to $BaTiO_3$ thin films are the Poole Frenkel (PF) and Enhanced Schottky (ES) mechanisms [10, 16, 17]. Both of these mechanisms involve lowering the barrier between the electrode and dielectric due to the application of a potential, but differ in the manner in which the barrier is lowered. The ES mechanism relies on lowering the barrier height enough to allow an electron to jump over the barrier and enter the dielectric material (Figure 6.a)[16]. A PF conduction mechanism effectively decreases this barrier with field-enhanced thermal excitation of traps near the interface of the two materials, allowing the electrons to pass into the dielectric (Figure 6.b)[16]. Both of these mechanisms can be determined based on the slope, β, of the $\log(I/V)$ versus $V^{1/2}$ plot, where the slope for a PF based system is

$$\beta_{PF} = \left(q^3/\pi\varepsilon\right)^{1/2} \quad <2>$$

with q being the electronic charge and ε representing the permittivity of the $BaTiO_3$. For an ES system the slope becomes

$$\beta_{ES} = (^{q^3}/_{4\pi\varepsilon})^{1/2} \quad <3>$$

Using the permittivities for these specimens acquired previously [15], theoretical β_{PF} and β_{ES} values were calculated (Table II). Figure 7 shows one of the typical $\log(^{I}/_{V})$ vs $V^{1/2}$ plots with the linear regressions for both the positive and negative potentials. As the positive and negative β values were comparable for the majority of the specimens, only the positive β is given in Table II.

A close examination of the data revealed that only 2 of the specimens had measured β values within the range of those predicted by equations 2 and 3. Sample R7 displayed a β of 0.372, which is comparable to the theoretical β_{ES} of 0.326, suggesting that the barrier lowering in this specimen is due to an Enhanced Schottky mechanism. Sample R9, however, resulted with a β of 0.103 which was near the theoretical β_{PF} value of 0.102 for this specimen, indicating the presence of a Poole Frenkel mechanism acting within this specimen. The remainder of the measured β values were mixed with 7 specimens displaying slopes greater those predicted by equations 2 and 3, and 4 with slopes below the predicted ES and PF values. As equations 2 and 3 rely on accurate permittivity values to correctly calculate the β_{ES} and β_{PF} values, these deviations may be due to inaccurate permittivity values gained from the previous studies. Since the permittivities were calculated based on overall device capacitance, any interfacial effects inherently affecting the measured capacitance (i.e. the presence of interfacial compounds or electrical dead layers) would give inaccurate permittivity calculations of the $BaTiO_3$ which are required for these calculations. It is also possible that these specimens are not following a PF or ES based phenomenon. Attempts to model the data with the DOE software were unsuccessful, likely due to the limited number of data points available to deal with systemic noise.

4.2. Hysteresis Plots

Following I-V analysis, hysteresis plots were taken for all of the specimens at room temperature to determine the dielectric nature of the sputtered $BaTiO_3$ (i.e. paraelectric or ferroelectric), and to gain a measurement of the devices' permittivities. Three general dielectric behaviors were observed for the specimens (Figures 8-10). The

first was consistent with a paraelectric-type response, with limited remnant polarization and general needle-like overall shape (Figure 8). This trend was observed for specimens R3 and R7, both of which were processed at 150 W and 10 $\%O_2$. The second behavior observed was the initial signs of ferroelectricity (Figure 9). Specimens exhibiting this trend (R1, R5, R6, R11,and R13) gave hysteretic loops with significant amounts of remnant polarization, but never developed the traditional "tails" at the maximum and minimum polarizations (observed at the maximum and minimum applied potentials). As the specimens showing this type of behavior had correspondingly high field tolerances as measured by the I-V plots, this lack of tail typically observed for ferroelectric hysteresis loops is likely due to a lack of complete saturation of these films at the maximum applied voltage of ±19 V. All of the specimens showing this behavior were deposited at elevated temperatures and generally higher $\%O_2$ values. The third type of hysteretic behavior observed was that of a lossy ferroelectric material (i.e. the plots resembled a capacitor and resistor in series), showing significant remnant polarization but no polarization plateau; instead, an immediate loss of stored charge once the voltage was reversed after reaching the maximum test voltage was observed. Whereas the more traditional ferroelectric behavior as seen in Figure 9 displays a constant remnant polarization across the test voltages, the lossy ferroelectric behavior as in figure 10 has a remnant polarization that is dependant upon the maximum voltage attained during that test cycle. Specimens showing this behavior (R4, R8, R10, and R12) were typically those sputtered at lower temperatures, lower $\%O_2$, and higher powers. Two specimens (R2 and R9) showed mixed behaviors depending on the test location chosen on the wafer. Both of these samples were deposited at 100 W and 30 $\%O_2$.

In addition to overall electronic behavior, hysteresis loops also permit a measurement of the permittivity based on the slope of the initial portion of the loop (i.e. while the voltage is increasing from 0 to V_{max}). The permittivities calculated from the hysteresis loops (Table III) were analyzed with the statistical DOE software, as were the remnant polarizations. Both resulted predictive models with an R^2 of 0.98 for the permittivity and 0.91 for the remnant polarization models (Figures 11-12). Each model displayed strong interactions between the power and both the percent oxygen in the

plasma and the deposition temperature, further indicating the complex nature of these sputtered films.

The low temperature model for the permittivity (Figure 11.a) showed a parabolic trend with respect to power with a minimum at 150 W and 10 $\%O_2$, which transitioned to an inverse parabolic relationship at 50 $\%O_2$ with a max at 150 W. The permittivity was also observed to be parabolic across the examined $\%O_2$ range for all powers (maximum approximately at 30 $\%O_2$). These trends continue to 300°C with the exception that increased oxygen content in the plasma was found to generally increase the permittivity of the deposited films (Figure 11.b).

The remnant polarization models for films deposited at 20°C (Figure 12.a) were observed to portray an inverse parabolic relationship with both the power and $\%O_2$, with a maximum in the permittivity at 150 W and 50 $\%O_2$. The power–$\%O_2$ relationship was more complicated as the temperature was increased to 300°C (figure 12.b), where the inverse parabolic nature of the response to oxygen was still prevalent but the maximum decreased to approximately 25 $\%O_2$. The power was observed to transition from a parabolic relationship at 10 $\%O_2$ (minimum at 150 W) to a more linear relationship at 50 $\%O_2$.

4.3. Elevated Temperature Tests

In addition to room temperature electrical testing, limited elevated temperature studies were also performed on specimens R1, R4, and R7. Leakage current testing was conducted at 85°C, 150°C, and 300°C at a maximum voltage for each specimen, which was observed to vary depending on the individual specimen breakdown strength at temperature. Hysteresis loops were also taken for the examined specimens at 150°C to determine the permittivity and remnant polarization at that temperature, as well as to observe any change in electronic behavior.

The leakage currents were observed to increase with increasing temperature, indicative of a decreasing resistance, which is typical for insulating materials as defects allowing conduction to occur are more active at elevated temperatures (Table IV). Following a standard Arrhenius relationship between conductivity (calculated as the inverse of the resistivity based on the I-V measurements) and temperature, the activation

energies were calculated for each of the specimens (Figure 13). Energies of 0.321, 0.165, and 0.887 eV for specimens R1, R4, and R7, respectively, fit well with the wide range of reported energies in the literature for different types of $BaTiO_3$ [2, 18-20].

Hysteresis data was also acquired for these specimens at approximately 150°C. The standard Curie temperature of $BaTiO_3$ is 125°C [21] beyond which all ferroelectric behavior has ceased. As such, it was expected that the hysteresis loops of these specimens at 150°C would result in paraelectric responses. Figures 14-16 show the hysteresis loops of the specimens at 150°C. As opposed to the expected paraelectric behavior, all specimens showed some amount of ferroelectricity. It is interesting to note that the elevated temperature loops follow the original room temperature measurements (Figures 8-10), but the loops appear to widen and display a larger remnant polarization (Table IV). The high temperature hysteresis also displays increased lossy behavior, which is in accordance with the increased leakage current. It has been suggested that thin films with nanocrystalline or amorphous structures may show a Curie region, as opposed to a Curie point [20], which may account for the observed ferroelectric-like behavior of these devices at elevated temperatures.

4.4. Model Verification and Optimization

Following the analysis of the DC electrical responses for the DOE specimens two additional wafers were fabricated. The first was a randomly selected combination of process variables that had not been studied by the DOE, and was used to verify the accuracy of the models. The second was based on a set process conditions determined by the DOE software given a set of optimization requirements.

The model verification condition chosen was processed at 150 W, 30% O_2, and 20°C deposition temperature. Despite the high model R^2 values, the measured values of the room temperature resistance, remnant polarization, and hysteresis based permittivity were significantly different from those predicted by the software (Table V). The room temperature resistance was measured at 166 GΩ, which was approximately 60% above the predicted 104 GΩ. A similar discrepancy was observed with the permittivity; 527 measured versus the 197 predicted. Lastly, the predicted remnant polarization of 42 $\mu C/cm^2$ was significantly over estimating the actual value of 5.4 $\mu C/cm^2$ (84% below the

expected value). These deviations potentially indicate higher order interactions between the variables (e.g. a third order interaction or higher) that was unable to be tested with the Box-Behnken DOE series. Despite these differences, the higher than expected permittivity and resistance indicated a potentially conservative predictive set of models, and were still capable of giving overall trends.

The data from the model verification run was entered into the DOE software to increase the effectiveness of the predicted models. Based on the updated models, an optimization scheme was developed to maximum the permittivity, room temperature resistance, and remnant polarization. The optimized process schedule was determined to be 195W with 16.7% O_2 at 20°C. As with the model verification specimen, the data measured from the optimized condition was found to be significantly below the predicted values. The permittivity was found to be approximately 79% below the predicted value (596 as opposed to 2791), with the resistance and remnant polarization to be 31% and 94% below the values given by the models. Again, these deviations in the measured values from those predicted by the models are likely due to higher level interactions within the system that was unable to be measured with a limited sample DOE regimen like the Box-Behnken used. Further testing under additional deposition conditions would likely result in more accurate predictive models, and gives increased understanding of the effects generated by the various process parameters. The easiest method in which to accomplish this task would likely be to develop a 3^3 full factorial DOE which would require 127 specimens to be created and analyzed.

4.5. Discussion

The previous paper in this series [15] related the observed AC dielectric properties to the competing factors of oxygen ion activity and film oxidation during the deposition of the $BaTiO_3$ films. To briefly restate, the process of sputtering in a plasma containing O_2 results in the formation of negatively charge oxygen ions, O^{2-}, that are propelled by the plasma sheath away from the sputter target and towards the substrate, potentially causing damage to the film in the form of material removal or added film defects [1, 22, 23]. The literature reports that increasing the concentration of O_2 in the plasma increases concentration of O^{2-} ions [17], as does increasing the sputter power [10,

24]. Although not directly stated in the literature, an increase in temperature is also likely to increase the concentration of O^{2-} ions in the plasma due to a lowering of the energy required for ionization.

While it is desirable to minimize the effects of the O^{2-} ions by decreasing their concentration in the plasma, it is also necessary to ensure complete oxidation of the $BaTiO_3$ film to ensure adequate electrical properties [10, 25]. The two most accepted methods to achieve the increased oxidation of the films is to increase the amount of O_2 present during deposition and to increase the temperature, both of which increase the probability of the film to oxidize via atomic contact in the plasma and through diffusion on the substrate. Decreasing the oxidation of $BaTiO_3$ films has been shown to decrease the film's resistance [25, 26], and to either increase [14, 20] or decrease [2, 11] the measured permittivity. It was proposed in part one of this series that the competition between these two factors drives observed electrical property changes between the different sputtering conditions [15]. If correct, this competition should also be able to account for the DC electrical properties reported in this paper.

The permittivities obtained from the hysteresis loops were found to be approximately one order of magnitude larger than those found via AC testing, but otherwise displayed the same general trends in the predictive models (Figure 2). This suggests that the same phenomena that were responsible for the AC permittivity changes were also responsible for those changes observed in the DC permittivity. To avoid repetition, the interested reader is directed to the previous paper for details regarding the interaction of the negatively charged oxygen ions and the film oxidation potential as it relates to the measured permittivity.

The resistance at 1 V was also found to follow the proposed competing forces concept (Figure 4). At 20°C the oxidation state of the film is primarily related to the amount of oxidation the Ba and Ti atoms can achieve during flight from the target to the substrate as no significant diffusion is possible without increased thermal input. With this assumption, a look at the low temperature model for the resistance showed that an increased $\%O_2$ resulted in increased resistance as long as the sputter power was kept below 150 W. At powers above 150 W, an increase in $\%O_2$ was found to decrease the resistance, suggesting the increased concentration of O^{2-} ions was increasing with the

increased power, and thus causing more film damage than film oxidation. By increasing the deposition temperature, and thus increasing the energy available in the system, more interaction was created between the two factors, resulting in a more complex response surface. At powers below 150 W, an increase in $\%O_2$ from 10% to 30% resulted in a decreased resistance as a result of the increased damage from the higher concentration of O^{2-} ions. As the $\%O_2$ was further increased between the range of 30% to 50% the resistance was found to increase due to the increased film oxidation as a result of the increased substrate temperature. Again, as the power was increased to greater than 150 W an increase in $\%O_2$ resulted in a general decrease in resistance due to increased film bombardment by the elevated O^{2-} ion activity generated by the higher power plasma.

The remnant polarization has not been readily addressed in the literature as a generally reported material property. As such, it is more difficult to determine the effects of the O^{2-} ions and film oxidation effects on this particular property. Given the fit of the other dielectric responses to the proposed competing forces concept, it can be assumed that the remnant polarization should likewise follow similar trends. As the degree of polarization is related to the movement of the Ti atom in the octahedral interstitial site of the oxygen atoms [1, 27, 28], it can be assumed that the closer the film is to its stoichiometric oxidation state the higher the remnant polarization is likely to be. Given this assumption, the low temperature model for the remnant polarization (figure 12) shows that an increase in $\%O_2$ at all power levels results in an increased remnant polarization. Likewise, at powers below 150 W, an increase in power was found to increase the stored charge. Both responses are due to the increased oxygen entrapped in the films. When the power was increased above 150 W, the activity of the O^{2-} ions began to take effect, and the resultant material removal from the substrate decreased the oxidation state of the film and decreased the remnant polarization. At elevated temperatures the film was found to retain a higher polarization as the $\%O_2$ was increased from 10% to 30%, but decrease as the concentration of O_2 was further increased to 50%. Again, this behavior fits the concept of the competing oxidation (which occurred at lower O_2 concentrations) and O^{2-} ion damage (occurring at higher O_2 levels).

5. Summary

The DC based dielectric properties of thin film $BaTiO_3$ with Ni electrodes have been determined and subsequently modeled for a DOE series of experiments over a wide range of oxygen concentrations (10% to 50%), sputter powers (100 W to 200 W), and deposition temperature (20°C to 300°C). The insulation resistance of the $BaTiO_3$ films were found to be between 16 and 270 GΩ at an applied voltage of 1 V. The I-V characteristics showed a system that was primarily symmetric across a range of deposition conditions, and the 10 MV/cm electric fields that were achievable with these devices. Hysteresis measurements showed a mix responses including ferroelectric (5 of 13 specimens), paraelectric (2 of 13), and lossy ferroelectric (4 of 13), with 2 specimens showing a mix of these three responses within the same sample depending on the location measured. Permittivities calculated from the hysteresis loops determined values of 170 to 10,000 depending on the deposition conditions of the $BaTiO_3$. Limited elevated temperature studies showed increasing conduction with increasing temperature, and corresponding activation energies of 0.3 eV to 0.9 eV for three specimens studied. Hysteresis loops obtained at 150°C also showed that persistent ferroelectric behavior beyond the accepted Curie point of bulk $BaTiO_3$, suggesting that the nanocrystalline or amorphous nature of these sputtered films has resulted in a Curie region as opposed to a Curie point.

The responses for the permittivity, remnant polarization, and resistance of these devices were statistically analyzed, which allowed for the development of models for the prediction of dielectric properties based on a set of process conditions. Despite the high R^2 values of these models ranging from 0.90 to 0.99, the models did not accurately predict the dielectric behaviors of two additional specimens. This was related to the likely presence of higher order interactions between the process variables that was able to be tested with the limited samples required for the Box-Behnken DOE regimen.

As with the AC properties, the modeled DC properties were found to follow a similar trend that were consistent with the activity of negatively charged oxygen ions in the plasma during deposition competing with the oxidation mechanisms of the depositing film. Based on the work presented in both above and in the previous paper in this series, it is proposed that the apparent, conflicting trends reported for the dielectric properties of

sputtered $BaTiO_3$ are likely due to the investigation of different portions of the same system.

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Figures

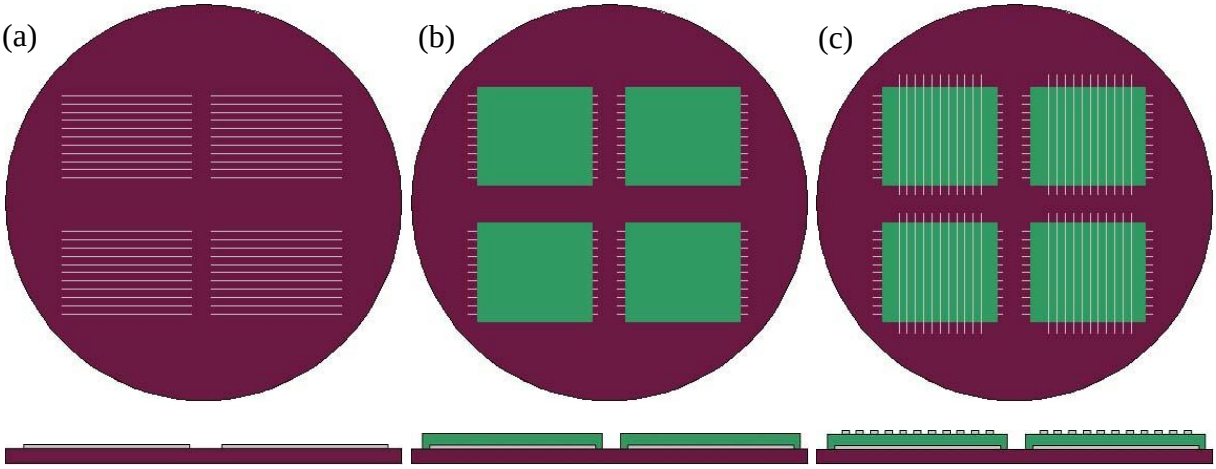

Fig. 1 – Process sequence followed for the patterned deposition of a single dielectric layer capacitor. 1st electrode layer (a), dielectric (b), and 2nd electrode layer (c). Top images are plan view looking at surface of substrate, and bottom images are cross sections. Vacuum was broken between layers to allow the exchanging of physical masks between depositions.

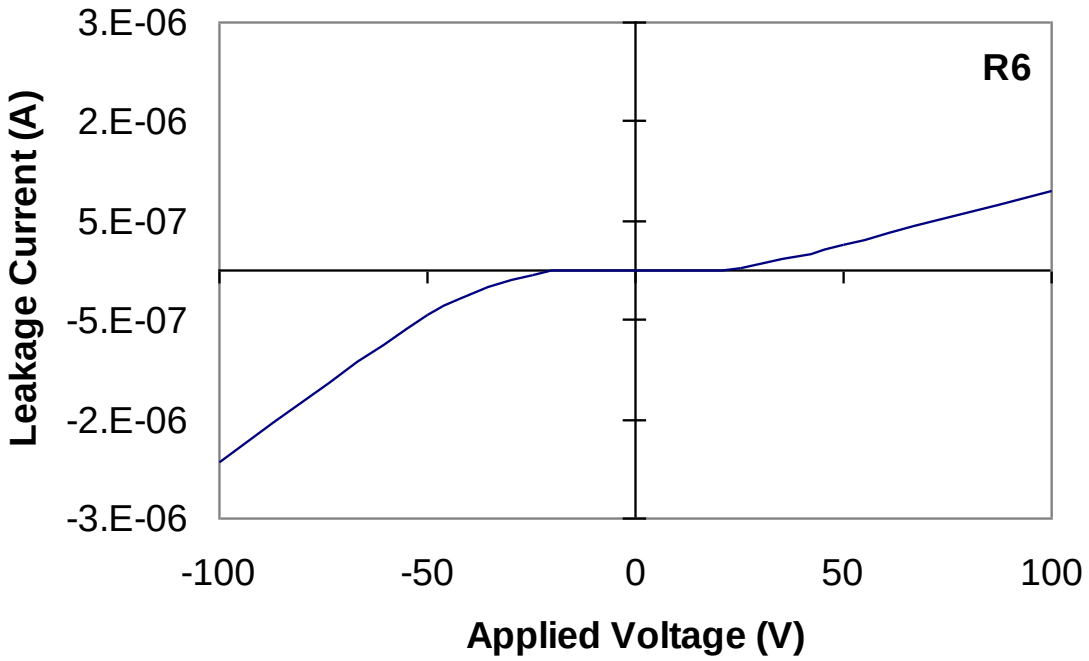

Figure 2 – I-V plot for R6 showing the two conduction mechanisms observed for most specimens: ohmic response at voltages < ±1V and either ES or PF at voltages > ±1V.

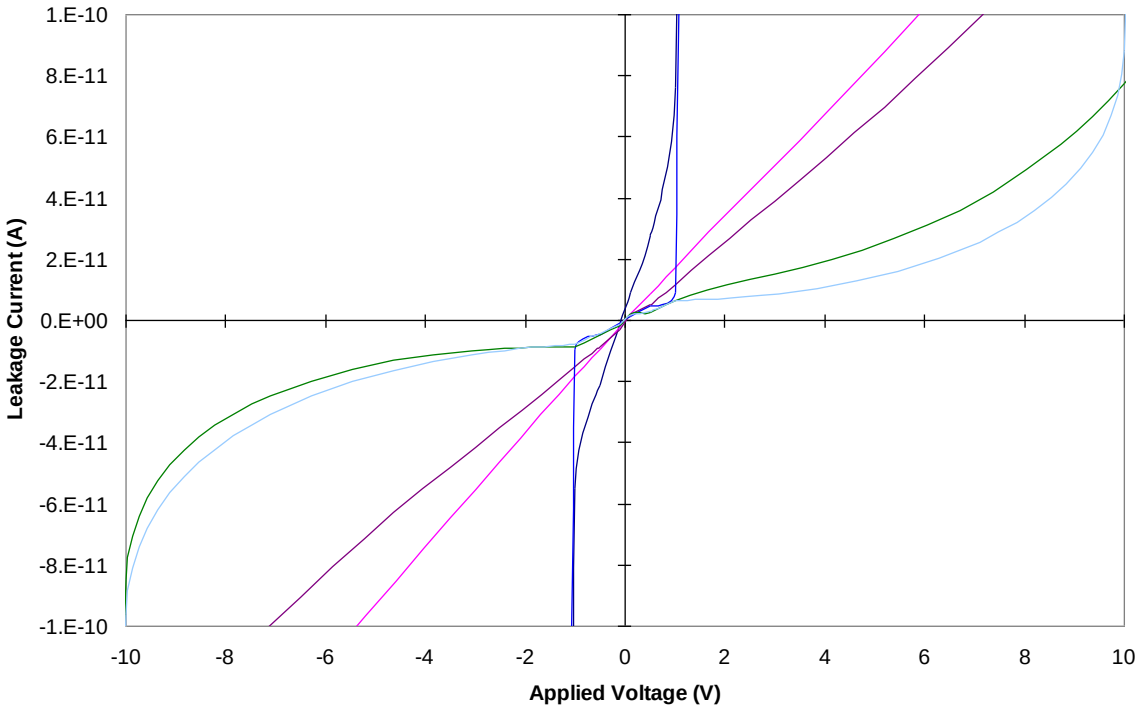

Figure 3 – Close up of the ±10 V region of the I-V plot showing a variety of the symmetrical behaviors occurring within the specimens at these lower voltages.

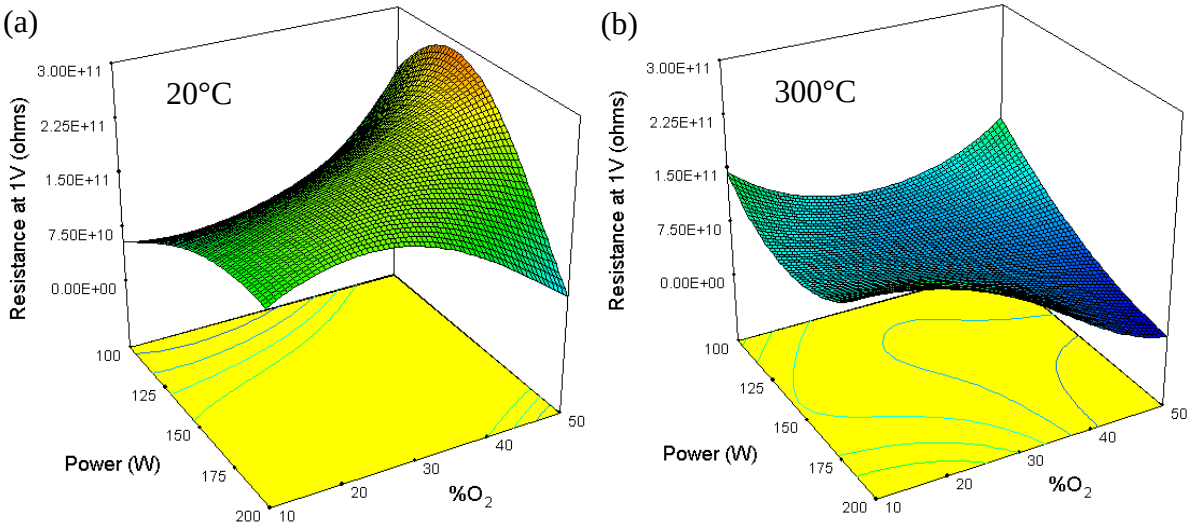

Figure 4 – Predictive surface models developed for the room temperature resistance at 1 V of sputtered $BaTiO_3$ deposited at 20°C (a) and 300°C (b). The model R^2 value was 0.90.

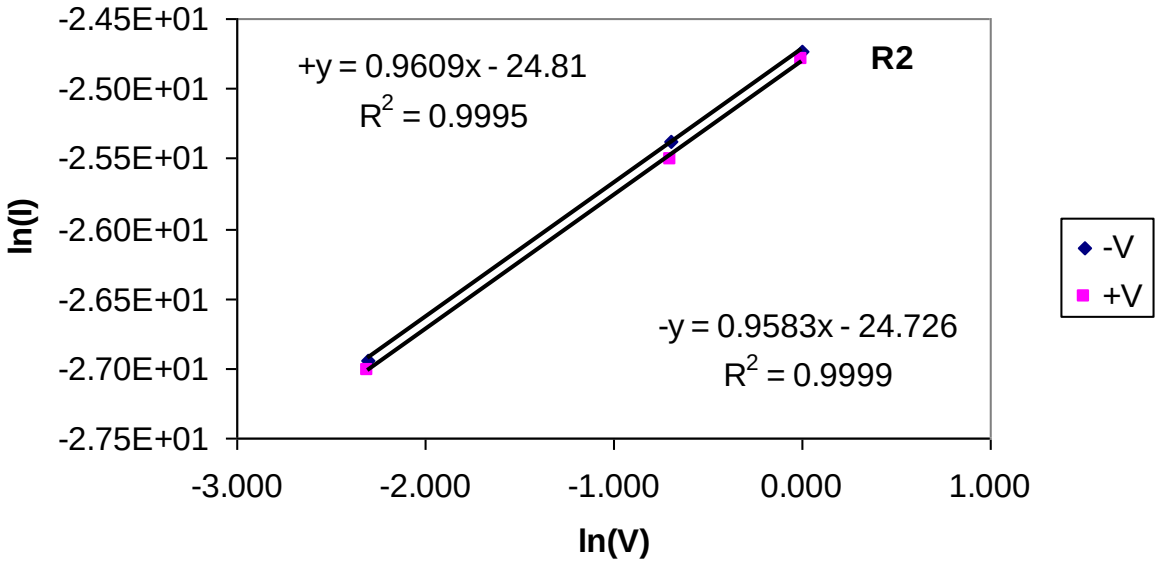

Figure 5 – Typical ln(I) vs ln(V) with linear regression for the determination of the power exponent in the ±1 V region.

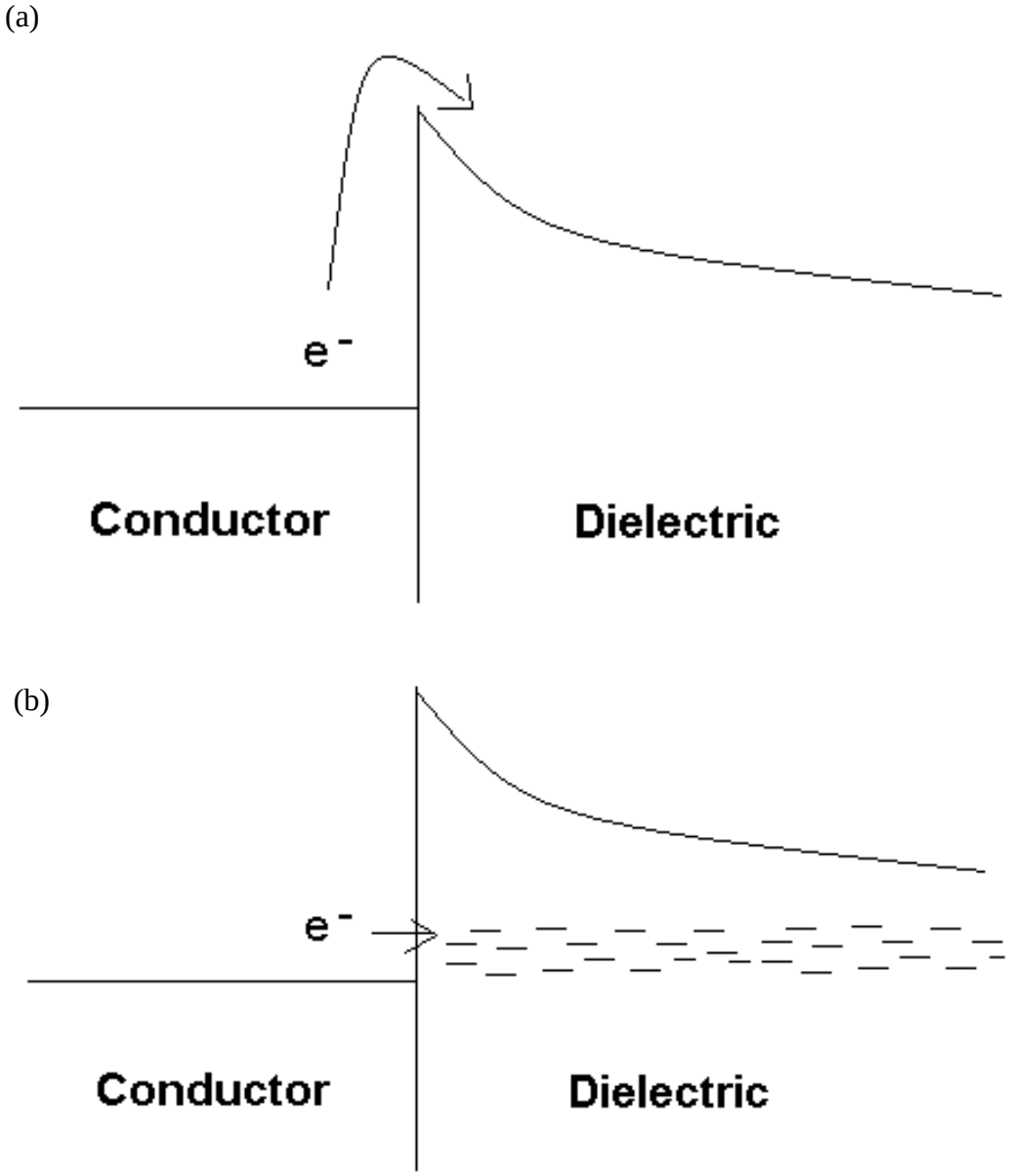

Figure 6 – Schematic diagrams for the Enhanced Schottky (a) and Poole Frenkel (b) conduction mechanisms at the interface of a conductor and insulator.

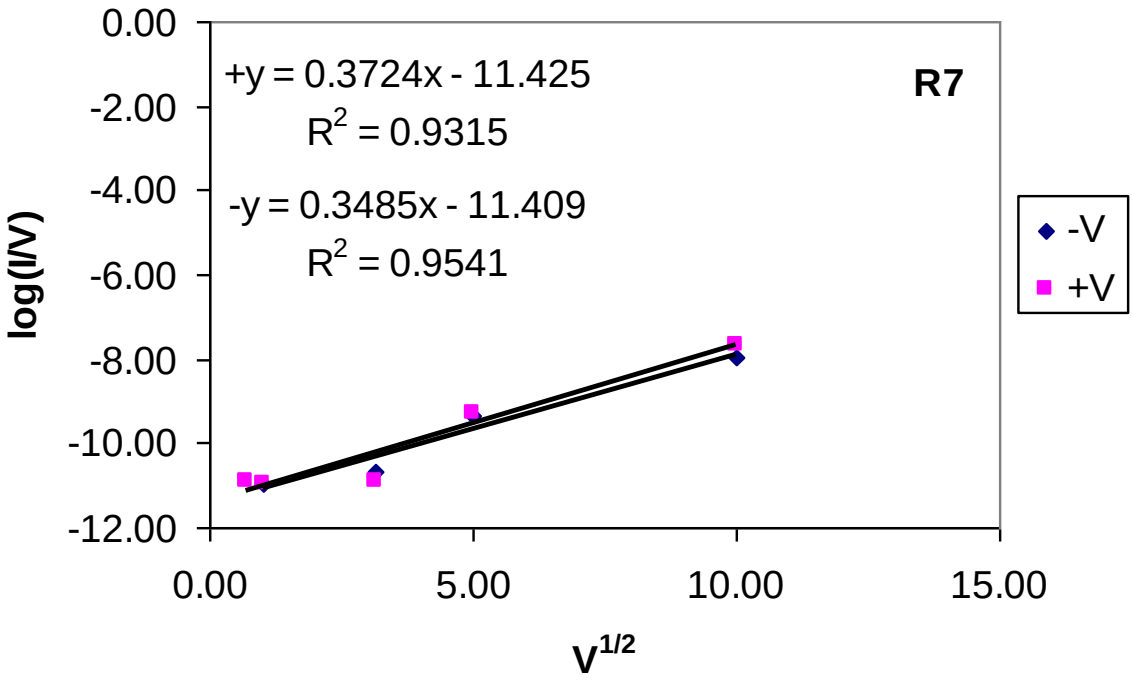

Figure 7 – Typical plot used to determine the β value for the high field conduction mechanism of the specimens.

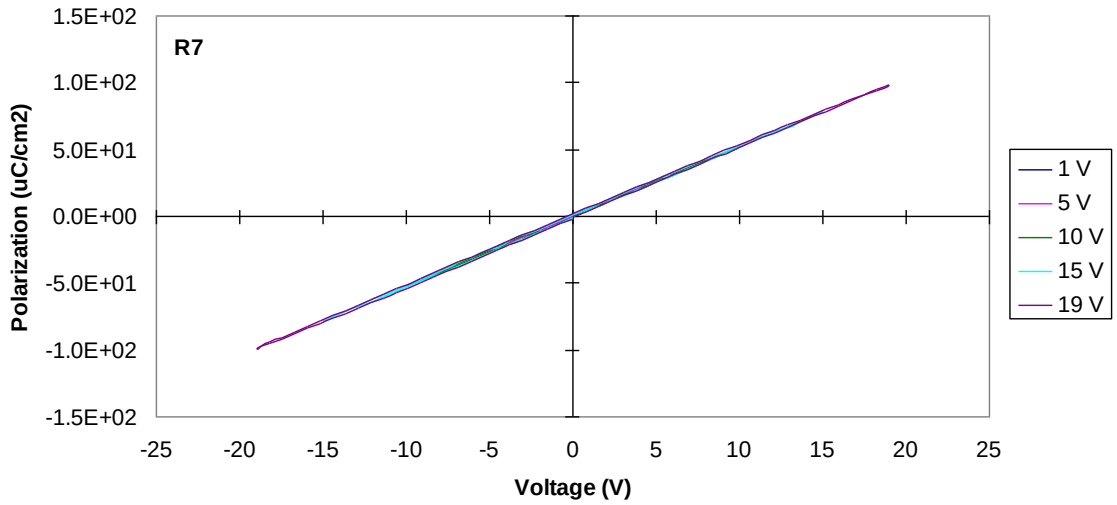

Figure 8 – Typical paraelectric response observed for the specimens R3 and R7.

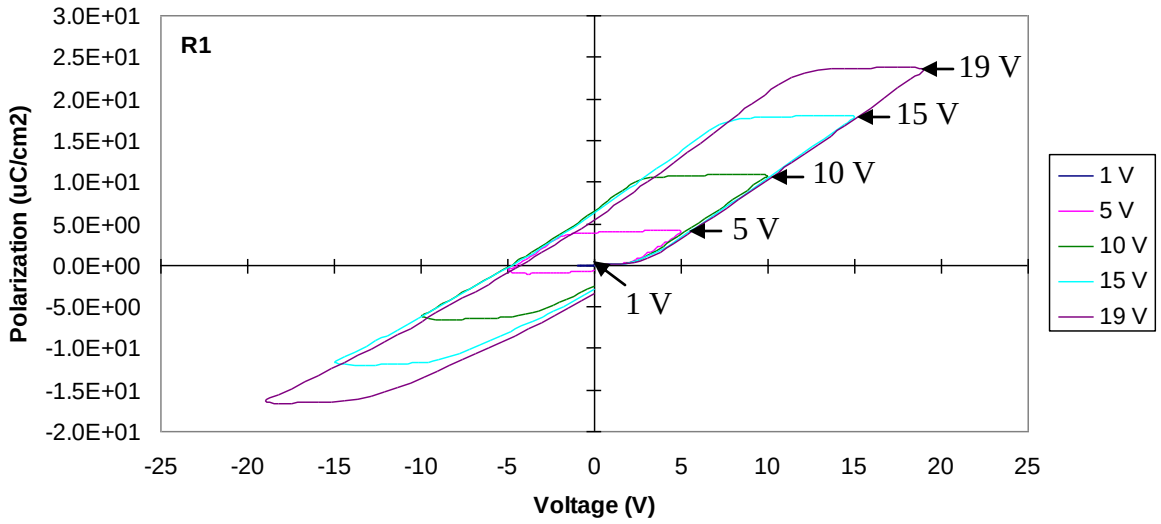

Figure 9 – Typical ferroelectric response observed in specimens R1, R5, R6, R11, and R13.

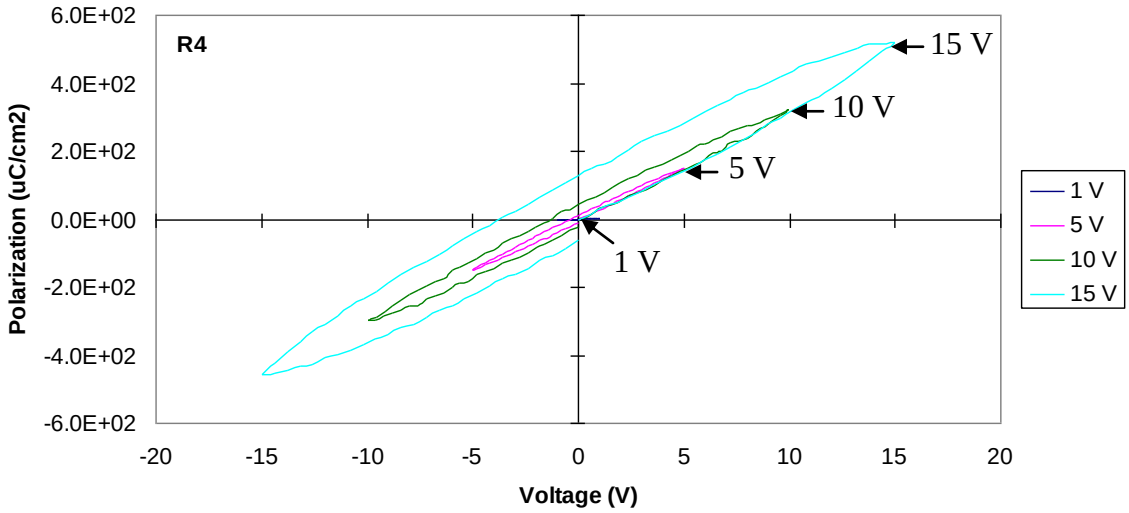

Figure 10 – Typical lossy ferroelectric response observed with specimens R4, R8, R10, and R12.

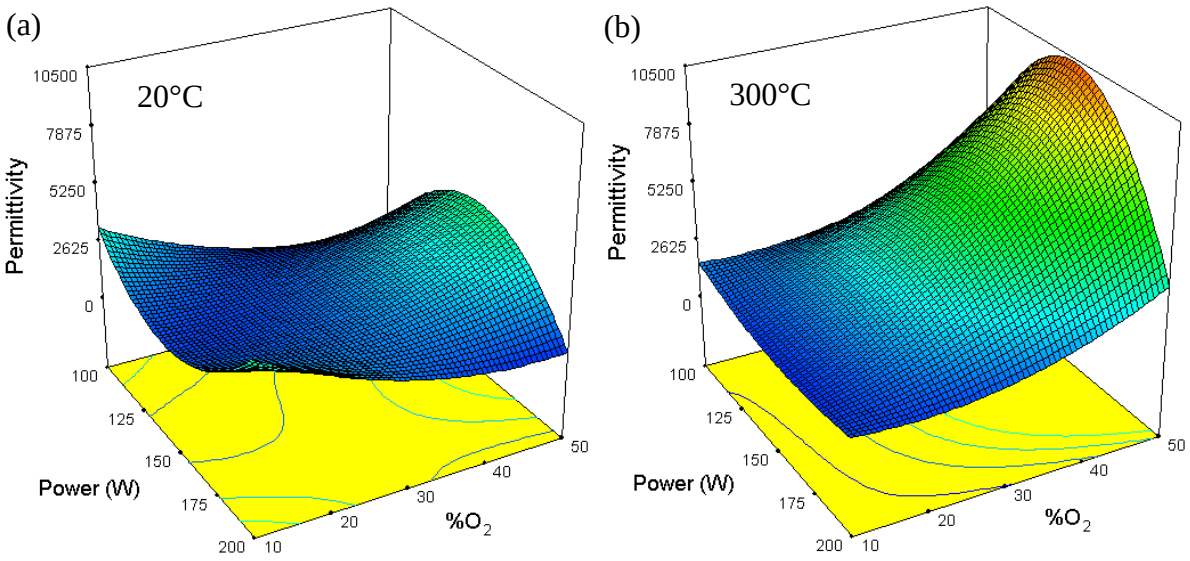

Figure 11 – Predictive surface models developed for the permittivity based on hysteresis data for sputtered $BaTiO_3$ deposited at 20°C (a) and 300°C (b). The model R^2 value was 0.98.

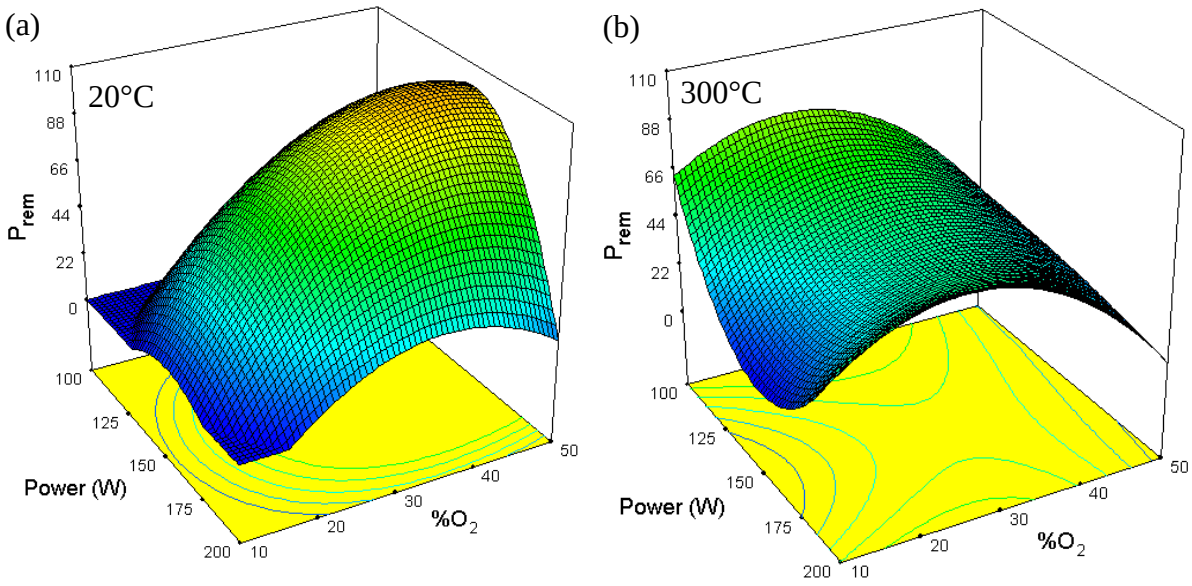

Figure 12 – Predictive surface models developed for the remnant polarization observed on hysteresis plots for sputtered $BaTiO_3$ deposited at 20°C (a) and 300°C (b). The model R^2 value was 0.91.

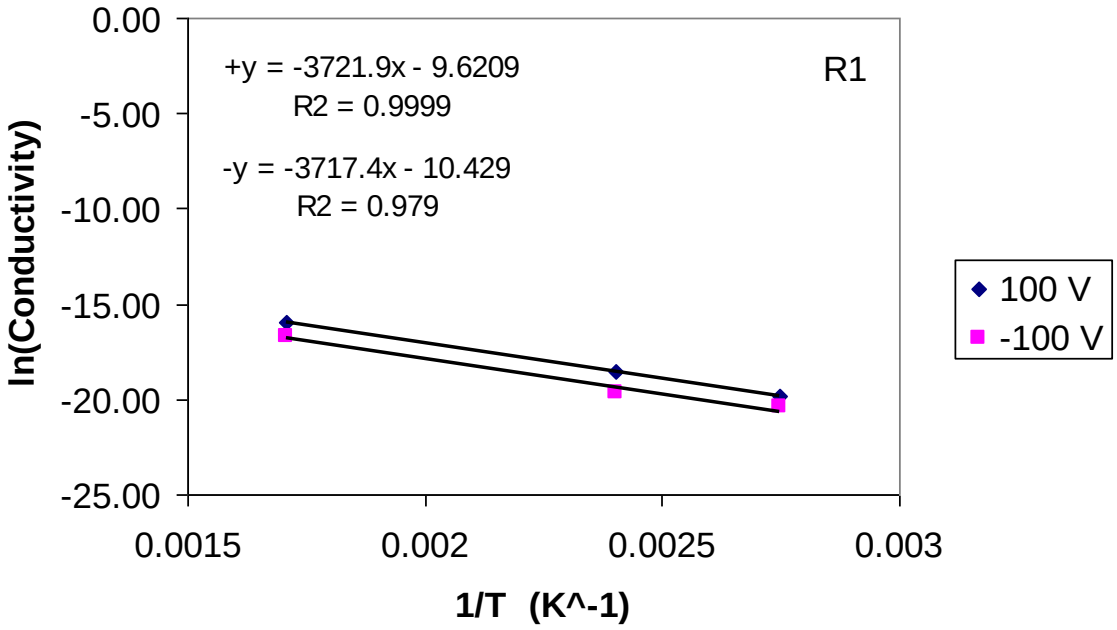

Figure 13 – Arrhenius plot of the temperature based leakage currents for R1 along with linear regression. The slope of the line was converted to eV for the reported activation energies in Table IV.

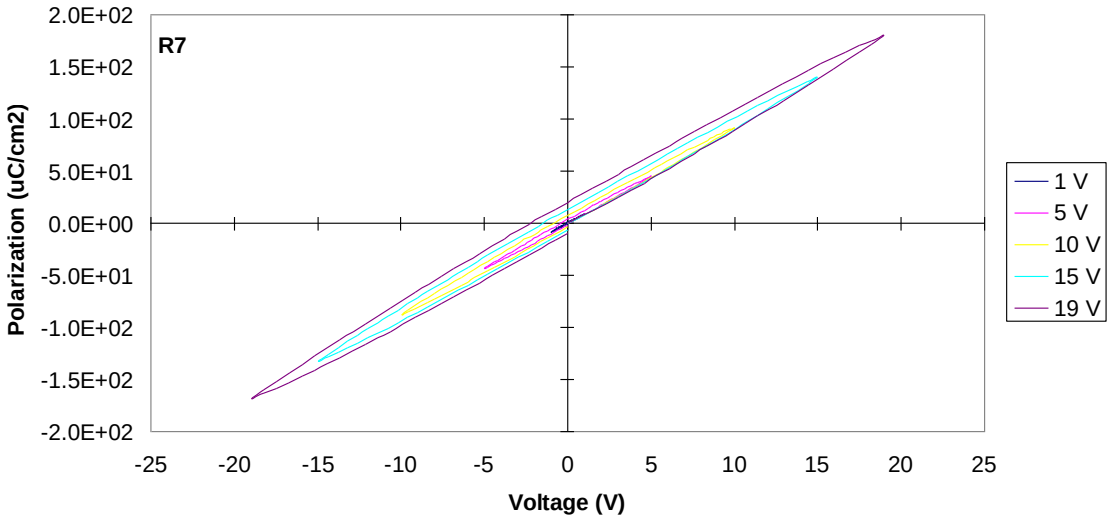

Figure 14 – Hysteresis loop for R7 taken at 150°C showing an increased remnant polarization over that observed at room temperature (refer to Figure 8).

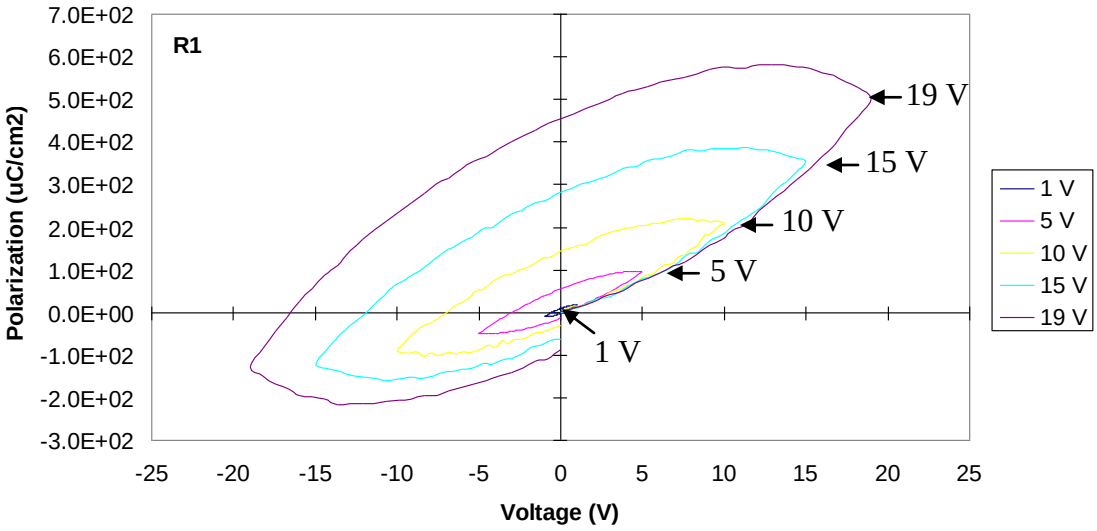

Figure 15 – Hysteresis loop for R1 taken at 150°C showing an increased remnant polarization over that observed at room temperature (refer to Figure 9).

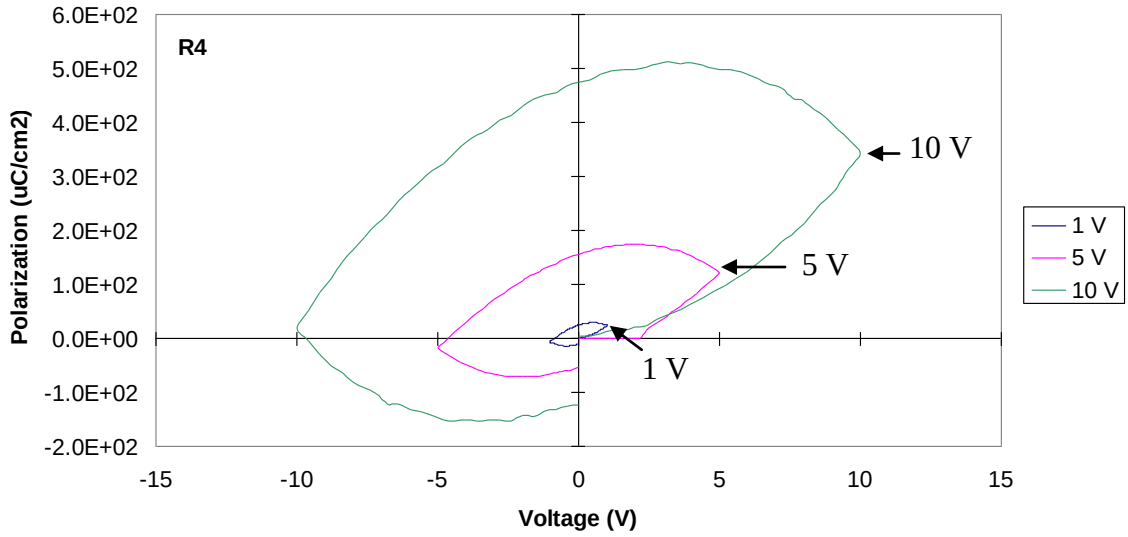

Figure 16 – Hysteresis loop for R4 taken at 150°C showing an increased remnant polarization over that observed at room temperature (refer to Figure 10).

Tables

Table I. Process schedules for the 13 DOE specimens

	Power (W)	**O2 Conc. (%)**	**Dep. Temp. (K)**
R1	200	50	433
R2	100	30	293
R3	150	10	293
R4	150	50	293
R5	100	10	433
R6	150	50	573
R7	150	10	573
R8	150	30	433
R9	100	30	573
R10	200	30	293
R11	200	30	573
R12	200	10	433
R13	100	50	433

Table II. Compilation of the data obtained from the I-V plots of the DOE specimens

	Voltage of Asymmetry (V)	**Resistance at 1 V (GΩ)**	**Breakdown Strength (MV/cm)**	**n-Exponent from Ohmic Region (< 1V)**	**Estimated β**		**Measured β (> 1 V)**
					β_{PF}	**β_{ES}**	
R1	> ±100	16	8.9	0.86	0.114	0.227	0.914
R2	±25	60	8.0	0.96	0.122	0.243	0.013
R3	±10	140	1.9	1.7	0.096	0.192	1.153
R4	> ±10*	270	0.94	0.40	0.085	0.170	1.541
R5	> ±25*	85	1.9	1.0	0.094	0.189	0.058
R6	> ±100	47	0.99	0.30	0.089	0.178	0.272
R7	±25	92	8.2	0.64	0.163	0.326	0.372
R8	> ±10*	110	0.87	0.84	0.108	0.216	2.043
R9	±5	76	2.0	0.96	0.102	0.203	0.103
R10	> ±25*	190	0.8	0.74	0.102	0.204	0.907
R11	±10	160	1.7	0.89	0.124	0.248	0.095
R12	±10	160	3.6	0.88	0.127	0.255	0.083
R13	> ±25*	160	2.5	0.96	0.128	0.256	0.535

*Specimens broke at next test voltage point, and further symmetry is unknown

Table III. Average permittivities and remnant polarizations based on the hysteresis loops acquired for the DOE specimens

	Permittivity	**Remnant Polarization ($\mu C/cm^2$)**
R1	170 ± 10	6.6 ± 0.7
R2	570 ± 440	7.2 ± 3.8
R3	970 ± 140	8.1 ± 4.2
R4	3,500 ± 1,400	100 ± 23
R5	640 ± 110	9.3 ± 2.6
R6	10,000 ± 870	19 ± 2.6
R7	690 ± 20	2.1 ± 0.6
R8	1,200 ± 83	64 ± 22
R9	2,000 ± 860	77 ± 21
R10	1,400 ± 180	31 ± 3.8
R11	660 ± 76	38 ± 13
R12	810 ± 47	8.4 ± 5.8
R13	490 ± 89	6.8 ± 4.2

Table IV. Results from the elevated temperature testing performed on R1, R4, and R7

	Voltage Tested (V)	**Test Temperature**	**Leakage Current (A)**	**Activation Energy (eV)**	**Permittivity at 150°C**	**Remnant Polarization at 150°C ($\mu C/cm^2$)**
R1	±100	85°C	$9.9x10^{-9}$	0.321	3500 ± 440	160 ± 31
		150°C	$1.2x10^{-7}$			
		300°C	$3.8\ x10^{-6}$			
R4	±1	85°C	$8.6\ x10^{-8}$	0.165	4300 ± 1000	25 ± 0.7
		150°C	$8.9\ x10^{-8}$			
		300°C	$3.6\ x10^{-8}$			
R7	±15	85°C	$2.9\ x10^{-9}$	0.887	1300 ± 130	20 ± 2.0
		150°C	$1.4\ x10^{-8}$			
		300°C	$2.2\ x10^{-5}$			

Table V. Predicted and measured room temperature values for the DC responses of a $BaTiO_3$ film sputtered at 150 W, 30% O_2, and 20°C

	Resistance at 1 V (GΩ)	**Permittivity**	**Remnant Polarization** ($^{\mu C}/_{cm^2}$)
Expected Value	100	200	42
Measured Value	170	530	5.4
Percent Difference	60%	170%	-87%

Table VI. Predicted and measured room temperature values for the DC responses of the optimized $BaTiO_3$ film sputtered at 195 W, 16.7% O_2, and 20°C

	Resistance at 1 V (GΩ)	**Permittivity**	**Remnant Polarization** ($^{\mu C}/_{cm^2}$)
Expected Value	210	2800	31
Measured Value	150	600	1.8
Percent Difference	-31%	-79%	-94%

PAPER IV

Thickness effects on the AC and DC electrical behavior of RF-sputtered $BaTiO_3$ nano-capacitors with Pt or Ni electrodes

by

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Abstract

Nano-scale $BaTiO_3$ capacitors were deposited on Si wafers at dielectric thicknesses of approximately 25, 50, 100, and 200 nm using RF-magnetron sputtering with either 25 nm thick Ni or Pt electrodes. Multiple DC and AC tests were conducted on these devices to determine the effects of $BaTiO_3$ thickness on the measured dielectric behaviors. All films were observed to have non-linear responses for resistance, permittivity, and loss with respect to dielectric thickness. The permittivity was found to follow a standard dead layer model behavior with measured values ranging from approximately 350 to 1700 for Ni electrodes and approximately 100 to 2500 for Pt electrodes, with losses from 0.020 to 0.250 and 0.025 to 0.140 for Ni and Pt electrodes, respectively. Resistances were observed to vary from 15 to 300 GΩ with Ni and $8x10^{10}$ to $4.7x10^{12}$ Ω-m with Pt, with the differences attributable to formation mechanisms of the interfacial layers between the $BaTiO_3$ and the metal electrodes.

1. Introduction

Dielectric thin films with high permittivity and resistance and low loss have many applications in the electronics industry. One of the most common industrial dielectric materials for capacitors is $BaTiO_3$ [1]. Typical applications for $BaTiO_3$ thin films include dynamic random access memory (DRAM) [2-5], tunable microwave devices [5-8], as well as more traditional discreet, solderable capacitors [1, 4, 6, 7]. In order to achieve higher capacitance densities for high-end electronic devices, the fabrication of capacitive components using traditional tape-casting technology becomes a limiting factor in achieving sub-micron dielectric layers [9, 10]. This limitation has made thin film techniques, such as sputtering, a potentially viable alternative for the fabrication of nano-scale ceramic capacitors.

As new techniques are developed to achieve the fabrication of these high energy-density devices, a better understanding of the electrical responses at the thicknesses being investigated is necessary. Limited work has been performed on the thickness dependence of sub-micron thick $BaTiO_3$ films deposited via magnetron sputtering. The majority of sources available in the literature on $BaTiO_3$ thin films deal with thicknesses greater than 100 nm [10-14], with only a few testing devices with dielectric thicknesses below 100 nm [15-17]. Of these available sources, the reported trends varied significantly with some sources suggesting a decrease in permittivity [12, 14-17], while others found an increase [13] with decreasing thickness. It is interesting to note that the first subset of the data indicating a decreasing permittivity with decreasing thickness were typically investigating thinner films (20 – 750 nm) whereas the report on increasing permittivity dealt primarily with thicker sputtered films (600 – 6,000 nm). Deviation is also found in the limited loss data available from these studies, with the data indicating either an increased loss with decreasing thickness [13, 14], or the presence of either a maximum or minimum at around 300 nm [10, 11]. Given these discrepancies in the available literature, a study on the thickness effects as a function of processing conditions and electrode material choice was performed.

2. Procedure

P-type Si wafers of <111> orientation with 1 μm thermal oxide were used as the substrates for all experiments. The 4 inch wafers were cleaned using a series of acetone, methanol, and DI water with a subsequent spin drying and dehydration bake at 200°C. For the purpose of statistical analysis, the wafer was patterned with a grid of 11 x 11 capacitors for each wafer quadrant resulting in 484 devices per wafer. The bottom electrodes were patterned with a physical mask consisting of 11 parallel lines measuring approximately 75 μm wide by 2.4 cm long to a thickness of ~20 nm per quarter wafer using a Denton Discovery-18 sputter deposition system with 3 inch targets (Fig. 1.a). The $BaTiO_3$ dielectric was patterned using another physical mask with 1 opening per quarter wafer measuring 2.7 cm square to the desired thickness of 25, 50, 100, or 200 nm (Fig. 1.b). The electrode mask was then rotated 90° from the bottom electrode layer, and the top electrodes were deposited to a thickness of ~20 nm (Fig. 1.c). This process resulted in 121 capacitors per quarter wafer with active device areas of 5.43×10^{-5} cm^2 each. Plasma composition for all depositions was controlled with two mass flow controllers attached to Ar and O_2 cylinders. The thickness of each of the three layers was measured using a Tencor Alpha-Step 200 profilometer.

For these investigations 3 different $BaTiO_3$ deposition conditions were analyzed at approximately 25, 50, 100, and 200 nm thickness between symmetrical electrodes of either Ni or Pt electrodes at approximately 20 nm thickness each (e.g. 20 nm bottom and 20 nm top). The three conditions were based on previous work investigating the effects of percent O_2, RF-power, and deposition temperature used during sputtering, and are detailed in Table I. The first series of electrical testing performed on these devices was in the form of current voltage (I-V) curves. The results from these tests gave a measure of the films' insulation properties. The second series of testing allowed the direct measurement of capacitance and loss values using a precision LCP meter.

Electrical AC measurements were then made with an HP 4149 at 1 kHz to measure capacitance and loss under a 1 V_{rms} potential with 0 V bias. Based on the measured capacitance and thickness values, the effective permittivity of the sputtered $BaTiO_3$ films were calculated. Additionally, DC measurements were made via I-V plots using an HP 4140B pA Meter from 0.1 to 100 V, with 30 second soak at voltage.

3. Results and Discussion

3.1. DC Properties

Current-voltage (I-V) measurements were taken to determine the effects of thickness variation on the leakage current response to a given applied electric field. These plots also allowed the observation of any conduction mechanism transitions occurring within the measured range of fields. Each specimen was measured in 3 different, randomly selected locations from 0.1 to 100 V with both positive and negative polarity, and the averages calculated at each voltage (Figures 2–3). In order to allow the plotting of the leakage currents on a log scale, all leakage currents are plotted as positive values. Plotting on a log scale makes it possible to determine symmetry between positive and negative potentials. For comparison purposes between the different dielectric thicknesses for each condition, the x-axis was plotted as applied field ($^{V}/_{m}$). It is interesting to note that both of the electrode materials exhibited high stability without breakdown at fields in excess of $1.0x10^{8}$ $^{V}/_{m}$ (Table II). These values were within relative agreement with other sputtered $BaTiO_3$ films reported within the literature [5, 13, 16, 18], and may be related to the "disorderliness" of the nanocrystalline or amorphous nature of the films impeding the ability of the electrons to rapidly traverse the film thickness.

The I-V plots also show the presence of two or more conduction mechanisms occurring depending on the applied field, specimen thickness, and $BaTiO_3$ deposition conditions. The first transition was found to uniformly occur in the Ni electrodes at ~ $2x10^{7}$ $^{V}/_{m}$ and in the Pt electrodes at ~ $5x10^{6}$ $^{V}/_{m}$, changing from a log-based trend at lower fields to more complex trends at higher fields. The difference in field strengths required to initiate this transition may be related to the differences in work functions of the two metals, thus modifying the activation energies required to overcome this interfacial barrier (Figure 4). A second transition to a third conduction mechanism was observed in several of the samples, occurring around $1–2x10^{8}$ $^{V}/_{m}$ for the two thicker (100 and 200 nm) $BaTiO_3$ films. The exceptions were the 50 nm thick R7-Ni and 25 nm thick R4-Pt which also showed a third conduction mechanism taking effect at approximately $1x10^{8}$ $^{V}/_{m}$.

The I-V plots also showed symmetric electrical responses for all specimens at fields between $5x10^{6}$ $^{V}/_{m}$ and $2x10^{7}$ $^{V}/_{m}$ for Pt and Ni electrodes, respectively, with both positive and negative polarity (prior to the 1st conduction transition). This indicates that the electrodes were chemically and electronically symmetric; namely that if there are interfacial reaction compounds or electronic effects occurring between the electrode and dielectric materials, they are present at the interfaces of the $BaTiO_3$ with both the top and bottom electrodes. These interfacial effects could be in the form of compounds from a reaction between the metal and dielectric [2, 19, 20] and/or the presence of a low permittivity layer, also known as a dead layer or space charge layer [12, 17, 21]. Any type of interfacial property, whether a physical material or an electrical barrier, will have a distinct set conduction mechanisms and an individual breakdown strength, which will affect the overall shape of the I-V plots. The presence of these interfacial effects are better observed through the investigation of the AC response behaviors over a change in dielectric thickness than can be done with I-V based property trends. Despite the nature of the interfaces, the presence of symmetry in the I-V plots indicates that whatever is occurring at one interface is occurring in equal measure at the opposite interface.

A measure of quality for any insulating film is the resistance at a given voltage. Assuming an ohmic relationship between the voltage and current at any set voltage (i.e. V=IR), the resistances of the films were calculated at 1 V and plotted versus $BaTiO_3$ thickness (Figure 5). Two trends are noticed on this plot. First, the Ni electrode specimens typically exhibit a higher resistance than the Pt electrode specimens. This again may be due to the presence of some interfacial effects between the electrodes and dielectric materials. As Ni is more reactive than Pt, it more likely that the Ni electrodes are interacting with the $BaTiO_3$ to form an interfacial film with a resistance higher than that of the metallic Ni, resulting in a system with 3 resistors in series (e.g. a “thick” interfacial layer, $BaTiO_3$, and a “thick” interfacial layer) effectively increasing the measured resistance of the devices. The second trend observed on the resistance-thickness plot was the maximum and minimums apparent with Ni electrodes that were otherwise absent with Pt electrodes. This phenomenon is not currently understood, but may be a result of the formation mechanisms of the interfacial layers during the different

deposition conditions for the $BaTiO_3$. The samples with Pt electrodes show the more expected decrease in resistance with decreasing thickness.

Neither the Ni nor the Pt electrodes showed a linear relationship as would be expected from a constant resistivity material following the general resistance equation:

$$R = \rho\left(L/A\right) \qquad <1>$$

where ρ is the resistivity of the material, L is the length of the resisting element (thickness in this case), and A is the cross-sectional area. The lack of linearity in both the Ni and Pt specimens further indicates the presence of a secondary, interfacial layer forming during deposition of these devices.

3.2. AC Properties

In addition to gaining a reliable measure of capacitance and loss values for these devices, the measurement of AC properties provided the opportunity to better understand the electrical interaction of the electrode and dielectric materials. Capacitance and loss data were taken at 1 kHz for 3 randomly selected locations per sample (Table III). The capacitance and thickness measurements were used to calculate the effective permittivity of the devices. The effective permittivity and measured loss values for each specimen was then plotted against $BaTiO_3$ thickness (Figures 6–7). The first general observation is the peak in permittivity at roughly 100 nm of $BaTiO_3$ thickness seen on all but the R7-Pt samples. It should also be noted that the greatest amount of variation in the data (in the form of the standard deviations) was observed at this thickness as well. This was also the same thickness at which the Ni samples showed the relative maximum or minimum in resistance. This may be the thickness where the interaction of the interfacial layers with the $BaTiO_3$ reaches its maximum effect. The second general observation from the plots in Figures 6 and 7 is the minimal change in loss until the thickness was reduced to 50 nm or below, at which point it typically increased to above generally acceptable loss values (i.e. > 0.100). This decrease in loss may be due to the lack of dielectric material available to moderate the in-phase current passing through the $BaTiO_3$.

The non-linear thickness response for the permittivity of thin films has been observed in multiple sources [12, 14, 17, 22]. The general capacitance equation is:

$$C = \varepsilon_o \varepsilon_r (A/d) \quad <2>$$

where ε_o is the permittivity of free space, ε_r is the effective permittivity of the dielectric, A the interaction area, and d the thickness of the dielectric; which can be rewritten as:

$$\varepsilon_r = Cd/\varepsilon_o A \quad <3>$$

This states that there is a linear relationship between the effective permittivity and the thickness of the dielectric. This trend has been found to be reliable for bulk ceramic films (i.e. on the order of microns or tens of microns and greater), but studies with thin films have shown that an interfacial phenomenon begins to dominate at sub-micron dielectric thicknesses and has been termed the dead-layer model. This interfacial phenomenon can be modeled with the assumption that the interface will act as a separate capacitive device, thus making the effective capacitance, C_{eff}, a function of the two or more capacitor layers in series. Assuming that the two interfacial layers (e.g. anode-dielectric and cathode-dielectric) are identical in nature, this trend can be modeled as:

$$1/C_{eff} = 2/C_{IL} + 1/C_{BT} \quad <4>$$

where C_{IL} is the capacitance of the interfacial layer, and C_{BT} is the capacitance due to the $BaTiO_3$. Combining equations 2 and 4:

$$d_m/\varepsilon_m = 2(d_{IL}/\varepsilon_{IL}) + d_{BT}/\varepsilon_{BT} \quad <5>$$

where d and ε are the measured thicknesses and effective permittivities, respectively, of the measured device (m), interfacial layer (IL), and $BaTiO_3$ (BT). Given the symmetry observed in the I-V plots, the dead-layer model assumptions should accurately describe the data. Using this model as a guideline and the assumptions that the interfacial layer is between 1 and 5 nm [17, 22] and that d_m approximately equal to d_{BT}, the AC data was replotted as $^{d_m}/_{\varepsilon_m}$ versus d_m (Figures 8–9). Linear trends imposed on the data plotted in this fashion result in average R^2 values of 0.94 for Ni electrodes and 0.92 for Pt electrodes, indicating that the assumed model would seem to accurately represent the observed trends for these specimens.

Using equation 5 and the calculated linear regressions in Figures 8 and 9, the permittivities of the $BaTiO_3$ and interfacial layers were calculated assuming a 1 nm thick interfacial layer (Table IV). This data shows that the permittivity of the $BaTiO_3$ was found to be 2-5 times higher for the samples with Pt electrodes than was calculated for those with Ni electrodes. This difference may be linked to the differences in diffusivities of the electrode materials into the $BaTiO_3$ during deposition [5, 20, 23], creating either a thinner layer of effective $BaTiO_3$ than was initially measured by profilometry, or by introducing doping effects into the $BaTiO_3$ thereby making the compositions of the dielectric chemically different.

The interfacial layer permittivity, ε_{IL}, was found to be within reasonable agreement between the Pt and Ni electrodes for the R1 and R7 $BaTiO_3$ compositions, but was observed to be approximately 5 times larger for Pt electrodes than Ni electrodes for the R4 composition. This difference may be a remnant of the numerical analysis of the data, and not represent any difference in chemical, physical, or electrical differences in the devices. The R^2 value with R4-Pt plot was less than 0.90 indicating that the model was not fitting the data as well for these data points as it was for the other devices. Based on this discrepancy in the R4-Pt data set and the behavior observed in the R1 and R7 devices, it would appear that the non-matching interfacial layer permittivities between the two R4 data sets is not reflective of a material or composition difference, but more likely a regression inadequacy related to scatter in the data.

3.3. Discussion

The results of the dead layer model suggest that the effective interfacial layer is a constant thickness. This would indicate that the differences in the observed permittivities between the different compositions of $BaTiO_3$ and the different electrodes are related to the bulk of the $BaTiO_3$ itself. It may be possible that, given the thin nature of these films, that the differences may be a result of the diffusion of the electrode materials into the dielectric film [5, 20, 23]. Diffusion of the electrodes into the dielectric would result in an effective doping of the $BaTiO_3$, resulting in the $BaTiO_3$ compositions being doped by different elements (Ni or Pt), thus giving different electrical responses. It is also possible, given the differences in the I-V characteristics between the Pt and Ni electrodes, that the observed difference may be caused by a different current injection mechanism occurring at the interface between the electrode and dielectric. Despite the source of the differences between the electrical responses, all of the data indicates the pronounced presence of interfacial layers that are directly impacting the measured responses of these films.

4. Summary

The thickness effects of three deposition conditions of RF-sputtered $BaTiO_3$ were investigated with respect to the Ni and Pt electrode materials. The deposition conditions were chosen based on the differences in loss and permittivity characteristics previously determined at a constant thickness of approximately 100 nm. The thickness of the $BaTiO_3$ was varied over four levels at approximately 200, 100, 50, and 25 nm, while the electrode thickness was kept constant at approximately 20 nm. Current-voltage tests displayed the presence of between 2 and 3 conduction mechanisms with transitions occurring at relatively set field strengths of $2x10^{7}\ ^{V}/_{m}$ for Ni and $5x10^{6}\ ^{V}/_{m}$ for Pt electrodes (all specimens), with a potential second transition at fields of approximately 1–$2x10^{8}\ ^{V}/_{m}$ (typically seen on the 100 and 200 nm thick $BaTiO_3$ devices). The DC characterization also showed these films to be highly insulating (averaging > 10 GΩ) across all thicknesses for both electrode materials. The resistance was observed to be non-linear with thickness, suggesting the presence of interfacial layers between the electrodes and $BaTiO_3$ layers.

AC testing was conducted at 1 kHz for direct measurement of the capacitance and loss tangent values. Using the measured capacitance and thickness values, a range of effective permittivities were calculated to be 350-1700 for Ni electrodes and between 100 and 2500 for Pt electrodes. The capacitance and loss were both observed to be non-linear with dielectric thickness. The loss was typically seen to increase with decreasing thickness, likely do to the decrease of material available to impede the motion of electrons through the $BaTiO_3$ layer. The non-linearity of the capacitance further supported the presence of interfacial layers between the dielectric and electrode layers. Based on the results, a standard dead-layer model consisting of two capacitors acting in series was assumed to be responsible for the observed trends. Linear regressions of the plotted data showed the assumption of multiple capacitors acting in series to fit with R2 values of 0.92 for Pt and 0.94 for Ni, and values for the permittivity of the $BaTiO_3$ were found to range between approximately 325 and 750 with Ni electrodes and approximately 900 and 2000 with Pt electrodes. The interlayer permittivities were calculated to be approximately 44±8 for both of the electrode materials assuming an interfacial layer thickness of 1 nm.

Based on the results of these investigations, it has been found that the effects of thickness on the electrical properties of a sputtered dielectric such as $BaTiO_3$ is affected not only by the sputtering conditions of the $BaTiO_3$ itself, but also on the choice of electrode material.

5. Acknowledgements

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Figures

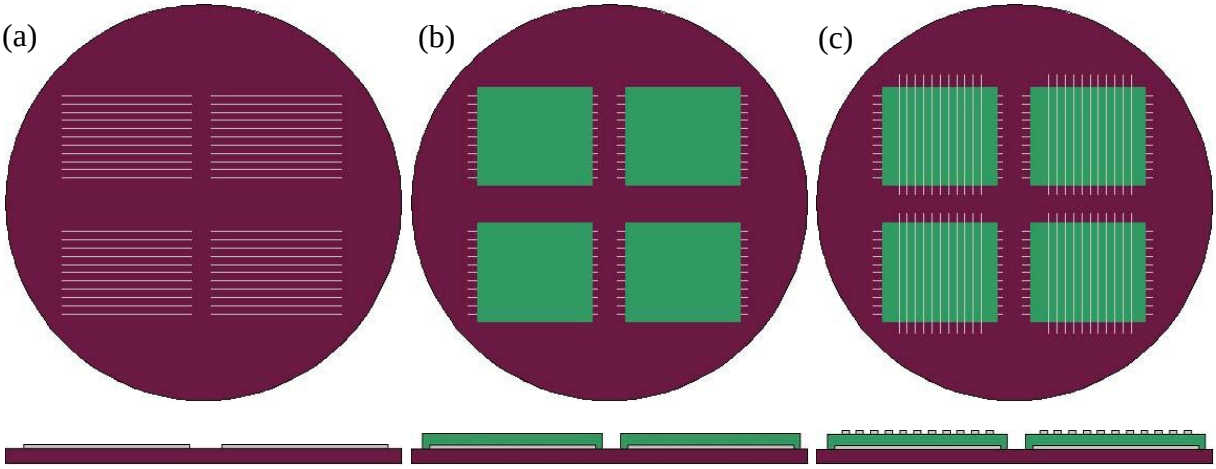

Fig. 1 – Process sequence followed for the patterned deposition of a single dielectric layer capacitor. 1st electrode layer (a), dielectric (b), and 2nd electrode layer (c). Top images are plan view looking at surface of substrate, and bottom images are cross sections. Vacuum was broken between layers to allow the exchanging of physical masks between depositions.

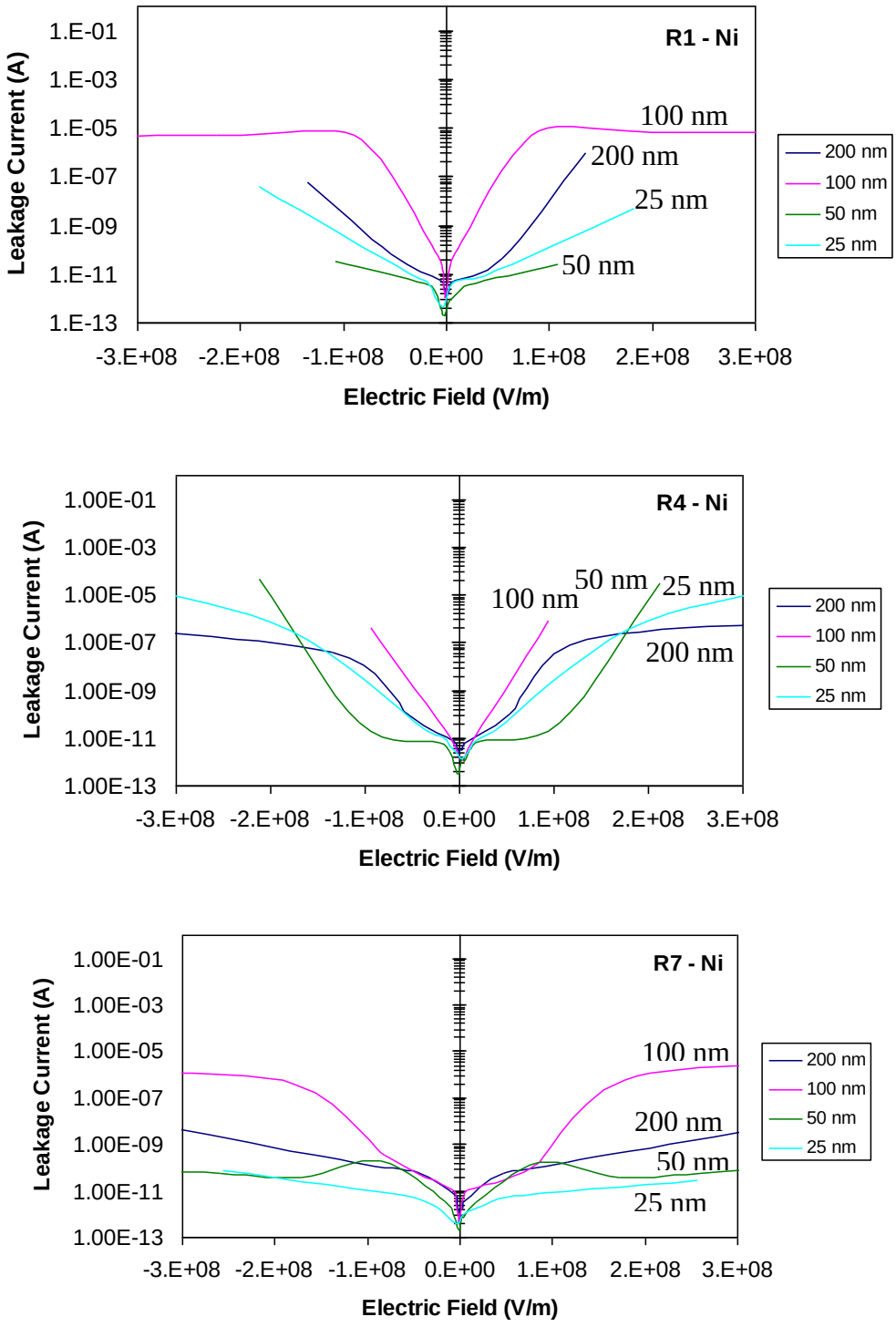

Figure 2 – I-V response for specimens with Ni electrodes. The voltage was plotted as applied field (V/m) to allow a more accurate comparison between the various thicknesses. All leakage currents were artificially made positive to allow plotting on a log-scale, and make symmetry more easily identified.

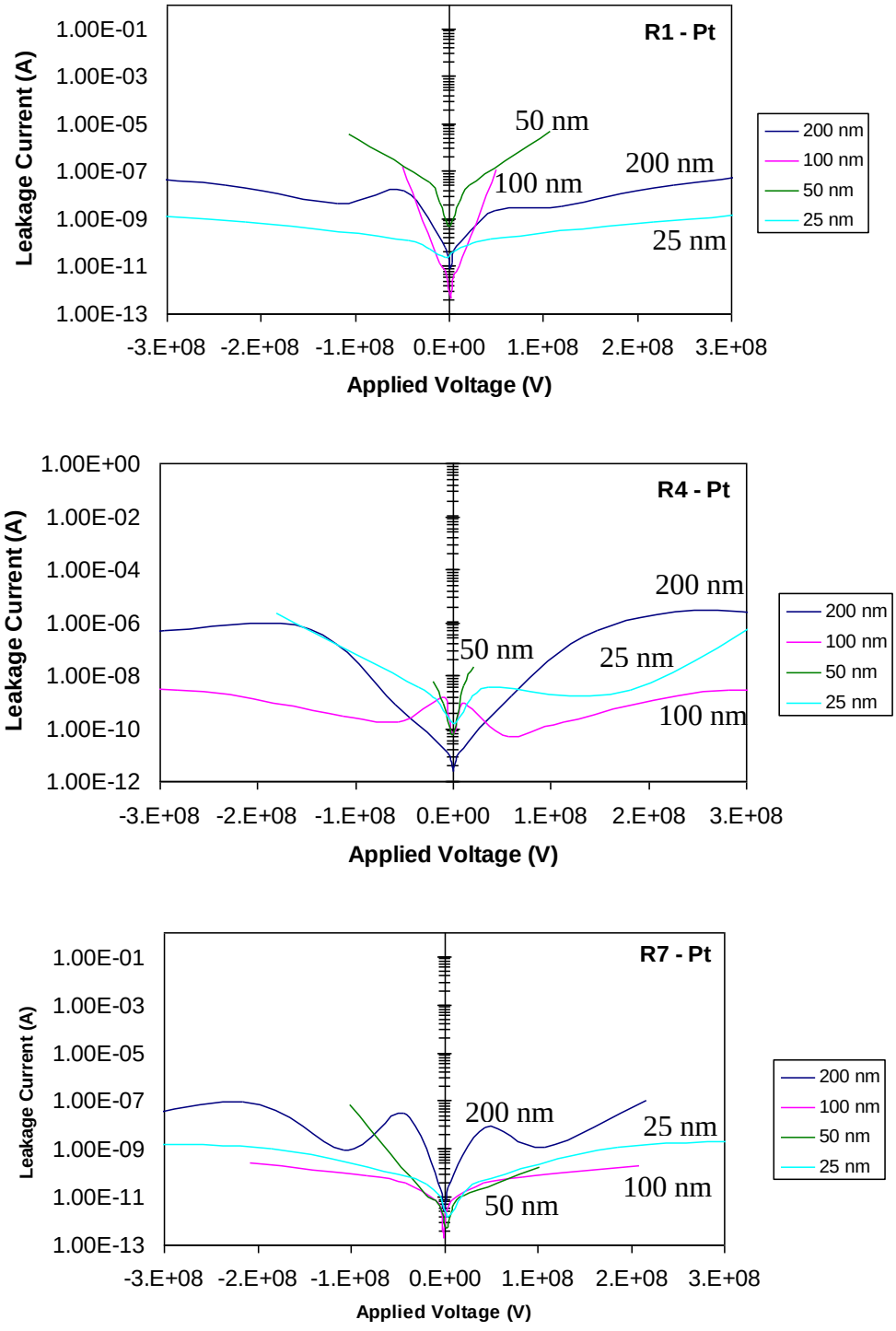

Figure 3 – I-V response for specimens with Pt electrodes. The voltage was plotted as applied field (V/m) to allow a more accurate comparison between the various thicknesses. All leakage currents were artificially made positive to allow plotting on a log-scale, and make symmetry more easily identified.

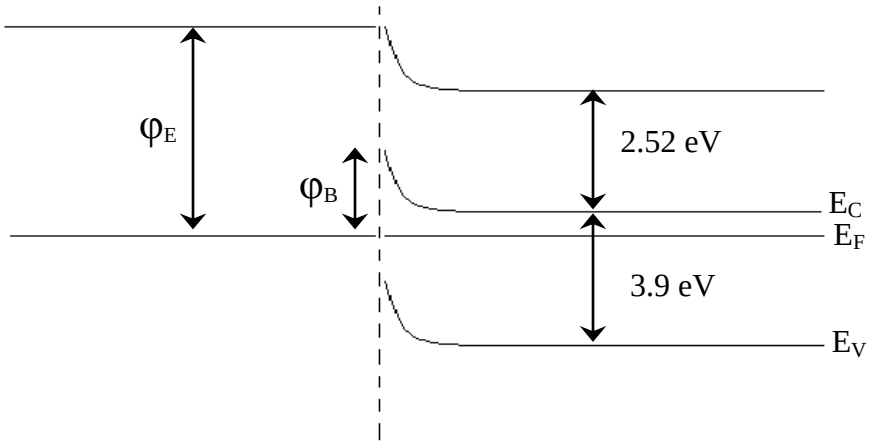

Figure 4 – Schematic drawing of the interfacial energies that may be affecting the measured dielectric properties. E_C, E_F, and E_V represent the conduction, Fermi, and valence band levels, respectively. φ_E and φ_B represent the electrode work function and barrier height, respectively. The work function of Pt is 5.6 eV and of Ni is 5.2 eV.

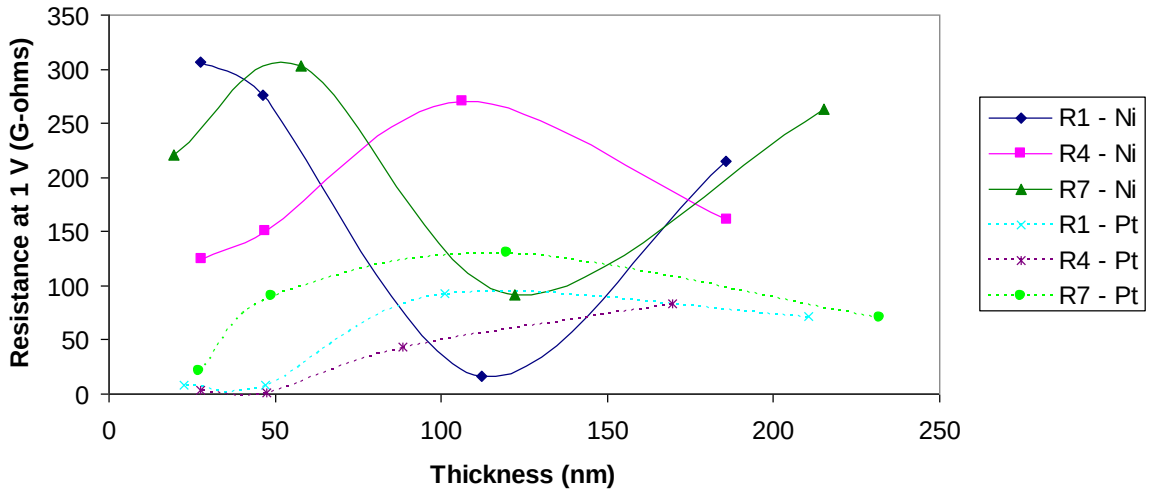

Figure 5 – Resistance at 1 V versus $BaTiO_3$ thickness for the 3 dielectric compositions with Ni electrodes (solid) and Pt electrodes (dashed).

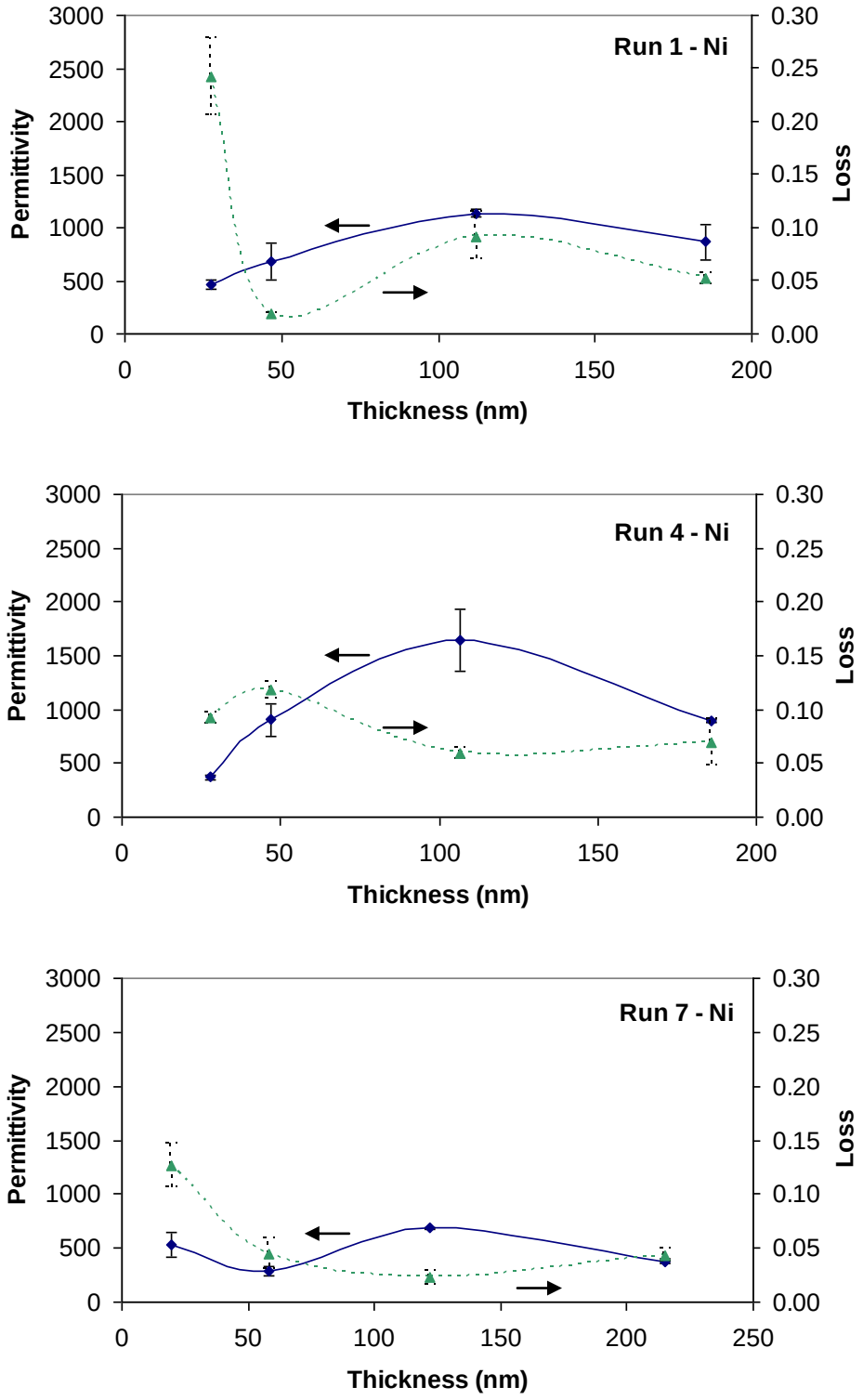

Figure 6 – Effective permittivity and measured loss values for samples Ni electrodes. Dotted lines correspond to loss and solid lines to permittivity. Error bars represent standard deviations of the measured averages used for plotting.

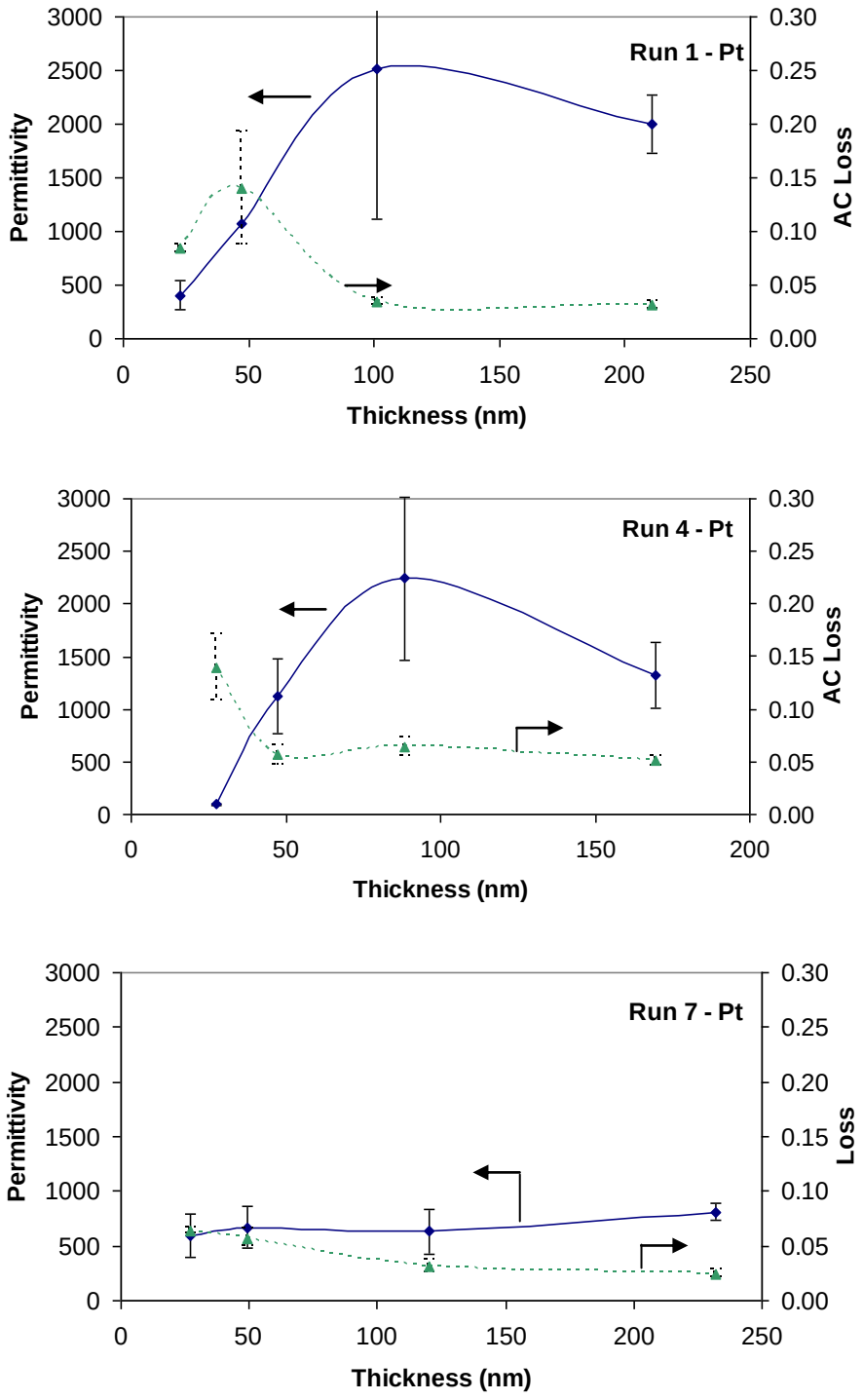

Figure 7 – Effective permittivity and measured loss values for samples Pt electrodes. Dotted lines correspond to loss and solid lines to permittivity. Error bars represent standard deviations of the measured averages used for plotting.

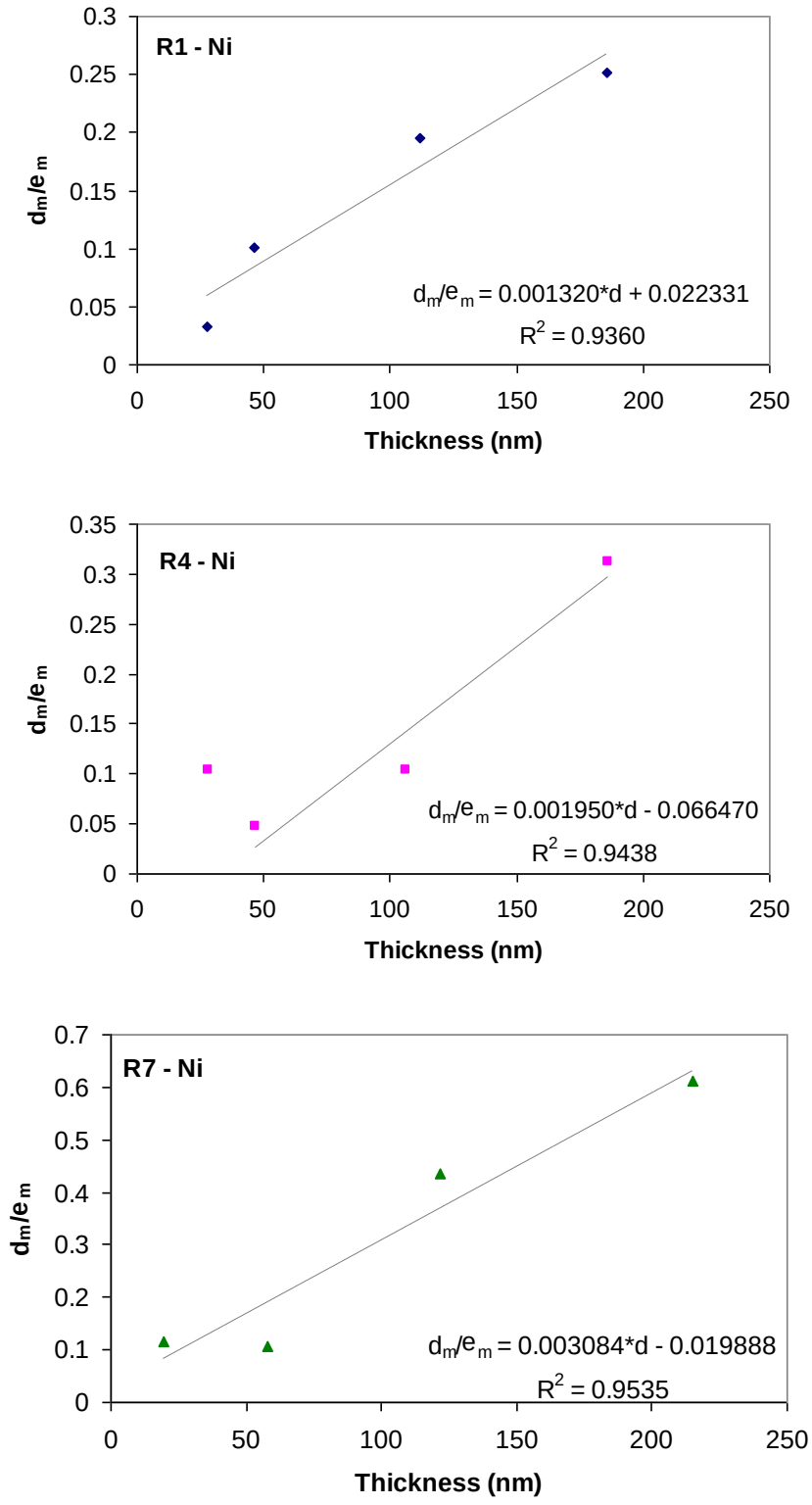

Figure 8 – AC permittivity data plotted assuming the presence of an interfacial layer acting as a capacitor in parallel with the $BaTiO_3$ for specimens with Ni electrodes.

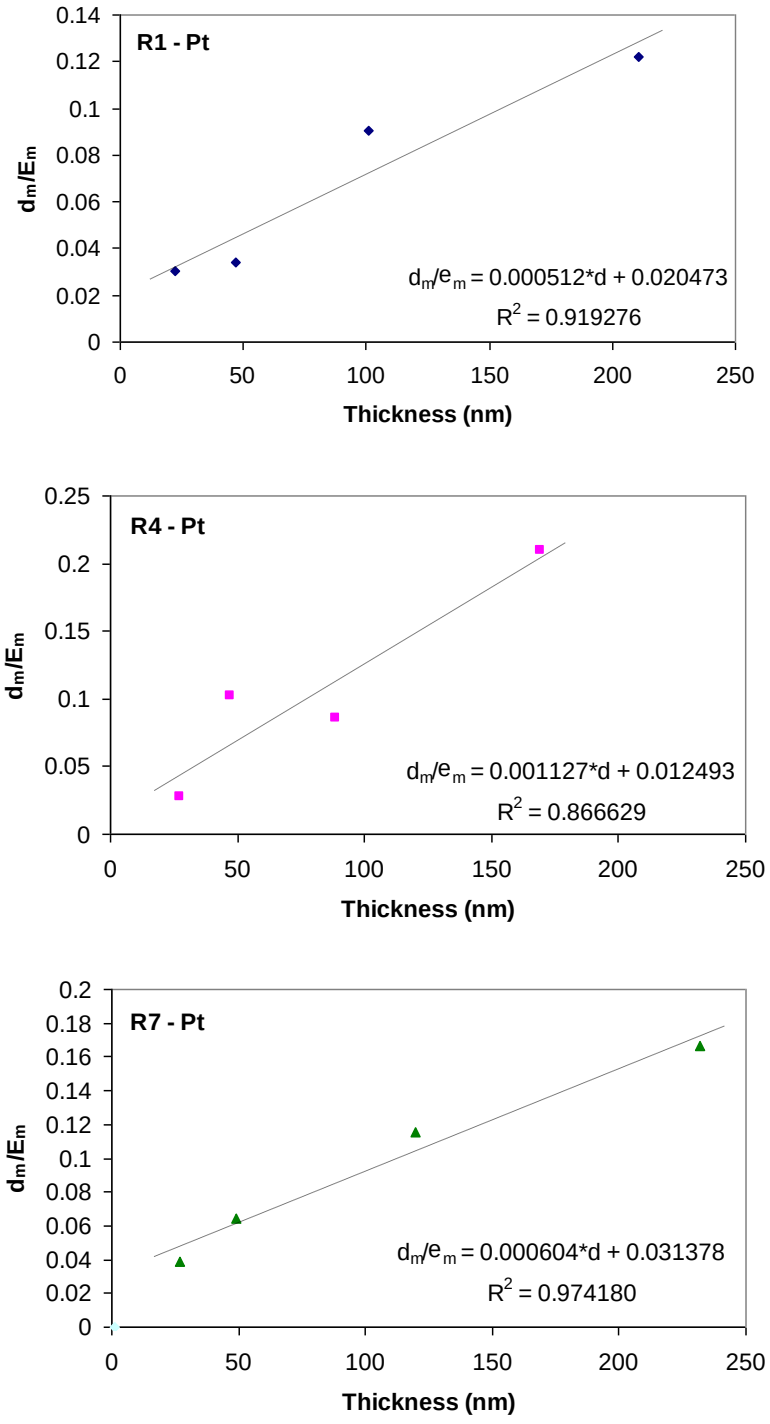

Figure 9 – AC permittivity data plotted assuming the presence of an interfacial layer acting as a capacitor in parallel with the $BaTiO_3$ for specimens with Pt electrodes.

Tables

Table I. Sputtering schedules for the three $BaTiO_3$ compositions studied

Film Label	**Oxygen Content in Plasma (%)**	**RF-Power (W)**	**Deposition Temp. (K)**
R1	50%	200	433
R4	50%	150	293
R7	10%	150	573

Table II. Maximum applied fields ($^{V}/_{m}$) achieved for each specimen examined

Approximate Thickness (nm)	**Ni Electrodes**			**Pt Electrodes**		
	R1	**R4**	**R7**	**R1**	**R4**	**R7**
200	1.4×10^{8}	5.4×10^{8}	4.7×10^{8}	4.8×10^{8}	5.9×10^{8}	4.3×10^{8}
100	8.9×10^{8}	9.4×10^{7}	8.2×10^{8}	5.0×10^{7}	1.1×10^{9}	2.1×10^{8}
50	1.1×10^{8}	2.1×10^{8}	4.3×10^{8}	1.1×10^{8}	2.1×10^{7}	1.0×10^{8}
25	1.8×10^{8}	3.6×10^{7}	2.6×10^{8}	4.4×10^{9}	1.8×10^{8}	3.7×10^{9}

Table III. Calculated permittivities based on the measured capacitance and measured loss values at 1 kHz and 1 V_{rms}

Approximate Thickness (nm)		**R1 - Ni**	**R4 - Ni**	**R7 - Ni**	**R1 – Pt**	**R4 - Pt**	**R7 – Pt**
200	**ε_r**	870 (±170)	890 (±12)	380 (±24)	2000 (±270)	1300 (±310)	810 (±81)
	tan δ	0.052 (±0.005)	0.069 (±0.022)	0.043 (±0.006)	0.031 (±0.004)	0.051 (±0.005)	0.024 (±0.004)
100	**ε_r**	1100 (±32)	1600 (±290)	690 (±7)	2500 (±1400)	2200 (±770)	630 (±210)
	tan δ	0.092 (±0.023)	0.059 (±0.005)	0.023 (±0.007)	0.035 (±0.003)	0.064 (±0.008)	0.031 (±0.006)
50	**ε_r**	690 (±170)	910 (±150)	290 (±46)	1100 (±18)	1100 (±350)	670 (±190)
	tan δ	0.019 (±0.001)	0.118 (±0.008)	0.044 (±0.015)	0.140 (±0.053)	0.056 (±0.009)	0.057 (±0.008)
25	**ε_r**	460 (±46)	370 (±27)	530 (±110)	400 (±140)	96 (±6)	600 (±200)
	tan δ	0.242 (±0.036)	0.092 (±0.005)	0.126 (±0.021)	0.084 (±0.003)	0.139 (±0.032)	0.064 (±0.003)

Table IV. Calculated permittivities of $BaTiO_3$ and interfacial layers assuming two capacitors in parallel model

	R1 - Ni	**R4 - Ni**	**R7 - Ni**	**R1 – Pt**	**R4 - Pt**	**R7 – Pt**
$\boldsymbol{\varepsilon_{BT}}$	760	510	320	2000	890	1700
$\boldsymbol{\varepsilon_{IL}}$	45	15	50	49	80	32

PAPER V

Effects of Ni electrode thickness on the dielectric properties of nano-scale, RF-sputtered $BaTiO_3$ capacitors

by

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Abstract

Nano-scale $BaTiO_3$ capacitors with Ni electrodes were sputtered on Si wafers to determine the effects of electrode thickness on the measured dielectric properties. The $BaTiO_3$ was deposited to a thickness of approximately 150 nm, while the Ni electrodes were deposited at approximately 25, 100, and 230 nm as determined by focused ion beam cross-sectional analysis. All devices were found to have a linear I-V response at ±1 V that transitioned to a nonlinear mechanism that remained active until the maximum test voltage of ±100 V. The I-V data also showed the resistances at 1 V decreasing by about 150 GΩ for the 25 nm thick electrodes. Hysteresis plots showed paraelectric behavior for all electrode thicknesses, with measured permittivity ranging from approximately 600 to 1400, with the 100 nm thick electrodes giving the highest permittivity. AC impedance data showed a decrease in permittivity from approximately 1100 to 550 with a decrease in electrode thickness from 230 nm to 100 nm, with losses remaining below 0.10 at 1, 10, and 100 kHz. At 25 nm electrode thickness, the permittivity was found to decrease from about 1050 to 250 and the loss to increase from approximately 0.06 to 0.57 as the test frequency was increased from 1 to 100 kHz. Temperature testing gave activation

energies for conduction of 0.055, 0.653, and 1.106 eV for the 230, 100, and 25 nm thick films, respectively. The results suggest that the electrodes play a critical role in thin film capacitor performance.

1. Introduction

In the commercial capacitor industry, $BaTiO_3$ is one of the most common dielectric materials [1]. Thin film applications for $BaTiO_3$ include dynamic random access memory (DRAM) [2-5], tunable microwave devices [5-8], and discreet capacitors [1, 4, 6, 7]. In order to achieve higher capacitance density for high-end electronics, the fabrication of these devices with sub-micron thicknesses using tape casting technology becomes impractical due to the necessity of powder precursors [8, 9]. This inherent limitation of the traditional capacitor fabrication technologies requires the use of techniques designed specifically for the deposition of thin films that are not based on powder processing.

Sputtering has been reported as having the capability of producing thin films with equal quality to that achievable with CVD [10, 11] that are more reproducible [5, 12] with high mass production potential [6]. Sputtering permits the customization of $BaTiO_3$ chemistry and morphology by allowing control of the percent O_2 in the plasma, deposition temperature, plasma pressure, and RF power resulting in a wide range of achievable dielectric responses [2, 10-14]. As the dielectric thickness continues to decrease, the electrode layers can also be decreased in thickness in order to reach the goal of maximal energy density per unit volume. There are numerous studies on the effects of insulator thickness variation on the measured dielectric properties [9, 12-22]. In contrast, a review of the literature reveals that electrode material and thickness are infrequently studied with the majority of the literature reporting the electrode material but not the thickness [11-13, 17, 23-30]. Of the electrode thicknesses reported for thin film capacitors, the thickness was kept constant among the tested devices and were in the range of 150 to 350 nm [5, 31-33], with only two papers mentioning thicknesses below 100 nm (i.e. 30 and 50 nm) [16, 34]. Given that thin film effects capable of reducing the conductivity of metal films begin to become prominent in the sub-micron thickness range [35], and that the majority of the reported electrode thickness values in the literature are

well below 500 nm, this study was done to investigate if the electrode thickness plays a significant role in the measured dielectric properties of thin film capacitors.

2. Procedure

All devices were fabricated on <111> Si wafers, with 1 μm of thermal oxide for electrical insulation. They were prepared by cleaning in subsequent baths of acetone, methanol, and DI water, followed by spin drying and a dehydration bake. A physical mask with approx. 74 μm wide by 2.4 cm long channels arranged with 11 parallel lines per of quarter wafer was centered on the wafer. Sputtering of the bottom Ni electrode was conducted using a Denton Discovery-18 sputter system to the desired thickness from a 99.9% pure metallic target (Figure 1.a). The wafer was then removed from the sputter system, and the mask replaced with another physical mask consisting of four square openings measuring approx. 2.7 cm per side was placed on the wafer. After reintroduction to the system, and the attainment of a minimum of $5x10^{-6}$ torr pressure, the $BaTiO_3$ was deposited at 195 W in a plasma with approximately 16.7% O_2 (balance Ar) at room temperature to a thickness of approx. 150 nm (Figure 1.b). The wafer was then removed again, and the original mask was replaced on the wafer having been rotated 90° from the bottom electrodes. Deposition of the top Ni electrode was repeated in the same manner as the first deposition (Figure 1.c). The final wafer consists of 121 test locations per quarter of wafer measuring approximately $5.4x10^{-5}$ cm^2 each. Plasma compositions were controlled with two mass flow controllers connected to Ar and O_2 cylinders.

The thickness of each layer was initially measured by profilometry using a Tencor Alpha-Step 200. The electrode thicknesses were also measured using images acquired from a Helios Nanolab 600 focused ion beam – scanning electron microscope (FIB-SEM), giving two measures of physical thickness. Effective electrode thickness was then calculated based on resistance measurements using a portable multi-meter (Wavetek Meterman 10XL) and the bulk resistivity values of Ni. Current-voltage (I-V) plots were made using an HP 4140B pA Meter from ± 0.1 to 100 V, allowing a 30 second soak at each voltage to account for system equilibration. Hysteresis plots were made using a Radiant Technologies RT6000HVS system at incrementing voltages of 1 to 19 V (the largest whole number voltage achievable for low voltage measurements). The AC

impedance measurements for capacitance and loss were made at 1, 10, and 100 kHz at 1 V_{rms} with 0 V DC bias using an HP 4149 Impedance/Gain Phase Analyzer. Based on thickness and capacitance values, the effective permittivity was calculated. All electrical testing was performed on three randomly selected locations of the total 484 total locations per wafer.

3. Results

In order to gain an understanding the effects of electrode thickness on the dielectric responses of these sputtered devices, a variety of testing methods was employed. The first series of testing was performed to characterize the electrodes in terms of physical thickness (profilometry and FIB-SEM) and effective electrical thickness (electrode resistance). Next, the devices were tested using both DC and AC currents to acquire a complete picture of the dielectric responses of these devices. DC characterization consisted of I-V and hysteresis plots, and AC characterization was limited to impedance measurements at 1, 10, 100 kHz. Finally, elevated temperature testing was conducted to calculate the activation energy of conduction, E_a.

3.1. Electrode Characterization

The electrode thickness was determined using three techniques; profilometry of glass slides co-deposited along side the wafer, analysis of FIB-SEM cross-section images, and based on calculations from the electrode resistance.

Profilometry measurements were performed on cleaned glass slides that were situated next to the wafer during each of the depositions. Thickness was determined based on the measured step height when the stylus transitioned from bare glass to top surface of the film. These measurements were made for both the electrodes and dielectric layers, taking 10 readings per layer to acquire a representative average and standard deviation. The average of the top and bottom electrodes for these wafers were 36 ± 3.9 nm, 351 ± 14 nm, and 682 ± 12 nm for what is hereon labeled as the thin, medium and thick electrode specimens.

The specimens' layer thicknesses were also calculated based on images acquired from FIB-SEM images (Figure 2). Based on these images, the thickness of the electrodes

were found to be 25 ± 4.7 nm, 89 ± 5.3 nm, and 230 ± 8.1 nm for the thin, medium, and thick specimens, respectively. These values were between 30 – 75% lower than those measured by the profilometer, and was likely due to the geometry of the physical mask used during the deposition of the electrodes. With a channel width of only 75 μm and a mask thickness of 125 μm, giving a depth to width ratio of approximately 1.7, the ability of the Ni atoms to reach the surface of the wafer during deposition time was shadowed by the presence of the sidewalls. As the glass slides were not shadowed by a narrow channel mask their profilometer measurements were thicker. As the FIB-SEM images allow a direct measurement of the film thickness, the measurements from the FIB-SEM was considered a more accurate measurement of the film's physical thickness.

Electrical resistance measurements (1 V DC) were also used to calculate the electrode thickness based on the basic resistivity equation:

$$R = \rho\left(^{L}/_{A}\right) \qquad <1>$$

Where R is the measured resistance (Ω), L the length of the electrode (approximately 2.4cm), and A is the cross-sectional area of the electrodes (74.5 μm x thickness), and ρ is the resistivity of Ni. The bulk resistivity of Ni was assumed to be 6.4×10^{-6} Ω-cm [36]. As the thin film electrodes were likely affected by surface effects, twice the bulk resistivity was used to calculate the effective thickness of the films as a worst case scenario [35]. Thicknesses calculated in this manner showed significantly thinner films than measured by either of the above methods (Table I). Use of doubled bulk resistivity was found to match well with a high resolution TEM image (Figure 3), which shows a highly crystalline Ni layer of approximately the same thickness as that calculated by this method with an interaction area on either side of this region accounting for the remaining physical thickness (i.e. resistance-based thickness measurements found the thickness of a specimen with thin electrodes to be 5 nm, and the TEM image showed a highly crystalline band of Ni with a thickness of approximately 4 nm).

Based on the above calculations, there exists some discrepancy in how the thicknesses of thin film electrodes are determined. The same films appear as 25, 90, and 230 nm based on FIB cross-sections, but when thicknesses are calculated based on the

measured resistance of the electrodes the values come close to the thickness observed on one high resolution TEM image. This suggests that the resistance based thickness calculations might be more accurate, but, given that only one TEM image has been acquired compared to the multiple FIB images, the FIB based thickness values have been used throughout the remainder of this report.

3.2. Current-Voltage Data

Current-voltage (I-V) plots were acquired from 0.1 to 100 V with both positive and negative potentials (Figure 4). All three tested specimens at each electrode thickness were capable of holding ±100 V with approximately 1-2x10^{-8} A of leakage current (5-10 GΩ at a field of approximately 7 MV/cm). The same conduction mechanisms were also observed between the three electrode thicknesses. The first of which was found to occur uniformly between ±1 V, and was observed to be linear and nearly identical for all three specimens (Figure 5). Past ±1 V the conduction was observed to change to a non-linear mechanism, with the leakage current increasing faster than the applied voltage (Figure 5). It was found that the medium thickness (90 nm resistance-based thickness) gave the minimal leakage current, followed by the thin electrodes (25 nm) and then the thick (198 nm). This trend was found to continue until approximately ±50 V, where deviation was found to occur between the specimens and whether the applied voltage was positive or negative in polarity. This later trend is likely related to the high fields imparted on the films at this voltage level (50 V ~ 3.5 MV/cm), and may not accurately depict the material behavior since only 3 locations were tested on each wafer at each electrode thickness.

The resistance of the films at ±1 V was also calculated. Assuming an ohmic relationship between the current and voltage at any set potential, the resistance of these devices at +1 V was calculated (Table II) and plotted against electrode thickness (Figure 6). It was interesting to note that the average resistance was found to decrease when the electrode thickness was below 90 nm. The associated standard deviation may suggest that the decrease was not as significant as the averages indicate, but there was a general decrease in the data. This trend suggests that some electronic phenomenon was occurring

with the thinnest electrodes that was increasing the flow of current through the $BaTiO_3$ film.

3.3. Hysteresis Data

The hysteresis data from all three specimens indicate that the sputtered $BaTiO_3$ was behaving as a standard paraelectric material (Figure 7). The lack of ferroelectricity in similar sputtered films has been reported by other authors [16, 19], and was determined to be due to the lack of significant perovskite crystallinity in the films. It has also been shown in previous research on similar films that the presence of ferroelectricity is strongly related to the processing conditions of the $BaTiO_3$ as well as the selection of electrode material [37]. In addition to the paraelectric nature of the films, hysteresis loops also allow a calculation of the permittivity (Table II). Based on these calculations, the permittivity was found to be maximized at approximately 1400 with the use of the medium thickness electrodes at approximately 90 nm (Figure 8). The measured permittivities also indicated that the thick electrodes (230 nm) were higher at a value of about 900 than the thin electrodes (25 nm) with a value of about 600. The large standard deviation associated with these measurements, however, indicate that the permittivities may be closer than the averages indicate. As the $BaTiO_3$ film should have been the same in all three cases, these variations in the hysteresis based permittivity appear to be associated with some electronic phenomenon occurring at the electrodes.

3.4. AC Impedance Data

The capacitance and loss tangent values for the three specimens were taken at 1, 10, and 100 kHz (Table III). The capacitance data was used along with the measured $BaTiO_3$ thicknesses to calculate the AC permittivity (Figure 9). It has been reported in the literature that modifying the thickness of the $BaTiO_3$ results in a non-linear trend in the calculated permittivities due to the presence of interfacial phenomenon at the electrode-dielectric interface [19, 22, 38]. These interfacial phenomenon have been related only to the dielectric thickness. As such, it was assumed that a change in electrode thickness should not have a significant impact on the permittivity of devices with the same dielectric layer thickness and composition. As seen in Figure 9, this may

not be correct. The permittivity was found to decrease from an average of 1100 to 541 across the three test frequencies when the electrode thickness was reduced from approximately 230 nm to 90 nm. In addition, the standard deviation for the calculated permittivity was found to significantly decrease at the 90 nm thick electrodes. As the thickness of the electrodes was further decreased to approximately 25 nm the permittivity was found to strongly depend on the test frequency, with the permittivity decreasing as the frequency was increased (1050 at 1 kHz, 800 at 10 kHz, and 270 at 100 kHz).

The loss was also assumed to be a function of the $BaTiO_3$ processing conditions, and not directly related to the geometry of the electrodes. Figure 10 shows that this assumption holds true at electrode thicknesses of about 90 and 230 nm, but was not valid when the thickness of the electrodes was decreased to 25 nm. The loss was found to be consistently below 0.100 for all three test frequencies when the electrodes were 90 or 230 nm. At 25 nm, however, the loss becomes highly frequency dependent, with the 100 kHz readings indicating the highest loss (0.570), followed by the 10 kHz (0.445) and the 1 kHz (0.061) readings. This sudden change in dependency of test frequency, which mirrors the observed behavior for the AC permittivity, again supports the assertion of some electrical phenomenon occurring in the 25 nm electrodes that were not as apparent in the 90 and 230 nm electrodes.

3.5. Elevated Temperature Testing

The final series of electrical testing was conducted using a series of elevated temperatures at 85°C and 150°C and measuring the leakage current at ±100 V (Table IV). The first observation from this data was the increase in leakage current with increasing temperature (Figure 11), which is typical for the increased motion of charge carrying defects in insulating ceramics. Data plotted following a standard Arrhenius relationship between the conductivity and temperature allowed the calculation of the activation energy of conduction, E_a, for the different specimens (Figure 12). Based on this analysis, the E_a was found to be the same for all three specimens between 25°C and 85°C at a constant 0.055 eV, which may be indicative of the electron hopping conduction mechanism in $BaTiO_3$ [19]. As the temperature was increased to 150°C the three specimens gave different responses. The thick electrodes (230 nm) continued the trend

observed at the lower temperatures (E_a = 0.055 eV). The 90 nm and 25 nm specimens however, increased their effective activation energies at temperatures from 85–150°C to 0.653 and 1.106 eV, respectively. These values were initially assumed to be a factor related to the dielectric and its inherent defect structure in conjunction with a defined set of electrical barriers due to the electrodes used, but otherwise independent of the electrode geometry [1, 19, 39]. The results of this study, however, indicate that the electrode geometry may play a more significant role in the conduction process than simply acting as an electron source at the interface of the dielectric and electrode.

3.6. Discussion

As the thickness of the electrodes continues to decrease along with the decreasing dielectric thickness it becomes more difficult to properly characterize the device. Based on these investigations, the question has become a matter of whether to report the physical thickness of the electrodes or the effective thickness due to the resistance, which was found to be significantly thinner than the physical thickness due to electrical thin film effects. The results of electrical testing also suggest that the effects of the electrodes on the measured dielectric properties were much more significant than previously assumed. Given the trends observed with these specimens, an in depth investigation into the effects of electrode materials on the dielectric properties as the electrode thickness is decreased into the nanometer range is warranted. It is also necessary to begin acquiring an understanding of the phenomena responsible for these electrode-based effects on the resultant dielectric properties.

4. Summary

The effects of electrode thickness on the dielectric properties of 150 nm thick sputtered $BaTiO_3$ with Ni electrodes was evaluated. Physical measurements determined the electrodes to be 25, 100, and 230 nm thick, but estimated thicknesses based on electrical resistance showed the same specimens to be 5, 56, and 198 nm thick. The significant differences between the physical and effective electrical thickness values were found to be due to thin film effects reducing the allowed thickness of material where conduction could occur with relative ease. As more data was available for the physical

thickness measurements, the FIB-based measurements were chosen to relate the thickness effects on the dielectric properties.

The I-V plots showed that all specimens were able to achieve field strengths in excess of 7 MV/cm without breakdown. These plots also allowed the calculation of the resistance of the devices at an applied potential of 1 V, which showed a decrease in resistance once the electrode thickness was below approximately 90 nm. Hysteresis plots showed that the films were paraelectric in nature, and that the DC permittivity showed a maximum with the 90 nm thick electrode specimen. AC testing showed that the specimens were unaffected by test frequency until the electrode thickness was decreased below approximately 90 nm. At 25 nm an increase in test frequency saw an increase in loss and decrease in permittivity. This phenomenon was not observed with the 90 and 230 nm thick electrode specimens. Elevated temperature testing showed two regimes of activation energies; one between 25°C and 85°C and the other between 85°C and 150°C. The first, low temperature, regime showed all specimens having an E_a value of 0.055 eV. Above 85°C, the E_a values began to deviate based on electrode thickness. The 230 nm thick electrode showed no change in E_a, but the 90 and 25 nm thick electrodes showed an increase to 0.653 and 1.106 eV, respectively. All of the responses indicate a phenomenon occurring at the electrodes that impacts the dielectric properties as the electrode thickness was reduced below 50 nm effective thickness.

5. Acknowledgements

Funding for this research was given by the Center for Dielectric Studies (CDS), a NSF funded industrial and academic research center. The physical mask used for patterning the electrodes was fabricated by Jonathan Keeth at Missouri State University. FIB-SEM and TEM operation and image acquisition was performed by Dr. Ming Zhang. James Reck would also like to thank the Department of Education for the Graduate Assistance in an Area of National Need (GAANN) fellowship which has funded his graduate studies.

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Figures

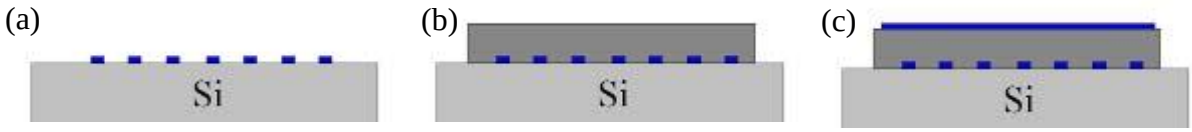

Fig. 1 – Process sequence followed for the patterned deposition of a single dielectric layer capacitor. 1st electrode layer (a), dielectric (b), and 2nd electrode layer (c). Layer thicknesses are proportioned approximately for 25 nm thick Ni with 150 nm thick $BaTiO_3$. Vacuum was broken between layers to allow the exchanging of physical masks between depositions.

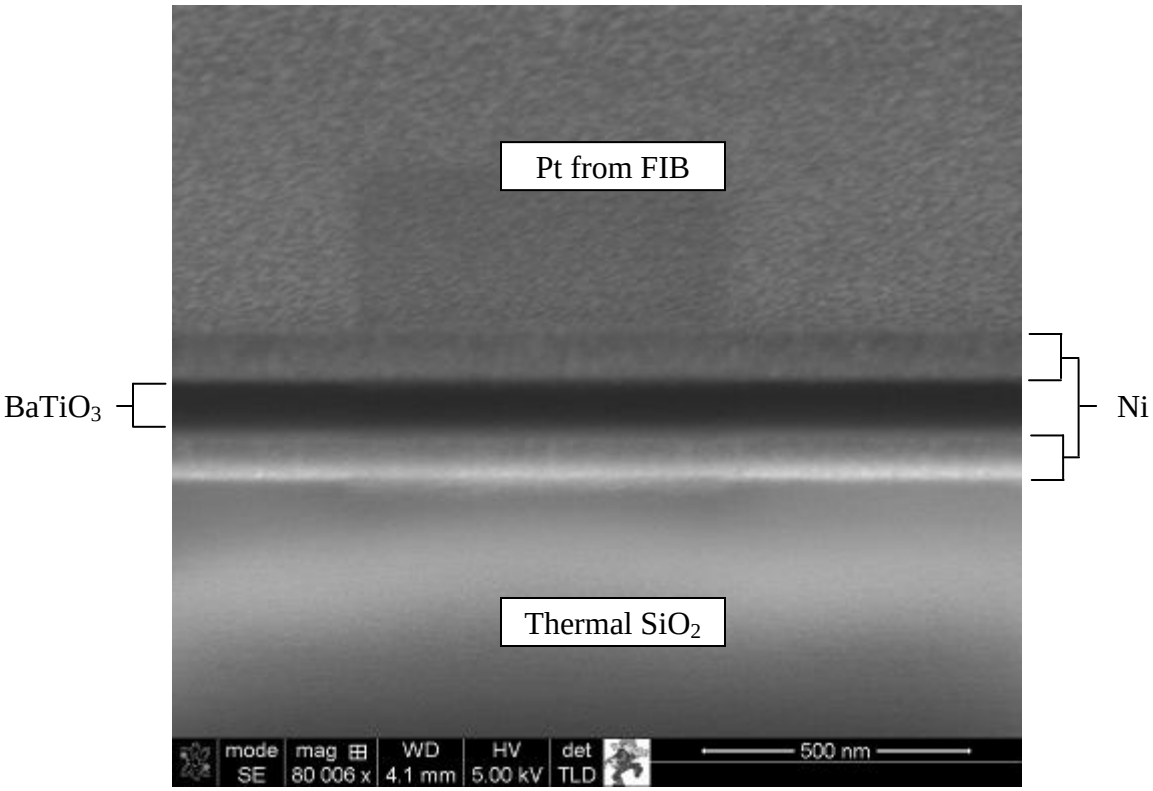

Figure 2 – Representative FIB-SEM image of the medium electrode sample showing an average electrode thickness of approximately 89.1 ± 5.31. Similar images were acquired for the other two electrode thicknesses.

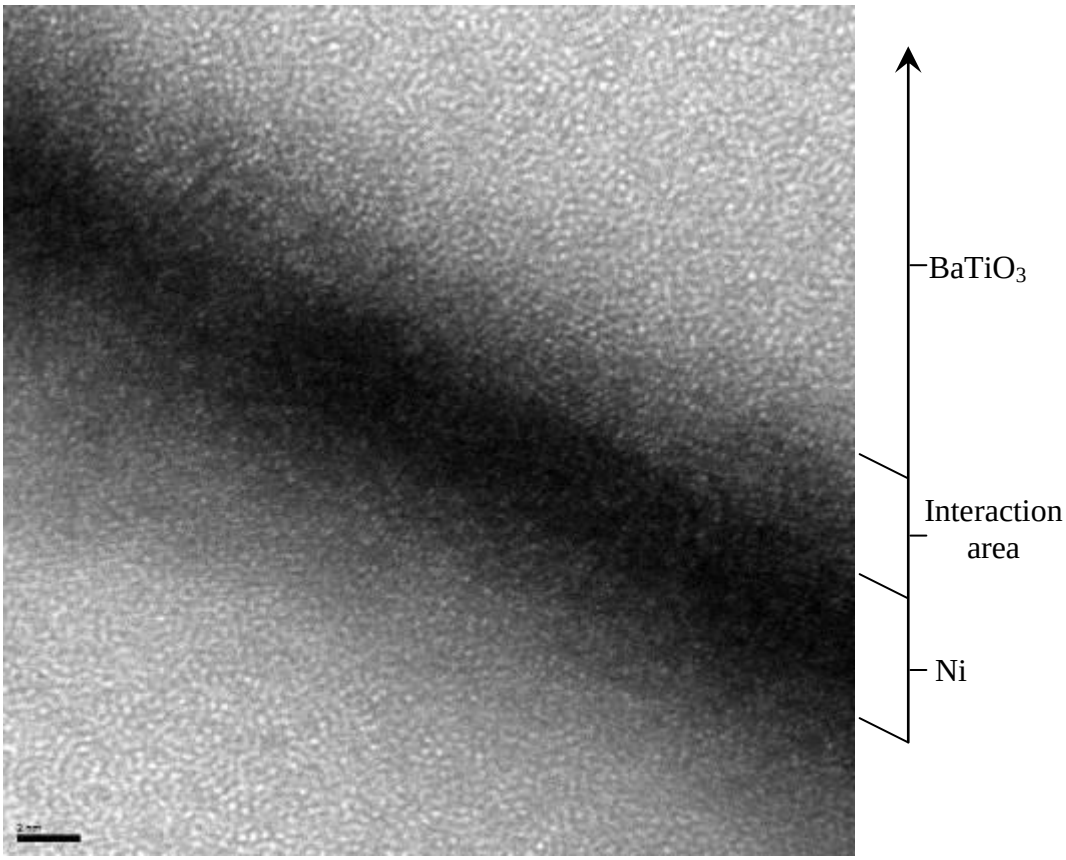

Figure 3 – High resolution TEM micrograph of an approximately 15 nm thick (FIB-based calculation) electrode specimen showing a strong polycrystalline Ni layer (black) at a thickness of approximately 4 nm. Resistance based calculations resulted in a thickness of 5 nm for this specimen.

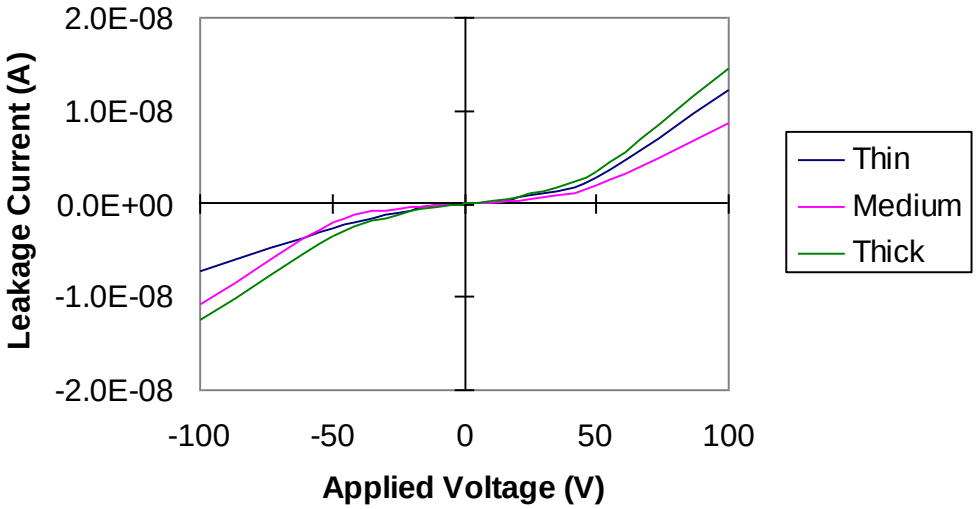

Figure 4 – I-V plot for the three electrode thicknesses. The resistance-based thickness values of the electrodes were approximately 5, 56, and 198 nm for the thin, medium, and thick specimens.

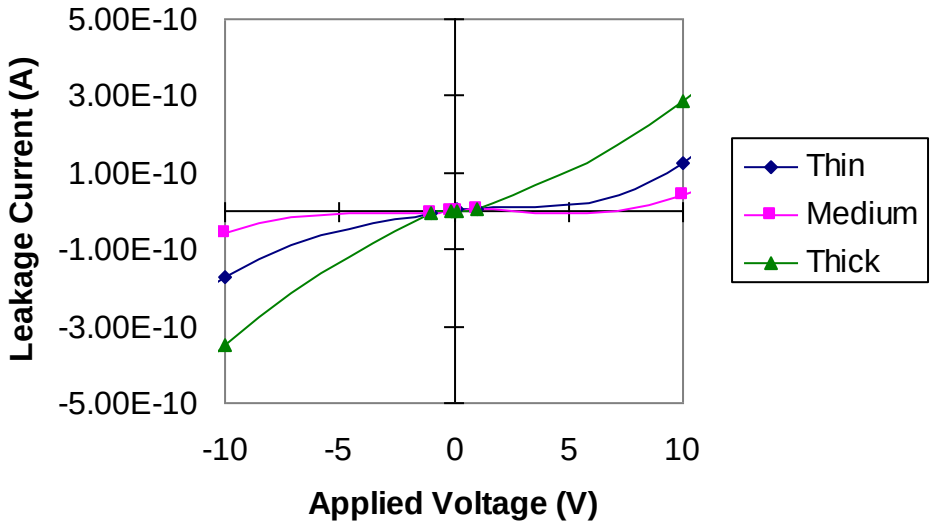

Figure 5 – A close-up of the ±10 V range of the I-V plot showing the linear portion of the data at ±1 V transitioning to the non-linear conduction mechanism by ±10 V.

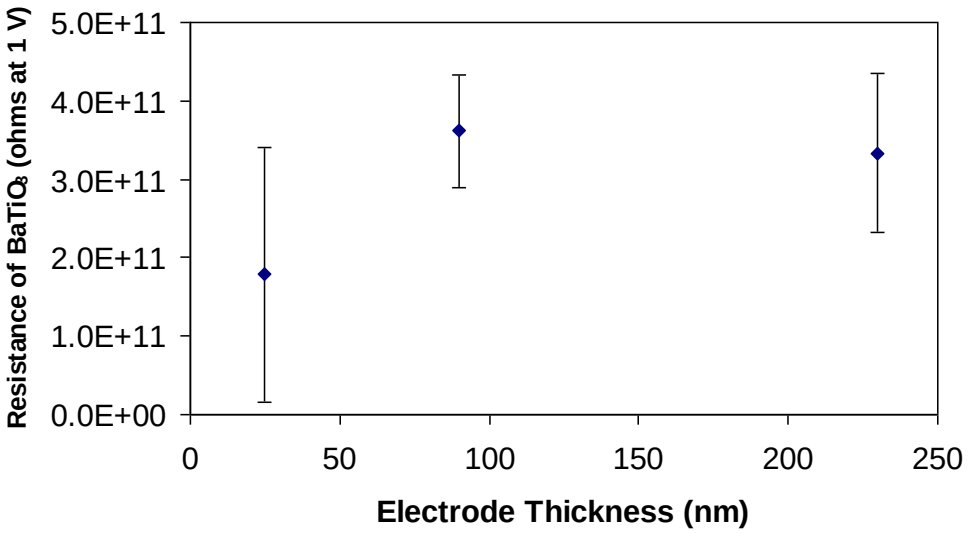

Figure 6 – The calculated $BaTiO_3$ resistance at +1 V versus the resistance-based electrode thickness showing a decrease in overall resistance for electrodes thinner than approx. 50 nm.

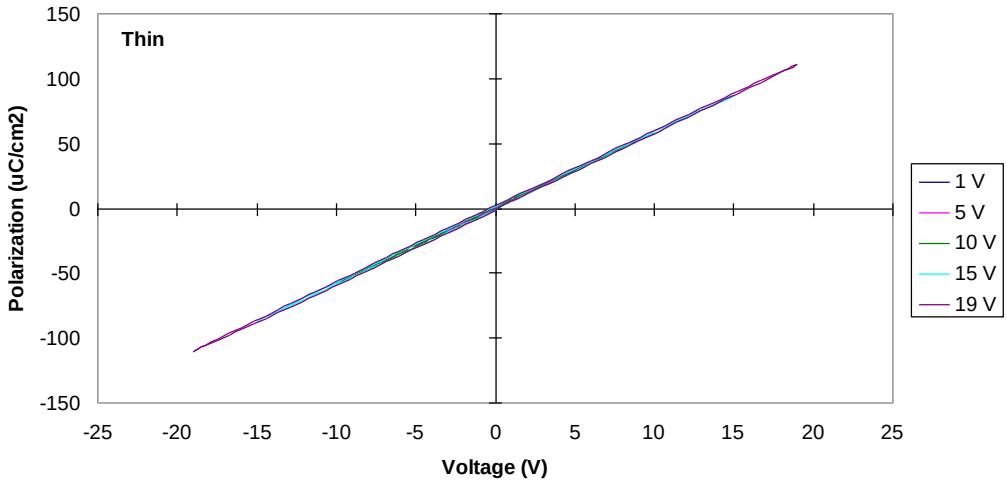

Figure 7 – Representative hysteresis loop of the thin (~5 nm) electrodes specimen showing the typical paraelectric response found for all three specimens.

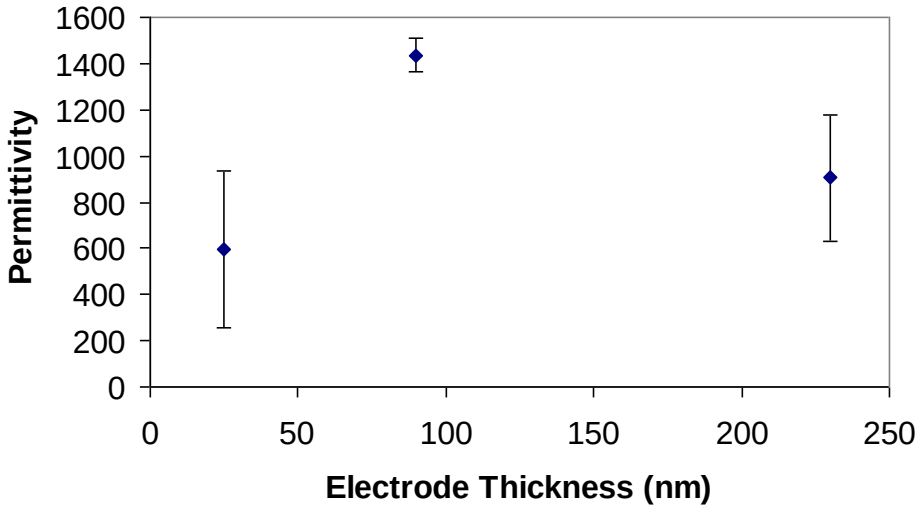

Figure 8 – The calculated permittivity versus electrode thickness shows a maximum at medium thickness (~56 nm) electrodes. The thick electrodes (~198 nm) are higher in value than those for the thin electrodes (~5 nm).

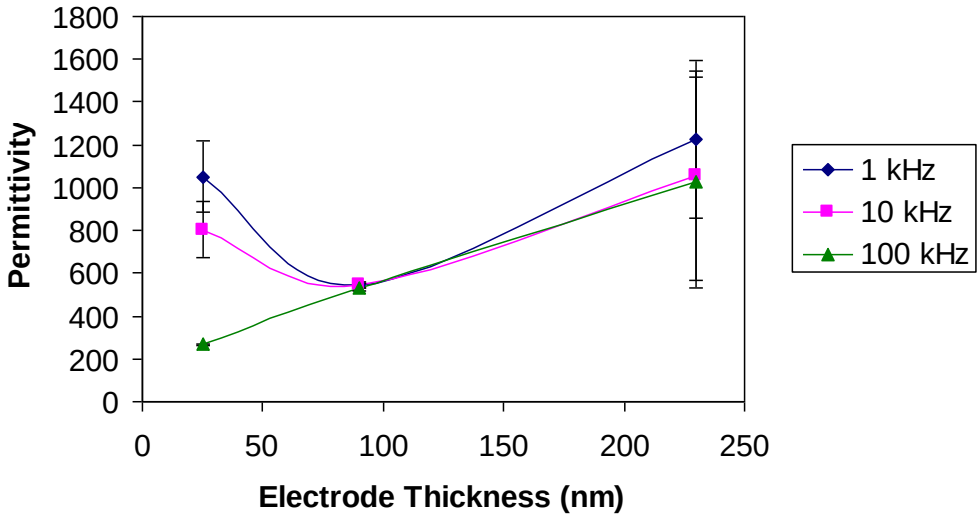

Figure 9 – The permittivity values as a function of electrode thickness at the three test frequencies showing non-linear trends.

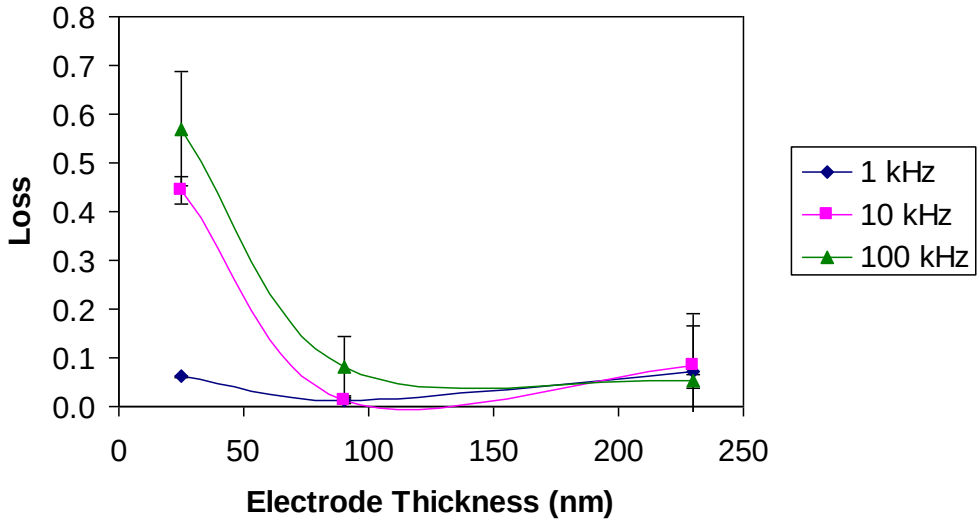

Figure 10 – Dielectric loss of the sputtered $BaTiO_3$ as a function of electrode thickness for the three test frequencies observed.

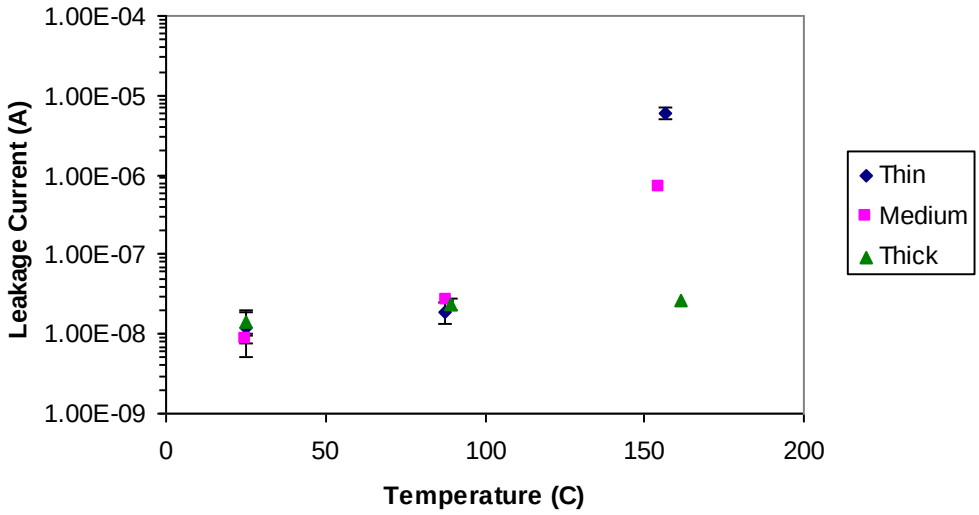

Figure 11 – The measured leakage current at +100 V at temperatures of 25°C, 85°C, and 150°C showing a general increase in leakage with increasing temperature.

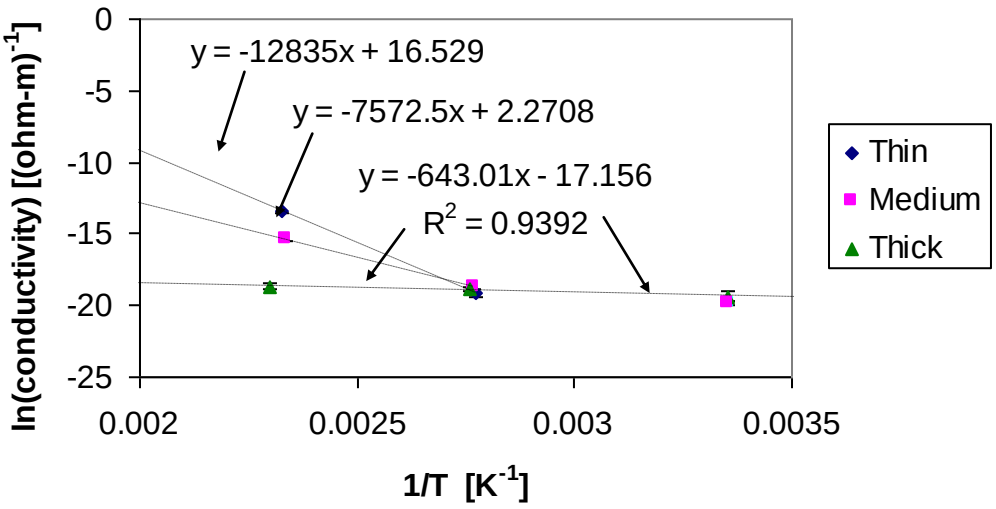

Figure 12 – Arrhenius plot of the conductivity for the three specimens examined. The slopes of the lines were used to calculate the activation energy of conduction presented in Table IV.

Tables

Table I. Measured electrode thicknesses by the three measurement techniques

	Thick	**Medium**	**Thin**
Profilometry Thickness (nm)	680 ± 12	350 ± 14	36 ± 3.9
FIB-SEM Thickness (nm)	230 ± 8.1	89 ± 5.3	25 ± 4.7
Resistance Thickness (nm)	200 ± 21	56 ± 6.3	5.0 ± 1.1

Table II. Compilation of the DC properties for the three specimens

	Thin	**Medium**	**Thick**
Resistance (GΩ)	180 ± 160	360 ± 72	330 ± 100
Permittivity	600 ± 340	1440 ± 73	910 ± 270

Table III. Compilation of the AC properties for the three specimens

	Frequency	**Thin**	**Medium**	**Thick**
Permittivity	1 kHz	1050 ± 170	550 ± 14	1220 ± 370
	10 kHz	800 ± 130	540 ± 13	1060 ± 490
	100 kHz	270 ± 2.0	530 ± 18	1020 ± 490
Loss	1 kHz	0.061± 0.003	0.013 ± 0.002	0.071 ± 0.093
	10 kHz	0.445± 0.028	0.013 ± 0.006	0.085 ± 0.105
	100 kHz	0.570± 0.117	0.083 ± 0.061	0.052 ± 0.014

Table IV. Leakage currents and activation energies for the specimens at elevated temperatures

	Test Temperature (°C)	**Leakage Current (Amps at +100 V)**	**Activation Energy (eV at 85°C – 150°C)**
Thin (~5 nm)	25	$1.2 \times 10^{-8} \pm 7.3 \times 10^{-9}$	1.106
	85	$8.7 \times 10^{-9} \pm 1.3 \times 10^{-9}$	
	150	$1.5 \times 10^{-8} \pm 4.8 \times 10^{-9}$	
Medium (~56 nm)	25	$1.9 \times 10^{-8} \pm 5.9 \times 10^{-9}$	0.653
	85	$2.6 \times 10^{-8} \pm 5.8 \times 10^{-10}$	
	150	$2.4 \times 10^{-8} \pm 3.5 \times 10^{-9}$	
Thick (~198 nm)	25	$6.0 \times 10^{-6} \pm 9.2 \times 10^{-7}$	0.055
	85	$6.8 \times 10^{-7} \pm 8.3 \times 10^{-8}$	
	150	$2.7 \times 10^{-8} \pm 4.9 \times 10^{-9}$	

PAPER VI

Chemical and microstructural characterization of rf-sputtered $BaTiO_3$ nano-capacitors with Ni electrodes

by

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Abstract

Chemical and microstructural evaluation techniques have been used to characterize 100-150 nm thick $BaTiO_3$ nano-capacitors with either Ni or Pt electrodes approximately 20 nm in thickness. Atomic force microscopy was used to measure the surface roughness of the electrode and dielectric materials. Electrodes were found to have a roughness, R_a, of about 0.67 nm over, and the $BaTiO_3$ had an average R_a value of 1.4 nm. The $BaTiO_3$ film chemistry examined with x-ray photoelectron spectroscopy found the films to have excess oxygen with Ba:Ti ratios ranging from 0.78 to 1.1 depending on sputtering conditions. X-ray diffraction showed a broad peak between approximately 20° and 35° 2θ, indicating the films were either amorphous or contained grain sizes less than 5 nm. Focused ion beam images confirmed the presence of smooth, conformal films, with no visible signs of macro-defects such as pin-holes, cracks, or pores. High resolution TEM and electron diffraction patterns confirmed the presence of an amorphous film with short range order. EELS data also confirmed that the $BaTiO_3$ films contain Ba, Ti, and O with no observable contamination from the electrodes. The amorphous nature of the films with excess oxygen were used to explain the presence of

high insulation resistance, low loss, high permittivity, and ferroelectric behavior observed during electrical testing of these films based on the presence of TiO_6 octahedra randomly dispersed throughout the sputtered dielectric.

1. Introduction

One of the most commonly used dielectrics for commercial capacitors is $BaTiO_3$ [1]. Typical applications for $BaTiO_3$-based capacitors include dynamic random access memory [2-5], tunable microwave devices [5-8], and discreet capacitors [1, 4, 6, 7]. One of the primary methods for achieving increased capacitance density for these type of devices is to reduce layer thickness. The traditional tape-casting method used for the fabrication of commercial scale capacitors has become a limiting factor in the achievement of sub-micron thick dielectric layers [9, 10]. This limitation of tape-casting has made the use of thin film techniques, such as sputtering, a potentially viable alternative for the fabrication of high-end, nano-scale ceramic capacitors.

As these devices continue to decrease in size, a better understanding of the electrical responses at the nanometer scale is necessary. Significant amounts of work have been published on the thickness effects of thin film dielectrics [10-21], effects of processing conditions on the dielectric responses [2, 8, 12, 14, 16, 18, 21-27], and different electrode options [18, 28, 29]. These properties have also been linked to the microstructural and chemical characteristics in many of these studies [2, 5, 30-33]. Based on previous research efforts conducted on sputtered $BaTiO_3$ with thicknesses in the range of 100 to 150 nm with either Ni or Pt electrodes [34-36], a better understanding of the effects of the microstructure and chemistry on the observed dielectric properties is warranted.

2. Procedure

Devices were fabricated on <111> Si wafers, with 1 μm of thermal oxide for electrical insulation. After cleaning in subsequent baths of acetone, methanol, and DI water, followed by spin drying and a dehydration bake, a physical mask with approx. 74 μm wide by 2.4 cm long channels arranged with 11 parallel lines per of quarter wafer was centered on the wafer. The bottom Ni electrodes were sputtered using a Denton

Discovery-18 to approximately 20 nm from a 99.9% pure metallic target (Figure 1.a). The wafer was then removed from the sputter system, and the mask replaced with another physical mask consisting of four square openings measuring approx. 2.7 cm per side was placed on the wafer. After the attainment of a minimum of $5x10^{-6}$ torr pressure was regained in the sputter chamber, $BaTiO_3$ was deposited at various powers (100 – 200 W), oxygen concentrations in the plasma (10 – 50% O_2, bal. Ar), and deposition temperatures (20°C – 300°C) (Figure 1.b). The original mask was then replaced on the wafer, rotated 90° from the bottom electrodes, and deposition of the top Ni electrode was repeated in the same manner as the first deposition (Figure 1.c). The final wafer consists of 121 test locations per quarter of wafer measuring approximately $5.4x10^{-5}$ cm^2 each. Plasma compositions were controlled with two mass flow controllers connected to Ar and O_2 cylinders.

The thickness of each layer was measured by a combination of profilometry and focused ion beam (FIB) cross section imaging techniques. Atomic force microscopy (AFM) was conducted on 15 x 15 μm sections of the films at selected locations, and the average surface roughness, R_a, was reported. X-ray photoelectron spectroscopy (XPS) was performed on 6 different $BaTiO_3$ films that had been deposited under differing conditions, and compared to a stoichiometric bulk $BaTiO_3$ ceramic analyzed on the same system under the same conditions. X-ray diffraction (XRD) was conducted in glancing angle mode at 2θ values between 5° and 90° using a Cu Kα source. Focused ion beam (FIB) images were acquired after controlled ion milling was performed to expose the cross-section of the nano-capacitors. High resolution transmission electron microscopy (TEM) with electron diffraction and EELS capability was used to examine the cross-section of one of the deposited devices.

3. Results and Discussion

A variety of surface and sub-surface characterization techniques have been used to gain an understanding of the chemical and microstructural nature of sputtered $BaTiO_3$ films both with and without electrodes.

3.1. Atomic Force Microscopy (AFM)

AFM scans were performed over 15 x 15 μm windows in three regions to examine the surface roughness of the electrodes, $BaTiO_3$, and bare Si wafer. All work was performed on a fabricated specimen consisting of three layers of approximately 100 nm thick $BaTiO_3$ each with alternating layers of Ni electrodes (about 20 nm thick each) for a device with a total thickness of roughly 380 nm. The first two regions to be studied was at the edge of the patterned $BaTiO_3$, in an area where two of the electrodes protruded onto the bare Si substrate (Figure 2). These regions allowed the measurement of 4 of the 5 areas of interest in this system (Figure 3); bare SiO_2, electrode over SiO_2, and $BaTiO_3$ over SiO_2 and over the Ni electrode (Table I). The bare SiO_2 was found to have an average R_a of 0.19 nm after testing two of these regions. The addition of two layers of Ni electrodes (total thickness of approximately 40 nm) resulted in an average roughness of 0.66 nm, and three layers of $BaTiO_3$ (for a total thickness of about 300 nm) gave an average roughness of 1.2 nm over the same two test regions. The last area in these test regions to be examined was a layer of $BaTiO_3$ over two layers of previous $BaTiO_3$ and two layers of patterned Ni electrode, which showed an average R_a value of 1.4 nm.

The final area examined was a randomly selected location along a top electrode between active areas (i.e. away from electrode cross-over areas) which allowed another measurement of the $BaTiO_3$ roughness over the bare substrate, and also allowed the measurement of the fifth area of interest which was the roughness of the Ni electrode over three layers of $BaTiO_3$ and 2 layers of Ni (Figure 4). In this region, which was not repeated elsewhere on the wafer, the top electrode (total thickness of underlying $BaTiO_3$ and Ni layers was about 380 nm) was found to have an R_a value of 0.67 nm, and the $BaTiO_3$ (with a total thickness of approximately 300 nm for the underlying three layers of $BaTiO_3$) again measured a roughness of 1.4 nm.

An overview of the data shows that the electrodes, whether over bare substrate or deposited $BaTiO_3$, has a roughness of approximately 0.67 nm (Table I). Likewise, regardless of whether the $BaTiO_3$ was deposited over the SiO_2 or the patterned Ni electrodes, a consistent roughness of 1.4 nm was observed. In both cases, the sputtered films were rougher than the bare SiO_2 surface of the substrate (R_a = 0.19 nm). The AFM

characterization also did not display the presence of any macro-defects in the films, such as cracks or pinholes.

3. 2. X-ray Photoelectron Spectroscopy (XPS)

Six sputtered $BaTiO_3$ compositions were selected to be examined by XPS (Table II). The results of these six specimens were normalized to a reference standard of stoichiometric $BaTiO_3$ ceramic that had been analyzed in the same system, by the same operator, and under identical conditions as the six unknown compositions (Table III). Data from all samples was gathered after a light sputter cleaning to remove surface contaminants. It was interesting to note that all but one of the six specimens was found to have between 8 and 33% excess oxygen compared to the stoichiometric amount. The one specimen that did not follow this trend was approximately 5% oxygen deficient. Excess oxygen in $BaTiO_3$ has been reported previously in the literature [37, 38]. The Ba:Ti ratio was found to vary depending on the deposition conditions. Two specimens (R4, R7) were found to be significantly Ti rich, two were Ba rich (R1, R8), and two were within approximately 3% of stoichiometric (R9, R10). A similar swing in Ba:Ti ratio has been observed based on other processing conditions (target-substrate angle, sputter pressure, crystallinity) in the literature [38, 39]. Both of these conditions (oxygen excess and varying Ba:Ti ratio) have been associated with the activity of negatively charged oxygen ions hitting the surface of the developing film during deposition in the sputter chamber [38].

Table III compares the XPS data to the measured dielectric properties of the sputtered $BaTiO_3$ films with approximately 20 nm thick Ni electrodes. The resistance at an applied potential of 1 V was found to range from approximately 16 to 270 GΩ. The permittivity (calculated from the AC capacitance at 1 kHz and 1 V_{rms} with 0 V bias) was found to be between approximately 280 and 1030 with losses between 0.02 and 0.09. Plots of these properties versus the XPS data in the form of Ba:Ti, (Ba+Ti):O, Ba:O, and Ti:O ratios showed no obvious correlations between the film chemistries and the electrical properties (Figure 5). Previous research efforts, however, have linked these properties to high order interactions between the deposition conditions [34]. As such, this lack of observable patterns in the data with respect to the XPS chemical data was

likely due to the reduced number of examined specimens (i.e. only 6 of the 13 specimens were analyzed from the original design of experiments) in addition to the complex nature of the interactions between the processing conditions responsible for the changes in measured dielectric properties.

3.3. X-ray Diffraction (XRD)

X-ray diffraction was conducted on three specimens, R1, R4, and R7 (processing conditions listed in Table II). All three specimens showed a broad peak between 2θ values of approximately 20° to 35°, indicating the films are either amorphous or have a grain size less than 5 nm (Figure 6). The presence of a moderate peak at approximately 30° 2θ may be due to the presence of the <111> Si wafer used as the substrate which has a strong <111> peak at 29°. It is interesting to note that the rhombohedral, orthorhombic, cubic, and tetragonal forms of $BaTiO_3$ exhibit <100> and <111> peaks at 22° and 39°, respectively. The broad peak beginning at approximately 20° 2θ may indicate the presence of some <100> $BaTiO_3$ characteristic in the films. This, however, is not capable of being determined with XRD testing methods, and requires the use of more advanced techniques such as electron diffraction discussed in section 3.4 below.

The literature reports that as-deposited films of traditional perovskite materials such as $BaTiO_3$ and $(Ba,Sr)TiO_3$ require minimum deposition temperatures of between 350° and 500°C to obtain crystalline films [14, 23, 25, 39]. It has also been stated that the sputter pressure and target-substrate angle can directly impact the crystallinity of the film [38], and that annealing of amorphous sputtered films at 550°C are required to initiate crystallization [39]. As such, the lack of crystallinity in these films was not surprising in itself, but combined with the presence of ferroelectric behavior as previously reported for these films [34] presents an unexpected combination of features. The presence of ferroelectricity for $BaTiO_3$ was generally considered to be a phenomenon resulting from the perovskite structure [1, 40, 41], and has only been reported in crystalline thin films [13, 30, 42]. The presence of ferroelectricity in these amorphous films, therefore, was an anomaly not previously encountered.

3.4. Electron Microscopy

The first series of electron microscopy images were obtained with the use of a focused ion beam (FIB). Cross-section images were obtained by ion milling a section of material from the surface of the sputtered films, and an image acquired of the exposed cross-section (Figure 7). These images, acquired for six specimens with three different compositions of $BaTiO_3$ and two different sets of symmetrical electrodes (Ni or Pt), confirmed the low surface roughness of the films as measured by the AFM. The images also confirm the lack of large scale defects such as pinholes and cracks, but also show no presence of pores within the film or any delamination between the films and substrates or between the sputtered layers. This indicated that high quality depositions were achieved.

The FIB was also used to create a specimen for examination in a high resolution transmission electron microscope (TEM). The specimen examined was a multi-layer capacitor (MLC) with three layers of $BaTiO_3$ and Ni electrodes. After an overall image of the cross-section was obtained (Figure 8.a), electron energy loss spectroscopy (EELS) spectrum were acquired from the center of one of the $BaTiO_3$ layers and one of the Ni layers (Figure 8.b and 8.c). The EELS analysis showed that the $BaTiO_3$ films consisted of the film constituents (e.g. Ba, Ti, and O) with no significant amounts of impurities including Ni from the electrodes in the observed range of energies. The analysis also showed that the Ni electrodes contained no observable amount of impurities.

Following the EELS analysis, a high resolution image of the interface between the $BaTiO_3$ and one of the Ni electrodes was acquired (Figure 9). This image showed lattice fringes within the Ni, indicating that the electrodes were polycrystalline. The image also showed an interfacial layer between the two materials (grey area between Ni and $BaTiO_3$) which confirmed an assumption made in previous research efforts regarding the presence of the an interfacial layer altering the dielectric properties at $BaTiO_3$ thicknesses in the nanometer range [35]. The high resolution image also confirmed the XRD results that the $BaTiO_3$ layer was amorphous. An electron diffraction pattern taken from the $BaTiO_3$ layer (Figure 9.b) showed a diffuse pattern indicative of a mostly amorphous material. Having a broad, continuous ring around the center transmission spot indicates the presence of short range order molecules or crystallites consisting of a small number of atoms randomly oriented through out the material. As stated previously, the presence of

ferroelectric behavior in these amorphous films was a phenomenon that had not been found within the available literature.

3.5. Discussion

Previous research efforts on these $BaTiO_3$ films with either Ni or Pt electrodes has shown the ability to achieve permittivities from 500 to over 1000 with losses from 0.01 to 0.10 and resistances consistently greater than 10 GΩ [34-36]. These same studies showed that $BaTiO_3$ films were capable of exhibiting ferroelectric behavior. All of the measured dielectric properties were found to be related to interactions between the process parameters during sputter deposition by a statistical design of experiments. The microstructural and chemical data reported above was done to provide insight on how these dielectric responses were being developed.

It has been noted in several sources that the grain boundaries in polycrystalline $BaTiO_3$ typically have lower leakage currents (and thus higher resistances), higher breakdown strengths, and higher capacitance than the grains [2, 12, 15, 43]. As grain boundaries can be considered disordered grains with limited chemical differences, the large measured resistances in the giga-ohm range and low loss values below 0.10 was not altogether surprising given that the deposited films were not observed to have any significant amount of cracks or pinholes through which the electrodes could bypass the $BaTiO_3$ and make electrical contact. The presence of permittivity values greater than 500 was also not unexpected from the amorphous films given the increased capacitance typical of $BaTiO_3$ grain boundaries [2]. The dielectric response that does not fit the previous patterns in the literature was the presence of ferroelectric behavior in a predominately amorphous film.

Literature has only reported the presence of ferroelectricity for polycrystalline films [1, 40-42]. Even thin films with nano-crystalline grain sizes portraying cubic or pseudo-cubic diffraction characteristics have been shown to develop well-defined ferroelectric hysteresis patterns [42]. No sources, however, have been found that relate the finding of the ferroelectric behavior in amorphous $BaTiO_3$. Films have generally required high deposition temperatures and/or high temperature annealing in order to develop a polycrystalline grain structure [13, 14, 23, 25, 39]. The use of elevated

temperatures, however, can lead to the formation of cracks and increased residual stresses within the films due to thermal mismatch [1, 6, 13]. Thus the presence of ferroelectricity in thin films not requiring the use of temperatures greater than 300°C is unique. The ferroelectric behavior of these amorphous films, however, requires a renewed look at the phenomenon giving rise to the unexpected hysteretic response.

The presence of remnant polarization in these films indicated that there was some amount of switchable dipoles within the $BaTiO_3$ material. As neither XRD nor TEM showed the presence of appreciable crystallinity, these dipoles were not likely due to the formation of a perovskite crystal structure. Thus, some other structural mechanism would have to be responsible for the dipole formation. The chemical data from XPS suggests a condition where there was an excess of oxygen atoms within the films. As the electron diffraction pattern showed a broad, diffuse ring typical of short range order, it is possible that the oxygen atoms formed octahedrons with Ti interstitials (e.g. TiO_6 octahedra). The Ba atoms would then be randomly dispersed throughout the structure between the randomly oriented octahedrons. In this arrangement the Ti would form a dipole in the interstitial site, which would account for the presence of the ferroelectricity in these films. The fact that there were no grains or any long range order would create a situation where there was no definable domain structure. It has been suggested that the disappearance of domain walls in a dielectric could lead to a significant increase in the polarizability of a material over the maximum achievable value in the bulk ceramic [42]. If this theory regarding the disappearance of domain walls is accurate, the fact that there are no domain walls in these films would account for the increased coercive fields and remnant polarizations observed during hysteresis measurements.

4. Summary

The chemical and structural characteristics of sputtered $BaTiO_3$ films with thicknesses between 100 and 150 nm with approximately 20 nm thick electrodes of either Ni or Pt was examined. Atomic force microscopy found that the Ni films had an R_a value of 0.67 nm and the $BaTiO_3$ films were roughly twice as rough with an R_a value of 1.4 nm. Chemical analysis performed by XPS showed the majority of the films were oxygen rich,

and contained varying Ba:Ti ratios depending on deposition conditions. No direct correlation between the chemical data and measured dielectric properties was observed.

The films were found to be amorphous by XRD, electron diffraction, and high resolution TEM. The electron diffraction pattern did, however, suggest the presence of short range order within the material. The ferroelectric behavior of these amorphous films was contradictory to observed trends in the literature, and was related to the short range order, which was likely due to the presence of TiO_6 octahedra randomly dispersed throughout the film. These octahedra were thought to be responsible for the formation of Ti dipoles within the material, which, combined with the overall amorphous nature resulting in a film with no domain walls, allowed the development of large coercive fields and remnant polarizations that are otherwise unachievable with bulk $BaTiO_3$.

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Figures

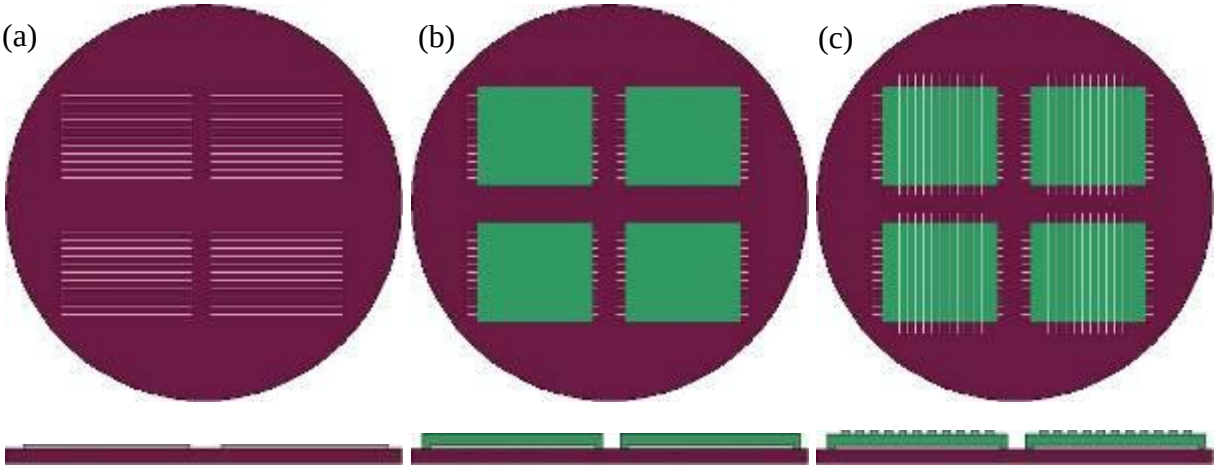

Fig. 1 – Process sequence followed for the patterned deposition of a single dielectric layer capacitor. 1st electrode layer (a), dielectric (b), and 2nd electrode layer (c). Top images are plan view looking at surface of substrate, and bottom images are cross sections. Vacuum was broken between layers to allow the exchanging of physical masks between depositions.

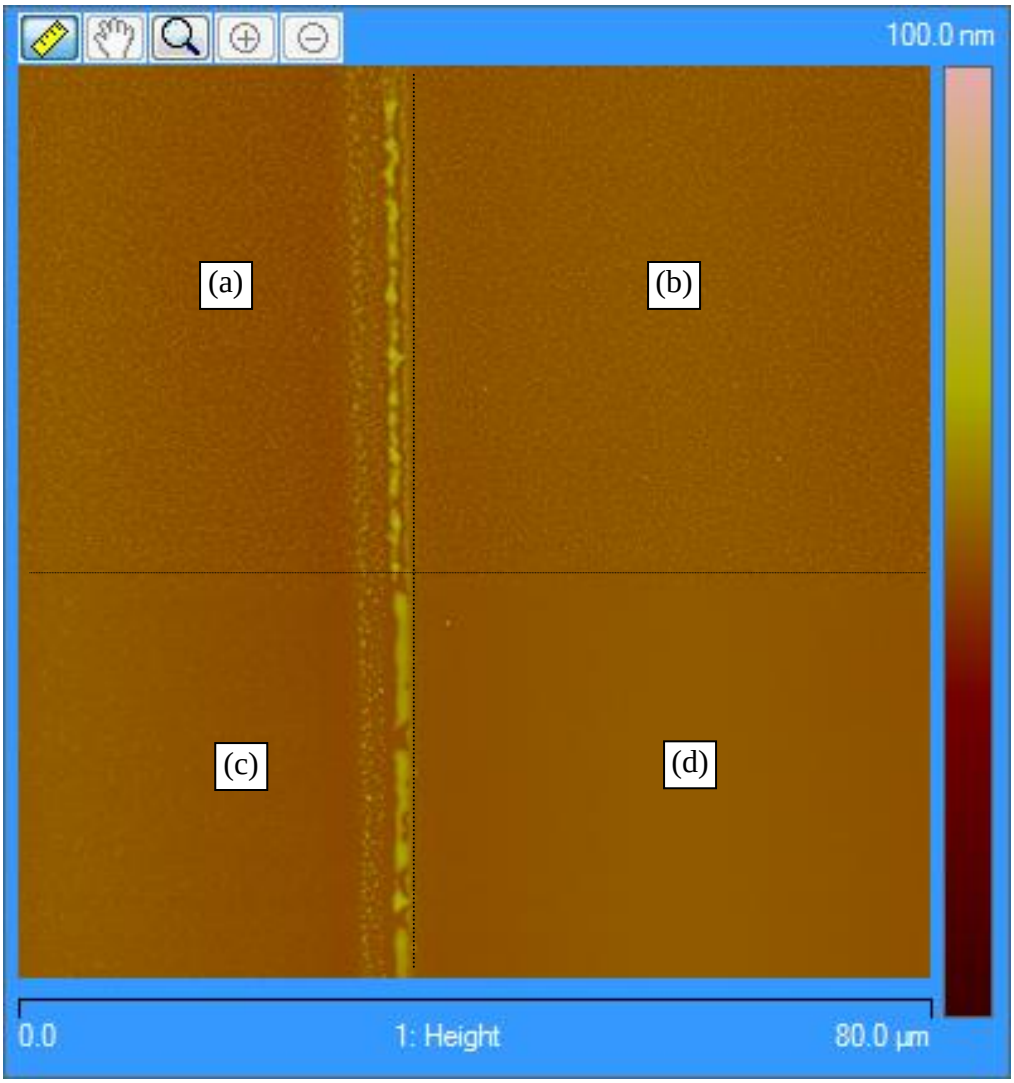

Figure 2 – Optical image of Region 1 examined by the AFM for surface roughness of the $BaTiO_3$ over Ni (a), $BaTiO_3$ over bare substrate (b), Ni electrode over substrate (c), and the bare substrate (d). Dotted lines added to aid in image interpretation. Region 2 examined by the AFM was another location similar to this.

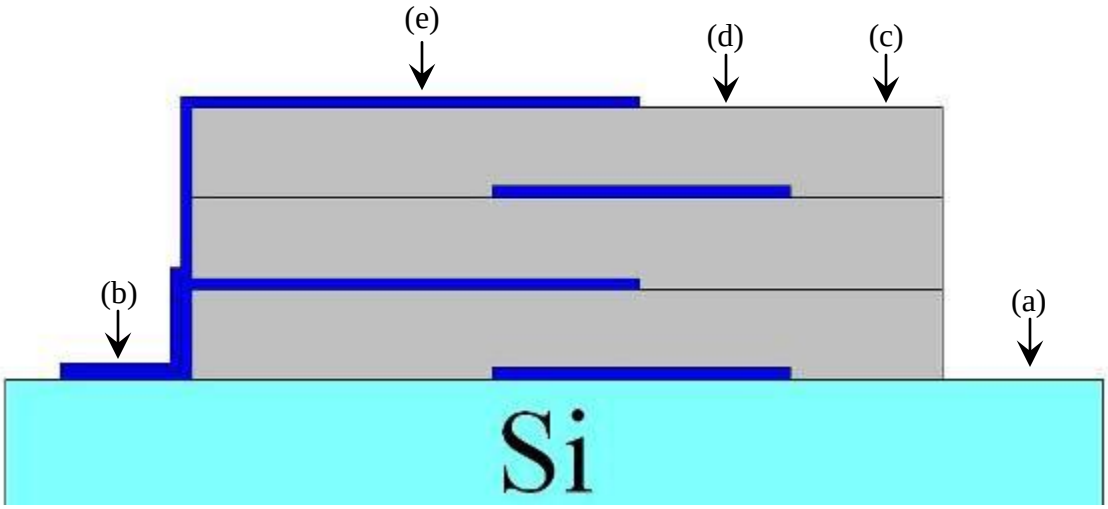

Figure 3 – Schematic cross-section of the five areas of interest for the AFM investigation; bare SiO_2 (a), two electrode layers over SiO_2 (b), three $BaTiO_3$ layers over SiO_2 (c), three layers of $BaTiO_3$ with two layers of electrodes (d), and an electrode layer over three layers of $BaTiO_3$ and one previous layer of electrode (e). Each $BaTiO_3$ layer was approximately 150 nm and each electrode layer was about 20 nm.

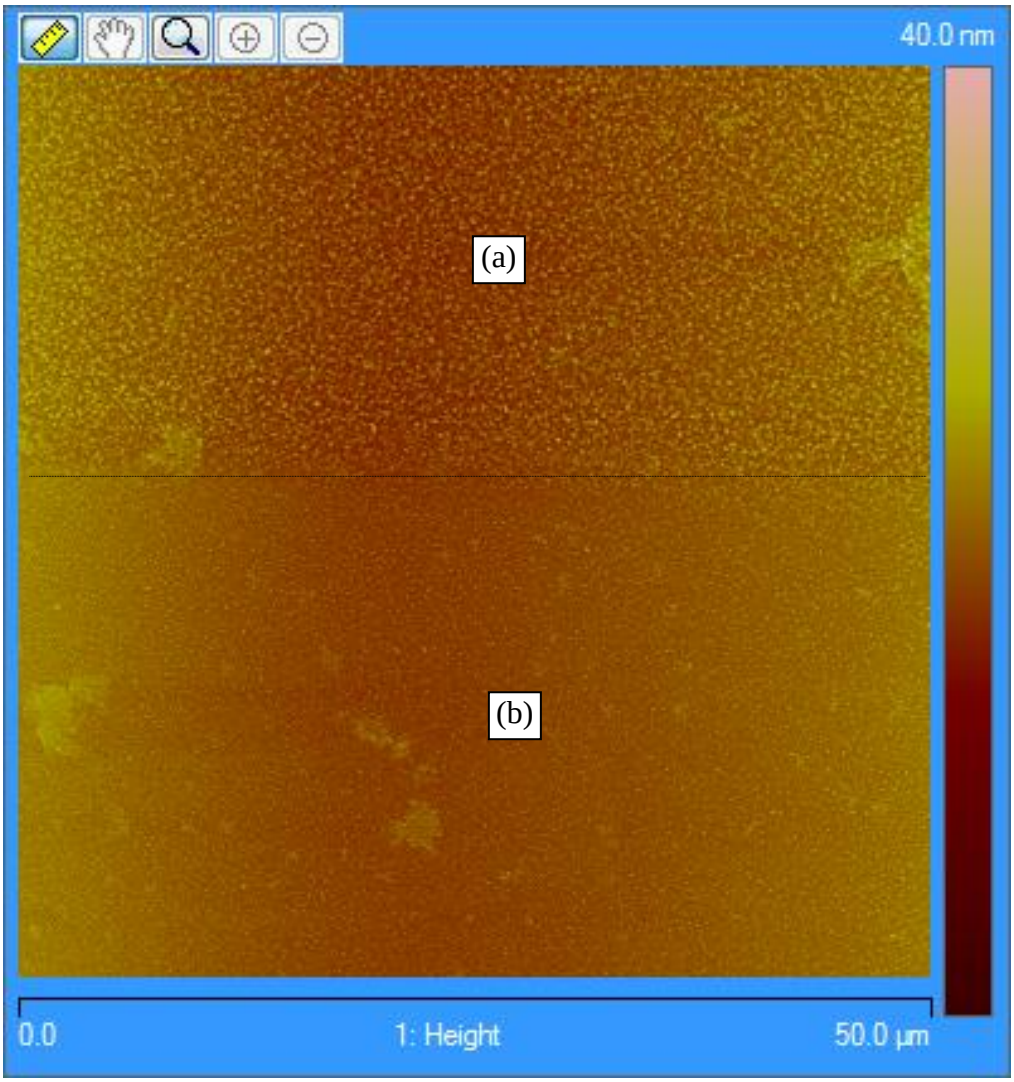

Figure 4 – Optical image of Region 3 examined by the AFM for surface roughness of the $BaTiO_3$ over the bare substrate (a) and Ni over $BaTiO_3$ (b). Dotted lines added to aid in image interpretation.

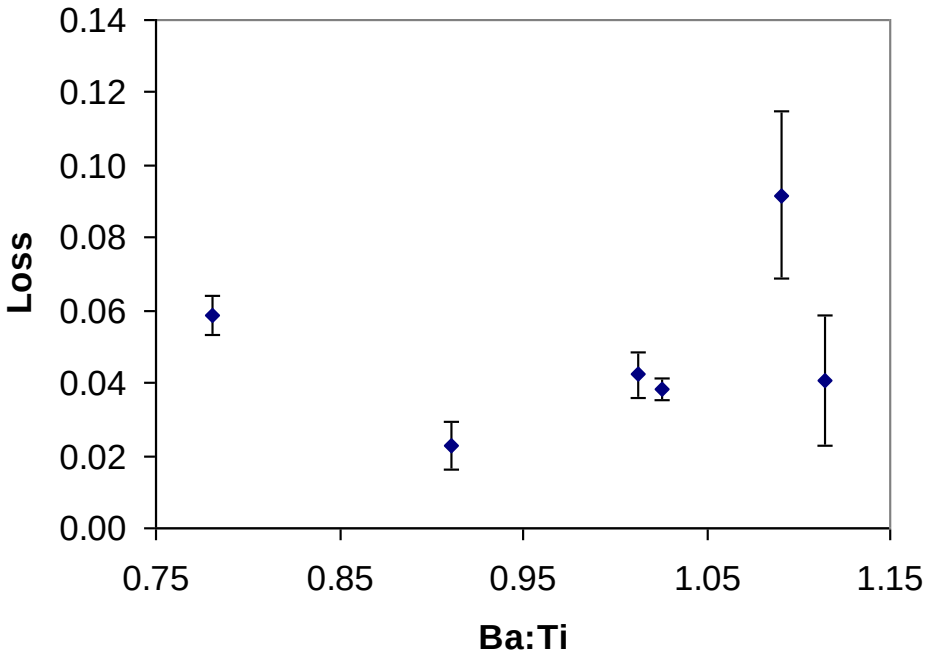

Figure 5 – Measured loss values of the six $BaTiO_3$ films examined by XPS versus the calculated Ba:Ti ratio. Plots were also made for the (Ba+Ti):O, Ba:O, and Ti:O ratios with a similar lack of observable trends between the chemical data and measured properties.

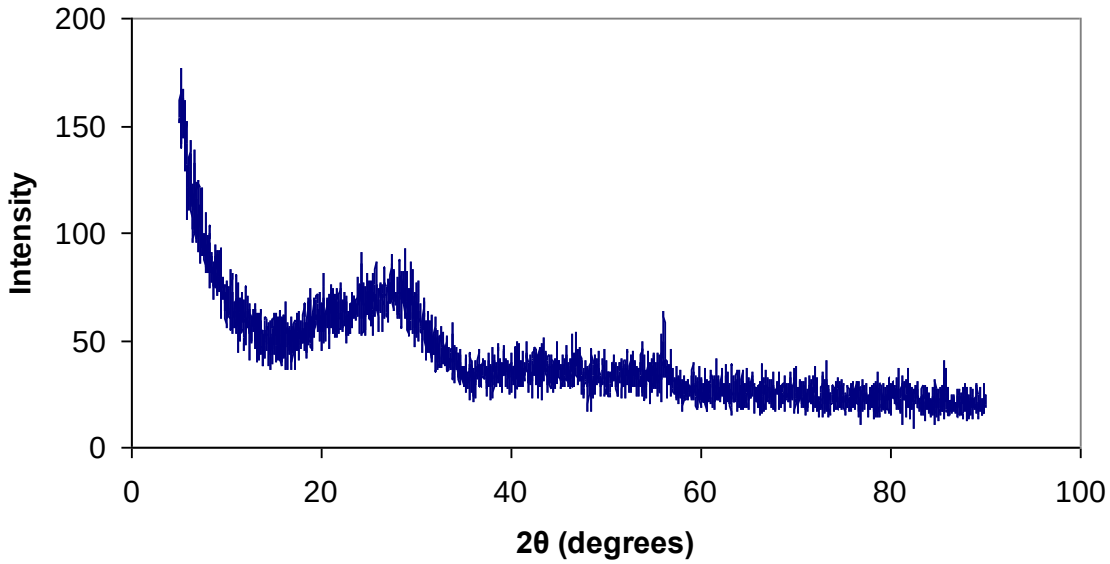

Figure 6 – Typical XRD plot observed for the R1, R4, and R7 specimens suggesting the films are amorphous. The peak for Si <111> is at 29°, and $BaTiO_3$ <100> and <111> was at 22° and 39°, respectively.

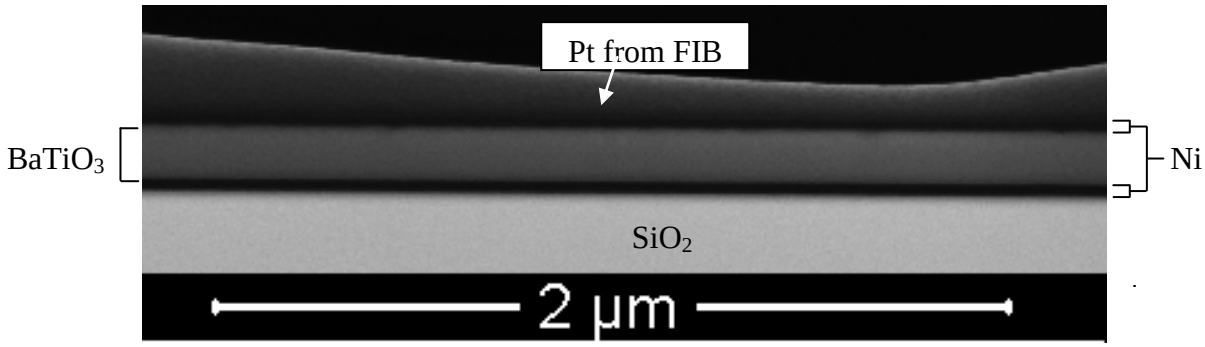

Figure 7 – Typical FIB image of a cross-section of a $BaTiO_3$ nano-capacitor. This image was taken from a device with Pt electrodes and a layer of $BaTiO_3$ deposited at 100 W, 30% O_2, and 573K.

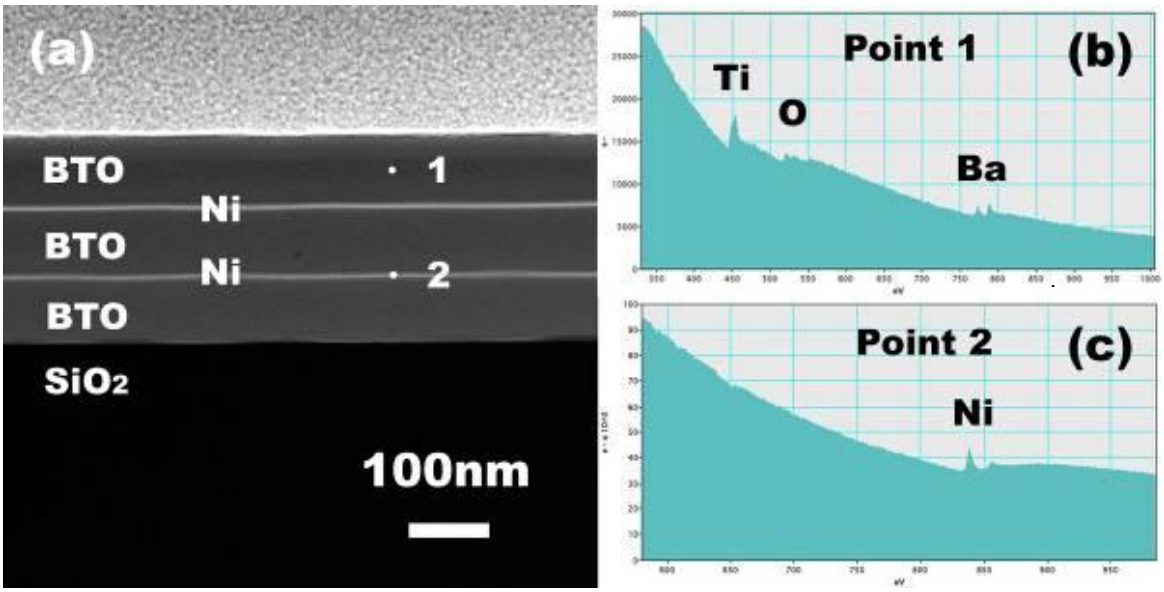

Figure 8 – Results of the EELS analysis from the three layer $BaTiO_3$ MLC with Ni electrodes.

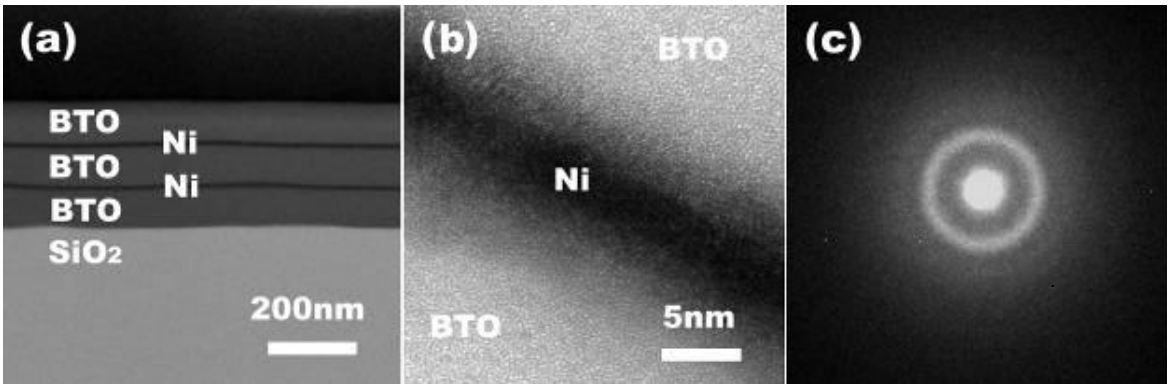

Figure 9 – A FIB cross-section image (a) showing a lower magnification view of the high resolution TEM cross-section image (b). An electron diffraction pattern (c) confirms the $BaTiO_3$ is mostly amorphous with only short range order.

Tables

Table I. Roughness measurements, R_a, for the three AFM examined regions

	Region 1 (Figure 2)	**Region 2**	**Region 3 (Figure 4)**	**Average Values**
Bare SiO_2	0.19 nm	0.18 nm	---	0.19 nm
Ni over $BaTiO_3$	---	---	0.67 nm	0.67 nm
Ni over SiO_2	0.63 nm	0.69 nm	---	0.66 nm
$BaTiO_3$ over Ni	1.3 nm	1.4 nm	---	1.4 nm
$BaTiO_3$ over SiO_2	1.2 nm	1.2 nm	1.43 nm	1.3 nm

Table II. – Processing conditions of the six specimens examined by XPS

	Deposition Power (W)	**%O_2 in Plasma**	**Deposition Temperature (K)**
R1	200	30	293
R4	200	50	433
R7	150	50	293
R8	100	30	573
R9	150	10	573
R10	150	30	433

Table III – Chemical data from the XPS investigation with the measured dielectric properties

	Ba:Ti	**(Ba+Ti):O**	**Permittivity**	**Loss**	**Resistance (GΩ)**
R1	1.1	0.58	575	0.092	16
R4	0.78	0.70	1033	0.059	270
R7	0.91	0.61	280	0.023	92
R8	1.1	0.45	635	0.041	110
R9	1.0	0.44	718	0.038	76
R10	1.0	0.49	713	0.042	190
Standard	1.0	0.66	---	---	---

General Conclusion

The initial study of sputtered $BaTiO_3$ with Ni electrodes using a Box-Behnken design of experiments showed the wide variety of electrical responses achievable with these devices. The permittivity was found to vary from 100 to 10,000 depending on process conditions and testing method (i.e. either AC or DC). Losses were found to be between 0.013 and 0.570 with resistances between 15 and 360 GΩ, again depending on the deposition conditions. The films were also determined to have either a paraelectric or ferroelectric nature depending on the sputtering parameters used. The results from the design of experiments allowed the prediction and fabrication of an optimized $BaTiO_3$ capacitor with a thickness of approximately 100 nm and Ni electrodes of approximately 20 nm in thickness. The predicted dielectric properties are compared to the measured values in Table I. The percentage differences between the predicted and actual values were found to vary from approximately 20% to 95% despite the high R^2 values associated with the statistical DOE models. This suggests the presence of higher order interactions between the process parameters that can only be modeled using a larger set of specimens. The ideal case would be the investigation of a 3^3 full factorial which would allow the modeling of all interactions between the parameters, but would require 127 specimens to be fabricated and tested.

Table I. Comparison of the predicted and measured dielectric properties for the optimized deposition of 100 nm $BaTiO_3$ with Ni electrodes

	Permittivity (at 1kHz AC)	**Loss**	**Resistance at +1 V (DC)**	**Hysteresis-based Permittivity**	**Remnant Polarization**
Predicted	760	0.011	210 GΩ	600	31 $\mu C/cm^2$
Measured	600	0.035	150 GΩ	2800	1.8 $\mu C/cm^2$
Percent Difference	21%	69%	31%	79%	94%

The results of the Box-Behnken DOE that was performed in Papers 2 and 3, although not as accurate as was hoped, are important for two reasons. First, although the predictive models are not as accurate as the R^2 values suggest, the fact that the data could be modeled to a certain degree suggests that the system can be more accurately modeled with additional test points. The models were also at least minimally predictive in the sense that they accurately predicted general trends in the data. Second, the specimens showed a repeatable and reliable series of dielectric data from location to location on a single wafer, and from wafer to wafer of the same deposition conditions. This gives promise for any potential commercial application of these films in that they deliver reliable properties.

The dielectric thickness studies resulted in two key findings. First, the sputtered $BaTiO_3$ nano-capacitors are highly susceptible to an interfacial layer that forms between the electrode and dielectric. This interfacial layer was found to behavior as a capacitor in series with the $BaTiO_3$, and had similar permittivities across the different deposition conditions and electrodes. The second, and perhaps more important, insight gained from this series of experiments was the conclusion that the electrode material, whether Ni or Pt, has a significant impact on the measured dielectric properties. Pt electrodes were found to impart a larger permittivity (from 890 to 1950), but also resulted in lower loss (0.024 to 0.114) and decreased device yield across the wafer (average of about 95%). The use of Ni electrodes resulted in permittivities between 320 and 760 with losses from 0.019 to 0.130 and yields of close to 99%. Minimum loss values were found to occur at $BaTiO_3$ thicknesses of between 50 and 100 nm.

Electrode thickness was also found to impact the measured dielectric properties. The maximum hysteresis-based permittivity (1440) and resistance (360 GΩ) was found when the electrodes were approximately 90 nm thick (as measured by FIB cross-section). Loss and permittivity as measured with an AC current was found to depend strongly on the frequency at electrode thicknesses below 90 nm, but otherwise consistent with thicker electrodes. In the frequency independent region, the 90 nm thick electrode was found to have the lowest average loss of 0.036 and lowest average permittivity of 540. The activation energy for conduction was also found to vary between 0.055 and 1.11 eV depending on the electrode thickness.

The microstructural and chemical investigations of a variety of the $BaTiO_3$ devices revealed the films to be amorphous and stoichiometrically rich in oxygen. The presence of ferroelectricity in amorphous films was not observed in the literature, which repeatedly stated that a minimum of a nano-crystalline structure was required to obtain such behavior. The presence of a broad, diffuse ring on the electron diffraction pattern suggested a short range order was apparent in the material. This finding combined with the determination by XPS of excess oxygen suggests the presence of TiO_6 octahedra that are randomly dispersed throughout the $BaTiO_3$ films. These octahedra, with the Ti in the interstitial, would result in the presence of a ferroelectric response on the hysteresis plots. The fact that these octahedra have no long range order results in a material that is not likely to have any domain walls, which results in the abnormally large remnant polarizations and coercive fields observed with these fields.

APPENDIX A

ANOVA TABLES AND STATISTICAL MODELS

1. Introduction

The following pages include the analysis of variance (ANOVA) tables from the DOE investigation of papers 2 and 3. These tables were calculated by Design-Expert 7.1.3 after the inclusion of the model verification and optimization specimens, and represent the most complete form of the data from the work performed. Following each of the ANOVA tables is the final mathematical equation that was calculated by the DOE software to model the given response as a function of the actual variable values (i.e. $\tan \delta = f(\text{power}, \%O2, \text{temperature})$).

Assuming a confidence level of 5% ($\alpha = 0.05$), a term is said to be significant if the associated p-value is less than 0.05. The first term on the ANOVA that was testing in this manner is the model p-value. If the model p-value is less that 0.05 the data was found to exhibit a significant pattern with respect to the process variables and/or variable interactions. If the model was found to be significant, the interaction and process variable terms were examined using the same criteria (i.e. a significant interaction between terms was found if the p-value was less than 0.05).

Some testing was conducting where enough data was collected to allow for a lack of fit test to be conducted on the model. This test measures the fit of the predictive model to the measured data points and give a reasonable assessment of the correlation between the two. A lack of fit with a p-value less than 0.05 indicated a significant lack of fit between the model and the data, and was an indication that despite the presence of a strong dependence on the process parameters (i.e. the model p-value was below 0.05), the calculated model does not accurately represent the available data.

2. Resistance

Table I. ANOVA table for the +1 V Resistance

Source	Sum of Squares	df	Mean Square	F Value	p-value Prob > F
Model	4.14E+11	12	3.45E+10	20.52	< 0.0001
A-Power	4.49E+10	1	4.49E+10	26.70	< 0.0001
B-%O_2	2.05E+09	1	2.05E+09	1.22	0.2797
C-Temp	1.09E+11	1	1.09E+11	64.86	< 0.0001
AB	1.10E+11	1	1.10E+11	65.56	< 0.0001
AC	1.27E+10	1	1.27E+10	7.54	0.0106
BC	4.29E+10	1	4.29E+10	25.53	< 0.0001
A^2	6.25E+09	1	6.25E+09	3.72	0.0645
B^2	4.90E+07	1	4.90E+07	0.03	0.8657
C^2	2.70E+09	1	2.70E+09	1.61	0.2159
A^2B	1.79E+10	1	1.79E+10	10.66	0.0030
A^2C	3.55E+10	1	3.55E+10	21.13	< 0.0001
AB^2	6.62E+10	1	6.62E+10	39.37	< 0.0001
Pure Error	4.54E+10	27	1.68E+09		
Cor Total	4.59E+11	39			

The Model F-value of 20.52 implies the model is significant. There is only a 0.01% chance that a "Model F-Value" this large could occur due to noise.

Values of "Prob > F" less than 0.0500 indicate model terms are significant. In this case A, C, AB, AC, BC, A^2B, A^2C, AB^2 are significant model terms.

Values greater than 0.1000 indicate the model terms are not significant.

$$R = -1.4 \times 10^6 + (24000 * P) - (47000 * \%O_2) + (4700 * T) + (540 * P * \%O_2) - (71 * P * T) - (21 * \%O_2 * T) - (75 * P^2) + (780 * \%O_2^2) + (1.01 * T^2) - (1.08 * P^2 * \%O_2) + (0.22 * P^2 * T) - (5.167 * P * \%O_2^2)$$

Where R is the resistance at +1V in Ω, P is RF-sputter power (W), $\%O_2$ is the percent oxygen in a 5 mtorr plasma (balance Ar), and T is the deposition temperature in Kelvin.

3. DC Permittivity (Hysteresis-based)

Table II. ANOVA table for the hysteresis-based, DC permittivity

Source	Sum of Squares	df	Mean Square	F Value	p-value Prob > F
Model	2.64E+08	11	2.40E+07	173.06	< 0.0001
A-Power	1.06E+04	1	1.06E+04	0.08	0.7845
B-%O_2	1.12E+08	1	1.12E+08	808.04	< 0.0001
C-Temp	2.20E+07	1	2.20E+07	158.96	< 0.0001
AB	1.78E+05	1	1.78E+05	1.28	0.2677
AC	2.08E+06	1	2.08E+06	14.99	0.0007
BC	2.65E+07	1	2.65E+07	191.34	< 0.0001
A^2	1.99E+07	1	1.99E+07	143.14	< 0.0001
B^2	7.70E+06	1	7.70E+06	55.55	< 0.0001
C^2	2.25E+07	1	2.25E+07	162.25	< 0.0001
A^2B	6.68E+07	1	6.68E+07	481.44	< 0.0001
A^2C	7.19E+06	1	7.19E+06	51.83	< 0.0001
Residual	3.61E+06	26	1.39E+05		
Lack of Fit	6.81E+03	1	6.81E+03	0.05	0.8296
Pure Error	3.60E+06	25	1.44E+05		
Cor Total	2.68E+08	37			

The Model F-value of 173.06 implies the model is significant. There is only a 0.01% chance that a "Model F-Value" this large could occur due to noise.

Values of "Prob > F" less than 0.0500 indicate model terms are significant. In this case B, C, AC, BC, A^2, B^2, C^2, A^2B, A^2C are significant model terms. Values greater than 0.1000 indicate the model terms are not significant.

The "Lack of Fit F-value" of 0.05 implies the Lack of Fit is not significant relative to the pure error. There is a 82.96 % chance that a "Lack of Fit F-value" this large could occur due to noise. Non-significant lack of fit is good – we want the model to fit.

$$\varepsilon_{DC} = 77000 - (803 * P) - (1800 * \%O_2) - (150 * T) + (21 * P * \%O_2) + (0.91 * P * T) + (0.56 * \%O_2 * T) + (2.77 * P^2) + (2.67 * \%O_2{}^2) + (0.09 * T^2) - (0.07 * P^2 * \%O_2) - (3.22 \times 10^{-3} * P^2 * T)$$

Where ε_{DC} is the hysteresis-based, DC permittivity, P is RF-sputter power (W), $\%O_2$ is the percent oxygen in a 5 mtorr plasma (balance Ar), and T is the deposition temperature in Kelvin.

4. Remnant Polarization

Table III. ANOVA table for the remnant polarization

Source	Sum of Squares	df	Mean Square	F Value	p-value Prob > F
Model	3.97E+04	11	3.61E+03	23.7	< 0.0001
A-Power	3.82E+01	1	3.82E+01	0.3	0.6211
B-%O_2	8.85E+03	1	8.85E+03	58.0	< 0.0001
C-Temp	5.68E+03	1	5.68E+03	37.3	< 0.0001
AB	3.54E-01	1	3.54E-01	0.0	0.9620
AC	9.71E+02	1	9.71E+02	6.4	0.0178
BC	4.21E+03	1	4.21E+03	27.6	< 0.0001
A^2	3.30E+03	1	3.30E+03	21.6	< 0.0001
B^2	8.12E+03	1	8.12E+03	53.2	< 0.0001
C^2	4.23E+01	1	4.23E+01	0.3	0.6028
A^2B	4.78E+03	1	4.78E+03	31.4	< 0.0001
A^2C	1.35E+04	1	1.35E+04	88.5	< 0.0001
Residual	4.12E+03	27	1.53E+02		
Lack of Fit	5.66E+01	1	5.66E+01	0.4	0.5525
Pure Error	4.06E+03	26	1.56E+02		
Cor Total	4.38E+04	38			

The Model F-value of 23.66 implies the model is significant. There is only a 0.01% chance that a "Model F-Value" this large could occur due to noise.

Values of "Prob > F" less than 0.0500 indicate model terms are significant. In this case B, C, AC, BC, A2, B^2, A^2B, A^2C are significant model terms. Values greater than 0.1000 indicate the model terms are not significant.

The "Lack of Fit F-value" of 0.36 implies the Lack of Fit is not significant relative to the pure error. There is a 55.25% chance that a "Lack of Fit F-value" this large could occur due to noise. Non-significant lack of fit is good -- we want the model to fit.

$$P_{rem} = -1300 + (16 * P) - (3.32 * \%O_2) + (3.18 * T) + (0.17 * P * \%O_2) - (0.04 * P * T) - (6.69 \times 10^{-3} * \%O_2 * T) - (0.05 * P^2) - (0.09 * \%O_2{}^2) + (1.27 \times 10^{-4} * T^2) - (5.65 \times 10^{-4} * P^2 * \%O_2) + (1.36 \times 10^{-4} * P^2 * T)$$

Where P_{rem} is the remnant polarization ($\mu C/cm^2$), P is RF-sputter power (W), $\%O_2$ is the percent oxygen in a 5 mtorr plasma (balance Ar), and T is the deposition temperature in Kelvin.

5. AC Permittivity at 1 kHz and 1 V_{rms}

Table IV. ANOVA table for the AC permittivity

Source	Sum of Squares	df	Mean Square	F Value	p-value Prob > F
Model	2.89E+07	13	2.22E+06	625.8	< 0.0001
A-Power	7.33E+03	1	7.33E+03	2.1	0.1514
B-$\%O_2$	9.59E+06	1	9.59E+06	2700.5	< 0.0001
C-Temp	4.97E+05	1	4.97E+05	139.8	< 0.0001
AB	3.06E+06	1	3.06E+06	860.5	< 0.0001
AC	2.45E+06	1	2.45E+06	688.6	< 0.0001
BC	2.20E+06	1	2.20E+06	620.3	< 0.0001
A^2	1.27E+06	1	1.27E+06	358.9	< 0.0001
B^2	3.07E+05	1	3.07E+05	86.5	< 0.0001
C^2	6.43E+05	1	6.43E+05	181.2	< 0.0001
A^2B	8.13E+06	1	8.13E+06	2288.5	< 0.0001
A^2C	3.99E+05	1	3.99E+05	112.3	< 0.0001
AB^2	3.25E+05	1	3.25E+05	91.6	< 0.0001
B^2C	3.47E+04	1	3.47E+04	9.8	0.0019
Pure Error	2.38E+06	670	3.55E+03		
Cor Total	3.13E+07	683			

The Model F-value of 625.77 implies the model is significant. There is only a 0.01% chance that a "Model F-Value" this large could occur due to noise.

Values of "Prob > F" less than 0.0500 indicate model terms are significant. In this case B, C, AB, AC, BC, A^2, B^2, C^2, A^2B, A^2C, AB^2, B^2C are significant model terms.

Values greater than 0.1000 indicate the model terms are not significant.

$$\varepsilon_{AC} = 1900 + (4.46 * P) - (204 * \%O_2) + (3.98 * T) + (2.03 * P * \%O_2) - (0.12 * P * T) + (0.07 * \%O_2 * T) - (0.01 * P^2) + (0.83 * \%O_2^2) + (3.87 \times 10^{-3} * T^2) - (5.78 \times 10^{-3} * P^2 * \%O_2) + (3.33 \times 10^{-4} * P^2 * T) - (2.88 \times 10^{-3} * P * \%O_2^2) - (6.14 \times 10^{-4} * \%O_2^2 * T)$$

Where ε_{AC} is the permittivity under an AC field at 1 kHz and 1 V_{rms}, P is RF-sputter power (W), $\%O_2$ is the percent oxygen in a 5 mtorr plasma, and T is the deposition temperature in Kelvin.

6. Dielectric Loss

Table V. ANOVA table for the loss tangent (tan δ) at 1 kHz and 1 V_{rms}

Source	Sum of Squares	df	Mean Square	F Value	p-value Prob > F
Model	4.65E-01	13	3.58E-02	80.64	< 0.0001
A-Power	1.62E-04	1	1.62E-04	0.36	0.5463
B-$\%O_2$	1.52E-02	1	1.52E-02	34.23	< 0.0001
C-Temp	2.94E-01	1	2.94E-01	662.27	< 0.0001
AB	1.61E-02	1	1.61E-02	36.19	< 0.0001
AC	1.65E-04	1	1.65E-04	0.37	0.5418
BC	1.20E-03	1	1.20E-03	2.71	0.1004
A^2	5.35E-03	1	5.35E-03	12.07	0.0005
B^2	8.71E-03	1	8.71E-03	19.65	< 0.0001
C^2	4.76E-03	1	4.76E-03	10.72	0.0011
A^2B	1.34E-02	1	1.34E-02	30.27	< 0.0001
A^2C	2.43E-01	1	2.43E-01	548.67	< 0.0001
AB^2	2.17E-03	1	2.17E-03	4.88	0.0275
B^2C	2.02E-01	1	2.02E-01	454.90	< 0.0001
Pure Error	2.97E-01	670	4.44E-04		
Cor Total	7.62E-01	683			

The Model F-value of 80.64 implies the model is significant. There is only a 0.01% chance that a "Model F-Value" this large could occur due to noise.

Values of "Prob > F" less than 0.0500 indicate model terms are significant.
In this case B, C, AB, A^2, B^2, C^2, A^2B, A^2C, AB^2, B^2C are significant model terms.

Values greater than 0.1000 indicate the model terms are not significant.

$$\tan\delta = -2.91 + (0.035 * P) + (0.043 * \%O_2) + (6.77 \times 10^{-3} * T) - (7.56 \times 10^{-5} * P * \%O_2) - (7.79 \times 10^{-5} * P * T) - (8.81 \times 10^{-5} * \%O_2 * T) - (1.17 \times 10^{-4} * P^2) - (6.55 \times 10^{-4} * \%O_2^2) - (3.33 \times 10^{-7} * T^2) + (2.35 \times 10^{-7} * P^2 * \%O_2) + (2.60 \times 10^{-7} * P^2 * T) + (2.35 \times 10^{-7} * P * \%O_2^2) + (1.48 \times 10^{-6} * \%O_2^2 * T)$$

Where tan δ is the dielectric loss under an AC field at 1 kHz and 1 V_{rms}, P is RF-sputter power (W), $\%O_2$ is the percent oxygen in a 5 mtorr plasma, and T is the deposition temperature in Kelvin.

APPENDIX B

DETAILED SPUTTERING PROCEDURE

1. Introduction

The following sections detail the precise methods and procedures used to sputter the nano-scale capacitors that were researched throughout the dissertation. Due to the necessity of brevity in the publications, a large amount of information regarding the deposition techniques had to be omitted from the text. The missing information is compiled here in the hopes of allowing future research efforts to be initiated with as little transition time as possible.

2. Wafer Cleaning

A properly cleaned wafer was observed to give optimal results. Given the laboratory environment used for the reported studies, a perfectly clean substrate was nearly impossible to obtain, but the following procedure was found to give adequate results with minimal effort and no harsh or environmentally hazardous materials.

Wafers were cleaned immediately prior to deposition, and a virgin wafer was always used. The wafer was initially submerged in laboratory grade acetone, and agitated beneath the surface of the liquid for three minutes. It was then allowed to air dry for a minimum of 30 seconds before submersion in laboratory grade methanol, and agitated for another three minutes. Following another air dry for at least 30 seconds, the wafer was submerged in fresh DI water, and agitated for another three minutes. The wafer surface was then sprayed with fresh DI water, and then spin dried at 6000 rpm for 90 seconds. To ensure complete dehydration of the wafer surface (necessary for adequate adhesion of subsequent layers) the wafer was placed on a standard hot plate pre-heated to approximately 200°C, and allowed to soak for 5 minutes. The wafer resulting from this procedure was found to have a minimum of surface particles, and gave the highest observable device yields post-deposition.

The agitation of the wafer within the liquid cleaners was performed with wafer tweezers at the edge of the wafer in an up-and-down motion. The intent was to ensure fresh liquid arriving at the surface of the wafer to maximize the cleaning efficiency. Clear liquids with no sediment in the container, and clean equipment (hot plate and spin coater) were also found to be necessary for optimum results, particularly with the thinner (< 50 nm) dielectric layers. Placing the cleaned substrate into the sputter deposition

chamber as soon after the dehydration bake as possible was found to minimize surface contamination and particle accumulation.

3. Additional Specimen Preparations

In addition to the cleaned wafer, a glass slide (cleaned with acetone on a Kimwipe towel), and two sets of four pre-cleaned pieces of Si/SiO_2 wafer cut into approximately 1 cm squares were also placed on the sample platen. The glass slide was set in place with one piece of tape running through the middle of the slide to allow for profilometer measurements on either side of the area patterned by the tape. The glass slide was replaced between each of the depositions. The wafer pieces were added to allow for specimens to be submitted for chemical and microstructural analysis without the loss of working devices. The first set of four Si/SiO_2 pieces were on the sample platen through all series of depositions in order to develop a specimen with the multi-layer structures. The second set was placed on the platen only for the dielectric deposition in order to more precisely measure the chemical characteristics of the $BaTiO_3$ without the presence of the electrode material.

Lastly, the shadow mask for the given deposition was always cleaned with acetone on a Kimwipe prior to alignment on the wafer. Additionally, the electrode mask channels were visually inspected to ensure they were clear of debris. All of the masks used for the research reported in this dissertation had a central hole in the mask to allow taping of the mask directly to the wafer, and minimize the effects of bowing resulting from taping the edges of the mask. In total, the mask was taped in five places on the wafer: the center and each of the four edges.

4. Sputtering Preparations

The loaded sample platen was placed in the sputter system load lock, and allowed to pump down to below 100 mtorr prior to insertion into the deposition chamber. After the platen was fully loaded the sputter system was allowed time to return to a base vacuum of at least 5×10^{-6} torr prior to any depositions. Once base vacuum was reached, the sputter target was cleaned prior to actual deposition. For the electrode metals, this included a five to ten minute sputtering in the target shutter in a pure Ar plasma at the DC

power and working pressure designated for that deposition. For the dielectric depositions, this cleaning was performed under the desired sputtering conditions for that deposition (i.e. chosen $\%O_2$, deposition temperature, and sputter power) for 30 minutes to ensure system equilibrium and the removal of any surface contaminants. If the deposition temperature was above room temperature, the system was allowed to soak at temperature for a minimum of 30 minutes to ensure thermal saturation.

It was necessary in a few instances, particularly at low RF-powers, to keep the specimen in the load lock during the target cleaning. This was accomplished by keeping the sample platen on the loading fork in the load lock, opening the gate valve between the load lock and the chamber, and allowing the load lock and chamber to pump down to the requisite base vacuum. The target cleaning was then performed with the shutter open. Afterwards, the platen was introduced to the chamber, and deposition allowed to continue as normal. This was not performed for all specimens due to the significantly increased time required to achieve base vacuum with gate valve open.

It should also be noted the ceramic $BaTiO_3$ target was slowly ramped up to the desired RF-power to prevent thermal shock of the target. This was accomplished by setting the initial power to 25 W, and after striking the plasma, allowing the target to soak for 60 seconds prior to initiating the ramp. After the soak, the power was increased by 25 W every 30 seconds until the desired sputter power was achieved. The same protocol was used after deposition to turn the power off (i.e. decreasing the power by 25 W every 30 seconds until 25 W was achieved).

5. Post Deposition Handling

After deposition of the final layer, the wafer was labeled with A-V along the bottom electrodes, and 1-22 along the top electrodes (or the first deposited electrode layer and second deposited electrode layer in the case of multi-layer capacitors). The wafer was then tested with the hand held multi-meter for initial device resistance and wafer yield calculations. Prior to further electrical testing the wafer was sectioned into quarters with a diamond scribe, and one of the quarters randomly selected for the in-depth electrical characterization.

APPENDIX C

RESULTS OF LOW TEMPEARUTRE ANNEALING IN AIR OR VACUUM

1. Introduction

In addition to testing in the as-deposited condition, the majority of specimens were also annealed at 300°C for one hour in either open air or under vacuum (1-5x10^{-6} torr). The open air condition was chosen as a basic oxidation atmosphere, and the vacuum as a de facto reduction atmosphere. The temperature of 300°C was selected due to the desire to minimize electrode diffusion into the dielectric and to avoid significant Ni oxidation. As annealing of $BaTiO_3$ devices based on powder processing techniques generally require temperatures of 500°C and higher [1-4], it was not known if 300°C was going to be sufficient to induce any significant change in the films.

2. Results

It was found that even at this low of an annealing temperature, the dielectric properties were found to be significantly altered (Tables B.1 and B.2). Analysis on the annealed DOE specimens revealed that the changes in AC permittivity and loss tangent at 1 kHz and 1 V_{rms} could be modeled based on the initial processing conditions. Like the as-deposited DOE results (Papers 2-3), this latter analysis on the annealed specimens revealed a complex interaction between the variables.

Table I. Annealing effects on loss and permittivity at 1 kHz and 1 V_{rms} for the DOE specimens

	As-Deposited		**Air Anneal**		**Vacuum Anneal**	
	Permittivity	**Loss**	**Permittivity**	**Loss**	**Permittivity**	**Loss**
1	580 ± 27	0.092 ± 0.022	19 ± 0.3	0.014 ± 0.005	570 ± 22	0.1038 ± 0.014
2	500 ± 18	0.042 ± 0.010	47 ± 1.2	0.040 ± 0.003	74 ± 0.3	0.0257 ± 0.003
3	800 ± 41	0.046 ± 0.005	47 ± 2.1	0.035 ± 0.006	840 ± 47	0.0680 ± 0.008
4	1030 ± 75	0.059 ± 0.005	19 ± 1.4	0.024 ± 0.010	550 ± 26	0.0481 ± 0.005
5	840 ± 80	0.039 ± 0.019	27 ± 2.6	0.018 ± 0.002	89 ± 7.3	0.0253 ± 0.005
6	940 ± 70	0.045 ± 0.003	21 ± 0.9	0.018 ± 0.001	25 ± 0.5	0.0149 ± 0.001
7	280 ± 80	0.023 ± 0.007	340 ± 6.7	0.081 ± 0.001	200 ± 4.9	0.0189 ± 0.005
8	630 ± 98	0.041 ± 0.018	150 ± 6.7	0.063 ± 0.010	460 ± 16	0.0539 ± 0.005
9	720 ± 24	0.038 ± 0.003	140 ± 7.2	0.031 ± 0.001	530 ± 18	0.0420 ± 0.006
10	710 ± 27	0.048 ± 0.006	160 ± 10	0.067 ± 0.013	550 ± 17	0.0796 ± 0.007
11	480 ± 17	0.042 ± 0.011	180 ± 5.8	0.052 ± 0.009	500 ± 15	0.0420 ± 0.005
12	460 ± 15	0.033 ± 0.002	160 ± 4.4	0.063 ± 0.002	94 ± 5.2	0.0321 ± 0.014
13	450 ± 16	0.062 ± 0.006	130 ± 2.7	0.076 ± 0.003	63 ± 0.6	0.0184 ± 0.003

Similar effects were also observed for the specimens from the $BaTiO_3$ thickness studies (Paper 4), electrode thickness studies (Paper 5), and the DOE model verification specimens (single layer and three layer MLC) as shown in Table B.2.

Table II. Annealing effects at 1 kHz and 1 V_{rms} for the non-DOE specimens

	As-Deposited		**Air Anneal**		**Vacuum Anneal**	
	Permittivity	**Loss**	**Permittivity**	**Loss**	**Permittivity**	**Loss**
R1-Thick	740 ± 26	0.052 ± 0.005	240 ± 30	0.064 ± 0.014	800 ± 33	0.035 ± 0.007
R4-Thick	590 ± 41	0.069 ± 0.022	140 ± 34	0.057 ± 0.012	790 ± 36	0.043 ± 0.010
R7-Thick	350 ± 12	0.043 ± 0.006	210 ± 31	0.060 ± 0.013	560 ± 210	0.036 ± 0.014
R1-Thin	460 ± 80	0.098 ± 0.019	60 ± 3.2	0.053 ± 0.006	530 ± 19	0.107 ± 0.009
R4-Thin	1000 ± 77	0.118 ± 0.008	220 ± 47	0.219 ± 0.037	320 ± 15	0.097 ± 0.012
R7-Thin	550 ± 120	0.044 ± 0.015	98 ± 7.5	0.118 ± 0.022	640 ± 260	0.055 ± 0.024
R1-ST	860 ± 80	0.242 ± 0.036	160 ± 40	0.163 ± 0.043	250 ± 23	0.097 ± 0.007
R4-ST	270 ± 23	0.092 ± 0.005	24 ± 3.7	0.069 ± 0.023	350 ± 12	0.142 ± 0.024
R7-ST	290 ± 84	0.044 ± 0.015	110 ± 31	0.099 ± 0.034	310 ± 140	0.058 ± 0.037
Pt-1-Thick	1730 ± 150	0.031 ± 0.004	790 ± 38	0.028 ± 0.002	750 ± 35	0.020 ± 0.001
Pt-4-Thick	810 ± 37	0.051 ± 0.005	1930 ± 990	0.055 ± 0.025	770 ± 46	0.042 ± 0.022
Pt-7-Thick	1400 ± 95	0.024 ± 0.004	620 ± 350	0.033 ± 0.022	270 ± 22	0.030 ± 0.002
Pt-1-Sm	1120 ± 130	0.035 ± 0.003	500 ± 130	0.039 ± 0.010	1290 ± 300	0.059 ± 0.016
Pt-4-Sm	1040 ± 130	0.064 ± 0.008	370 ± 25	0.045 ± 0.007	540 ± 120	0.047 ± 0.006
Pt-7-Sm	1040 ± 130	0.031 ± 0.006	620 ± 130	0.227 ± 0.083	1030 ± 260	0.049 ± 0.015
Pt-1-Thin	1370 ± 340	0.140 ± 0.053	750 ± 290	0.080 ± 0.018	330 ± 38	0.037 ± 0.005
Pt-4-Thin	470 ± 83	0.056 ± 0.009	1060 ± 280	0.079 ± 0.033	730 ± 100	0.070 ± 0.024
Pt-7-Thin	760 ± 61	0.057 ± 0.008	360 ± 110	0.044 ± 0.017	580 ± 39	0.047 ± 0.005
Pt-1-ST	740 ± 56	0.084 ± 0.003	590 ± 1.1	0.082 ± 0.008	610 ± 41	0.081 ± 0.005
Pt-4-ST	990 ± 230	0.139 ± 0.032	1070 ± 7.8	0.158 ± 0.018	1400 ± 410	0.235 ± 0.077
Pt-7-ST	700 ± 67	0.064 ± 0.003	420 ± 130	0.071 ± 0.027	530 ± 36	0.063 ± 0.003
Verification	820 ± 81	0.096 ± 0.075	170 ± 17	0.041 ± 0.017	700 ± 250	0.045 ± 0.015
MLC-3L	430 ± 40	0.099 ± 0.026	51 ± 1.9	0.014 ± 0.013	570 ± 63	0.093 ± 0.039

3. Summary

No conclusions are offered as to the nature of the observed changes in the dielectric properties due to the 300°C annealing due to the lack of supporting data for any such statements. The literature shows that internal stresses can have an impact the measured properties of thin films [5], and the relief of this stress by a low temperature anneal may account for a portion of the observed changes. This explanation does not, however, relate the differences from the different atmospheres used. As 300°C is well below the 500° to 600°C temperatures reportedly required to initiate crystallization [1], it is not likely that the observed changes are related to any significant crystallographic changes [2-4]. It is possible that the different atmospheres are affecting the film chemistries due to the differences in O_2 concentrations at the surface of the films, which could either oxidize (air anneal) or reduce (vacuum anneal) the $BaTiO_3$ from the as-deposited conditions. It is also possible that the electrodes are diffusing into the $BaTiO_3$ and causing doping effects. In order to determine the accuracy of any of these possibilities would require more extensive chemical and microstructural testing of these devices, as well as additional annealing temperatures and times.

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2. Pratt, I.H., *Characteristics of RF sputtered barium titanate thin films.* Proceedings of the IEEE, 1971. **59**(10): p. 1440-1447.
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5. Morito, K. and T. Suzuki, *Effect of internal residual stress on the dielectric properties and microstructure of sputter-deposited polycrystalline (Ba,Sr)TiO thin films.* Journal of Applied Physics, 2005. **97**: p. 104107-1 - 104107-5.

APPENDIX D

CONNECTION OF CUSTOM FARADAY CAGE TO TEST EQUIPMENT

1. Introduction

As the Faraday cage used for a portion of the electrical testing through papers 4 – 6 was custom made, there is no available manual for the connection to various electrical test equipment. As such, this appendix will detail the connection of the Faraday cage to the three pieces of equipment that were commonly used throughout the series of testing.

The Faraday cage has four electrical throughputs; two co-axial and two tri-axial connectors (Figure D.1). On the outside of the box these throughputs are standard bayonet connectors, and attach as normal to the appropriate co-axial or tri-axial cable. Inside the cage the co-axial throughputs are wired to individual, female banana terminals that allow for the insertion of either cables with male banana terminations or the clamping of smaller diameter pins. The tri-axial throughputs are connected to two of the same type of female banana terminals each to allow access to the two conducting (non-shielding) wires within the tri-axial cable. The rear side of these female banana terminals are exposed, and allow alligator clips to be attached to the co-axial and tri-axial connections.

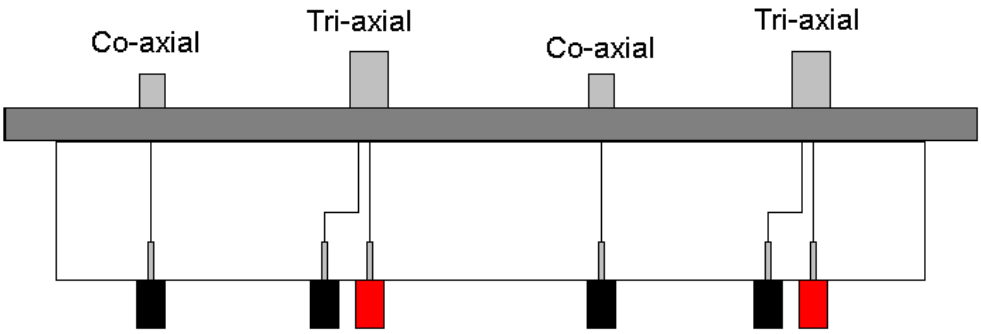

Figure 1. – Co-axial and tri-axial throughputs on the custom made Faraday cage.

2. Connection to HP 4140B

The HP 4140B required the use of one co-axial and one tri-axial connection (Figure D.2). A co-axial cable was connected to the V_a output of the HP 4140B and a chosen co-axial throughput on the Faraday cage. A tri-axial cable was then connected to the HP 4140B and one of the tri-axial throughputs of the cage. Inside the Faraday cage, the outer conductor of the tri-axial throughput (black banana terminal of tri-axial) was

connected directly to the co-axial throughput. One of the micro-probes was then connected to the inner conductor of the tri-axial throughput (red banana terminal of tri-axial) via the pin clamp feature of the banana terminal. The second micro-probe was then shorted directly to ground. For the purposes of consistency, the grounded probe was always connected to the bottom electrode (or the first deposited electrode layer of a MLC) for all testing.

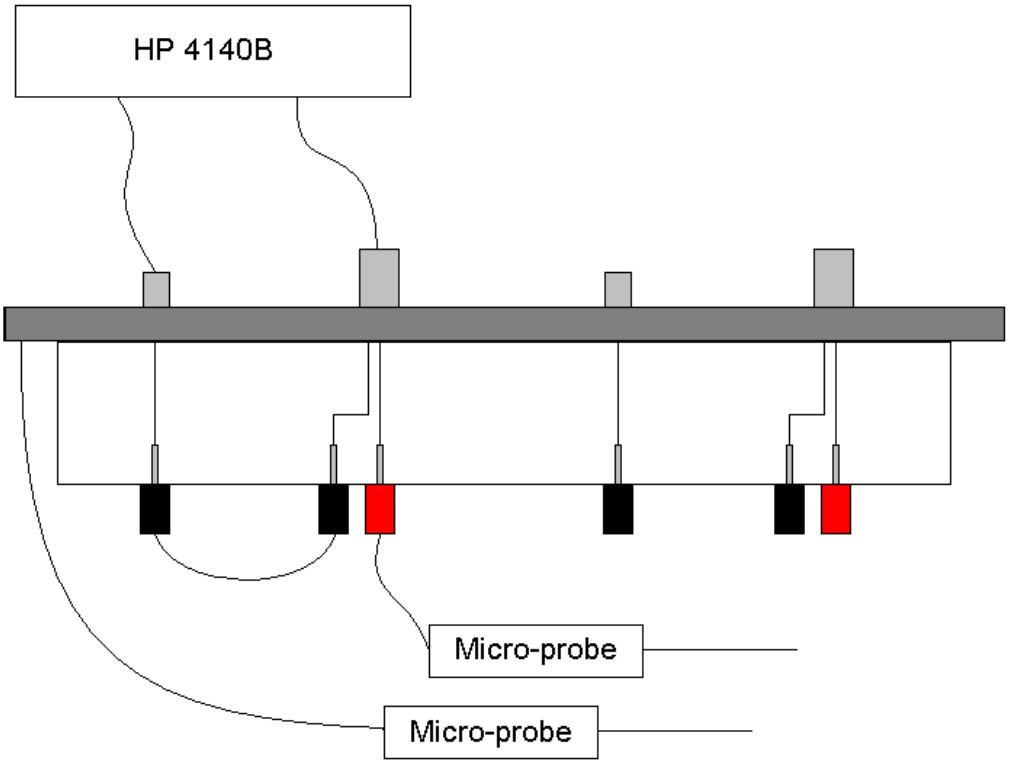

Figure 2. – Connection of Faraday cage to the HP 4140B.

3. Connection to RT6000HVS

Connection to the RT6000HVS for hysteresis measurement was more simplistic (Figure D.3). For low voltage measurements (< 19.9 V) the terminals of the RT6000HVS system were bayonet co-axial connectors, allowing for the use of two co-axial cables to connect the test system to the Faraday cage. The micro-probes were then connected to the co-axial throughputs with the pin clamps on the banana terminals. For high voltage testing (> 300 V) the co-axial cables were detached from the Faraday cage,

and the high voltage cables (supplied only with alligator clip terminations) were attached directly to the posts on the rear side of the banana terminals inside the Faraday cage. In this latter setup, care must be taken when closing the lid of the Faraday cage to ensure the high voltage cables are not crimped or pinched.

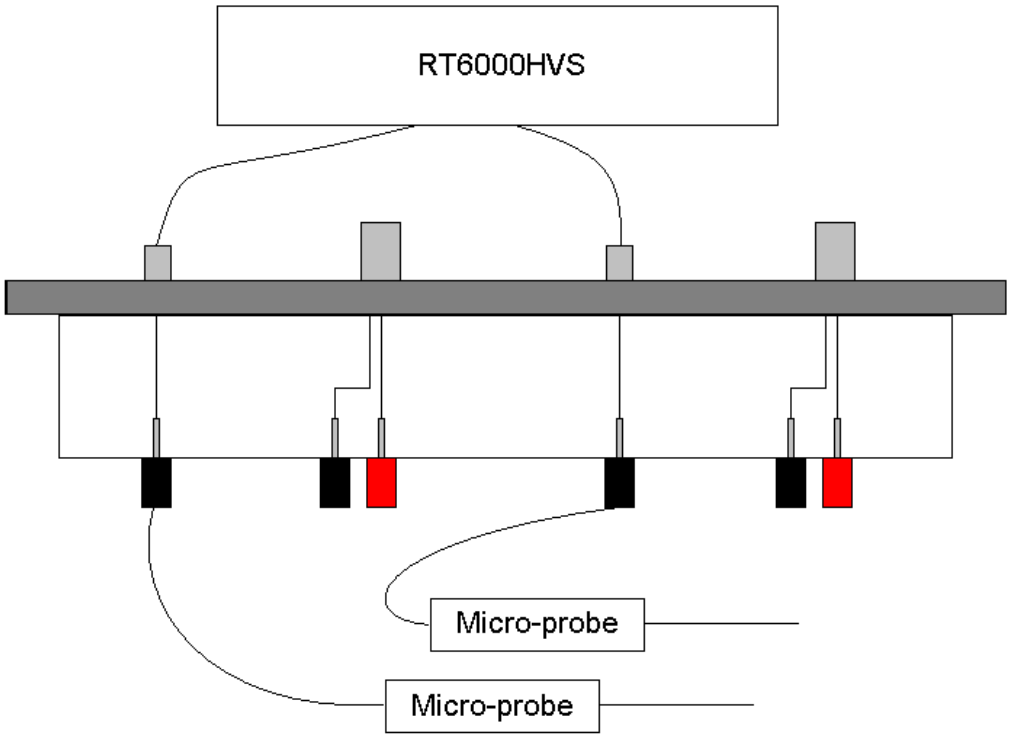

Figure 3. – Connection of Faraday cage to the RT6000HVS.

4. Connection to HP 4194

Connection to the HP 4194 for AC impedance analysis was achieved with two single core cables with alligator clips on both ends. One end of each cable was attached to the post on the rear side of the co-axial banana terminations inside the Faraday cage, and the ends were connected to the HP 4194 as shown in Figure D.4. Having the alligator clips span both of the terminals on the HP 4194 allows for the proper application of a DC bias if such a measurement in required to be made. As with the RT6000HVS, care must taken during closing of the Faraday cage to ensure the cables are not crimped or pinched.

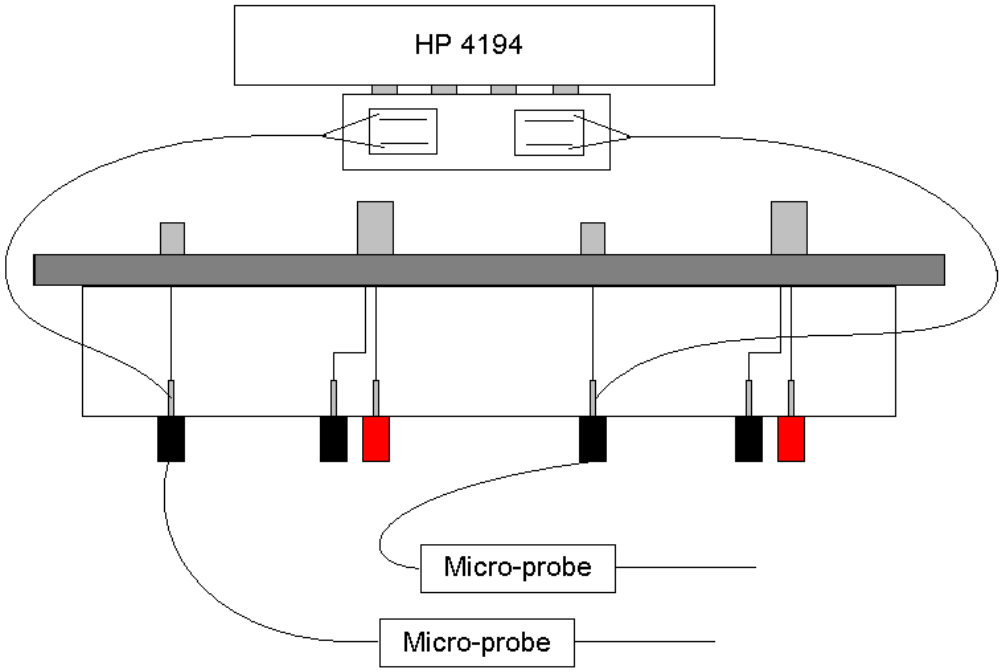

Figure 4. – Connection of Faraday cage to the HP 4194.

APPENDIX E

FUTURE WORK

1. Introduction

The work presented in papers 1 – 6 have left more questions than were answered. This appendix attempts to summarize some the potential future work that could be conducted to further the understanding of the deposition and optimization of $BaTiO_3$ thin films with thicknesses in the nano-meter range. The areas of research have been broken into the following two categories: sputtering optimization and interfacial effects.

2. Sputtering Optimization

As stated in papers 2 and 3, the Box-Benhken DOE was not effective in the precisely modeling the sputter deposition of $BaTiO_3$. A general series of trends were observed and related to the effects of competing forces within the deposition chamber, but accurate numeric models of the dielectric properties as a function of the process parameters has not been accomplished. In order to achieve this level of modeling a full factorial DOE is required. The proposed matrix would be a 3^3 full factorial requiring 127 specimens to be examined. The results of this DOE would have enough degrees of freedom to potentially fully characterize the deposition of $BaTiO_3$ as a function of the process parameters.

In addition to a more in depth DOE, other processing variables could also be examined. A set working pressure of 5 mtorr was used for all of the $BaTiO_3$ work presented in the above papers. The target to substrate distance was also kept at a constant distance of approximately 5 inches. Altering either of these two conditions would affect the energy and number of negatively charged oxygen ions that impacted the substrate during deposition. Along the same logic, a different regime for any of the three studied process variables could also be examined (i.e. 50% - 100% O_2 as opposed to the 10% - 50%).

Appendix C has shown the effects on the dielectric properties of these devices annealed at 300°C either in air or under vacuum for 1 hour. Further annealing studies would also help to identify the optimum conditions necessary for the development of viable thin film $BaTiO_3$. Such studies might include a continued investigation at 300°C with additional times at temperature (i.e. a range from 30 minutes to 24 hours) in the same atmospheres. Additional atmospheres would also be of interested, such as an O_2/N_2

atmosphere with a series of pO_2 values. Lastly, a study on the effects of increasing annealing temperature (i.e. ranging from 300°C to 700°C) would also be of interest to determine the temperature required to achieve optimum performance.

3. Interfacial Effects

A continued investigation of the interface between $BaTiO_3$ and both the Ni and Pt electrodes with high resolution TEM would be of great benefit to understand the differences between the two systems resulting in the observed property changes. Investigating these interfaces under a variety of conditions (i.e. as-deposited/untested, as-deposited/electrically tested, annealed/untested, and annealed/electrically tested) would potentially give insight into the variations of the thickness and composition of the interfacial layer. This work would also likely allow for more accurate dead-layer model approximations to be made, which would in turn allow more accurate prediction of dielectric behavior at $BaTiO_3$ thicknesses in the double and single digit nano-meter range.

As the effect of the interfacial layers are determined in large part by the chosen electrode material, additional materials other than Ni and Pt should be investigated. Au, Pd, Al, and Cu have all had a significant presence in the literature, and all are likely to impact the dielectric properties to various degrees. An understanding of the electrode material impact on device performance would allow for more informed choices to be made when attempting to achieve a desired set of dielectric properties. This work could also be combined with TEM work mentioned above to fully characterize the effects of the electrodes.

Another area of investigation that has seen limited exposure in the literature has been the effect of electrode geometry on the device properties. This research area would include the study of the size of the interaction area (i.e. $5x10^{-5}$ cm^2 versus $10x10^{-5}$ cm^2) as well as electrode shape (i.e. square versus round). Additionally, the use of electrodes patterned using photolithography to create complex patterns such as fractals or micron sized parallel bars would give another approach to device optimization.

4. Summary

The above description of potential research areas is not an all inclusive list, but just an initial starting point for future efforts. The interested individual could find many additional avenues of research based on the work presented in this dissertation. Below is a shortened listing of the mentioned areas of future work that could be investigated to carry on this work.

1. Full factorial DOE
2. Additional variables in addition to power, percent O_2, and deposition temperature
3. Different variable levels
4. Annealing studies
5. High resolution TEM of dielectric-electrode interfaces
6. Additional electrode materials
7. Various electrode geometries

VITA

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