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Printed circuit board power distribution network modeling, analysis and design, and, statistical crosstalk analysis for high speed digital links

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PRINTED CIRCUIT BOARD POWER DISTRIBUTION NETWORK MODELING, ANALYSIS AND DESIGN, AND, STATISTICAL CROSSTALK ANALYSIS FOR HIGH SPEED DIGITAL LINKS

by

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ABSTRACT

High-speed digital systems are moving to higher data rates and smaller supply voltages as the scale of integration goes smaller. With the smaller bit periods and the smaller operating voltages, the tolerable timing and noise margins are reducing. There are many sources of disturbances contributing to the tolerance margins. These margins have to account for inter symbol interference (ISI), reflections, jitter, noise from power distribution networks (PDN) and crosstalk. An important task during the design phase of the system is to find and mitigate the noise from such sources. This thesis proposes modeling and analysis methodology to resolve some of the problems while proposing relevant design methodologies to reduce the system design cycles.

PDN design forms a critical part of a high-speed digital design to provide a low-noise power supply to the integrated circuits (ICs) within some peak voltage ripple for normal functioning. Switching of transistors in the IC leads to a high-frequency current draw and generates the simultaneous switching noise (SSN), which propagates along the PDN from the chip to the PCB and causes several EMI and SI problems. A physics-based modeling approach for PCB PDN is proposed which is used for analysis and design guideline development. A design methodology is developed which guides the designer to make better design decisions, knowing the impact on PDN performance without the use of full-wave tools. Crosstalk forms a critical part of the budget, and if ignored, can lead to design failures. A statistical method to find the distribution of crosstalk at the victim using the single bit response principle is proposed. The methodology is extended to multiple-aggressor system, and, can be used to identify worst case crosstalk and find dominant crosstalk contributors in a system.

ACKNOWLEDGMENTS

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I also thank all my friends, who have taught, helped, supported me in achieving what I have now. I am really grateful to have had such great company.

I dedicate this Ph.D. to my parents, brother, and my entire family who stood by me in this journey, and supported all my decisions to get here. I would like to specially attribute my work to my late father Ravindra Shringarpure and late uncle Nandkumar Shringarpure, for their strong encouragement and support, without which I could not have succeeded.

Finally, I thank God Almighty, for making all of this possible.

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1. INTRODUCTION

The thesis proposes practical solutions to three connected problems found in general high speed digital system designs. It is identified that, in general, the link path performance is limited by not only the design of the link itself, but also other sources of noise present in the system. The other sources of noise could be other links in the vicinity of the said link, or other sub-systems which can couple noise to this link through radiation, conduction or direct coupling. In some cases, the noise can affect the power rails that drive the said link, and indirectly couple into the signal carried by the link. The power distribution network (PDN) noise and the crosstalk noise are chosen as the sources of interest for this thesis.

The introductions to each Section provide a brief review of the work done in each of these areas. The PDN modeling methodology for real boards, the analysis of the PDN model, its application to developing design guidelines, and to find a design methodology, are presented in Section 2, Section 3, Section 4, and Section 5 respectively. The PCB PDN design problem is thus addressed in a complete manner by modelling a practically board accurately, and proposing how to improve a design or have a best possible design within the available resources.

The Section 6 presents an over view of link to link cross talk problem. Based on layout and applications, the digital links may be required to be routed through via fields, traces, connector's breakout region, and connectors itself. The solution presented can accommodate any number of digital aggressors which will induce a crosstalk into the victim link to be designed. It allows identifying the dominant aggressors and the worst case source data, which can lead to link failure.

2. LUMPED ELEMENT MODEL FOR A REAL PCB

2.1. INTRODUCTION

Power distribution network (PDN) is a critical part of a high-speed digital design. The PDN on a printed circuit board (PCB) extends from the voltage regulator module (VRM) to the IC pins. The objective of the PDN design is to provide a low-noise power supply to the ICs within some peak voltage ripple. There is a significant similarity in the PDN for the package and chip for substrates that use substantial, solid area fills, which ultimately provide the power and power return currents to individual transistors. The switching of these individual transistors causes a transient current draw from the supply, and leads to a voltage disturbance on the PDN. When many such transistors switch simultaneously, there can be a large voltage ripple, which propagates along the PDN from the chip to the PCB [1]. The PDN is designed to limit the voltage ripple to meet the system requirements for normal IC functioning [2].

The voltage disturbance initiated from the transient switching propagates along the PDN, and can easily couple to other power or signal nets. In mixed-signal designs, the PDN noise generated at the digital devices, can reach the power network of a phase locked loop (PLL) and cause significant jitter in its output, which propagates through the system. PDN noise can also increase the phase noise on the RF oscillator. When present in the IO driver power network, the PDN noise will affect the rise/fall time of IO signals, contributing to the jitter in the signal [3]. In highly integrated systems, voltage disturbances can also directly couple to the signal nets due to electromagnetic coupling at vias as signals transition through layers, affecting the jitter and eye height of high-speed digital signals [4]. The clock frequencies and data rates of ICs continue to increase, while at the same time the logic levels decrease [5]. This reduces both the timing margins and the noise margins for the signals.

Radiation can occur from a PDN geometry at the edges of the power – power return area fills at the resonant dimensions, on the package or the PCB. Also noise on the PDN can couple to other structures such as, traces, vias, or other overlapping area fills and then couple off the PCB. Noise can couple onto vias of pins of I/O connectors, and

be conducted outside the shielded enclosure and produce emissions. If not suppressed, the supply noise can radiate directly, or though some coupled structures [6-9].

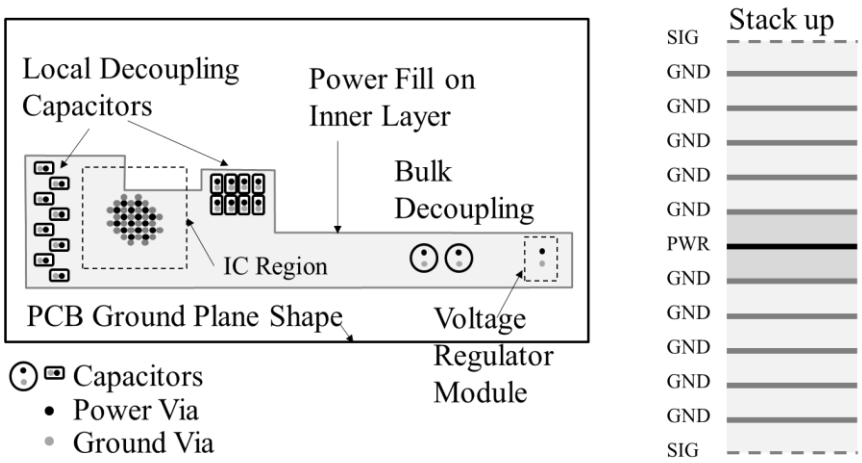


Figure 2.1. PCB with a typical PDN. The IC is connected to an area fill on the inner layer, to which several decoupling capacitors and the VRM are also connected.

High layer count PCBs, have many power, power-return, and signal-return planes and/or area fills, which form several resonant cavities, as shown in Figure 2.1. The PDN is comprised of complex shaped area fills for the power net and the power return net. The IC pins and the decoupling capacitors, placed on the top or the bottom of the PCB, are connected to the power fill using plated through holes or vias. For such real PCBs, the PDN impedance has been conventionally used as an approach to analyze the PDN design [10], because this impedance can be used to calculate the noise voltage developed due to a noise current[11]. Also, the transfer impedance between two ports on the PDN is a measure of the noise voltage at a victim IC resulting from a current draw at a different IC.

For PDNs that employ area fills for power nets in the PCB, there are several methods to calculate the PDN impedance. Numerical solutions like the finite difference time domain (FDTD) method [12], [13] and the finite element method (FEM) [14] have been used. Boundary integral formulations have also been used [15]. Other numerical formulations including the transmission line matrix (TLM) method [16], and partial

element equivalent circuit (PEEC) [17] method, and, circuit extraction from mixed potential integral equations method (CEMPIE) [18], are approaches from which a SPICE compatible equivalent circuit model for the PDN geometry can be extracted. A transmission line matrix method has also been used that is compatible with the simulation tools that include transmission line modeling [19]. The technique in [20] extracts a circuit model from the physics based resonant cavity formulation with a lumped circuit representation for each mode. But due to the complexity of the geometry, for the simulations to converge with good accuracy, this model has to account for a large number of modes and hence uses a large number of circuit elements.

These modeling techniques provide solutions for discovery and post-layout analysis from the lower frequency where the power planes are electrically small to the higher frequency where the distributed resonances occur. But for the real geometry, these techniques lead to time and memory intensive simulations, or complex circuit models which do not provide clear insight for design. Moreover, to use these techniques for a real high layer count PCB is not straight forward, merely due to the complexity of the geometry.

In this paper, the multi-layered stack up is divided into plate-pair cavities to be solved individually. Within each plate-pair cavity, using inductance extraction [21], based on a cavity model formulation [22], the inductance of the vias and planes can be extracted and represented as circuit elements. As these cavities only couple through the vias they are stitched together at via nodes in a network fashion [23]. A lumped element model can be created with the extracted via/plane inductance and the capacitance of parallel plates. But, for a real or product PCB geometry, such a model, with an inductor to represent every via in every cavity, will result in a circuit with a large number of elements. Additionally, the inductors, representing the vias within a cavity will have mutual inductances with each other. This results in the difficulty of a large element count in the equivalent model for the PDN. A previously reported circuit reduction approach combined the parallel inductor elements by grouping them according to the direction of current on the vias [23]. This assumption that the direction of currents on the return vias is known limits the application of this methodology from being used for a real board design, which has many return vias not clearly associated with just the IC or decaps.

To overcome this limitation, a new way to treat the reduction is proposed herein, where all the return vias are treated as elements connected in parallel between two return planes, without assuming any current direction on them. Then an equivalent inductor for all the return vias can be obtained, representing an effective return current within a parallel-plate pair. The dielectric loss in the parallel plate cavity is added to the model with a conductance in parallel with the plate-pair capacitance. Many practical assumptions for modeling a real PCB geometry are discussed and implemented. It provides the detailed handling of circuit elements, and issues with the real world PCB geometries. This model, which can be easily used in with a SPICE solver, still preserves the physical representation and hence allows the designer to identify the contributions from individual geometry features. It thus provides the PDN designer with an increased intuition and understanding of the physics in PDN design.

The contribution of this paper is to provide a practical methodology to model a real multi-layered PCB with many decoupling capacitors and return vias, using a circuit model with comparatively small number of circuit elements. The methodology proposed herein, aims at modeling the low frequency behavior of the PDN accurately, while not capturing the distributed behavior manifested in the modal resonances of the planes. Included comparison of model results and measurements show the low frequency behavior and the inductive trends at high frequencies are captured well, but the cavity modes are not.

In this thesis, Section 2.2 reviews the inductance extraction from the cavity model and shows a novel reduction technique to get an equivalent circuit model for a real PCB. The methodology is used to extract a model for a real PCB and the response is compared with measurements and full wave simulations in Section 2.3.

2.2. METHODOLOGY

The PDN geometry has a cavity structure formed by the area fills of the power net and the power return (also denoted the ground) net. The cavity model is used to get an analytical expression for the self and transfer impedance between the vias in the cavity [22], [24], [25]. The impedance for a rectangular cavity can be written as a sum of the parallel plate capacitance and an equivalent frequency dependent via-plane inductance as,

$$Z_{ij} = \frac{j\omega\mu d}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{N_{mni}N_{mnj}}{k_{mn}^2 - k^2} = \frac{1}{j\omega C_p + G_p} + j\omega L_{ij}(\omega)\ ; \tag{2.1}$$

$$C_p = \varepsilon\frac{ab}{d}; L_{ij} = \frac{\mu d}{ab}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{N_{mni}N_{mnj}}{k_{mn}^2 - k^2}\Bigg|_{(m,n)\neq(0,0)}\ . \tag{2.2}$$

where,

$$k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2, \qquad k^2 = \omega^2\mu\varepsilon,$$

$$N_{mni} = c_m c_n \cos\left(\frac{m\pi x_i}{a}\right)\cos\left(\frac{m\pi y_i}{b}\right)\mathrm{sinc}\left(\frac{m\pi W_{xi}}{2a}\right)\mathrm{sinc}\left(\frac{m\pi W_{yi}}{2b}\right), \quad \text{and}$$

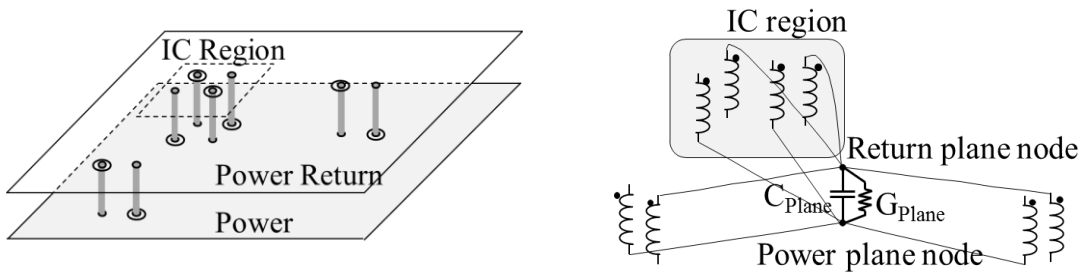
$$c_l = \begin{cases} 1 & , l = 0 \\ \sqrt{2} & , l \neq 0 \end{cases}.$$

Here, m and n are the modal indices the x and y direction, respectively. The cavity dimensions are a, b and d in x, y, and z directions, respectively. The port locations are centered at the co-ordinates (xi, yi) and the port dimensions are Wxi and Wyi for the ith port, and similarly for the jth port. The permittivity in the cavity is ε and the permeability is μ. Perfect magnetic conductor (PMC) boundary conditions are used for (2.1) in which there are no fringing electric fields.

The (m, n) = (0, 0) mode in (2.1) represents the capacitance of the cavity and rest of the modes contribute to the inductance of the vias and planes [21]. The frequency dependent Lij is relatively constant up to 60% of the first cavity-resonance frequency [26]. The low frequency value is then the same as the dc value from (2.2). A lumped circuit model is created using the low inductance value and capacitance of the cavity. Here, each inductor represents the self and mutual inductance associated with the current in a via and the plane region around it. Above the first cavity-resonance frequency, some modes will not be evanescent, and their contribution may introduce an error [26].

A parallel-plate cavity as shown in Figure 2.2 (a) can be modeled with the circuit shown in Figure 2.2 (b) within the bounds previously discussed. The geometry has several power and return vias. Some power vias may be connected to the IC and other power vias may be connected to the decoupling capacitors. The model uses an inductor element for each via with a mutual inductance between every pair, and, a capacitor (C_{Planes}) and conductance (G_{Planes}) for the parallel plate capacitance with lossy dielectric.

The observation port uses the nodes of inductors representing the IC power via as a positive terminal of the port and the reference is the top plane node for the top layer. The decoupling capacitor models can be connected to the inductors representing the respective power vias.



(a) (b)

Figure 2.2. (a) A Rectangular power cavity with a power plane and return plane, where some power and return vias connected to the respective planes. (b) The lumped circuit model for the geometry in 2(a), with the parallel plate capacitance and inductors for each via and the mutual inductances.

This model is based on a rectangular cavity shape which will affect the calculation of inductance if the position of the via is close to the edge [27]. Fig. 3(a) shows the geometry of a rectangular plane pair with one via connected to the bottom layer and a shorting via placed at a certain distance. The two geometries are used to illustrate the distribution of current on the planes, for different distances of shorting via. When this distribution is affected by the shape of the plane (when via is close to the edge), the inductance calculation is shape dependent, but otherwise, it will not depend on the shape of the plane as long as vias are away from the plane edge. This conclusion is also supported by the results and physics articulated in [27].

Thus in the PDN designs with power and return vias placed at larger distances, compared to distance from the edge, the shape matters. When there are enough return vias placed close to the power vias compared to the edge distance, there is less dependence on the plane shape, for the inductance calculations. An application of this concept when modeling the multi-layer geometry is that if the power and return current

path is observed, then only the part of current path where the return current vias are away is when cavity is formed by the power layer and return layer. All plane-pairs formed by the return layers would have high current distributions around vias and between the vias carrying opposite direction currents.

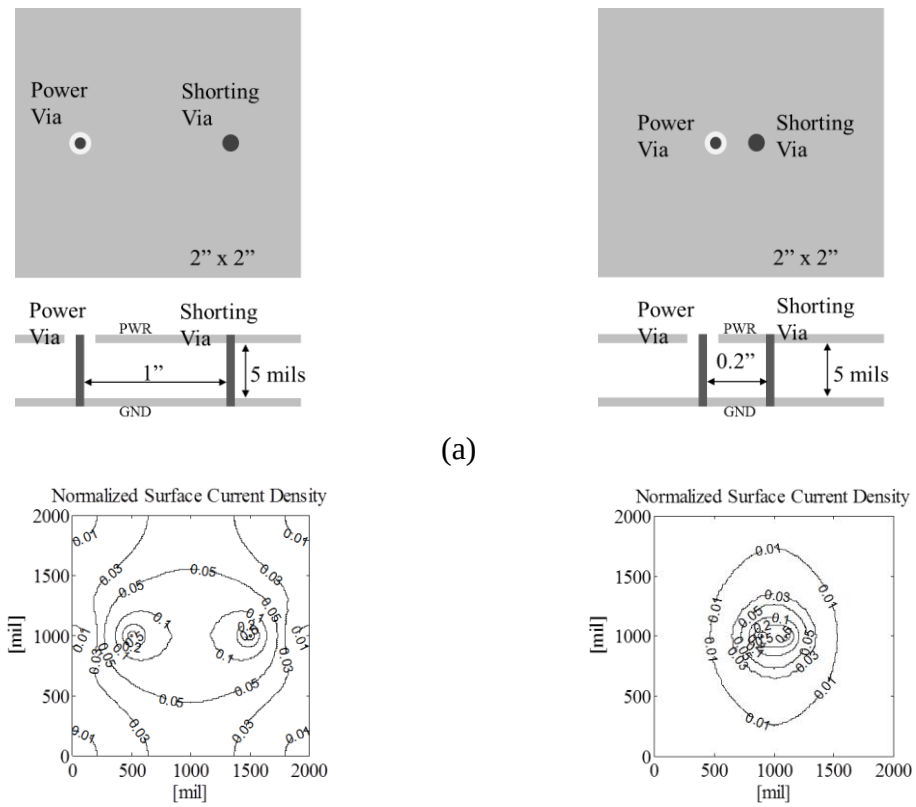


Figure 2.3. (a)A cavity with a power via and a shorting via placed 1" and 0.2" apart (b)Current density on the planes for the geometry shown in (a).

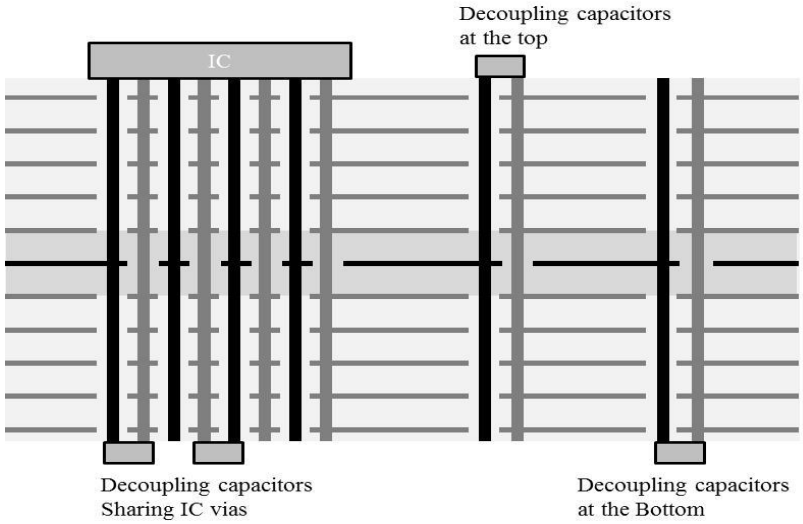
Many non-ideal geometry features in a real PCB make its modeling more challenging. In a real PCB, the IC may have many power nets, each with an arbitrary shaped power net fill at some layer connected by many power vias. The power and return net fills are then connected with vias to many decoupling capacitors placed on either side of the board. Depending on the design requirements, the number of decoupling capacitors used could vary from a few to several hundred. Every capacitor has dedicated vias which

connect it to the power and return nets. Figure 2.4(a) shows one such PCB with an IC on the top layer connected to a power net fill on an inner layer through many vias. Decoupling capacitors on top and bottom of PCB connect to the power fill through vias. Some decoupling capacitors are also present on the bottom of the IC, which share the IC power vias to connect to the power area fill. The power cavity, formed with neighboring return planes is high-lighted. There are many return vias on the PCB for providing a good return path to the power current.

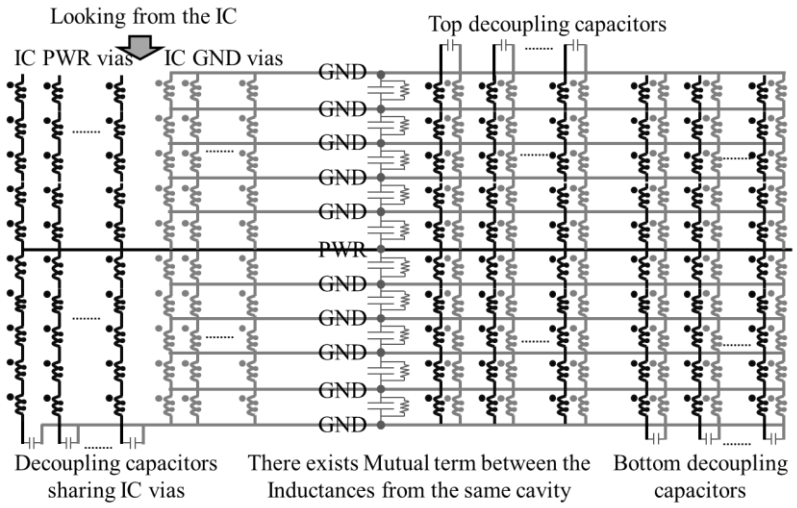
The model for such a multilayered PCB could be extrapolated from the single cavity modeling approach. The multi-layer geometry is divided vertically at the plane layers into plate-pair cavities and each cavity is then modeled individually. Planes assigned to other power nets (or floating nets) can be ignored since they do not affect the input impedance of the model for the power net being studied. The inductance extraction in [21] is used to extract the L matrix which has the self-inductance and the mutual inductance corresponding to each via location in the cavity. The inductance extraction assumes a rectangular cavity. The shape and size of the cavity remains the same as board size, except for the cavities formed by the power layer with return layer above and below it, as highlighted in the stack up in Figure 2.4 (a). The board size is used for inductance calculation for larger cavities, and a smaller equivalent rectangle is used for the power cavity. The inductance values are linearly proportional to cavity height, so the inductance calculation is run once for the small power cavity and once for the board size cavity and then scaled for all other cavities with different heights. When the lumped circuit models for all the cavities are stacked together and connected at the corresponding via nodes, a large circuit of inductors is created with an inductor for each via in each cavity, as shown in Figure 2.4 (b).

Here the capacitance of each cavity is calculated assuming parallel plates and negligible fringe. The cavity capacitor is connected in the model between the nodes representing each plane layer. The vias which are connected to these plane layers also have corresponding inductor terminals shorted to the plane layer node. The model accounts for the dielectric loss using conductance placed in parallel with the capacitor. The model represents the geometry from topmost plane layer to bottommost plane layer, the region where the cavity model can be used to calculate the inductance. The

decoupling capacitors are connected to terminals of the inductors representing the corresponding power vias. The model for the decoupling capacitors should include the parasitic effect of the interconnect structure above the top plane or below the bottom plane, as required. Thus, the model for the PCB PDN, along with decoupling capacitors is complete.



(a)



(b)

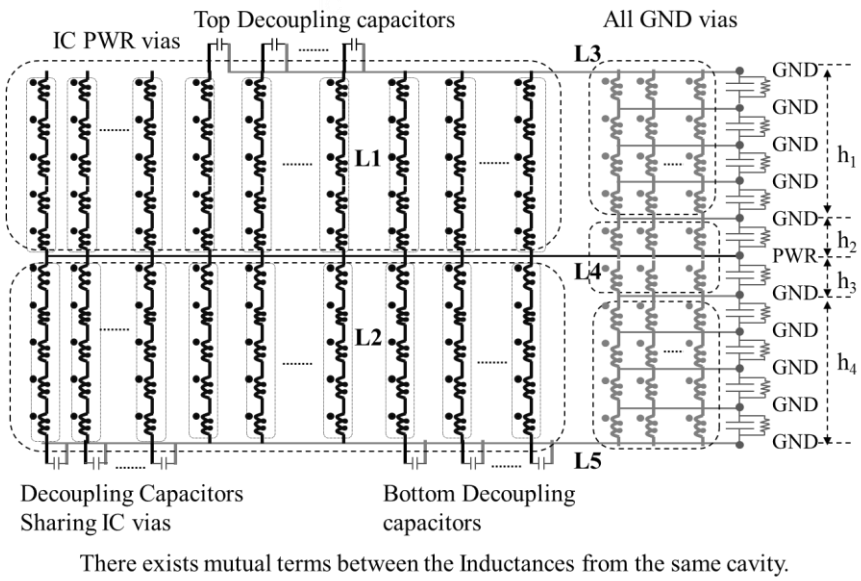
Figure 2.4. (a) The geometry of a high layer count PCB, with IC connected to the power layer near the center of the stack up, and through it to the capacitors placed on bottom and top layers; (b) The circuit model for the geometry in Figure 2.4 (a) with no simplification.

However, in a real PCB, with high layer count, hundreds of return vias, and many decoupling capacitors and IC power pins, the number of elements in the shown model will be very high, requiring a lot of computational resources. To resolve this, an improved model reduction technique over [20] is developed, which can easily handle real or practical structures. Once in the circuit domain, the inductors for all the return vias and the power vias are grouped as shown in Fig. 5(a). The return net is shown in black and the power net in grey. The grouping of inductors is based on their connections and nets represented. There are five groups, of which two groups are formed with power net elements, L1 and L2, and three groups with return net elements, L3, L4 and L5. The power net inductors from top layer to the power layer (layer with power fill) are grouped as L1. The inductors from the power layer to the bottom layer are grouped as L2. To group the return net elements, the closest return net layers above and below the power layer are identified, and the groups are divided at these layers. From the top layer to the closest return layer above the power layer, all return net inductors are grouped as L3. Between the closest return layers above and below the power layer, the return net elements from the group L4. From the closest return layer below the power layer to the bottom, the return net elements are grouped as L5.

For the groups L3 and L5, the inductors representing return net vias are shorted at each return plane node, in parallel with the ‘C’s and ‘G’s for each cavity. These inductors represent the conduction current path along the planes and vias, and the ‘C’s and ‘G’s represent the alternate displacement current path for the return current. In the frequency range of interest, the return vias offer lower impedance compared to the plane-to-plane capacitors, and removing these capacitors and resistors between return planes does not affect the model response. Physically, this means that at the critical frequencies for PDN on PCB, the return path is dominated by the conduction current through return vias. A single C and G pair is connected from top return plane to closest return plane above the power layer, also from the closest return plane below power layer to bottommost return layer. These are series combinations of all the components representing the displacement currents between return planes.

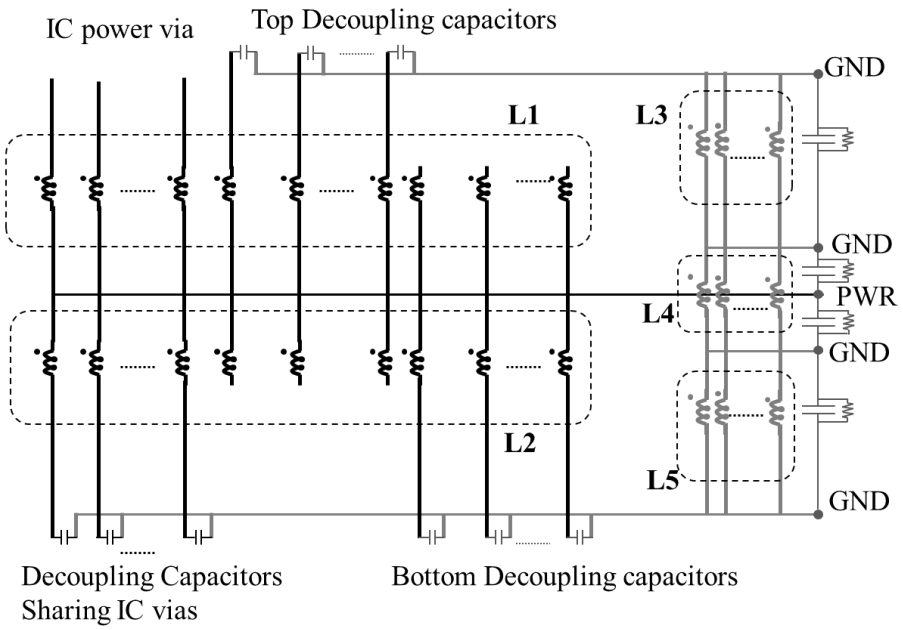
There are two steps in the circuit reduction. The series elements are combined first, as in Figure 2.5(b). The reduction accounts for the mutual inductance terms, as

shown in this paper. The series inductances in group L1 and L2 can be combined. For L3, L4 and L5 groups also the inductors can be added like series elements, as the inductor values from cavity to cavity are just scaled by the same factor. In this step, the mutual terms which exist between the elements in different groups are also added, as the series combination preserves the current on the element and the equivalent new element has the same voltage across it as the sum of voltages all the elements that were combined. The circuit is then reduced to Figure 2.5(b), and if there are many cavities in the original circuit, then this step will show a large reduction in the number of elements in the circuit.

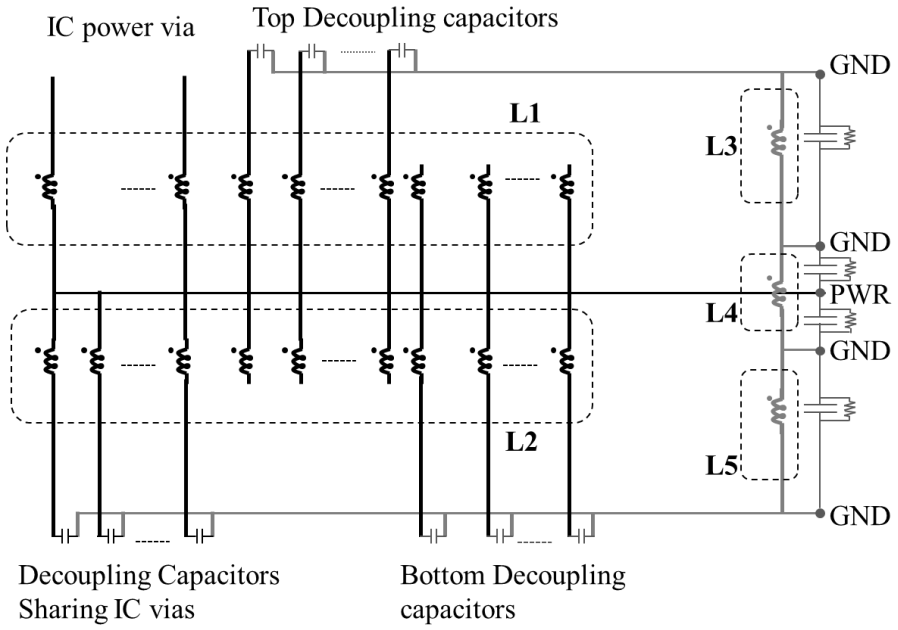


(a)

Figure 2.5. (a) Lumped circuit for multiplayer PCB PDN. (b) Step1 Circuit reduction by combining series elements from (a). (c) Step2 Circuit reduction by combining parallel elements corresponding to the return vias from (b).



(b)



(c)

Figure 2.5. Lumped circuit for multiplayer PCB PDN. (b) Step1 Circuit reduction by combining series elements from (a). (c) Step2 Circuit reduction by combining parallel elements corresponding to the return vias from (b). (Cont.).

The next step combines the parallel elements in every group. All the return via representing groups, L3, L4, and, L5, have their elements in parallel, thus reducing to a single element each. The L1 and L2 represent the power net vias. However, when the PDN impedance is observed from the IC with multiple power pins, to define a port between the power and return nets, all the power via nodes at the IC can be combined together. Then, all the elements in L1 representing the IC power vias also occur in a parallel connection between the power plane node and the Top layer where the IC port is defined. These elements can also be reduced to a single element.

Considering m return vias and n power vias, the reduction of the m return vias is illustrated. The current-voltage relation for the inductor can be can be used to write a matrix equation as,

$$j\omega \begin{bmatrix} \overline{\overline{L_{11}}} & 0 & \overline{\overline{L_{13}}} & \overline{\overline{L_{14}}} & 0 \\ 0 & \overline{\overline{L_{22}}} & 0 & \overline{\overline{L_{24}}} & \overline{\overline{L_{25}}} \\ \overline{\overline{L_{31}}} & 0 & \overline{\overline{L_{33}}} & 0 & 0 \\ \overline{\overline{L_{41}}} & \overline{\overline{L_{42}}} & 0 & \overline{\overline{L_{44}}} & 0 \\ 0 & \overline{\overline{L_{52}}} & 0 & 0 & \overline{\overline{L_{55}}} \end{bmatrix} \begin{bmatrix} \overline{I_1} \\ \overline{I_2} \\ \overline{I_3} \\ \overline{I_4} \\ \overline{I_5} \end{bmatrix} = \begin{bmatrix} \overline{V_1} \\ \overline{V_2} \\ \overline{V_3} \\ \overline{V_4} \\ \overline{V_5} \end{bmatrix}. \tag{2.3}$$

where, the inductance matrices (i, and j take values from 1 to 5), represent the self-inductance and the mutual inductance matrices for the elements in the L1 to L5 groups. The vectors and vectors represent the currents through and voltages across each element in the corresponding groups. The voltages across the parallel elements are assumed to be the same so the voltage vector has the corresponding terms repeated as,

$$\overline{V_3} = \begin{bmatrix} V_3 & \dots & V_3 \end{bmatrix}^{\mathrm{T}}, \ \overline{V_4} = \begin{bmatrix} V_4 & \dots & V_4 \end{bmatrix}^{\mathrm{T}} \text{ and, } \overline{V_5} = \begin{bmatrix} V_5 & \dots & V_5 \end{bmatrix}^{\mathrm{T}}. \tag{2.4}$$

The current through the equivalent single element is the sum of all the individual currents. As the L3, L4 and L5 groups are reduced to a single element,

$$\sum \overline{I_3} = I_3, \ \sum \overline{I_4} = I_4 \text{ and, } \sum \overline{I_5} = I_5. \tag{2.5}$$

In order to reduce the parallel circuit elements, the inverse of the inductance matrix is taken, denoted as , and the rows and columns in $\overline{\overline{B}}$ corresponding to the m return vias in L3, L4 and L5 groups are added as shown in (2.6) below.

$$\begin{bmatrix} \overline{\overline{B}}_{nxn} & 0 & S_{i,2n+1}^{i,2n+m}\left(B_{ij}\right) & S_{i,2n+m+1}^{i,2n+2m}\left(B_{ij}\right) & S_{i,2n+2m+1}^{i,2n+3m}\left(B_{ij}\right) \\ 0 & \overline{\overline{B}}_{nxn} & S_{i,2n+1}^{i,2n+m}\left(B_{ij}\right) & S_{i,2n+m+1}^{i,2n+2m}\left(B_{ij}\right) & S_{i,2n+2m+1}^{i,2n+3m}\left(B_{ij}\right) \\ S_{2n+1,j}^{2n+m,j}\left(B_{ij}\right) & S_{2n+1,j}^{2n+m,j}\left(B_{ij}\right) & S_{2n+1,2n+1}^{2n+m,2n+m}\left(B_{ij}\right) & S_{2n+1,2n+m+1}^{2n+m,2n+2m}\left(B_{ij}\right) & S_{2n+1,2n+2m+1}^{2n+m,2n+3m}\left(B_{ij}\right) \\ S_{2n+m+1,j}^{2n+2m,j}\left(B_{ij}\right) & S_{2n+m+1,j}^{2n+2m,j}\left(B_{ij}\right) & S_{2n+m+1,2n+1}^{2n+2m,2n+m}\left(B_{ij}\right) & S_{2n+m+1,2n+m+1}^{2n+2m,2n+2m}\left(B_{ij}\right) & S_{2n+m+1,2n+2m+1}^{2n+2m,2n+3m}\left(B_{ij}\right) \\ S_{2n+2m+1,j}^{2n+3m,j}\left(B_{ij}\right) & S_{2n+2m+1,j}^{2n+3m,j}\left(B_{ij}\right) & S_{2n+2m+1,2n+1}^{2n+3m,2n+m}\left(B_{ij}\right) & S_{2n+2m+1,2n+m+1}^{2n+3m,2n+2m}\left(B_{ij}\right) & S_{2n+2m+1,2n+2m+1}^{2n+3m,2n+3m}\left(B_{ij}\right) \end{bmatrix}_{\substack{(2n+3)\\ \times(2n+3)}} \begin{bmatrix} \overline{V}_1 \\ \overline{V}_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} = j\omega \begin{bmatrix} \overline{I}_1 \\ \overline{I}_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix}, \quad (2.6)$$

where, $S_{i1,j1}^{i2,j2}\left(B_{ij}\right) = \sum_{i=i1}^{i2}\sum_{j=j1}^{j2} B_{ij}$; $S_{i1,j}^{i2,j}\left(B_{ij}\right) = \sum_{i=i1}^{i2} B_{ij}$; $S_{i,j1}^{i,j2}\left(B_{ij}\right) = \sum_{j=j1}^{j2} B_{ij}$.

Taking an inverse of resulting $\overline{\overline{B}}$ matrix from (2.6), gives

$$\begin{bmatrix} \overline{V}_1 \\ \overline{V}_2 \\ V_3 \\ V_4 \\ V_5 \end{bmatrix} = j\omega \begin{bmatrix} \overline{\overline{L}}_{11} & 0 & \overline{\overline{L}}_{13} & \overline{\overline{L}}_{14} & 0 \\ 0 & \overline{\overline{L}}_{22} & 0 & \overline{\overline{L}}_{24} & \overline{\overline{L}}_{25} \\ \overline{\overline{L}}_{31} & 0 & L_{33} & 0 & 0 \\ \overline{\overline{L}}_{41} & \overline{\overline{L}}_{42} & 0 & L_{44} & 0 \\ 0 & \overline{\overline{L}}_{52} & 0 & 0 & L_{55} \end{bmatrix} \begin{bmatrix} \overline{I}_1 \\ \overline{I}_2 \\ I_3 \\ I_4 \\ I_5 \end{bmatrix} \quad (2.7)$$

Some inductor groups which did not have a mutual inductance term before reduction may get some mutual inductance terms due to the reduction after two matrix inversion processes. This is still physical as this was an indirect coupling, which after reduction showed up as a direct coupling. As the number of return vias in real PCBs is very large, a major portion of the circuit is reduced with this step. This reduction technique can reduce the size of matrix from 2*n+3*m to 2*n+3, where, m is the number of return vias and n is the number of power vias.

Also, if the observation port has many power vias, included in the L1 group, then these could also be further reduced simplifying the circuit, in the similar method. The Figure 2.5(c) showed such combination of IC power vias and also the reduction of return vias. If the analysis requires more ports to be defined, the one-to-one relation between the

geometry features and circuit elements allows defining more ports at required locations in the model.

Thus, the response of the final reduced physics based circuit model shown in Figure 2.5(c), can be run with a SPICE engine to find the input impedance of the PDN over frequency. As the model is physics based, there is a relation between the geometry to the circuit model elements to the response, based on the current path physics in each frequency range.

2.3. VALIDATION WITH MEASUREMENTS

To validate the modeling methodology proposed in this paper, a real production level PCB was modeled. A comparison of the modeling results and the measurements is shown in this section. The modeled board has many ASICs, and each has a number of power nets.

The PCB has a 28 layer stack up is used, shown in Figure 2.6. The power net of interest is routed on the 16th layer, where it has an area fill. There are many plane layers for signal and power return (ground). Also, other power nets fills are present on different layers in the stack up. There are other power nets routed on layers 13 through 15. The power return is on layer 12 and 17. The top and the bottom layers of the board are return planes.

In this board, shown in Figure 2.7, there are 43 surface mount capacitors connected to the concerned net, of which 17 capacitors are under the ASIC, 7 are on the bottom but away from the ASIC, and 19 on top layer around the ASIC. There are 243 return vias in the vicinity of the power net and the caps, all included in the modeling. The input impedance is measured between a pair power and return pads at the top plane where the ASIC is supposed to connect. The measurements were taken in 3 steps: Step1 with one capacitor connected at the bottom, Step2 with 19 top capacitors connected at the top layer and, Step3 with all 43 capacitors connected at both top and bottom, as shown in Figure 2.8.

The model is built in the same manner as described in Section 2.2. The final models for each verification step are shown in Figure 2.9. The inductance matrix is first calculated for all via locations, 43 power vias and 243 return vias, in one cavity. As

mentioned before, rectangular approximate shape is used for the power cavity inductance calculation, and the complete size of the board is used for inductance calculation of all other cavities. The effect of the irregular power plane shape or the effect of power plane edge vicinity on the via inductance is accounted for by using an approximate rectangle. This matrix is scaled using cavity heights to find the self and mutual inductance in each group described in Figure 2.5. The parallel element reduction technique is used to reduce the number of return via representing inductors.

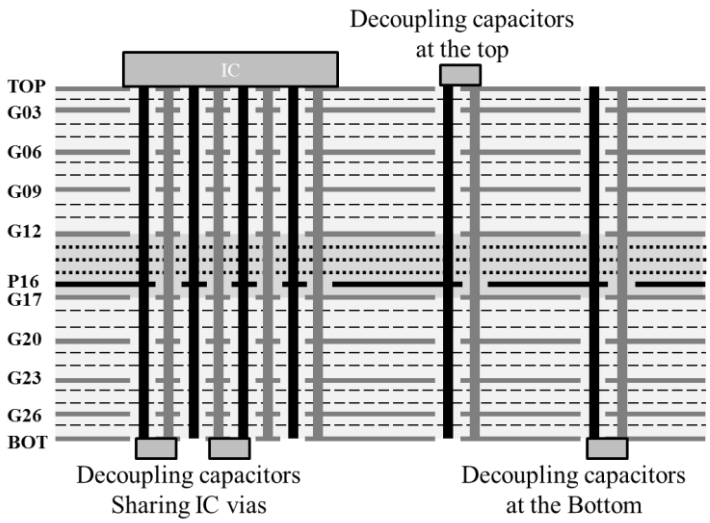


Figure 2.6. Case 1 geometry used for the sensitivity analysis with one decoupling capacitor placed on top of the board, and Case 2 geometry with one decoupling capacitor used at the top and the bottom each of the board.

In the model, the power plane area is used to find the parallel plate capacitance with its neighboring return planes. The area fills belonging to other power nets (not being studied) act as floating nodes between two return nodes or between a return node and a power net node under study. Effectively, it acts as a connecting node between two plane–pair capacitors in series, and can removed by replacing two series capacitors with an effective capacitance. This provides another useful reduction in modeling the real boards: when studying one power net, all other power nets can be considered as floating. This particular simplification restricts the use of this model for studying inter-power-net

coupling. For the present application of studying the input impedance of one power net, this works sufficiently well.

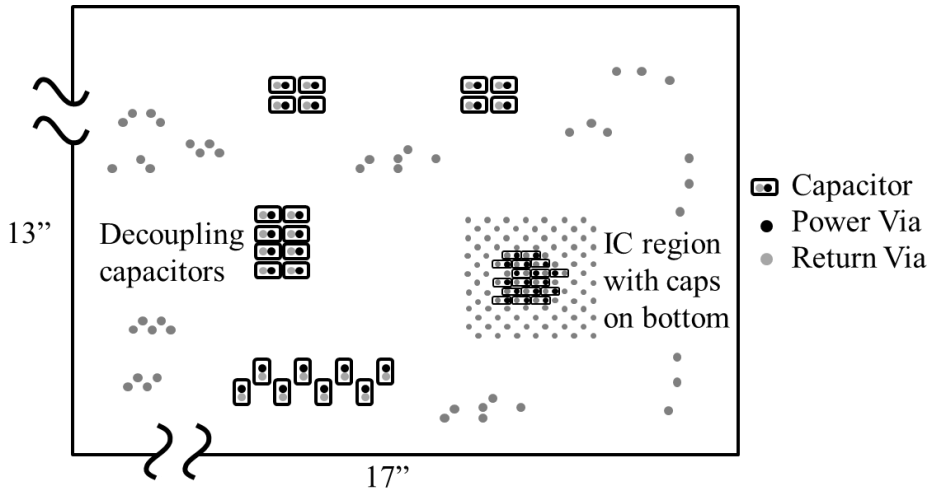


Figure 2.7. (a) PCB with a 28 layer stack up and the power net is routed through the 16th layer, (b) An area fill of an irregular shape, is used to connect to 43 decoupling capacitors as shown in the Top view.

The model described is for the complete set of IC vias, power and return planes, the vias connecting the decoupling capacitors, and all the return vias in this region. The models for the three steps only differ in connection of decoupling capacitors to the PCB. The Step1 model will have one capacitor model connecting between the respective power via node and the bottom layer node. The Step2 model will have 19 capacitors models connected between the respective power via inductor nodes and the top layer node. The Step3 has all 43 capacitors connected between the power via inductor nodes and the bottom or top layer nodes, depending on their location. The Figure 2.9 is used to describe the model, but does not show all the capacitors for the Step2 and Step3, to reduce the complexity of the circuit model. Also, the mutual inductance between the inductors is accounted for as explained in Section 2.2 and not explicitly shown in the models. Each case is simulated by connecting a vendor provided SPICE model of the capacitor with parasitics, across the power via inductance node and top/bottom return layer nodes.

The model response comparison with measurements is shown in Figure 2.10. The measurements are made across one particular IC power net via and its neighboring return net pad using calibrated wafer probes. For a meaningful comparison, the IC port in the model is defined across the same via node at the Top layer with the return net node at the Top layer. The measurements have high noise floor problems due to the dynamic range of the measuring instrument and the setup. The low frequency measurements were not available for the Step1, so the measurement data starts at 80 MHz for this case.

The response of a typical PCB PDN is observed to be a combination of inductive and capacitive regions separated by poles and zeros. Each feature in the response depends on a specific set of circuit model elements, which represent corresponding geometry features. As physics from the current path in each frequency region defines this dependency, it can be used to evaluate the model performance.

Low frequency capacitance is the total decoupling capacitance, is fairly captured in Step2 and Step3, which depends on the tolerance of the capacitor values. The mid frequency inductance depends on the current path from the IC to decaps and back, modeled by the self and mutual inductances between the different vias and planes, along with the capacitor SPICE models. The mid frequency inductance changes from Step1 to Step3 as more capacitors are progressively added to the PDN, and captured well by the model. The high frequency inductance representing the current path between the IC and power cavity, and is not affected significantly by the number or location of the capacitors. This is captured in all cases, and remains almost constant from Step1 to Step3 since the current path remains the same. The lumped resonance (pole) frequencies are captured well but the magnitudes are off, because the model accounts for the dielectric losses only. The distributed resonances, seen in the measurement data, cannot be captured with this methodology, which is a known limitation.

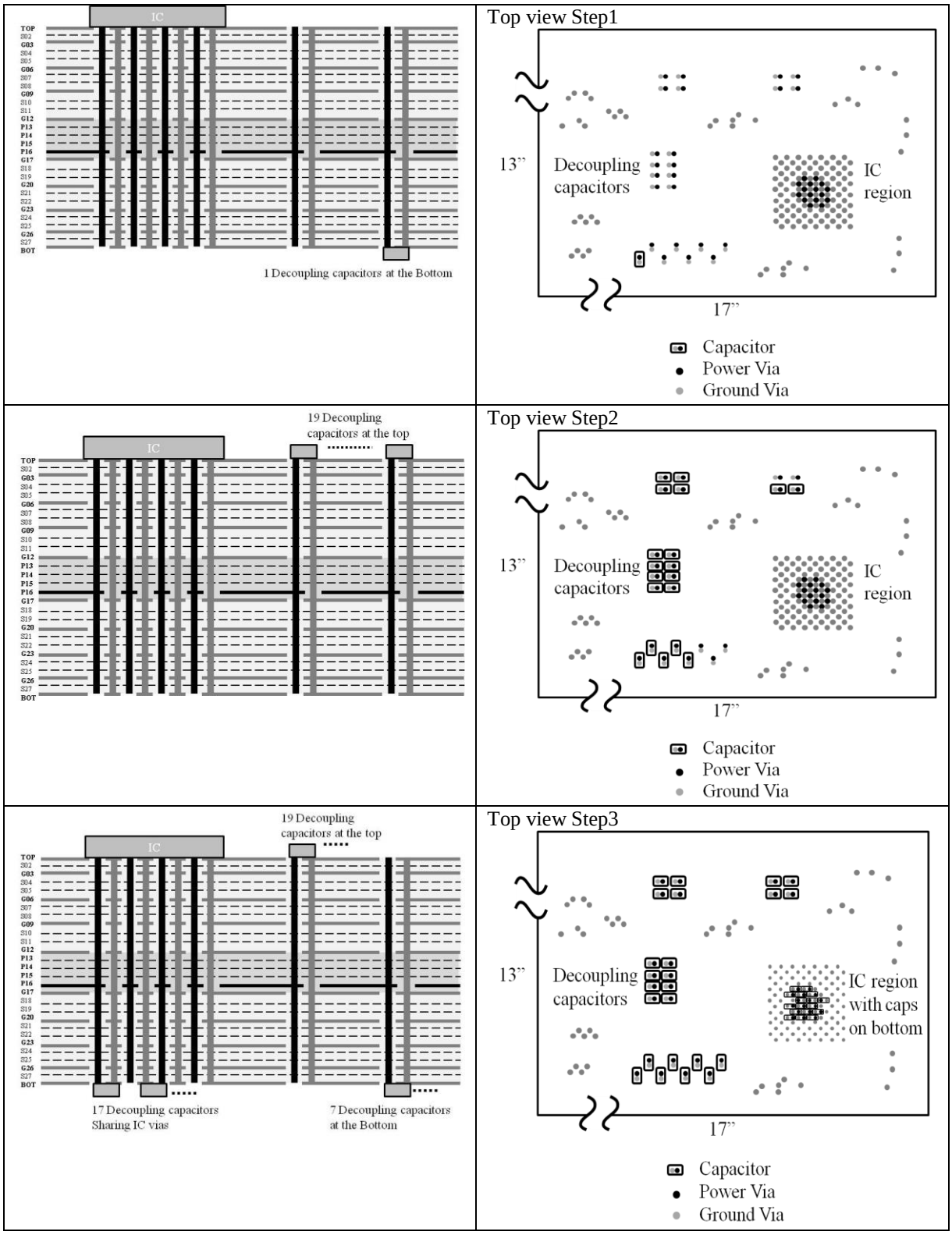


Figure 2.8. Shows the geometry of the real board used in the three steps.

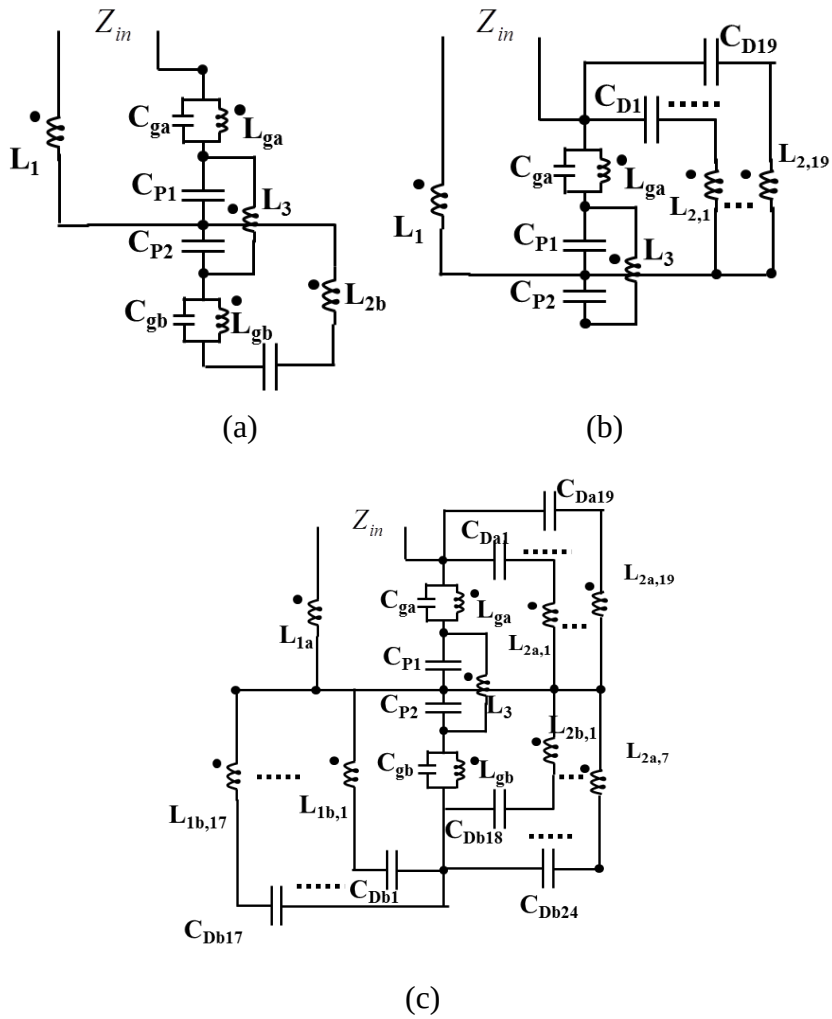
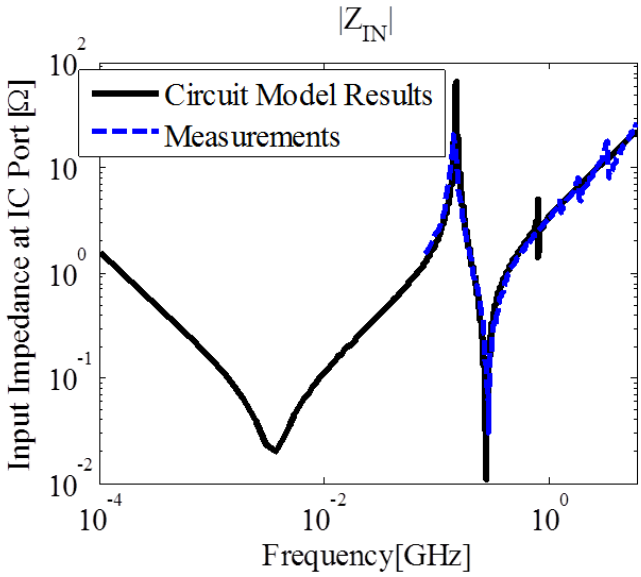
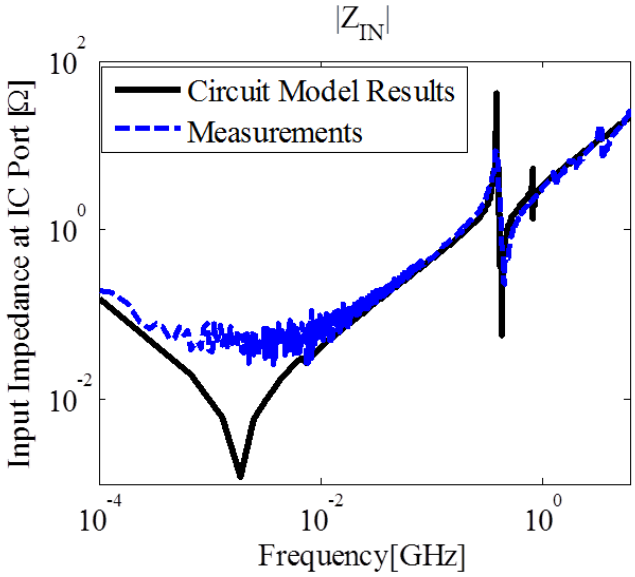


Figure 2.9. Circuit models after reduction for the three cases: (a) Step1, (b) Step2, and, (c) Step3.

The Figure 2.10(d) provides a more practical picture of the input impedance, as it shows the input impedance of the PDN seen with all 17 IC vias used as the observation port in the circuit model. The change affects the current path from the IC to the power cavity and by comparison, it is observed that the mid frequency and high frequency inductance both are significantly reduced.

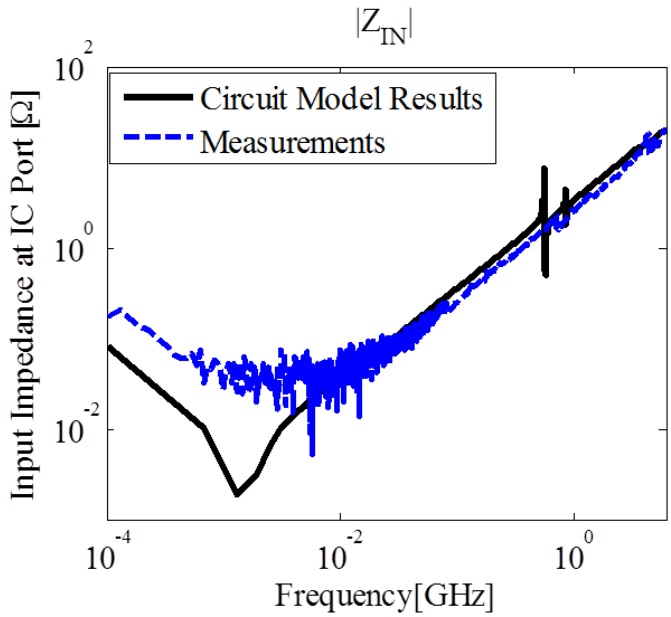


(a)

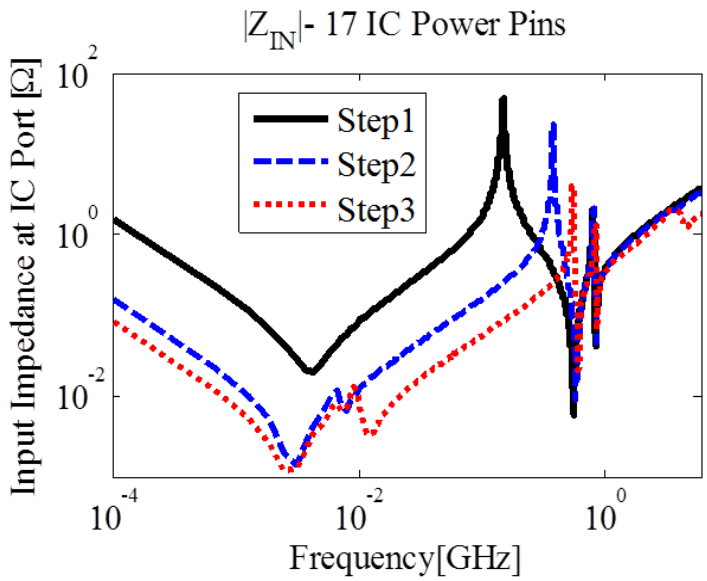


(b)

Figure 2.10. Comparison of the circuit model response and measurements for all three steps, in (a), (b), (c) and comparison of the circuit model responses for all three steps in (d) with the port defined using all 17 IC power pins.



(c)



(d)

Figure 2.10. Comparison of the circuit model response and measurements for all three steps, in (a), (b), (c) and comparison of the circuit model responses for all three steps in (d) with the port defined using all 17 IC power pins (cont.)

2.4. DISCUSSIONS

The methodology was illustrated for the one power layer design, but can be extended easily to the case with the power net having area fills on multiple layers. Also,

the geometry is assumed to have at least one return layer above and below the power layer. This implies that the high layer-count boards would not have the power layer on the topmost plane layer or bottommost plane layer, which is usually the case in real PCBs. There may be signal layers at the top or bottom, which allow for routing and component layout. A signal layer at the topmost or bottommost layer in the PCB will require some parasitic elements to be added to the capacitor model, but for the scope of this paper, we use a solid return plane on top and bottom of the PCB.

The circuit model is based on inductance extraction from the rectangular cavity model and its limitations are also inherited. The exact shape of the power layer is used to find the capacitance of power cavity correctly. However, the inductance accuracy is dependent on how close is the used rectangular shape to the real shape. As long as the power vias are far away from the real power shape edge, which is not a part of the approximated rectangular shape, the approximation will have a small effect on the accuracy of the inductance extraction. This assumption about the negligible effect of power plane shape for inductance calculations was demonstrated to hold in the modeled PCB. Some PDNs use traces for routing power, and cannot make use of this methodology unless a model is inserted for the power traces.

2.5. CONCLUSION

The new methodology proposed in this Section can be used to model the real PCB-PDNs with good accuracy. This was verified by modeling a real production level PCB structure and comparing the model response with measurements. The methodology provides a reduced circuit which can be simulated in a SPICE based solver to get the input impedance of the PDN. The model is physics-based, which helps to map the circuit elements onto the corresponding geometry features. It provides for an insight to the designer, to relate the design choices to the PDN impedance features. The model has also been reduced to a great extent, considerably reducing the simulation time, and hence is suitable for optimization algorithms.

3. ANALYSIS OF CIRCUIT MODEL

3.1. INTRODUCTION

High- speed digital systems are moving to higher data rates and smaller supply voltages as the scale of integration goes smaller [5]. Such systems require DC power to be delivered from the voltage regulator modules (VRM) to the integrated circuits (ICs), with very small tolerances on the supply voltages ripples. Power distribution networks (PDNs) on a printed circuit board (PCB) are implemented to ensure such a low-noise, steady power supply from the VRM to the IC, within some peak voltage ripple.

Switching transistors, in the IC, need charge at the signal's rising or falling edges to charge or discharge their capacitive loads, leading to a high frequency current draw. The current draw when a large number of such transistors are switching, while synchronized to a system clock, results in a disturbance or ripple on the supply rails, known as the simultaneous switching noise (SSN) [2]. The SSN can propagate in the system, along the PDN and couple to other nets, causing several signal integrity (SI) and electromagnetic interference (EMI) problems [3, 4, 6-9]. To avoid these problems, the PDNs are designed with several charge storage units, called decoupling capacitors, along the different stages in the system, like the die, the package, and the PCB. These decoupling capacitors will supply charge in different frequency ranges. The placement and value of these decoupling capacitors can affect the system performance.

Performance of a PCB PDN design is conventionally analyzed using the PDN impedance looking into the PCB from the IC [10]. The impedance shows a frequency domain profile of the noise voltage created for a broadband IC power current draw. Since the PDN design is based on guidelines and designers' experience, or 'trial and error' with full wave tools, the designers' intuition and understanding of the physics behind the PDN performance, will impact the design process significantly.

An analytical PDN modeling methodology was proposed in [28]. This methodology models a real complex multi-layer PCB with power and return planes, several IC power pins, several decoupling capacitors, and, a large number of power and return vias, with a reduced SPICE circuit model with comparatively small number of circuit elements. This model is physics-based, that is, there is a one-to-one relationship

between the circuit model components and the individual geometry features or current path physics which they represent. Such analysis of the model response for the PCB PDN and the relationship between the response features to the geometry features was not discussed in [28].

An interpretation of the reduced model response is presented, herein, showing that the frequency domain input impedance of the PCB PDN has a generic trend. This generic response holds for different power plane shapes or locations in the PCB stack up, for different capacitor numbers, sizes, locations, and for different IC power pin number and patterns. Using sensitivity analysis on analytical model response for two cases with one and two capacitors, the dependence of the individual response features on model components and hence dependence on the geometry, is established. These conclusions are extended to cases with several capacitors placed at different locations. This provides a mapping between the response to the circuit model to the geometry features and material properties. The conclusions of this analysis are discussed in the light of current path physics for different frequency regions, which can be used to establish PDN design guidelines.

The main contributions of this paper are to show that the PCB PDN input impedance follows a generic trend with features, which can be mapped to specific PDN geometry. A clear relationship is provided between individual response features, the circuit model components, and, the geometry features, using a sensitivity analysis. A way to extend the physics to multiple capacitor cases is explained, which leads to strong PDN design conclusions for general multi-layer PCB PDNs.

3.2. REDUCED CIRCUIT MODEL AND GENERIC PCB PDN INPUT IMPEDANCE

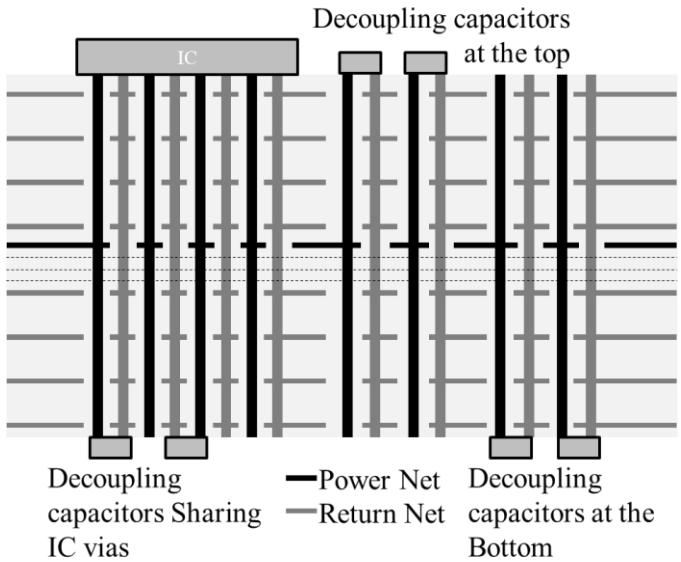
The methodology to generate a circuit model for a real PCB was shown in [28]. The final model created has an intuitive circuit representation which is very useful for designing a PDN, as it relates the circuit elements with the geometry features or material properties based on the physics used in the model. This means that the model element values can be controlled by changing geometry features or material properties. Generic

PCB geometry and its circuit model are shown in Fig. 3.2, where the relationship between different parts of the geometry and the circuit model are shown.

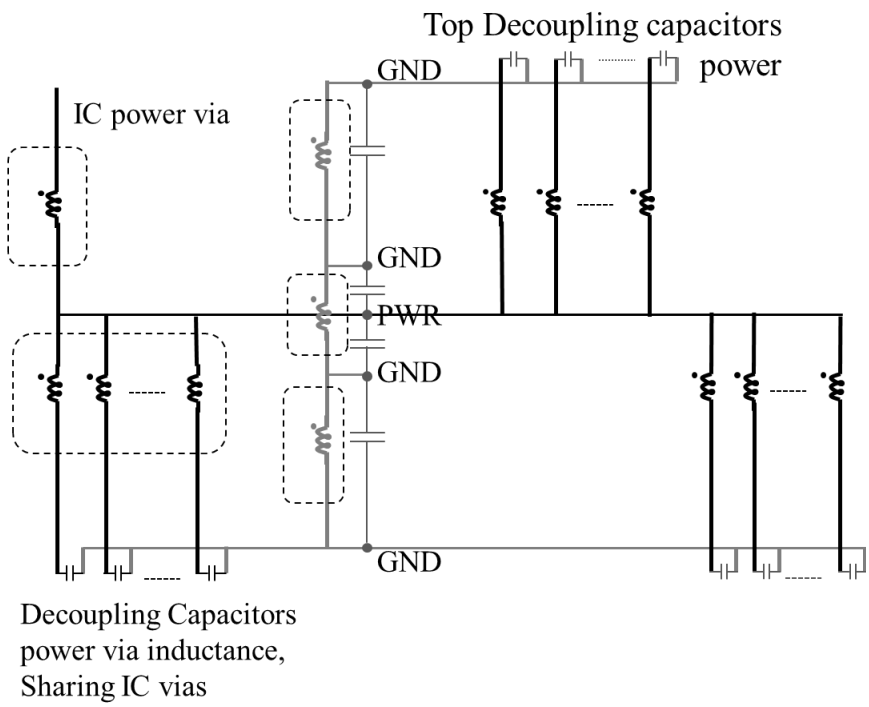
Fig. 3.1(a) shows generic PCB PDN geometry with one power layer placed deep in the stack up with several return layers, and several decoupling capacitors. The decoupling capacitors may be placed under the IC sharing the IC vias, or placed on top or bottom layer away from the IC with their own connection vias. The circuit model in Fig. 2(b) shows one inductor representing the IC power vias, one inductor each representing the power vias connecting the decoupling capacitors. All the return net vias are represented an effective return via inductance which is divided into three parts to allow separate the parts above and below the nearest return planes from the power plane. All via inductances are coupled with mutual inductances. The plate pair capacitances are represented but individual capacitor elements. The decoupling capacitors model are connected between the via nodes and top or bottom return planes.

The trends in a typical response of the PCB PDN model are identified in Fig. 2. It shows the simplified input impedance of the circuit model, looking in from the port at the IC, into the power and return vias, using asymptotes of the dominant elements of circuit model as the frequency increases. The frequency of interest is limited from the region where the decoupling capacitors are effective, to the high frequency region where the package decoupling takes over. The different parts of the response are based on the impedance in the current path as the frequency increases.

The low frequency is dominated by the total capacitance, C_{Total}, which includes the decoupling capacitors, and the capacitance between the power plane and the neighboring return planes, also referred to as plane capacitance C_P. The inductive region after the total capacitance region is determined by the equivalent path inductance, L_{EQ}, between IC and the total capacitance. The pole after this inductive region is termed as the 1st pole, which is followed by the plane capacitance C_P. The high frequency impedance is also inductive, named L_{High}, which is dominated by the inductance between IC and the power plane capacitance.



(a)



(b)

Figure 3.1. (a) Geometry of multi-layer PCB PDN with several decaps placed on both sides of the PCB, (b) Reduced circuit model using the methodology shown in [28].

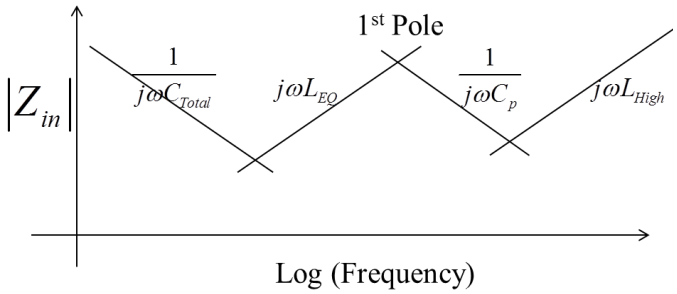


Figure 3.2. Simplified asymptotic PCB-PDN impedance representation shown as a combination of poles and zeros formed by capacitive and inductive dominated impedance regions.

The simplified response shows only one pole (parallel-resonance) to represent the dominant parallel resonance behavior. If capacitors with different values are used, many small poles are usually observed in the low frequency or L_{EQ} region. Also a pole may occur after the shown 1st Pole, if the power plane has a return plane above and below it in the stack up, but this pole will not be seen in the measurements due to the losses in the geometry.

To justify the response features and physics stated above, which is mostly empirical, a sensitivity analysis was used with the proposed circuit model, to relate the important features of the response to the corresponding circuit elements, and hence to the physical geometry influencing that response feature.

3.3. ANALYSIS OF PDN IMPEDANCE

To get a mapping of the response features on the circuit elements a sensitivity analysis is performed on the response features as a function of the circuit element values. To establish relationship between the response and the circuit model, an analytical expression for the impedance is required. This rigorous expression can be written for a few capacitors but will become too complicated to derive for many capacitors. In this section, two test cases are created with one and two capacitors each and analyzed methodically to derive this relationship. Then the input impedance expressions are analyzed to extract individual features, and a sensitivity analysis is used to find the circuit element dependence.

3.3.1. Geometry Description of Test Cases. Two test cases will be studied for sensitivity analysis. Both cases use a PCB with a 28 layer stack up, same as the real board stack up in [10], as shown in Figure 3.3. Case1 has one decoupling capacitor on the top layer and Case2 has two decoupling capacitors, one each on top and bottom layers. They share the same stack up, with the power net of interest routed on the 16th layer, where it has an area fill. There are many plane layers used for return net. Also, other power nets fills are present in the stack up, e.g., some power nets are routed on layers 13 through 15 with area fills. The closest return plane is on layer 12 and 17. The top and the bottom layers of the board are also return planes.

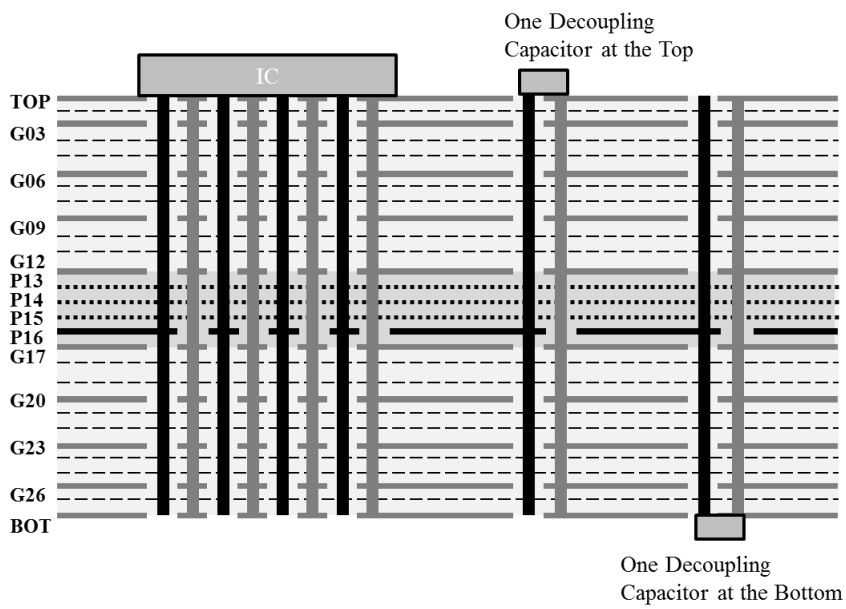


Figure 3.3. Case 1 geometry used for the sensitivity analysis with one decoupling capacitor placed on top of the board, and Case 2 geometry with one decoupling capacitor used at the top and the bottom each of the board.

3.3.2. Circuit Model and Analytical Solutions. The reduced circuit model for Case1 geometry, using [10] is shown in Fig. 3.4, where it is redrawn with current definitions for mesh analysis. The loss in the model is ignored for now to reduce the complexity of the expressions being derived. The inductors L1 and L2 represent the

power via inductance for the IC via and decoupling capacitor via inductance respectively. Lg represents the return vias from top layer to the last return plane before the power layer, Cg represents the parallel plate capacitance for the return layers. L3 represent the inductance of the return vias, between the nearest return planes on each side of the power plane, CP1 and CP2 represent the parallel plate capacitance to the return planes above and below the power plane.

Circuit analysis on the circuit shown in Figure 4 will give the expression,

$$\mathbf{Z}\left(\begin{bmatrix} I_1 & I_2 & I_3 & I_4 \end{bmatrix}^T\right) = \begin{bmatrix} V_1 & 0 & 0 & 0 \end{bmatrix}^T, \tag{3.1}$$

$$\mathbf{I} = \mathbf{Z}^{-1}\mathbf{V}, \tag{3.2}$$

where,

$$\mathbf{Z} = \begin{bmatrix} sL_1 + \frac{1}{sC_{p1}} + \frac{1}{sC_g} & -\frac{1}{sC_{p1}} - sM_{13} & sM_{13} + sM_{1g} - sM_{12} & -sM_{1g} - \frac{1}{sC_g} \\ -\frac{1}{sC_{p1}} - sM_{13} & sL_3 + \frac{1}{sC_{p1}} + \frac{1}{sC_{p2}} & -sL_3 - \frac{1}{sC_{p2}} + sM_{23} & 0 \\ sM_{13} + sM_{1g} - sM_{12} & -sL_3 - \frac{1}{sC_{p2}} + sM_{23} & s(L_2 + L_g + L_3) - 2s(M_{23} + M_{2g}) + \frac{1}{sC_D} + \frac{1}{sC_{p2}} & s(M_{2g} - L_g) \\ -sM_{1g} - \frac{1}{sC_g} & 0 & s(M_{2g} - L_g) & sL_g + \frac{1}{sC_g} \end{bmatrix}, \tag{3.3}$$

$$\mathbf{I}^T = \begin{bmatrix} I_1 & I_2 & I_3 & I_4 \end{bmatrix}, \text{ and,} \tag{3.4}$$

$$\mathbf{V}^T = \begin{bmatrix} V_1 & 0 & 0 & 0 \end{bmatrix}. \tag{3.5}$$

The input impedance looking at the port of IC pin for PDN can be written as,

$$Z_{in} = \frac{V_1}{I_1} = \frac{1}{\mathbf{Z}^{-1}(1,1)}, \tag{3.6}$$

$$\mathbf{Z}=\begin{bmatrix} s(L_1+L_{ga}-2M_{1\_ga})+\dfrac{1}{sC_{p1}} & -\dfrac{1}{sC_{p1}}-sM_{13} & 0 & \begin{pmatrix} s(-L_{ga}+M_{13}+M_{1\_ga} \\ -M_{1\_2a}+M_{2a\_ga}) \end{pmatrix} \\ -\dfrac{1}{sC_{p1}}-sM_{13} & sL_3+\dfrac{1}{sC_{p1}}+\dfrac{1}{sC_{p2}} & -\dfrac{1}{sC_{p2}}-sM_{2b\_3} & s(-L_3+M_{2b\_3}+M_{2a\_3}) \\ 0 & -\dfrac{1}{sC_{p2}}-sM_{2b\_3} & \begin{pmatrix} s(L_{2b}+L_{gb} \\ -2M_{2b\_gb})+\dfrac{1}{sC_{p2}} \end{pmatrix} & \begin{pmatrix} -s(L_{2b}+L_{gb}-2M_{2b\_gb}) \\ +sM_{2b\_3} \end{pmatrix} \\ \begin{pmatrix} s(-L_{ga}+M_{13}+M_{1\_ga} \\ -M_{1\_2a}+M_{2a\_ga}) \end{pmatrix} & \begin{pmatrix} s(-L_3+M_{2b\_3} \\ +M_{2a\_3}) \end{pmatrix} & \begin{pmatrix} -s(L_{2b}+L_{gb} \\ -2M_{2b\_gb}-M_{2b\_3}) \end{pmatrix} & \begin{pmatrix} s(L_{ga}+L_3+L_{gb}+L_{2b}+L_{2a} \\ -2M_{2a\_ga}-2M_{2b\_gb} \\ -2M_{2b\_3}-2M_{2a\_3}) \end{pmatrix} \end{bmatrix}. \quad (3.7)$$

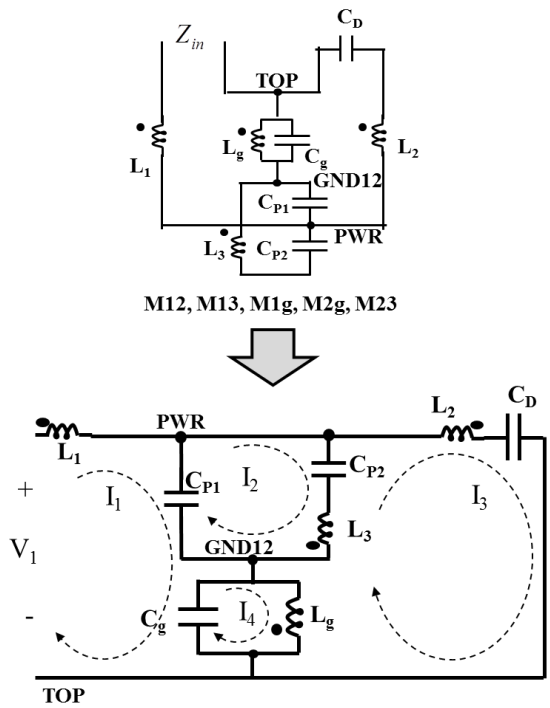


Figure 3.4. The reduced circuit model for Case1 on the top redrawn into the representation on the bottom used to write the analytical expressions.

A similar procedure, as Case1, can be used with the Case2. The circuit models for Case2, original and redrawn, are shown in Figure 3.5. The nomenclature is same as for Case1, with an extra subscript ‘a’ and ‘b’ added for elements representing geometry above the power layer and below the power layer, respectively. The decoupling capacitors are shorted to reduce the order in ‘s’ of the solution. So for Case2, the response

will start with the equivalent inductance of the current path from IC to the capacitors, i.e., L_{EQ}. Also, the losses in the model are ignored to reduce the complexity of the model.

The input impedances expressions for Case1 and Case2 are found using (3) and (7), respectively, in (6). The input impedances calculated from these analytical expressions are plotted against frequency in Figure 3.6 for both cases. Loss is neglected in the model, so the resonances have a very high Q factor.

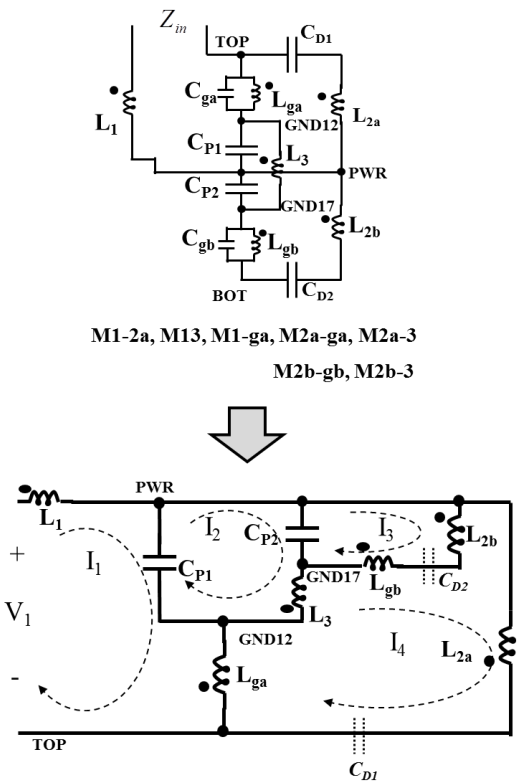
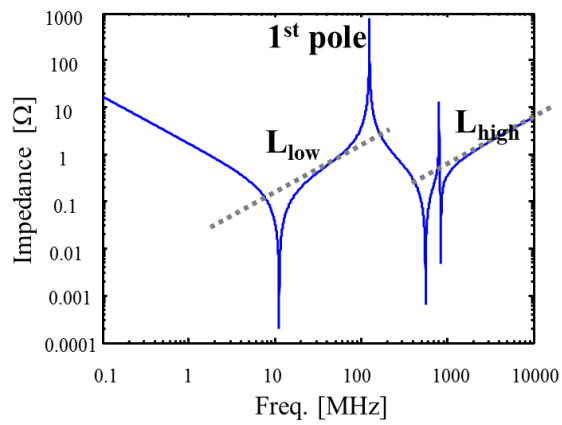


Figure 3.5. Circuit model for Case2 with a decoupling capacitor on top layer and bottom layer each, transformed for circuit analysis on the bottom with the decoupling capacitors shorted.

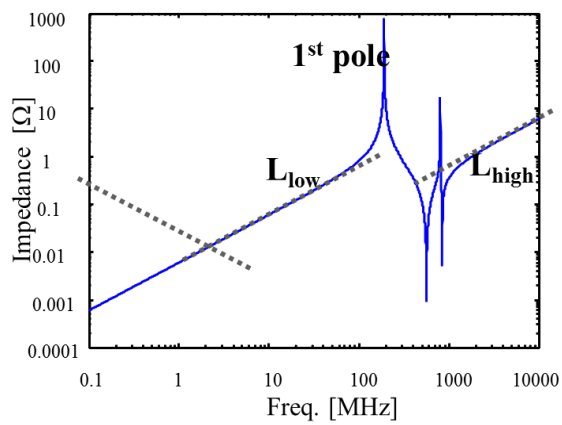
3.3.3. Sensitivity Analysis. The expressions of frequency dependent input impedance can be analyzed for individual features like low frequency and high frequency trends, poles, and zeroes of the input impedance. The expressions for these features are very complicated and it becomes difficult to clearly derive conclusions about their dependence on the individual elements. Hence, sensitivity analysis is performed with

these expressions for the individual features of the input impedance. Then, the element values for the circuit models under study are used to get the sensitivity in the form of numerical values which can be compared to derive conclusions. The sensitivity of feature 'X' to the circuit element 'a' is defined as,

$$S_a^X \triangleq \frac{a}{X}\frac{\partial X}{\partial a}. \tag{3.8}$$



(a)



(b)

Figure 3.6. (a) Input impedance plot vs frequency from the analytical expressions for Case 1 and (b) Input impedance plot vs frequency from the analytical expressions for Case 2, where the Case 2 analytical expression has the decoupling capacitors shorted, so the response start from an inductive behavior at low frequency.

For sensitivity analysis, the important features of the response are identified, and using (8), the sensitivity of each feature to each circuit element is calculated. Three response features are identified as critical response features for any PDN design. These are the equivalent inductance from IC to the capacitors, the first pole frequency and the high frequency inductance of the model from the IC vias connecting to the power plane, referred to, herein, as L_{EQ}, f_{Pole1} and, L_{High} respectively.

L_{EQ} is the inductance of the circuit, when the decoupling capacitors are shorted, and plane capacitances are open circuited, as,

$$L_{EQ} = \left(Z_{in} \big|_{C_g, C_{p1}, C_{p2}=0; C_d \to \infty} \right) \Big/ j\omega . \tag{3.9}$$

Qualitatively, this is inductance of the current path from IC to decoupling capacitors through the power planes and its return. The pole frequency is the first root of denominator in the analytical solution of the PDN impedance. The solution to,

$$\frac{1}{Z_{in}(f)} = 0 , \tag{3.10}$$

gives the 1st Pole frequency. The L_{High} is found by shorting the plane capacitors C_{P1} and C_{P2}, as,

$$L_{High} = \left(Z_{in} \big|_{C_g, C_{p1}, C_{p2}, C_d \to \infty} \right) \Big/ j\omega \ . \tag{3.11}$$

The sensitivity analysis is carried out for the two cases for the three features of the response identified above based on equations (3.1) through (3.11), and the results are summarized in Table I. The circuit element values, listed in the table, are obtained from the circuit models used for the two cases.

The sensitivity value is the percentage change in the feature value when the element value is changed by 1 percent. The sign denotes the direction of change, so negative sign indicates inverse proportionality. The sensitivity is referred to as high, in this paper, if the value is more than 1/10th of the maximum sensitivity value for that

feature. Such values are highlighted in bold fonts. Figure 7 also shows a graphical representation, highlighting the dominant circuit elements in the sensitivity analysis results of each response feature.

3.4. INTERPRETATION OF SENSITIVITY ANALYSIS RESULTS

The results shown in Table I are specific to the two test cases used in this paper. These can be used as evidence of the dependence of the response features on the particular circuit elements and to extract the physics of the circuit model behavior, but, the specific sensitivity values are valid only in the neighborhood of the specific element values used in the sensitivity calculations. To keep the circuit element values physical, practical geometries were used which could be rigorously studied. The interpretation of the results and the extracted physics is articulated in this section.

3.4.1. Test Case Results.

3.4.1.1 L_{EQ}. The Case1 results show that the L_{LOW} is controlled by L_1, L_2, and also the mutual term between them, which form the path from IC to the decoupling capacitors and its return. For Case2, the same current will flow towards both capacitors, thus L_1, L_2 and L_g and the related mutual terms are the responsible elements. This low frequency inductance is the equivalent inductance of the entire path from the IC to the capacitors, and its return. All the decoupling capacitors have a series resonance frequency after which the capacitor can be assumed as shorted so only the series inductance is seen, or, another interpretation is that the series inductance will have comparatively higher impedance, and hence dominates the response. There is a contribution from the return current path as well, which shows up in the mutual terms. All the geometry along the current path will affect L_{EQ}, the IC power and return vias number and pattern, the power cavity thickness and size, the decoupling capacitor location and via connections, and, the capacitors internal series inductance as well.

Table 3.1. Sensitivity values for the response features to various circuit element values.

Case 1					Case 2				
		1st Pole	**L_{EQ}**	**L_{HIGH}**			**1st Pole**	**L_{EQ}**	**L_{HIGH}**
Circuit Element	**Value**	128 MHz	2.22 nH	99.7 pH	**Circuit Element**	**Value**	191.4 MHz	0.95 nH	98.9 pH
L_1	1.09 n	0	**0.53**	**11.31**	L_1	1.09 n	0	**1.16**	**11.0**
L_2	3.06 n	**-0.7**	**1.47**	0.01	L_{2a}	3.19 n	**-0.28**	**0.57**	0.01
L_3	246 p	-0.03	0	**1.69**	L_{2b}	2.36 n	**-0.44**	**0.86**	0.01
L_g	820 p	**-0.19**	0	**8.18**	L_3	246 p	~0	0.09	**1.66**
M_{12}	1.03 n	0	**-0.99**	-0.45	L_{ga}	823 p	**-0.07**	0.30	**8.00**
M_{13}	204 p	0	0	**-3.45**	L_{gb}	821 p	**-0.15**	0.30	.004
M_{23}	203 p	0.07	0	0.07	M_{1_2a}	1.03 n	0	**-0.90**	-0.41
M_{1g}	820 p	0	0	**-16.7**	M_{13}	205 p	0	-0.25	**-3.38**
M_{2g}	817 p	**0.39**	0	0.35	M_{1_ga}	823 p	0	**-1.02**	**-16.3**
C_{p1}	235 p	**-0.16**			M_{2a_ga}	819 p	**0.15**	0.42	0.32
C_{p2}	510 p	**-0.3**			M_{2a_3}	203.5	0.01	0.10	0.07
C_g	5.4 n	~0			M_{2b_gb}	820.5	**0.31**	**-0.60**	-0.01
					M_{2b_3}	41.72	-.002	-0.03	-0.02
					C_{p1}	235 p	**-0.17**		
					C_{p2}	510 p	**-0.33**		

3.4.1.2 First pole. The first pole in the response for Case1 is controlled by the dominant cavity capacitance CP1 and CP2, and the inductances L2 and Lg, and their mutual inductance. This shows that the parallel plate capacitance and the inductance of the current path, from the power plane to the decoupling capacitor and its return, form a parallel resonant circuit, which gives the first pole in the input impedance. In an analogous manner, for the Case2 also, the first pole depends on the cavity capacitance, CP1 and CP2, and the inductance in the current and current return path to the decoupling capacitors, L2a, Lga, L2b, and Lgb. As the Case2 has two decoupling capacitors, the current paths involve all the elements contributing to this current and its return path. The inductances related to the IC power vias do not affect the first pole frequency in either case. The geometry that can control this pole is the power cavity size and thickness for the capacitance, the decoupling capacitor connection vias number and size, and, capacitors internal parasitic inductance.

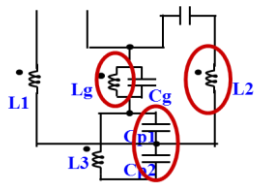
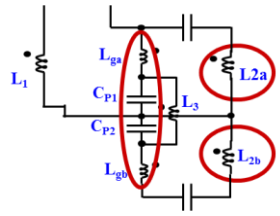
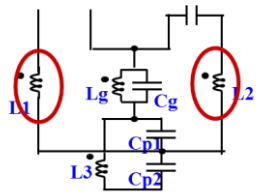
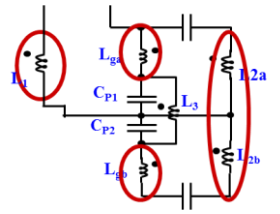
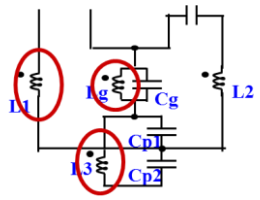
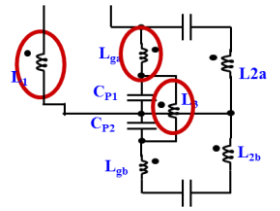
Feature	Case1-Dominant elements	Case2 - Dominant elements
1st Pole		
L_{LOW}		
L_{HIGH}		

Figure 3.7. A summary of the sensitivity analysis results for the cases.

3.4.1.3 L_{HIGH}. The high frequency inductance, L_{HIGH} in Case1 depends on the L_1, L_g, L_3, and the mutual terms between them. These inductors represent the current path from the IC to the power planes and the corresponding return current path. The Case2 also has exactly the same elements responsible for the high frequency inductance, as the high frequency current path remains same for both cases. So the high frequency inductance is not affected by the decoupling capacitor vias, but the IC to power cavity connection via number, pattern, pitch, and size, along with the power cavity location in the stack up will have significant effects on this value.

3.4.2. Extension to Multiple Capacitor Cases. The analysis was performed using one capacitor on Top layer in Case1 and one each on Top and Bottom layers in Case2. The results of the sensitivity analysis are in terms of the dominant circuit

elements, which are representative of the specific geometry features due to the physics based modeling approach. The analysis results support the physics used to identify the dominant current paths in the different frequency ranges, which led to the simplified response in Figure 3.1(c). Therefore, the extrapolation to multiple capacitor case is done using the same frequency dependent current paths. The current paths qualitatively remain the same as the Case1 and Case2, i.e., the current still flows from the IC to the power planes, from power planes to the capacitors, and has a return current path. So the response of the model for multiple capacitors is also similar to the Case1 and Case2 response, i.e., has the same features.

When multiple capacitors are used, there will exist as many parallel current paths from the power planes to the capacitors and their corresponding return current paths. These are represented as parallel circuit branches with decoupling capacitors connecting to the plane capacitance in the model. As these parallel circuit branches have the same topology as the single branches considered in Case1 and Case2, the response features controlled by the single branches will be controlled by the parallel capacitor branches from the multi-capacitor models.

L_{EQ} and the 1st Pole frequency were both affected by the decoupling capacitor branch inductance. These two features depend on the current path from power planes to the decoupling capacitors. So, in multi-capacitor models, these two features will also depend on the parallel capacitor branches. The difference being that a parallel combination of several current paths has to be considered and these branches may be mutually coupled. More branches may reduce the effective inductance to reach the capacitors from the power planes, and hence reduce L_{EQ}. Also, smaller effective inductance of these parallel branches will increase the 1st Pole. Thus the number, pattern and connection vias of the

The extension to real multi-capacitor cases can be demonstrated using a set of results presented in [28]. These set of results have been shown in Figure 3.8, for convenience to the reader. There are two families of results, first with one IC power via and the second with seventeen IC power vias used in the IC port. The one IC power via family has been compared to micro-probing measurements as a validation. The family with seventeen IC power vias model a more practical situation as the IC is connected to

all 17 power vias. The used circuit model does not capture the loss accurately, resulting in poles with very high Q factor. Also the second pole is observed in the simulations but is shown to be damped with the losses in the system in[28], so not analyzed herein.

The low frequency, where the current flows from the IC to the decoupling capacitors, through the power planes, is affected by the number of decoupling capacitors. The low frequency capacitance is the total capacitance in the circuit, which is seen to increase in both families of curves, as number of capacitors is increased. The low frequency inductance, LEQ, also decreases with the increase in number of parallel branches of decoupling capacitors. For each family the part of current path from the IC to the power planes is different, so, they show different magnitudes but have the same trends. The 1st Pole frequency shift higher with more capacitors as the parallel resonance is inversely proportional to the effective inductance of all the decoupling capacitors. As this 1st pole frequency does not depend on the part of current from the IC to the power planes, it remains the same for the cases with same number of capacitors.

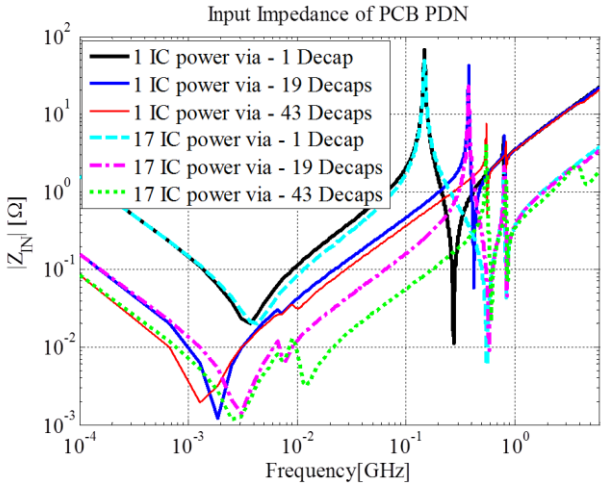


Figure 3.8. Comparison PDN input impedance results from [10] for a real PCB for a combination of number of decoupling capacitor and number of IC power vias used in the port, to demonstrate the relation between the geometry and the circuit model response.

At higher frequencies, beyond the 1st Pole frequency, the current path is from the IC to the power plane capacitance. As number of IC power vias will significantly reduce the inductance of this path, the LIC is seen to reduce significantly between the two

families. Also the number of capacitors does not affect this part of the current path, except for some small effect of the mutual terms with the capacitor branches.

3.5. DISCUSSIONS

The sensitivity analysis results are interpreted in a manner such that the current path physics is validated for different frequency ranges to be used to extrapolate the qualitative conclusions to the multiple decoupling capacitor cases. This section discusses the assumptions and limitations of this analysis and also provides the design guidelines in a ‘how to think about it’ sense.

As mention earlier, the specific sensitivity values are valid only in the neighborhood of the specific element values in the multi-dimension space of the features as functions with the element values as the variables. More qualitative conclusions are derived from this analysis which support the physics and can be used in arbitrary cases. The precise sensitivity value should not be used for quantitative calculations for arbitrary cases, as it may not remain true if the geometry or any element values change.

The dielectric loss accounted for in the actual model, was not a part of the analysis performed herein, to simplify the analytical expressions to the extent that they can provide some meaningful results. As a result the effect of the loss on the pole magnitude, which is where the loss affects the most, is not discussed explicitly. Also, as a result of no loss in the model, there is a second pole in the response shown in Figure 6, which is not in the simplified response or the features analyzed, herein. It was found that this pole depends on the power cavity capacitances, and the return via inductance connecting the return planes above and below the power layer, but is significantly damped in real measurements and barely noticeable[28].

When extending to multiple capacitors with the different values, or locations, or patterns, the similar capacitors will individual resonances in their respective connection branches at different frequencies [29]. This fact is used by some designers to place different value capacitors in different frequency ranges. In most PDN design, these are the smaller poles that occur along the L_{EQ} region. In the simplified response, these are ignored as the dominant pole will have a bigger impact on the PDN performance.

The physics illustrated in this paper can be used to formulate some basic design guidelines for PCB PDNs. The guidelines would provide some ways to modify the

geometry to influence particular response features. These guidelines are based on the principle that the current follows the path of least impedance, in each frequency range, and so the return current flows through the nearest return vias and uses the neighboring return planes to have least inductance in the path.

The decoupling capacitors provide the charge at the low frequencies, where the current path impedance is dominated by the capacitive reactance, controlled by the number and the values of decaps adding up to C_{Total}. This can be controlled by adding more capacitors or using higher value capacitors in the same package size. At some frequency the inductance in the current path becomes dominant, and the capacitors act as short circuits compared to the path inductance accrued by current to reach them. The inductance in this frequency region is named equivalent inductance, L_{EQ}. A designer can change the L_{EQ} by introducing a change in the current path, which is from IC to decoupling capacitors through the power planes and its return. Adding more return vias on IC side or at the decoupling capacitor side, using thinner power-return cavity, moving power layer in the stack up closer to the IC, or arranging capacitors in a pattern to take advantage of the mutual inductance between them, or just adding more capacitors, are some of the ways to reduce L_{EQ}, if so needed.

The 1st Pole is the pole in the input impedance comes from a parallel resonance between the dominant power cavity capacitance (C_P) and the effective inductance of current path, from the dominant power cavity to decoupling capacitors, which is a part of L_{EQ}. To push this pole frequency higher, the effective inductance of reaching the decoupling capacitors can be reduced by putting capacitors on the side closer to the power cavity, or adding more capacitors to create parallel current paths, or spreading the capacitors such that the effective inductance to reach the decoupling capacitors is can be reduced [30], [31].

After the 1_{st} Pole frequency, the power cavity capacitance offers lower impedance path than the decoupling capacitors, so the current flows from IC to the power cavity capacitance (C_P) and returns. The plane capacitance is dominant in this frequency region, till the inductance of this path becomes comparable and dominates as frequency increases. This inductance of the current path, from the IC to the power cavity and back, is L_{HIGH}. It is barely dependent on the decoupling capacitors and can be changed by the

location of the power cavity or number and pattern of the IC vias connecting the IC to the power cavity. The small dependence of L_{HIGH}, on the decoupling capacitors, if any, would come from the mutual inductance between the IC and decap vias.

3.6. CONCLUSIONS

A methodology to analyze the PCB PDN based on a simplified asymptotic response was shown herein. The PCB PDN response is found analytically to use sensitivity analysis for mapping the important response features onto the elements of the circuit model. The model is physics-based, which helps to map the circuit elements in the model onto the responsible geometry features. It provides for an insight to the designer, for connecting the design choices to the features of the response of the PDN model. The trends in different response features are discussed for changes in the geometry of design.

4. CASE STUDIES FOR DESIGN GUIDELLINE DEVELOPMENT

Power delivery network (PDN) design has become more and more critical as the industry moves towards lower supply voltage levels [5]. The PDN is designed such that the peak to peak noise on the power and power return nets is within a certain tolerance. As lower supply voltages are used, the maximum allowable peak to peak noise on the power and power return nets has to reduce proportionately. Noise on the PDN nets can cause several issues from jitter in IO signals, to EMI problems for the system [3], [9]. So it becomes critical to have a good PDN design for successful system design.

In a printed circuit board (PCB), the power and power return nets are routed from the VRM to the IC footprint as shown in Figure 4.1. Several capacitors are placed between these nets to act as charge reservoirs. The large bulk capacitors supply large current at lower frequencies, and the smaller surface mount capacitors provide less charge or current, but upto higher frequencies. This depends on the interconnect inductance which controls the time constant for charge delivery. The power net fill and power return net fills on two preferably consecutive layers in the stack up form a plane-pair capacitor. These area fills make it convenient to connect lumped capacitors placed on either sides of the board, using vias. The plane pair capacitor also acts a charge reservoir but with low charge capacity compared to lumped elements and higher speed.

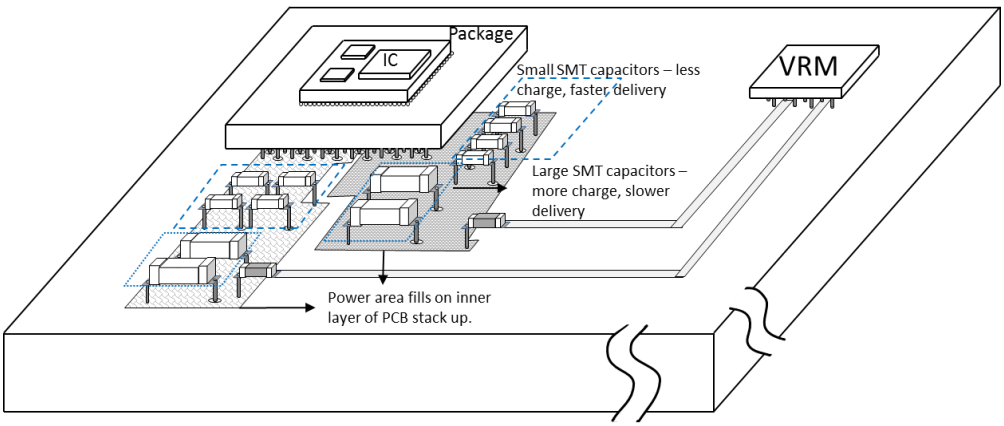


Figure 4.1. Shows a real high layer count PCB with many ICs, each having a number of power nets, with their own PDNs

The designer has control over several factors in the PDN, based on the desired performance of the system. As such, the designer will have to make several decisions regarding the capacitor values, package sizes, locations, the pattern in which capacitors are placed, power plane location in stack up, and so on. These options raise some questions such as: *how close do the capacitors need to be? Does bottom or top side placement make a difference? Which layer to use for the power fill?*

The present solution is mostly based on experience, some best engineering design practices and also some full wave and 2.5D optimization tools. But the physics behind the solution is not clear to many. This paper aims at developing a methodology to find the answer by relating the geometry to a circuit model and then to a response. The response can predict the performance of the design and hence can be used as a design criterion.

The PDN impedance is used to analyze the performance of the PDN. This is the response of the used circuit models or measurements on the real board. The PDN impedance is the impedance looking into the board from the IC pads, between the power and power return nets. The impedance profile can be analyzed by understanding its different features which are controlled by different parts of the geometry, as shown in Figure 4.2. The response can be changed by making changes in the particular geometry associated with a feature. A target impedance [10] is defined to judge the performance of the PDN. The PDN is designed to have its impedance below the target impedance. The target impedance was originally defined as a constant magnitude curve, but as shown in Figure 4.2, the target impedance is better defined with a slope at the high frequency to avoid over design [32]. The target impedance value suggests that the voltage noise generated due to a max current draw at any frequency would be within tolerance. If the PDN impedance value exceeds the target impedance, then a maximum current drawn would create a noise voltage at the IC pads, which is not acceptable for proper operation of the IC.

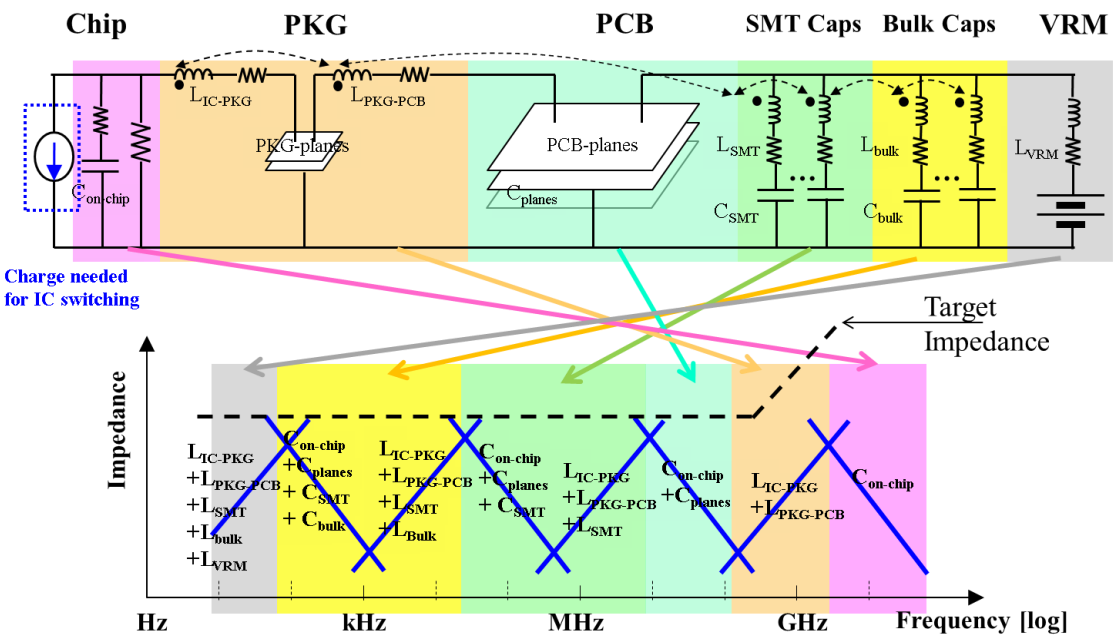


Figure 4.2. Important features of PDN controlled by the designer related to the typical PDN impedance response.

In Figure 3.2, the important features of the response, the L_{EQ} , and the L_{IC}(also known as L_{High} in PCB PDN response in Section 3), were highlighted in the response, which are shown here as a part of the bigger model response including the VRM, package and chip in Figure 4.2. These features are related to the current paths in these frequency regions, as shown in Figure 4.3. The L_{EQ} represents the inductance seen by the IC as the current travels from the IC to the capacitors through the power plane and back. All the geometry along this path contributes to the L_{EQ}. Thus, the vias connecting the IC to the power planes, the power – power return plane-pair, the connecting vias from the power plane to the capacitor and the return path will contribute to L_{EQ}. The L_{IC} represents the inductance seen by the IC as the current travels from the IC to the power planes and back along return vias. The geometry, modeled circuit elements and associated response features for L_{EQ} and L_{IC} are clearly shown in the Section 3.

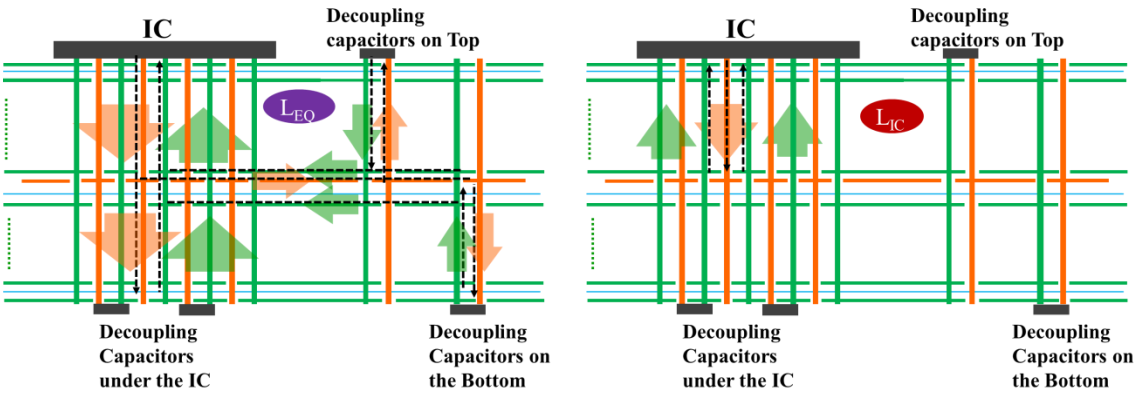


Figure 4.3. Current paths in different frequency ranges, which influence the L_{EQ}, and L_{IC} in the PDN impedance.

4.1. CASE STUDY FOR HIGH LAYER COUNT PCBS

The performance of the modeling methodology and the details of the implementation are explained in detail in Section 2. The methodology is used, herein, to perform a case study which will provide an understanding of the effect of design decisions on the response, with the help of the physics and the circuit model. The cases all start with a base geometry and variations are introduced in this geometry to observe the change in the model and the response.

Figure 4.4 shows the stack up used for all the cases. This is a 44 layer stack up, with the option to place the power layer near the top, or the center of the board or the bottom. This is a generic stack up for high layer count boards used such that the conclusions can be extended to other stack ups. The power- power return cavity is 3 mils thick, with the board about 165 mils thick. There are sixteen capacitors placed around the IC region at a distance of 300 mils from the IC edge. The capacitors have two vias, one each for the power and the power return nets. The capacitors are modeled using a spice circuit model which has a series inductance of 0.6 nH and series resistance of 100 mΩ. The distance between them is 100 mils unless specified. The IC region has 16 power pins and 170 power return pins placed with pitch of 1 mm. The large number of power return vias is used to represent the situation in real ICs where several power nets share a return net.

There are several variations in geometry that can be chosen as cases to understand the PDN behavior. Some of these cases are organized and shown in the Table 4.1. These cases will be studied in detail in this paper. The organization of the table is in terms of the geometry or layout factors along the column that can have a number of variations, as shown along the row. Some cases for capacitor pattern study are illustrated in [30], to show the impact of capacitor patterns on the PDN response. IC power via number and pattern of placement with return vias can be used as a case study. But, as these geometry factors may not be under the PCB design engineer's control, these are not included in this paper.

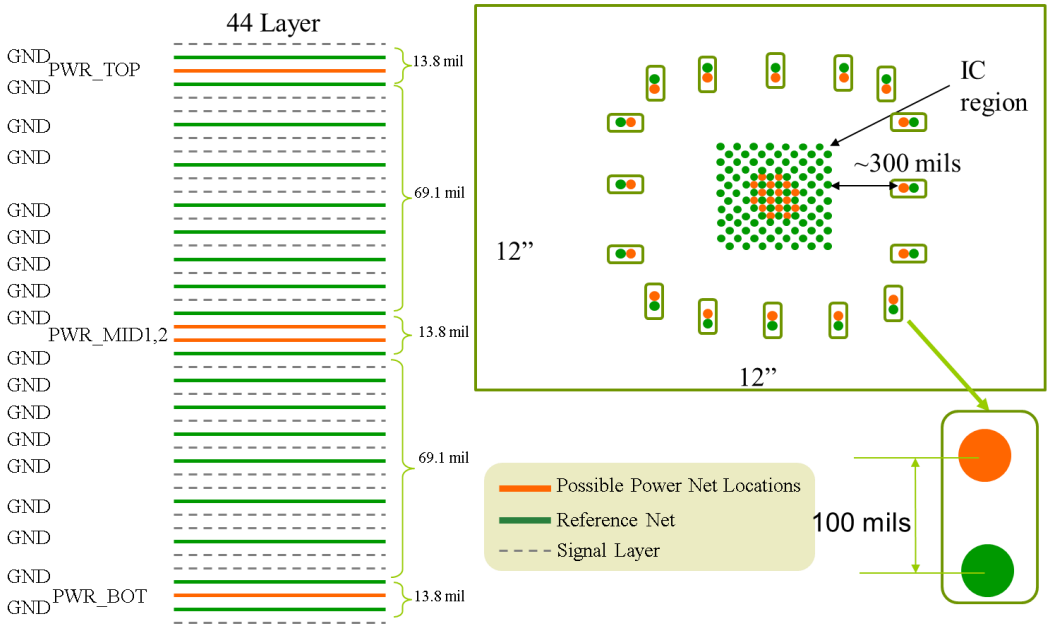
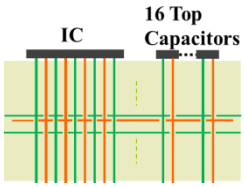
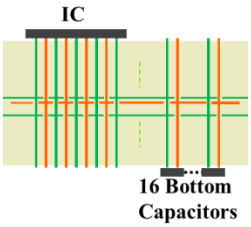
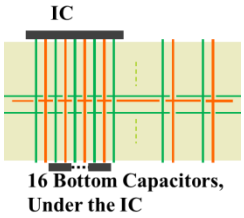
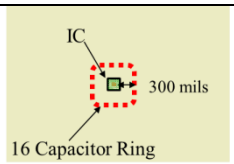
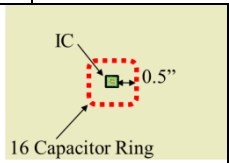
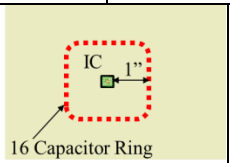
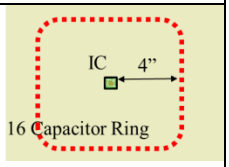
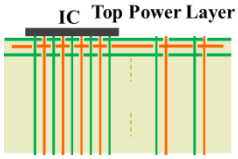
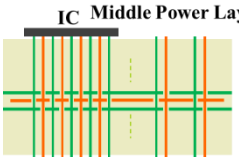
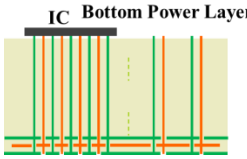
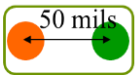
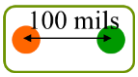
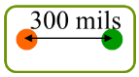
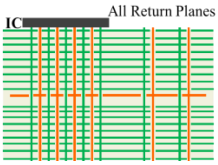
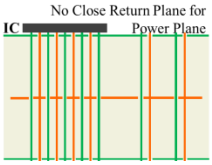
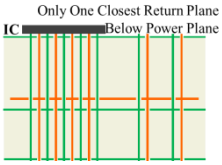


Figure 4.4. Stack up and layout of the reference geometry.

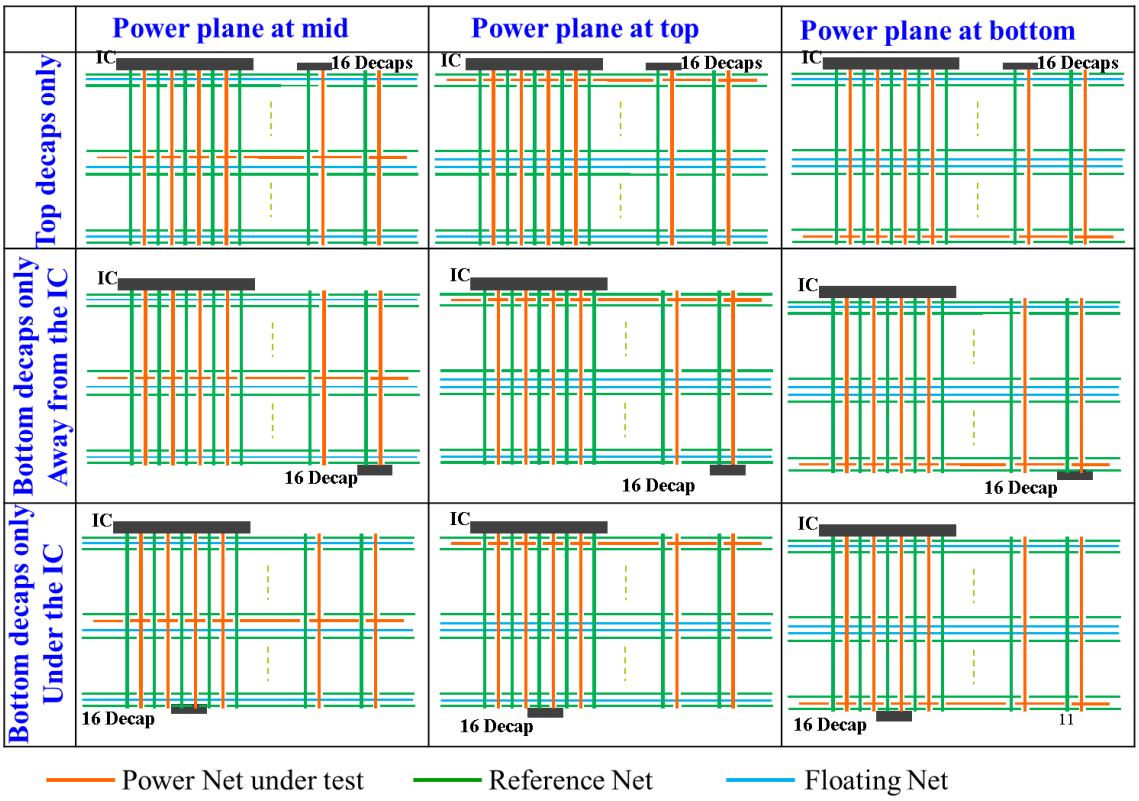
4.1.1. Case 1: Capacitor Placement. The capacitor location case has capacitors placed on top layer at 300 mils, or at the bottom layer at 300 mils, or at the bottom layer sharing the IC vias, as shown in Figure 4.5(a). The three capacitor placement options can be considered for three power plane locations, namely top, middle and bottom.

Table 4.1. Factors and variations used for the case study

Factors	Variation 1	Variation 2	Variation 3 …
Capacitor Location			
Capacitor Distance				
Power Plane Location			
Return Via for Capacitor			
Return Planes				

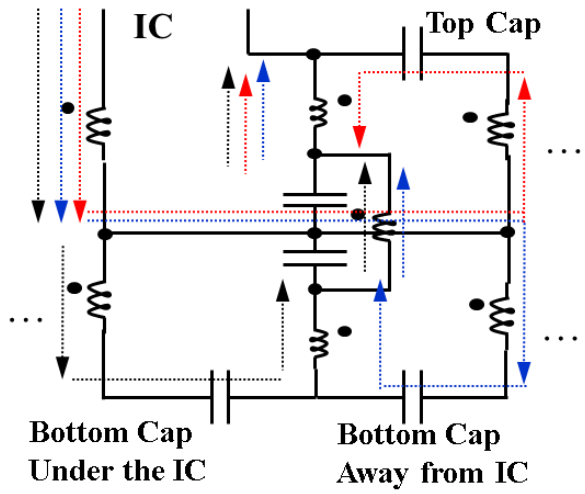
Circuit models and response comparison for the capacitor placement case are shown in Figure 4.5b and Figure 4.5c. The model shows the current paths for three cases in dotted lines, and the response comparison with corresponding colors, red – top capacitor, blue – bottom capacitor and black for bottom capacitor under the IC. The model element values are proportional to the dimensions of the geometry. For the top power plane case, L_{EQ} would be the lowest for the top capacitor placement. Both other placements will have long vias in current path, making L_{EQ} larger. For the power plane at the center of the stack up, the capacitors, placed at the top or bottom, would show L_{EQ} current path almost the same except for the effect of some mutual terms between the IC

vias and the top decoupling capacitor vias. Practically, they should have the same L_{EQ} if the capacitors are far enough. L_{EQ} for capacitors placed under the IC at the bottom layer of the PCB, would have a smaller value as the current does not have to travel along the planes for this case. For the power planes placed near the bottom of the PCB, the capacitors at the top would have the longest current path for L_{EQ}. The capacitor placed at the bottom of the PCB, both, away from IC and under the IC, would have a similar L_{EQ} except that when the capacitors are under the IC, there is no current along the planes, reducing the L_{EQ} further.

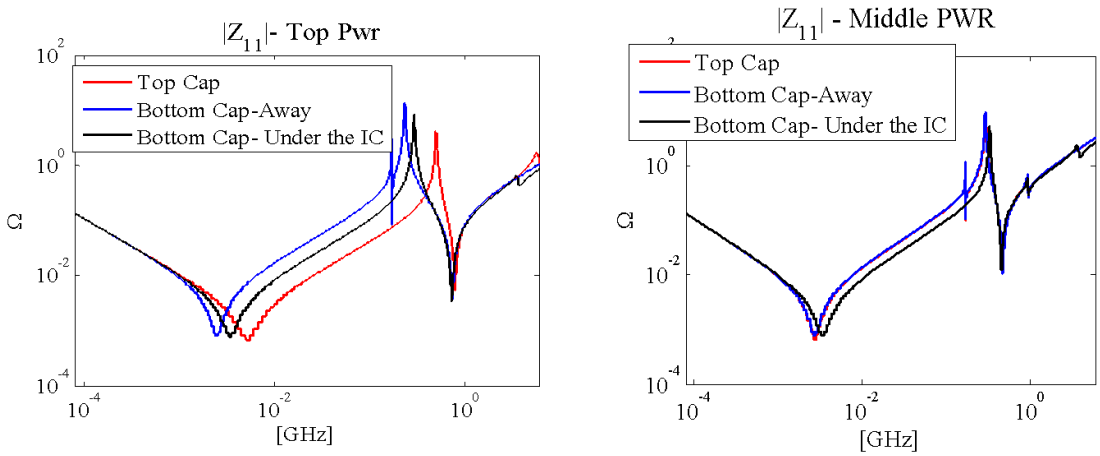


(a)

Figure 4.5. (a) PCB Capacitor placement at top, bottom away from IC, and, bottom under the IC for power plane location near the top, middle of bottom of PCB, (b) Circuit model with the current paths illustrated for three capacitor placements, (c) PDN impedance comparison for three capacitor location when power plane is at the top and middle of the PCB.



(b)



(c)

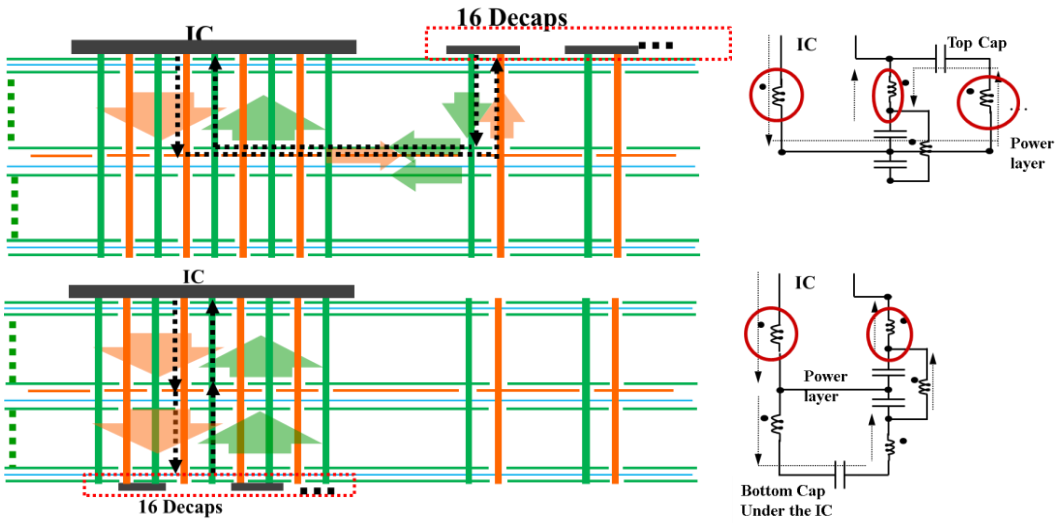
Figure 4.5. (a) PCB Capacitor placement at top, bottom away from IC, and, bottom under the IC for power plane location near the top, middle of bottom of PCB, (b) Circuit model with the current paths illustrated for three capacitor placements, (c) PDN impedance comparison for three capacitor location when power plane is at the top and middle of the PCB. (cont.)

L_{IC} is dependent on the current from the IC pads to the power planes. As each comparison is for a fixed location of power plane, all three capacitor locations show the same L_{IC}. This supports the observation that L_{IC} is independent of capacitor location. The change in L_{IC} with power plane location in the stack up is studied in the following cases. Above analysis suggests that, to achieve a lower L_{EQ}, the capacitors are best placed closest to the power planes.

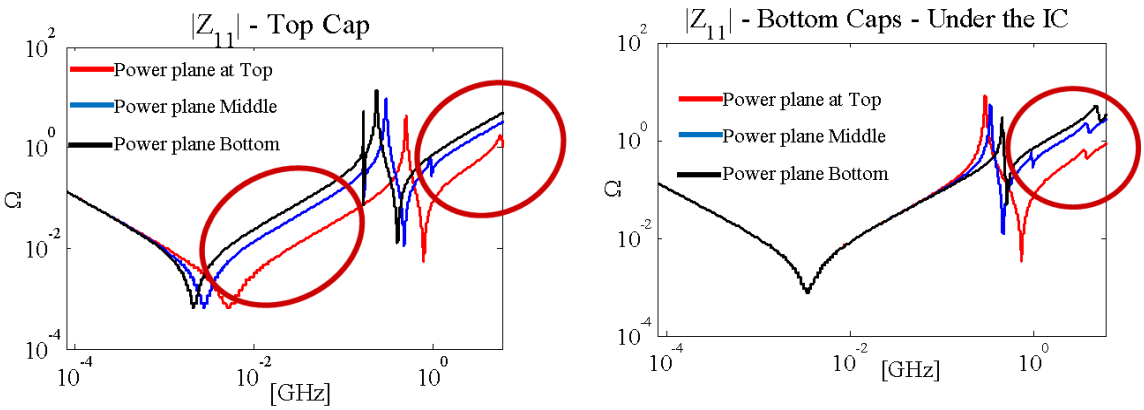
4.1.2. Case 2: Location of the Power Planes in Stack Up. The Figure 4.6(a) shows the geometries used for effect of location of power planes in PCB stack up. The three options explored are near the top, near the bottom, and near the center of the PCB stack up. From the circuit model in Figure 4.8b, the effect of the location of the power planes on L_{EQ} is more meaningful for a fixed location of the capacitors. L_{EQ} is the affected the most for the capacitor placed on the top layer of the PCB, and the power plane location is changed. Here, the current path influencing L_{EQ} will have to reach the power plane from the IC and come back up to the top. For capacitors placed under the IC, sharing the IC vias, the path to the capacitor does not change with the location of power plane, so no change in L_{EQ} is expected. For L_{IC}, the location of capacitors would not matter, but the location of the power plane significantly impacts the L_{IC}. The Figure 4.8c shows the response comparison for different location of the planes.

The power plane location in the stack up will affect the L_{IC} significantly. L_{EQ} is also affected, provided the capacitors are not placed under the IC. The power plane is best placed closest to the IC to get a small L_{IC} and small L_{EQ} except for the capacitors placed under the IC.

4.1.3. Case 3: Capacitor Distance. Case 3 geometry variations are shown in Figure 4.7(a). The capacitors around the IC are moved from 300 mils to 4” with some intermediate steps. The corresponding circuit model is shown in the Figure 4.7(b), where the power vias are represented by 2 inductors to represent the via part and the power-power return cavity part. Though the model can be reduced further by combining the 2 inductors, the break-up is essential to explain the physics.



(a)



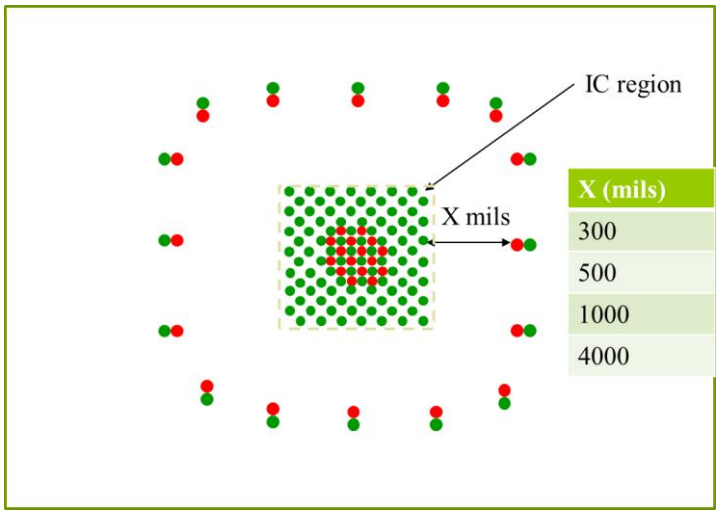
(b)

Figure 4.6. (a) Current paths and corresponding circuit models for the capacitor placement on top and under the IC, with the elements in the model which depend on the location of the power plane in the PCB stack up are indicated. (b) PDN impedance comparison between different power plane locations in the stack up, for two capacitor locations, with the associated differences corresponding to the circuit elements highlighted in (a).

As the distance of the capacitors from the IC increases, the contribution to the inductance from the power plane current increases and the mutual inductance between IC vias and capacitor vias decreases. The inductance in the power plane is proportional to the power-power return cavity thickness. When the power layer is near the center of PCB

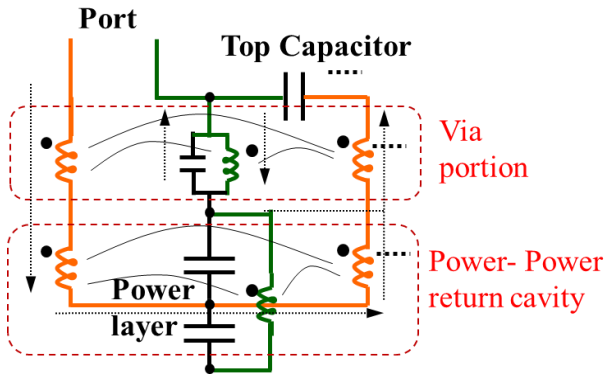
stack up, with the power cavity thickness small compared to the depth of the power plane in the stack up, the contribution from the currents in the power cavity is very small compared to the inductance in the vias. Then the increase in L_{EQ} due to increase in distance is small. The response, shown in the Figure 4.7(c), shows a small difference in L_{EQ} for the power layer near the center of the PCB stack up, as L_{EQ} is dominated by the inductance in the vias for the IC and the capacitors.

The inductance from the current on the power and power return planes depends on the power cavity thickness, and the pattern of capacitors around the IC. For very thin cavities and the capacitors placed around the IC in a ring, the inductance is very small and distance between the IC and capacitors will not show significant difference. When the power cavity thickness is comparable to the distance of IC or capacitors from the power planes in the stack up, or the placement of capacitors in not in a ring around the IC to spread out the power and return current, the capacitor to IC distance will be important, provided the capacitor via pair spacing is small to contribute less inductance compared to the power – power return cavity.

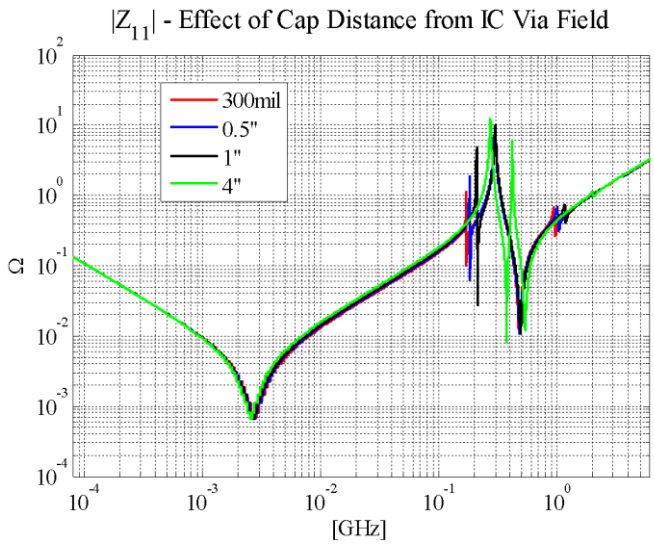


(a)

Figure 4.7. (a) PCB top view with the IC region and capacitors placed in a ring around the IC at a distance which varies as from 300 mils to 4” (b) Circuit Model for the geometry in (a) with the inductor element split in via portion and power cavity portion, that is affected by the capacitor distance (c) PDN impedance comparison for different capacitor distances with the power plane located near the center of PCB, shows very little change with capacitor distance, for the power cavity placed at the center of PCB stack up.



(b)



(c)

Figure 4.7. (a) PCB top view with the IC region and capacitors placed in a ring around the IC at a distance which varies as from 300 mils to 4" (b) Circuit Model for the geometry in (a) with the inductor element split in via portion and power cavity portion, that is affected by the capacitor distance (c) PDN impedance comparison for different capacitor distances with the power plane located near the center of PCB, shows very little change with capacitor distance, for the power cavity placed at the center of PCB stack up. (cont.)

4.1.4. Case 4: Effect of Power Return Via Distance from Capacitor Power Via.

The capacitor connects to the power plane and all return planes using two vias, one for each net. The distance between these vias significantly affects the mutual inductance between the vias, and also the distance that the return current travels around each return

plane, as shown in Figure 4.8(a). The power plane is considered at the center of PCB stack up, and the capacitors are located at the top layer. The return via distance from the power is varied from 50 mils to 300 mils. When the distance is 300 mils, the IC's current return vias are used instead of a dedicated return via for each capacitor. The circuit model is shown in Figure 4.8(b). The change in the return via location will change the inductance value for return via, and the mutual inductance between the power and the power return vias of the capacitor. As the return via associated with each capacitor moves away from the power via, the return current path inductance going on increasing, thus increasing L_{EQ}. The return current path for the current through the capacitor does not contribute to the L_{IC}, so it remains the same. The response comparison in Figure 4.8(c), shows the change in L_{EQ} and no variation in L_{IC}. A return via should be placed for every capacitor as close as possible to the power via of the capacitor.

4.1.5. Case 5: Effect of Return Planes in Stack Up. The Figure 4.9(a) shows the geometry variation for this case. The original geometry has the stack up as shown in Figure 4.3, with the power plane placed near the center of PCB stack up. The next geometry has all return planes removed except the top-most and bottom-most. Then two more geometries are formed by adding one closest top and bottom side return planes in second geometry. The objective is to see the effect of all other return planes, as compared to the closest return planes. Two placements of capacitors are used, the top layer around the IC and at the bottom under the IC, for all stack up variations. The change in geometry will change the return path of the power current for the L_{EQ}, and L_{IC}. For the top capacitor placement, the part of the current along the power- power return cavity is affected by the geometry variation. In the geometry with no other return planes except the top most and bottom most ones, the return current forms a big loop, as the power-power return cavity itself is so big. For the remaining cases, atleast one return plane is placed close to the power plane, will have a thin power-power return cavity. In these two cases with a close return plane, the case with closer return plane will have smaller inductance and hence smaller L_{EQ}.

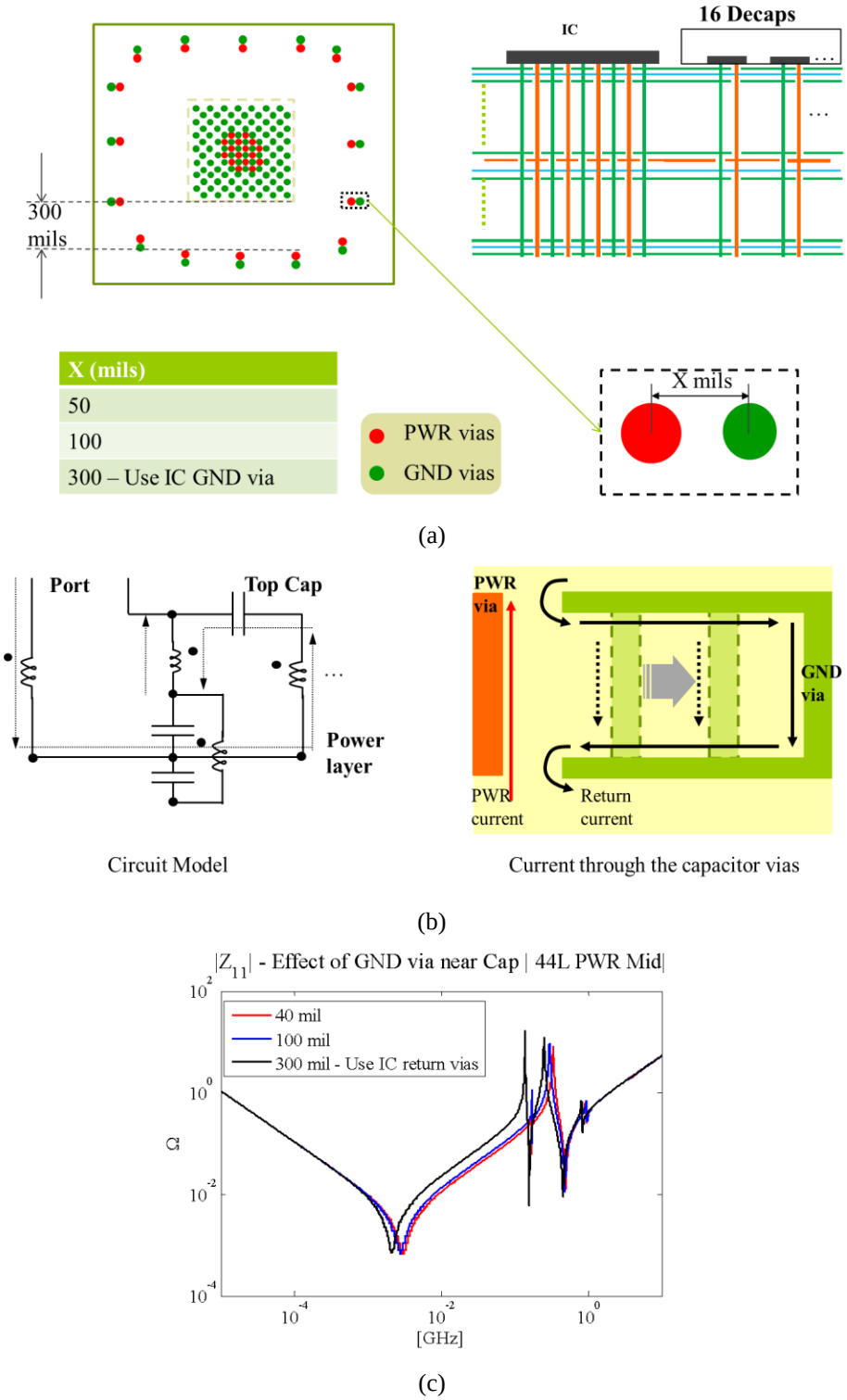
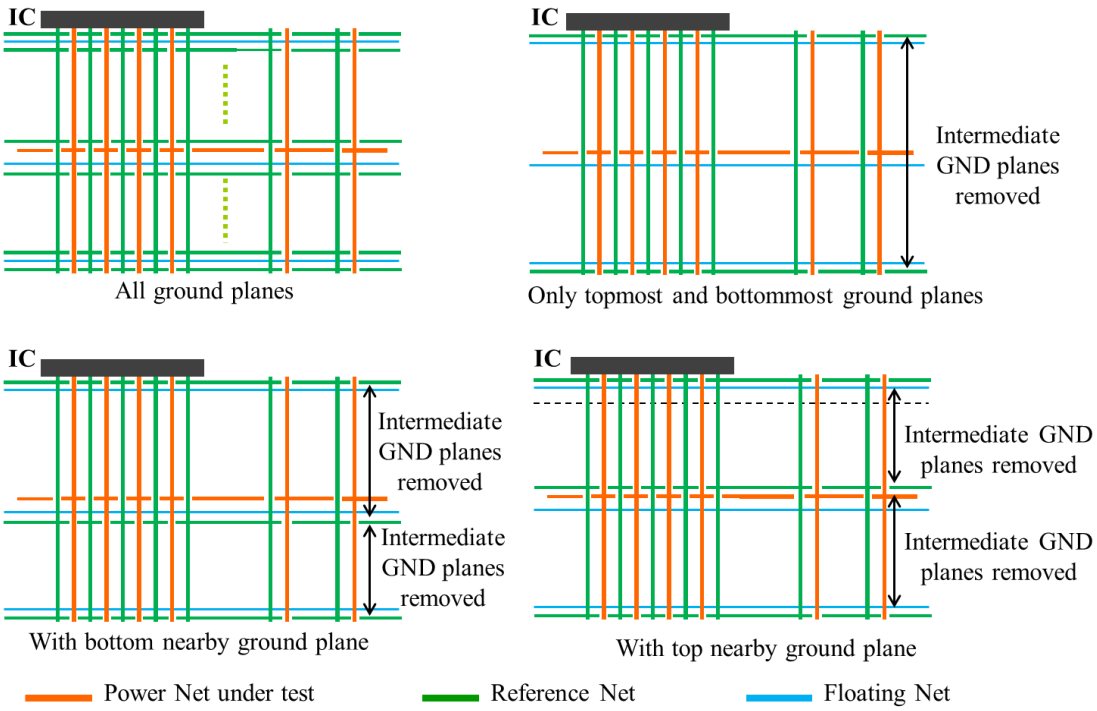


Figure 4.8. (a) Capacitors placed at the top of the PCB around the IC at 300 mils, with distance between the capacitor vias is changed 40 mils to 300 mils. (b) Circuit model and current path for the capacitor via pair, shows increase in return path inductance and decreasing mutual inductance between the capacitor via pair. (c) PDN impedance comparison as the return via of the capacitors is moved away from their power via.

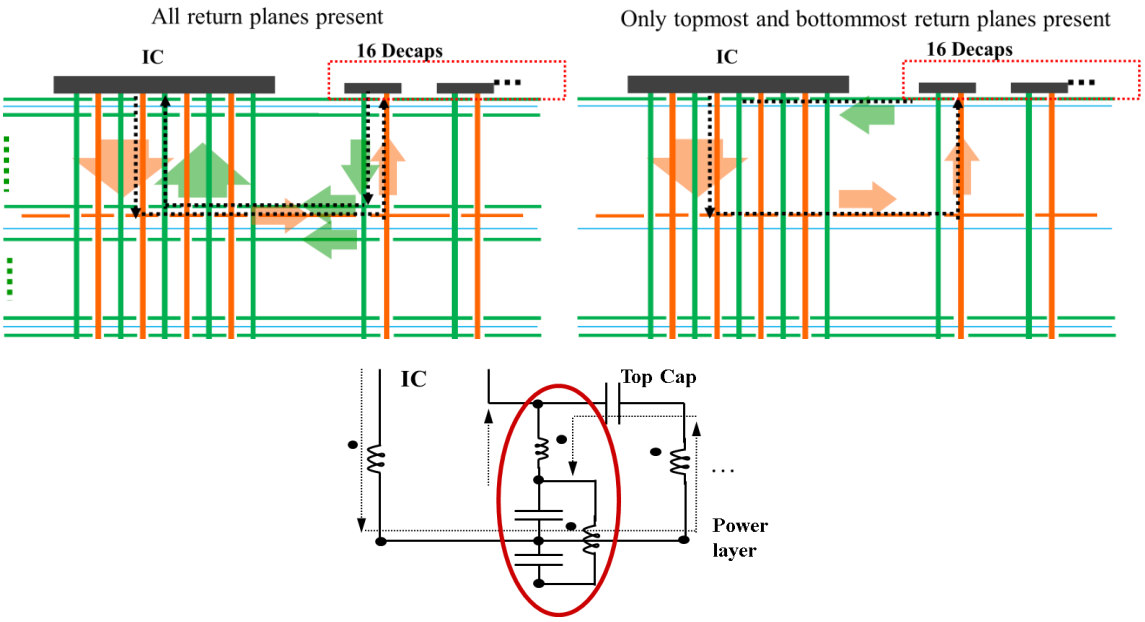
For bottom layer capacitor placement, under the IC, return current does not use the power return plane, so the L_{EQ} should not change for the return plane variation. As the current contributing to the L_{IC} is from the IC to the power –power return plane pair and back, its thickness does affects the return current. In the geometry with only topmost and bottom-most return planes, the power current is only on the power vias, and return current on the topmost return planes. The L_{IC} increases with the increase in thickness of power-power return cavity for a fixed depth of power plane in the stack up, as a greater part of the current on power vias does not have a close return current path on neighboring vias.

The circuit model shown in Figure 4.9(b), has two nodes representing the return planes above and below the power plane. As the geometry changes, the value of the elements, connecting these nodes to the topmost return plane node and bottom-most return plane node, will change in value. Also, the mutual inductance, between the return via inductor and power via inductor is proportional to the length of the return net via carrying the return current (upto the closest return plane from the power plane). As the closest return planes move away from the power plane, the mutual inductance reduces proportionally, increasing the L_{EQ} and the L_{IC}. The response, shown in Figure 4.9(c), shows the difference in the L_{EQ} and the L_{IC}, for the variation in the power- power return cavity. For capacitors placed on the top layer, L_{EQ} and L_{IC} are highly dependent on the closest return plane. For the capacitors placed on the bottom layer under the IC, the L_{IC} is dependent on closest return plane, but L_{EQ} is not affected by it.

The closest return plane influences the return current path, and affects the entire response. A power plane should always have a return plane on a neighboring layer in the stack up. The dielectric between the power and power return layers, should be as thin as possible.

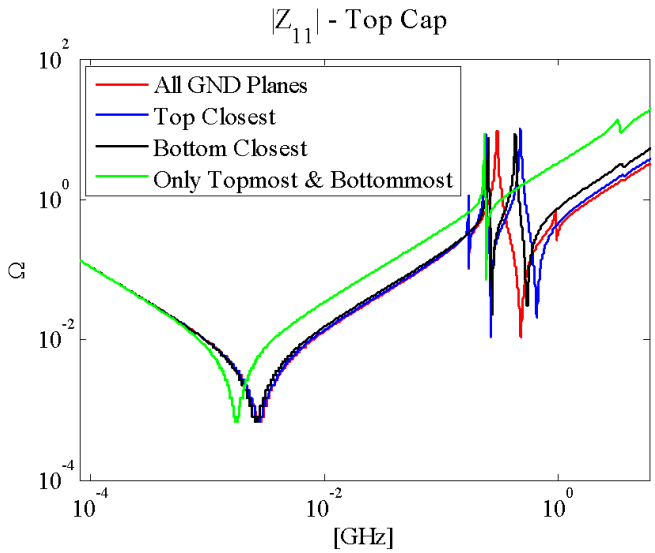


(a)



(b)

Figure 4.9. (a) Geometry variation for studying the effect of return plane in PCB stack up. (b) Current paths for two extreme variations in return planes, and the circuit model highlighting the elements representing the return current path. (c) PDN impedance comparison for geometry variation in (a), shows that a closer return plane will provide a low inductance return path.



(c)

Figure 4.9. (a) Geometry variation for studying the effect of return plane in PCB stack up. (b) Current paths for two extreme variations in return planes, and the circuit model highlighting the elements representing the return current path. (c) PDN impedance comparison for geometry variation in (a), shows that a closer return plane will provide a low inductance return path (cont.)

4.2. DESIGN TRENDS FOR STACK UP VARIATION

The case study conclusions developed in the previous section are for the stack up with 44 layers and specific thicknesses of the board and the power cavity. These values may influence the conclusions of the case study, so there is a need to generalize the results to be used for a range of board thicknesses, or layer counts. One way to generalize the results is to run simulations for a range of board thickness or depth of power plane in the stack up. The original nature of the stack up is preserved with three options for the power plane locations, and close return planes for each location. The trends in L_{EQ} and L_{IC} are observed, which summarize the PDN impedance trends and are useful in making design decisions.

The Figure 4.10 shows the stack up used, indicating the depth h_1 for the power planes and the power-power return cavity thickness h_2. The depth can also be normalized

to the power cavity thickness, which helps in some cases to observe the tradeoff between the contributions from different parts of the geometry.

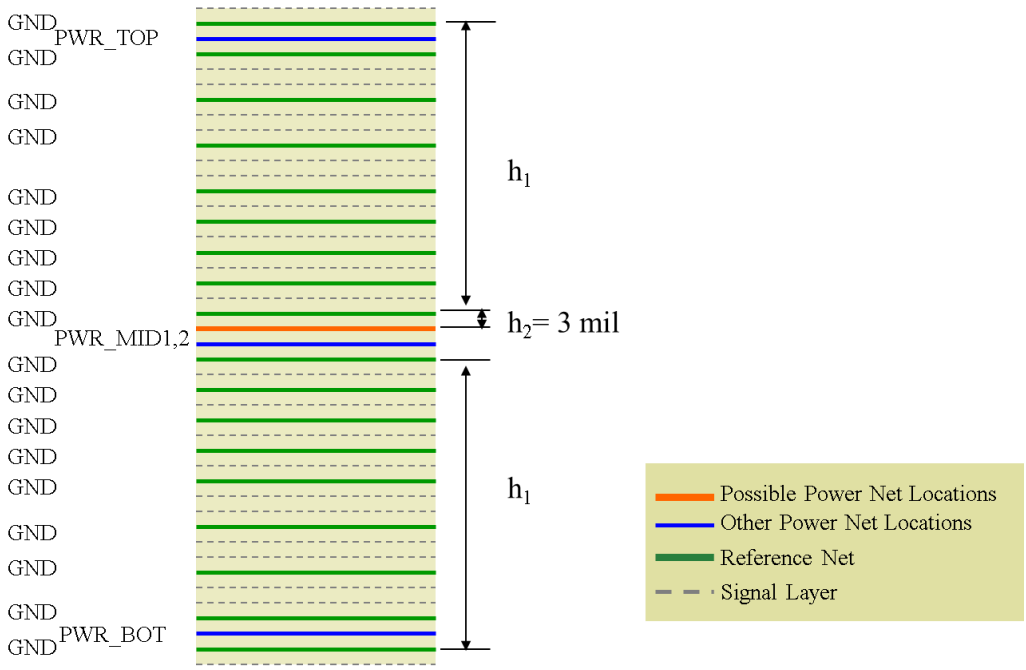


Figure 4.10. Stack up with power plane depth h_1 and power cavity thickness h_2.

The capacitor locations on the board affect the L_{EQ} feature of the PDN impedance. Figure 4.11 shows the L_{EQ} for the different capacitor locations, plotted for a range of PCB thicknesses while keeping the power plane near the center of the stack up. The power-power return cavity thickness, h_2, is 3 mils and h_1 takes values in the range 0 to 120 mils. As the power plane is deeper in the PCB stack up, the L_{EQ} value goes on increasing linearly with the same slope in case of top or bottom capacitor away from the IC. When the capacitors are placed under the IC, the increase in L_{EQ} is linear but with a smaller slope. This is due to the different contribution to L_{EQ} of the IC vias as compared to the capacitor vias. The deeper the power planes are placed in the PCB stack up, the greater is the L_{EQ}, but the increase is slower for capacitors placed at the bottom under the IC. Capacitors placed under the IC perform better than the capacitor on the bottom away from the IC.

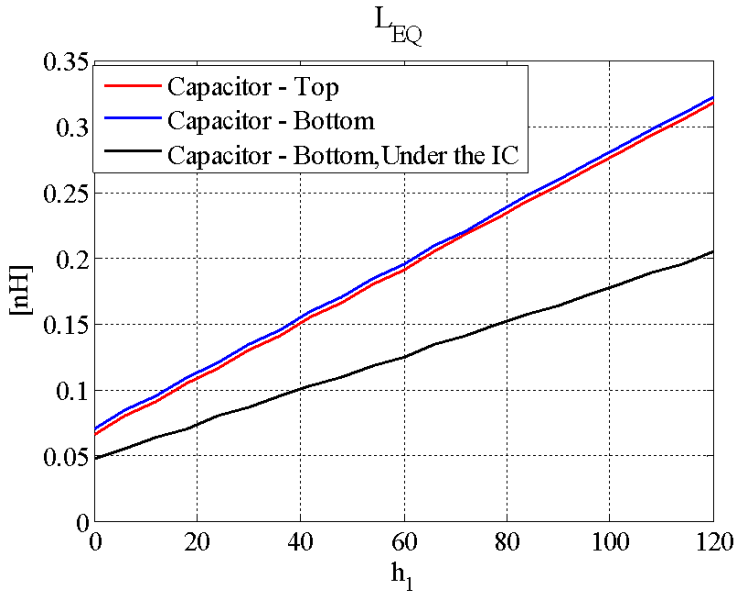


Figure 4.11. L_{EQ} for different capacitor locations vs the depth h_1 of the power plane in the PCB stack up.

The Case 2 in the case study shows the effect of varying power layer depth in the PCB stack up using three locations in a fixed stack up. The location power layer affects the L_{EQ} and the L_{IC}, but L_{EQ} also depends on the capacitor location. The effect of stack up variation for different locations of capacitor was seen in the Figure 4.11. Figure 4.12 shows an increase in L_{IC} with the increase in depth, h_1, of power planes in the stack up, for 16 IC power vias placed in an alternating pattern with return vias, with a pitch of 1 mm, as seen in Figure 4.4. The increase in L_{IC} is linear with the depth of power planes. The slope depends on the number of IC power vias and the patterns of placement.

The power plane should be as close as possible to the IC, to have a small L_{IC}. The PDN impedance has a pole between the package capacitance and a combination of the package inductance and L_{IC}, as seen in the Figure 4.2. Thus it is important to control the value of L_{IC}.

The effect of change in capacitor distance from the IC was seen for a fixed stack up in Case 3 of the case study. The results suggests that if the power cavity is thin, there is a small contribution to the L_{EQ} from the plane currents, then the increase in distance of

capacitor from the IC will not show significant increase in L_{EQ}. The Figure 4.13 shows the L_{EQ} from the Case 3 for a range of power plane depth in the stack up.

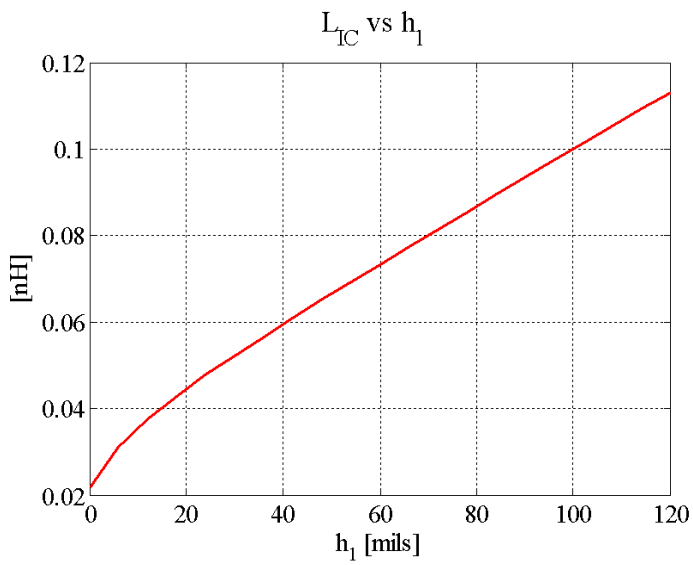


Figure 4.12. L_{IC} vs the depth of power layer (h_1) in the stack up, for 16 IC power vias placed in an alternating pattern with the return vias with 1 mm pitch.

As the power planes go deeper in the stack up, the change in L_{EQ} due to change in capacitor distance, becomes less significant as the inductance in the vias connecting the capacitors and IC to the power plane will dominate the L_{EQ}. When the planes are close to the capacitor side, the distance between IC and capacitors is important, but if the power plane is deep in the PCB stack up compared to the power cavity thickness, then the distance between IC and capacitors will not cause a significant difference. Work is in progress to quantify the exact contribution of the current on the planes and in the vias in a cavity, to understand the trends further.

Case 4 shows the effect of the capacitor via spacing, which affects the L_{EQ}. The return via spacing of capacitor controls the mutual inductance between the vias carrying currents in opposite direction. The mutual term will reduce the overall inductance from the capacitor vias. Also, the return current path on the return planes also increases with spacing, shown in Figure 4.8(b). As the length of the capacitor vias carrying the power

and power return currents increases, the significance of spacing between the via pair increases for L_{EQ}. This is seen in Figure 4.14, showing L_{EQ} plotted vs power plane depth for 16 capacitors placed on the top layer, for different via spacing in capacitor layout.

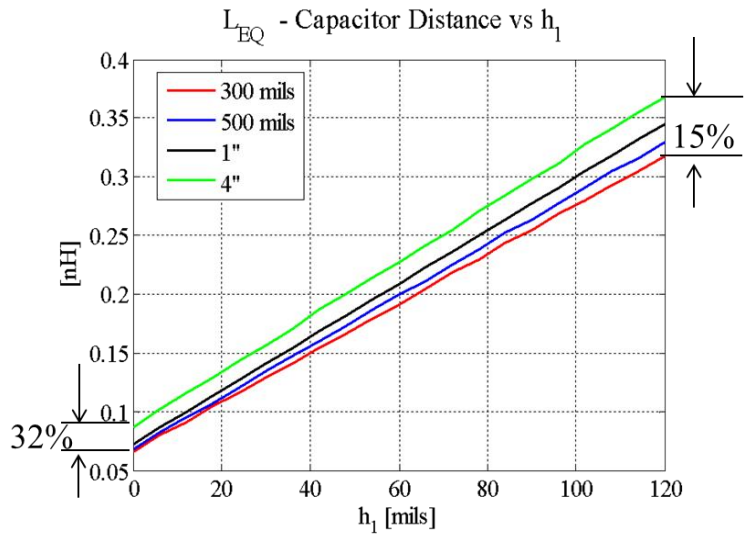


Figure 4.13. L_{EQ} vs power plane depth in stack up, for different capacitor distances from IC when capacitor are placed on top, shows the capacitor distance becomes less significant as power plane is away from capacitor, 32% to 15 % with respect to L_{EQ} 300 mils placement.

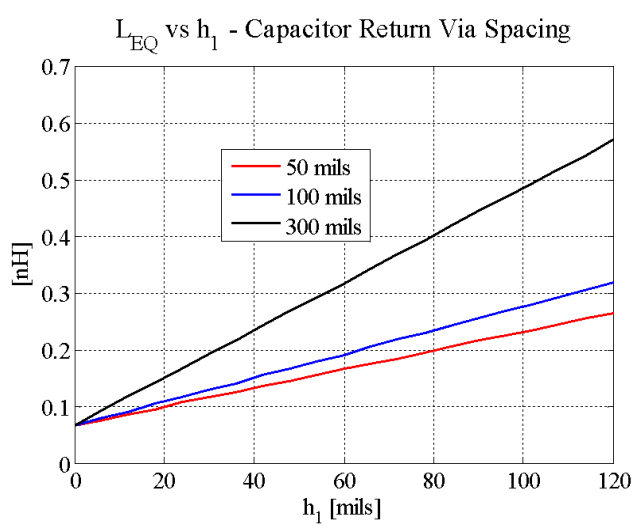


Figure 4.14. Effect of capacitor via spacing on L_{EQ} as the depth of power plane increases.

4.3. CONCLUSIONS

The guidelines developed in this paper are derived from a physics based modeling approach. They facilitate the analysis in the impact of a design decision on the PDN response using a simplified circuit model. This fast and accurate approach provides better decisions in early design phase, without having to run a complete full wave simulation.

The five case studies, presented in this paper, provide simple guidelines for a PDN design which can be summarized as follows:

- Place the power layer as close as possible to the IC.
- Place the capacitors on the side closer to the power plane. The placement of capacitors at the bottom under the IC, sharing IC vias, is the best placement, except for thick boards with power layer near top of PCB.
- There should be a return plane placed as close as possible to the power plane. As the cavity thickness increases, the inductance contribution in all frequency ranges increases.
- Every capacitor should have a return via placed close to the power via.
- The capacitor should be placed close as possible to the IC, but as the power cavity gets thinner, these can be placed further away from the IC without causing a very significant increase in equivalent inductance.

The pattern of capacitors can be optimized to lower the L_{EQ}. As studied in [30], the pattern can affect the results when the capacitors are placed close to each other.

Though the guidelines are simple, a real board design does not have enough space or layers to provide the best possible geometry for all power nets, and this leads to trade-offs in important geometry features. The paper provides an analysis of the trends in key response features, for the possible variation in geometry. These trends help to understand the significance of change in geometry, and allow the designer to make a compromise without having a big impact on the final response of the multiple power nets.

5. PDN DESIGN METHODOLOGY USING AN EQUIVALENT INDUCTANCE CONCEPT FOR MID-FREQUENCY PDN INPUT IMPEDANCE

5.1. INTRODUCTION

Power distributions networks (PDNs) in a printed circuit board (PCB) consist of the voltage regulator module (VRM) connected to the integrated circuit (IC) through a set of power and return planes, which have several decoupling capacitors connected along the way. The decoupling capacitors, referred to, in this paper, as ‘decaps’, are used as charge storage units which can be classified into two groups, local decaps and bulk decaps. The local decaps are meant for faster charge delivery and the bulk decaps for slower charge delivery but carry far more charge.

The IC requires the PCB PDN to deliver enough charge to satisfy the current draw requirements which arise from the switching currents in the IC. As the switching currents depend on the data rates used in the digital system, it may be in several GHz or several hundred MHz frequencies. The quick charge delivery local decaps have to be enough to meet the requirement at higher frequencies, and the bulk decaps replenish the local caps and/or satisfy the requirement at lower frequencies. If the charge delivery requirements are not met, a voltage ripple is created on the voltage rails which may propagate through the planes and cause electromagnetic interference (EMI) issues, or couple to signal nets leading to signal integrity (SI) issues.

A PCB PDN design is evaluated based on the input impedance, as seen by the IC looking into the PCB PDN. This provides a measure of the voltage ripple generated for a current draw at the IC, with lower ripple voltage for lower impedance profiles for the same current draw. Decaps are used as tools to reduce the impedance in different frequency ranges, where these decaps are active.

Decaps are limited in speed of charge delivery (frequency range) by the series inductance in the current path, from the IC to the decap, and back. As the frequency increases, the decap’s series inductance dominates over its capacitance in terms of impedance. Thus at higher frequencies the impedance looking into the PCB PDN, is dominated by the series inductance of the local decaps. The decaps are said to be

ineffective at higher frequencies where the impedance they offer is very large, so no charge can be delivered from it at those frequencies.

Several studies about decap placements and effectiveness have been done in the past for two or four layer boards which have a single plane pair of power and return nets. As the digital systems move to higher complexity with more functionality and number of channels, the number of layers in the PCBs has to increase to accommodate the routing. For such multilayered PCBs, the topology of the PDN is also significantly modified, as new variables or design choices are introduced in terms of location of power layer in the stack up and relative thickness of power cavity. Several case studies have been presented to understand the impact of the design choices in multilayered PCBs, on the overall response. These provide some insight into the broad range of design decisions and their general impact, thus leading to many guidelines for the designers. Due to the complexity of the system and higher priority to channel routing, PDN design or capacitor placement is done using the space left over after routing choices have been made. The placement decisions are generally made by guidelines or previous experience. Hence, a mature PCB PDN methodology with well-defined steps is yet to be developed.

As a step towards developing a sound methodology in PDN design, the effect of number of capacitor placed in certain patterns is shown in [33]. It was shown that the equivalent inductance, L_{EQ}, when the decaps are effective, can be broken down into three portions. These components are, the contribution of connection of the decaps, L_{Decap}, the contribution from the power and return cavities, L_{Planes}, and the contribution from the IC connection to the power and return cavities, L_{IC}. The results show illustrate how the equivalent inductance converges to the L_{IC} value as the number of capacitors is increased in a pattern.

As an extension to [33], analytical expressions are derived, herein, for the convergence of the individual components of L_{EQ}, namely, L_{Decap} and L_{Planes}. The inductance for the vias and planes is extracted using the formulation in [23], which is based on the cavity model [24]. This provides a solution contribution from the via and plane currents in a cavity. Several practical capacitor patterns are considered for L_{Decap} and L_{Planes}, including the ones in [33]. The analytical formulations are put together to find the L_{EQ} convergence for a particular pitch size, number of IC power vias, and, a particular

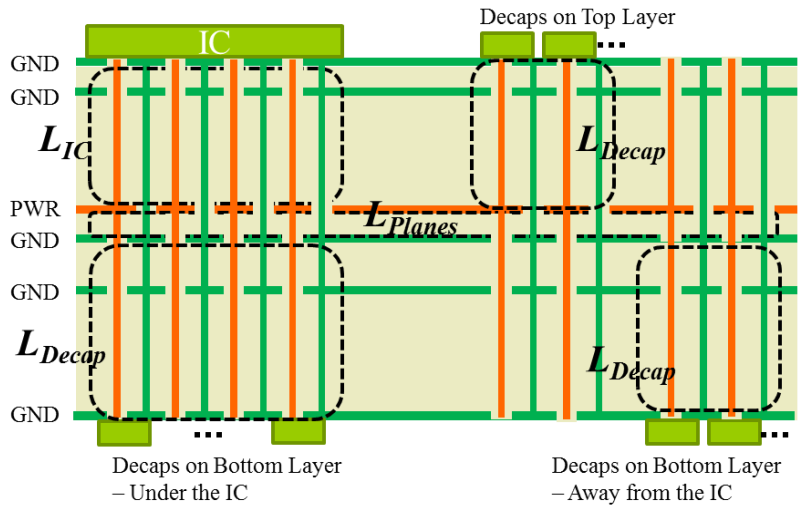
stack up. This will enable the designer to analytically quantify the number of capacitors, based on a convergence criterion.

The main contributions from this paper are the analytical formulas derived for the convergence of equivalent inductance, which help calculate the required number of capacitors for each power net. The expressions are account for variable stack up and via pitch sizes, thus can be used for a vast majority of general PDN designs. This completes an important step in the design methodology for the multilayered PCB PDN design, choosing pattern and number of decaps. The formulas also help find a lower limit for L_{EQ}, which is L_{IC}. Thus adding more capacitors cannot improve the performance of the design beyond this limit.

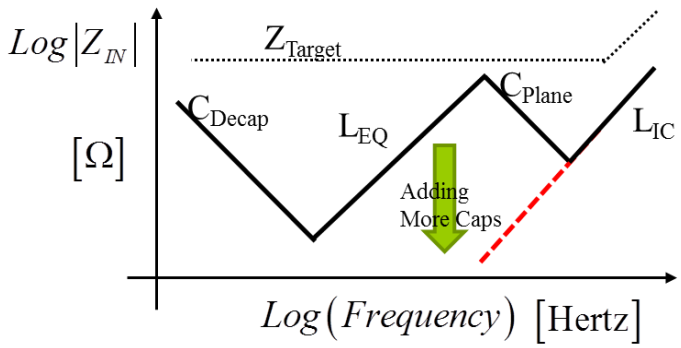
Section II explains briefly two different methodologies to calculate the inductance contribution of the parallel-plate cavity with vias, and then introduces the L_{EQ} concept and how it can be segregated into parts. The different geometry patterns for each constituent part of the L_{EQ} are described in Section III and the results and trends are shown in Section IV. Section V provides some useful discussions about the application of this approach.

5.2. METHODOLOGY

The analysis of a real PCB requires segmentation to divide the board into smaller blocks which can be individually modelled. The segmentation approach requires that there is little or no coupling between the segmented blocks. This restrict our analysis to clever designs where the parts of the geometry belonging to the IC and decaps do not couple strongly. Figure 5.1(a) shows an example of a high layer count stack up and top view of a PCB–PDN with many decaps placed on the top layer around the IC, bottom of the IC and on the bottom layer but away from the IC. Figure 5.1 (b) shows the generic (asymptotic) response for such a PCB-PDN. The circuit model for this geometry can be created using the cavity model approach introduced in [5], where this approach has also been validated with measurements.



(a)



(b)

Figure 5.1. (a) High layer count stack up and top view of a PCB–PDN with many decaps placed on the top layer around the IC, bottom of the IC and on the bottom layer but away from the IC, (b) A generic (asymptotic) response for a PCB-PDN, with target impedance as defines in [32].

The input impedance has two features very critical for the design, the equivalent inductance L_{EQ}, and the IC connection inductance L_{IC} [4]. The equivalent inductance, is the inductance in the power current path from the IC to the decaps, passing through the power planes, and the return current path back to the IC. L_{IC} is the inductance in the current path from IC to the power planes and return current path back to the IC. The connection inductance of the decaps is termed as L_{Decap}, and the inductance contribution of the power/ power-return cavity is L_{Planes}. Thus the L_{EQ} can be expressed as,

$$L_{EQ} = L_{IC} + L_{Planes} + L_{Decaps} + M_{IC,Decaps} \tag{5.1}$$

where, $M_{IC,Decaps}$ is the mutual inductance between the L_{Decaps} and the L_{IC} portion.

The L_{IC} depends on the geometry features in the current path between the IC and the power/ power return cavity. It depends on the number of IC power pins, the IC pin pattern, and the distance between the IC and the power/ power-return cavity. Thus the L_{IC} is independent of the decaps, and does not change with the decaps.

The L_{Planes}, depends on the power/power return cavity thickness, the distance between the IC and decaps, and the number of decaps and their placement patterns, as the current distribution on the planes and the mutual inductance between the vias affects the L_{Planes}. The L_{Decap} depends on the distance between the decap and the power/ power return cavity, the distance between the decap power via and power-return via. If the decaps are placed close together, with power via distances comparable to nearest return via, then their mutual inductances need to be considered, and then L_{Decap} is calculated a lumped contribution instead of individual numbers.

The $M_{IC,Decap}$ are the mutual terms, between the IC vias. It is assumed that the IC vias and decap vias are sufficiently apart to neglect the mutual terms between them, except for the power/ power return cavity, where they are always considered. This is because, the power/ power return cavity has current only on the power via or the power-return via, and not both. Whereas, in the geometry corresponding to the L_{IC} and the L_{Decap}, the power and power-return vias, placed close together, carry equal and opposite currents, so the mutual inductance with vias placed further apart is not significant.

The L_{EQ} contains L_{IC}, which is independent of the decaps. Thus, LIC is the lowest value that L_{EQ} will converge to if the L_{Planes} and L_{Decap} terms can be minimized by the decap number and placement. Thus, the dependence of L_{Planes} and L_{Decap} on the number of decaps is studied for individual placement patterns. The rate of convergence depends on how the mutual inductance between the vias contributes in L_{Planes} and L_{Decap} calculation, as studied in the next section.

5.3. CAPACITOR PLACEMENT PATTERNS

To find the number of capacitors required for a PDN to achieve optimal performance, the individual parts of L_{EQ} have to be optimized. Various geometry patterns are introduced in this section, to span the design space of the generic geometry and observe the trends in each of L_{IC}, L_{Planes} and L_{Decap}.

5.3.1. IC Via Patterns. The IC vias occur on a grid, with a specific pitch size. The number of IC power pins and the pattern is controlled by the package designers or IC designers but is still shown here for completeness. As LIC is the lowest value that LEQ can achieve, it is recommended to minimize LIC before other components of LEQ. Two test patterns are used and some might be similar to [12], alternating pattern, and grouped pattern, as shown in Figure 5.2. The IC vias are placed on a grid of 1mm pitch. For each pattern the effect of number of IC power pins is studied while maintaining the same IC pin pattern and the results are shown in the next section.

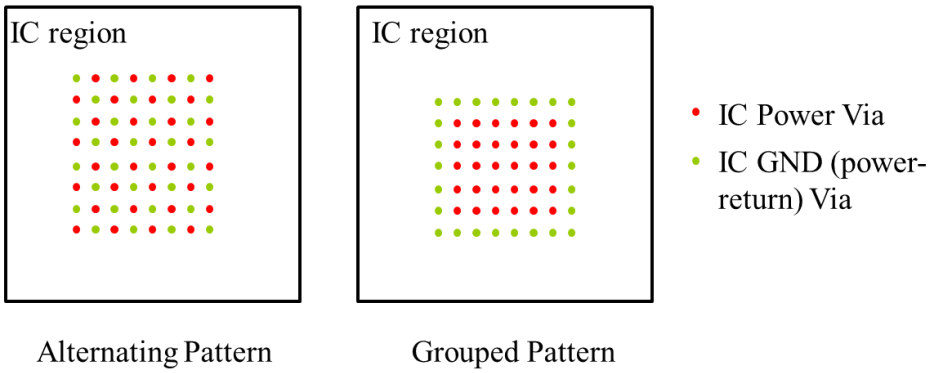


Figure 5.2. The power and power-return net via maps used in the alternating pattern, and grouped pattern for the L_{IC} calculations.

5.3.2. Decap Placement Pattern. Three decap placement patterns are used, as shown in Figure 5.3, the Arc, the Row and the Grid placement, where the decaps are placed along a ring, in a row and clumped together, respectively, at a distance D from the IC edge. The decaps use a footprint with the power and power-return vias 100 mils or 2.5 mm apart, so the grouped decap placement has the decap grid pitch of 2.5 mm. Decaps

vias can be placed in regular or alternating order as shown in the Figure 5.3(b). The via patterns can be used to take advantage of the mutual inductance between opposing currents compared to same direction currents. The convergence of the equivalent inductance with the number of decaps will be dependent on these mutual term contributions and in turn on the patterns used.

Decaps can be placed at one of four distances from the IC center, 0.5”, 1”, 2” and 3”. Usually it is difficult to use the space close to the IC edge for decaps as it would limit the signal break out region around the IC, forcing the designer to place the decaps away from the IC. A combination of the distance, the number of decaps and the pattern are used to find trends in convergence for L_{Planes}. The L_{Planes} will also change with the number of IC power pins and so 1, 4, 16, and 32 power pins are used. The L_{Decaps} on depends on the pattern, and the number of decaps. The trend in L_{Planes} with the number of decaps and the number of distances is shown in the next section.

5.4. ANALYTICAL SOLUTION TO CONVERGENCE WITH NUMBER OF DECAPS FOR EACH PATTERN

5.4.1. L_{DECAP}. The decap patterns, shown in Figure 5.3, have a difference in the current distribution and coupling to the neighbors, leading to difference in the inductance convergence as the number of decaps is increased. A methodology employed to find L_{Decap} for each pattern is to form unit cells, one for each decap, using the power and return via patterns. Each unit cell consists of one decap power via and its closest return via. The unit cell is used as an element to write the KVL system of equations as,

$$j\omega \mathbf{L}_{\mathbf{Decap}} \mathbf{I} = \mathbf{V}, \tag{5.2}$$

where,

$\mathbf{I} = \begin{bmatrix} I_1 & I_2 & \cdots & I_n \end{bmatrix}^T$,

$\mathbf{V} = \begin{bmatrix} V_1 & V_2 & \cdots & V_n \end{bmatrix}^T$,

I_k is the current through the kth decap, and,

V_k is the voltage across the decap looking from the power and return cavity.

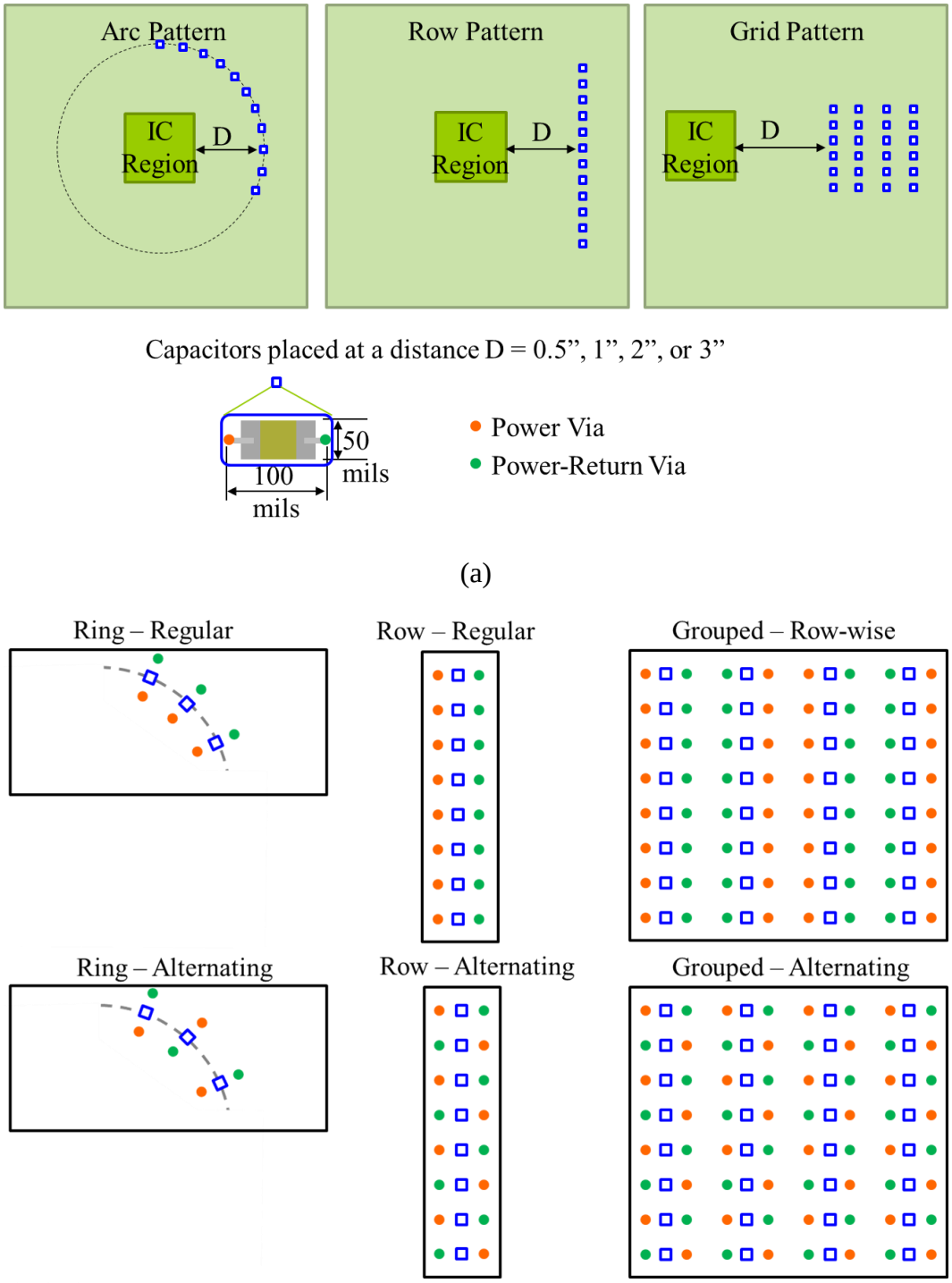


Figure 5.3. (a) Three decap placement patterns, Arc, Row and Grid, with the decaps placed at a distance D from the IC, along a ring, in a row and clumped together, respectively. (b) Via placement options for different

As all the capacitors are connected to the power and return planes, the total current through all the decaps can be used to find the effective L_{Decap} assuming voltages across them are the same. Thus,

$$j\omega L_{Decap} I_{Total} = V_{Decap}, \tag{5.3}$$

where,

$I_{Total} = I_1 + I_2 + \cdots + I_n$, and,

$V_{Decap} = V_1 = V_2 = \cdots = V_n$.

Then, using (5.2) and (5.3), a rigorous relationship can be defined between effective inductance L_{Decap} and the unit cell inductance matrix, $\mathbf{L_{Decap}}$, as,

$$L_{Decap} = \left(\sum_{columns} \sum_{rows} \left[\mathbf{L_{Decap}} \right]^{-1} \right)^{-1}, \tag{5.4}$$

where the only assumption is that the potential difference across each decap via is the same, which is true for the frequencies below the first cavity resonance of the power – return cavity.

The relationship in (5.4) has an inverse matrix operation which will make the formulation very complicated to extract any physics from. The formulation is redone without the inverse for individual patterns, by using the unit cell approach and assuming each capacitor carries the same current. If the inverse can be avoided, then an analytical dependence can be found on the number of capacitors and via separations. For the Arc and the Row placement of caps, it is found to give very similar results, as long as the radius of the arc is much larger than the via separations. So they are studied under the Row placement pattern. Also, the alternating vias are found to perform a lot better than the regular pattern so the alternating cases are used for the formulation as the most critical cases required for this study.

5.4.1.1 Arc and row pattern. For an arc or row pattern of decap placement, the $\mathbf{L_{Decap}}$ can be formulated using the unit cell with one power and one return via, as shown in Figure 5.4. The unit cell self-inductance is defined as,

$$L_{Self}^{Row} = L_{PP} + L_{GG} - 2M(x), \tag{5.5}$$

where, L_{PP} and L_{GG} are self inductances of the power via and return via, respectively, and $M(x)$ is the mutual inductance between them, in a unit cell. If the decaps are not close to the board edge, the mutual inductance is dependent on the distance between the vias, so written here as a function of the distance between the vias in a unit cell.

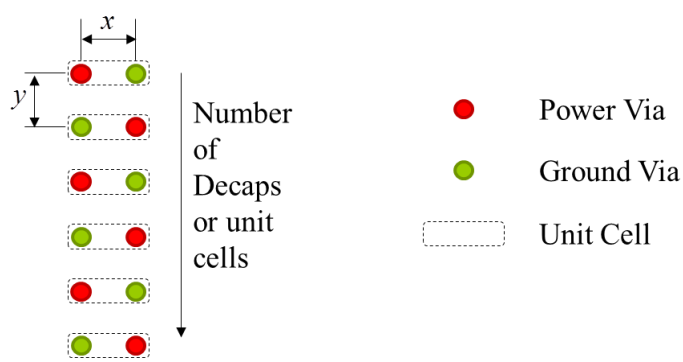


Figure 5.4. The unit cell definition for the Arc or Row patterns.

The mutual-inductance between neighboring cells can be found in terms of the mutual inductances of the vias. The mutual inductance between the nearest neighbors is,

$$L_{Mutual}^{Row} = 2M\left(\sqrt{x^2 + y^2}\right) - 2M(y). \tag{5.6}$$

The $M\left(\sqrt{x^2 + y^2}\right)$, and $M(y)$ are the mutual terms between vias in the neighboring unit cells, between power- power or return -return vias, and between power and return via, respectively, based on the distance between them. This is specific to the alternating

pattern and will be different for the regular pattern. Also, the mutual inductance between the unit cells further apart can also be written similarly, but would not be required as the mutual terms would decrease with the increase in distance between the unit cells. If only the first immediate neighboring unit cell is considered to have significant mutual inductance, the unit cell inductance matrix for *n* capacitors will take the form,

$$\mathbf{L_{Decap}} = \begin{bmatrix} L_{Self}^{Row} & L_{Mutual}^{Row} & 0 & \dots & 0 \\ L_{Mutual}^{Row} & L_{Self}^{Row} & L_{Mutual}^{Row} & \ddots & \vdots \\ 0 & L_{Mutual}^{Row} & \ddots & \ddots & 0 \\ \vdots & \ddots & \ddots & L_{Self}^{Row} & L_{Mutual}^{Row} \\ 0 & \dots & 0 & L_{Mutual}^{Row} & L_{Self}^{Row} \end{bmatrix}_{n\times n}, \tag{5.7}$$

where, the unit cell self terms and mutual terms are calculated using (5.5) and (5.6) for the ring or row patterns. There is only one neighbor for the unit cells (decaps) at the end of the row or arc, and two for all others, which is seen in the matrix as the first and last elements have only one off-diagonal terms, whereas, all other elements have two off-diagonal terms. The L_{Decap} can now be found approximately by assuming all the decaps carry equal currents as,

$$\left(L_{Self}^{Row} + 2L_{Mutual}^{Row}\right)\frac{I_{Total}}{n} = V_{Decap}, \tag{5.8}$$

$$L_{Decap} = \frac{V_{Decap}}{I_{Total}} = \frac{\left(L_{Self}^{Row} + 2L_{Mutual}^{Row}\right)}{n}. \tag{5.9}$$

Using (5.5) and (5.6) in (5.9),

$$L_{Decap} = \frac{\left(2L - 2M\left(x\right) + 4M\left(\sqrt{x^2+y^2}\right) - 4M\left(y\right)\right)}{n}. \tag{5.10}$$

The comparison of the analytical formula from (5.10), to the direct calculations using matrix inverse from (5.4) for the Arc or Row pattern is shown in Figure 5.5. The decaps are placed at 100 mil pitch and the distance between the power and return vias of each

decap is also 100 mils. If the separation between the decaps is smaller than the separation between the decaps power and return vias, then more number of neighbors may need to be considered.

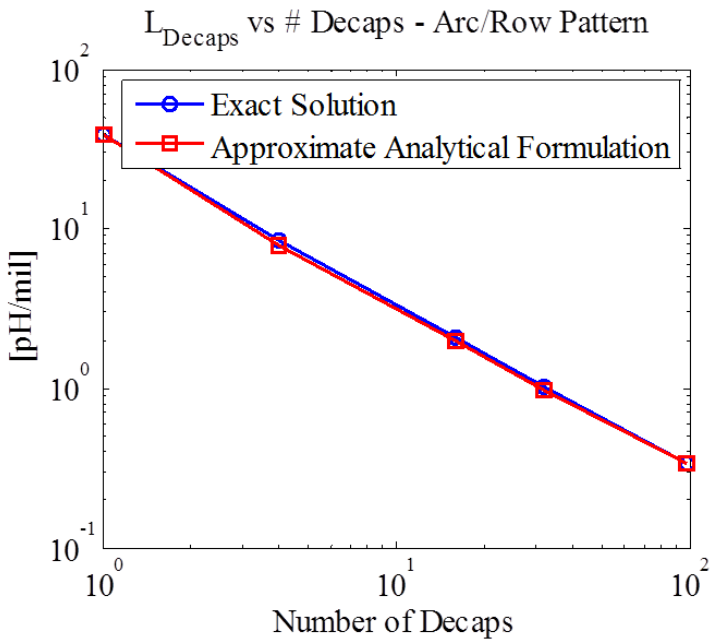


Figure 5.5. Comparison of the analytical formulation with the exact solution which uses the matrix inverse method for the Arc or Row patterns.

5.4.1.2 Grid pattern. The grid pattern has a different kind of unit cell as every power via, used for decap connection, has four return vias at same distance. The Figure 5.6 shows the unit cell definition and the neighboring cells which may have significant mutual coupling. To find the cell equivalent inductance, it is assumed that the power current in each cell returns equally on the four return vias in the cell. The cell equivalent self-inductance and equivalent mutual inductance between neighbors is calculated by assuming superposition of each cell current, thus the return currents on the on the return vias can be added linearly. The self inductance between the cells can be written as,

$$L_{Self}^{Grid} = \frac{5}{4}L - 2M(x) + \frac{1}{2}M\left(\sqrt{2}x\right) + \frac{1}{4}M(2x). \tag{5.11}$$

where,

L: Self-inductance of a single power or return via in the cavity,

$M(x)$: Mutual inductance between power via and nearest return via,

$M(\sqrt{2}x)$: Mutual inductance between two vias placed closest in the diagonal direction,

$M(2x)$: Mutual inductance between two vias placed at two pitch sizes from each other.

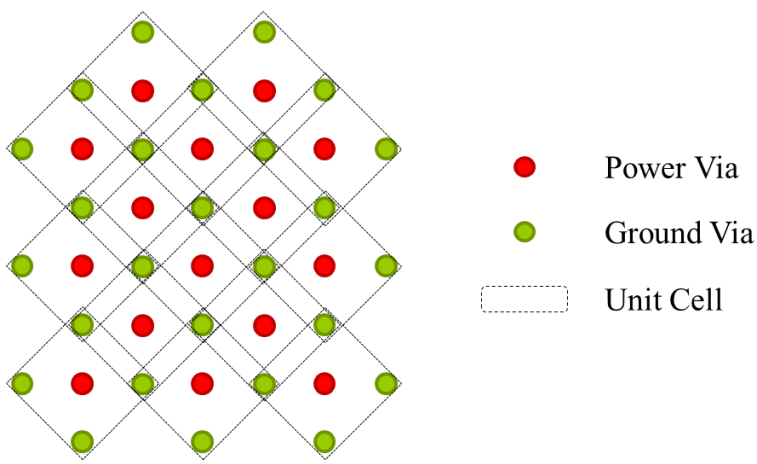


Figure 5.6. The unit cell definition for the Grid pattern of decap placement.

Using, the assumption that the current through each decap is the same, the L_{Decap} can be calculated by ignoring the mutual inductance between the units as a first approximation. Thus the approximate analytical formula is given as,

$$L_{Decap} = \left[\frac{5}{4}L - 2M(x) + \frac{1}{2}M\left(\sqrt{2}x\right) + \frac{1}{4}M(2x)\right] \Big/ n, \tag{5.12}$$

where, n is the number of decaps used in the pattern. This is a basic formula where it is assumed that the effect of neighboring unit cells is small. A comparison of results from (5.12) to the exact solution using (5.4) is shown in below in Figure 5.7. The grid pattern is used with a pitch of 100 mils in both x and y directions. The results show close that the

unit cell self term is alone enough to get an approximate result and may not need to add more mutual terms between the if the accuracy is enough.

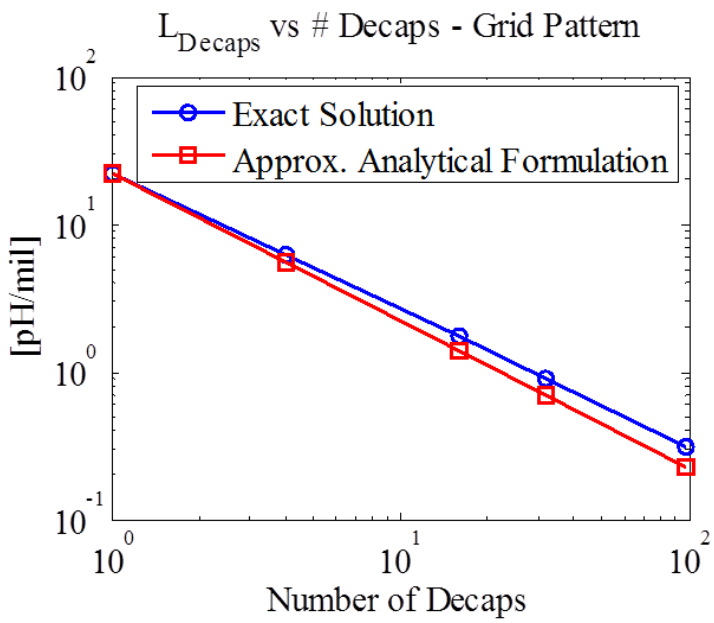


Figure 5.7. Comparison of the approximate analytical formulation with the exact solution which uses the matrix inverse method for the Grid patterns.

5.4.2. L_{Planes}. The inductance contribution of the L_{Planes}, comes from two cavities, upper cavity and lower cavity, formed by the power layer with the closest return planes above and below it in the stack up, respectively. The current paths are based on the location of the capacitors and the ratio of thicknesses of the upper and lower cavities. Figure 5.8 shows the geometry for different locations of the decaps. The cavity with smaller thickness will carry the dominant current as it offers lower inductance path along the planes. For the case with the decaps placed right under the IC, the current will not travel along the planes and the thicknesses of the cavities would not matter.

Based on the locations of the decaps, a circuit model can be formed to identify the inductance contribution, as shown in Figure 5.8. Each circuit model has a short at the location of the decaps, to model the inductance when the current flows from the IC to the decaps in L_{Planes} part of the geometry. The inductance can be calculated analytically for

one pair of power and return vias at the IC and one decap, and later extended to a more general case with several IC power and return vias and several decaps. Each decap location will be treated separately to demonstrate the methodology.

The inductance matrix can be written for the geometry with decaps placed on the top side, using a set of KVL equations written across each via or inductor. For a single power and return via pair at the IC and the decap, the set of equations can be written in the matrix form as,

$$j\omega \begin{bmatrix} L_{11} & M_{12} & M_{13} & M_{14} \\ M_{21} & L_{22} & M_{23} & M_{24} \\ M_{31} & M_{32} & L_{33} & M_{34} \\ M_{41} & M_{42} & M_{43} & L_{44} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}. \tag{5.13}$$

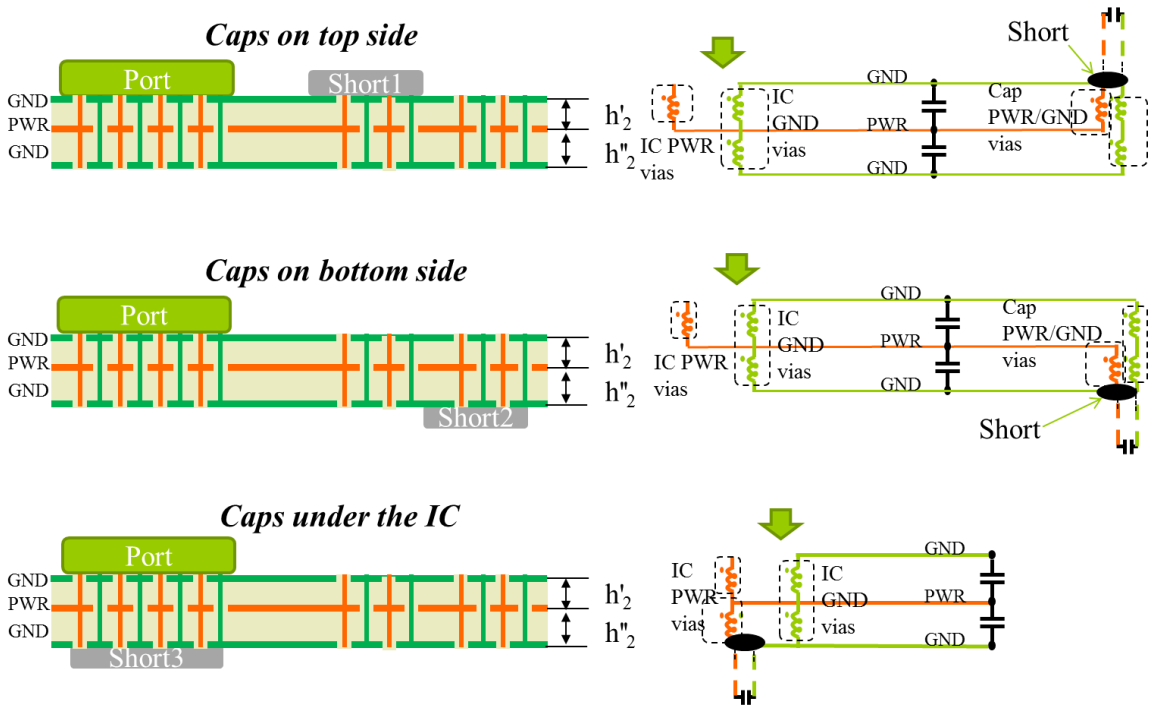


Figure 5.8. The geomtry and corresponding circuit models for the L_{Planes} part.

The currents defined as show with the circuit model, are such that the source current has to return back, and the frequency range is same as the L_{EQ} region of the PDN

impedance, i.e., the conduction currents dominate and plane capacitors have too comparatively high impedance so carry very little current. The power via currents travel in the upper cavity planes and the return via currents travel along the lower cavity planes, so the relation between the via current can be shown to be,

$$I_1 = -I_2;\ I_3 = -I_4. \tag{5.14}$$

The voltages across the return vias adds up to zero in a KVL loop, and across the power vias is used to define the voltage across the port, i.e., IC power via top node and the top reference plane node, as,

$$V_3 = V_4;\ \text{and}\ V_{Planes} \triangleq V_1 - V_2; \tag{5.15}$$

L_{Planes} is the scalar value that satisfies,

$$j\omega L_{Planes} I_1 = V_{Planes}. \tag{5.16}$$

The current and voltage relations in (5.14) and (5.15) can be enforced on (5.13) with row and column transformations, to get,

$$j\omega \begin{bmatrix} L_{11} + L_{22} - 2M_{12} & \begin{pmatrix} M_{13} - M_{14} \\ -M_{23} + M_{24} \end{pmatrix} \\ \begin{pmatrix} M_{31} - M_{32} \\ -M_{41} + M_{42} \end{pmatrix} & L_{33} + L_{44} - 2M_{34} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_{Planes} \\ 0 \end{bmatrix} \tag{5.17}.$$

Then, (19) can be re-written to get,

$$L_{Planes} = L_{11} + L_{22} - 2M_{12} - \frac{\left(M_{13} - M_{14} - M_{23} + M_{24}\right)^2}{L_{33} + L_{44} - 2M_{34}}. \tag{5.18}$$

This can be further extrapolated to a more practical case with multiple vias at the IC and decap locations. Then each element in the inductance matrix in (5.13) has to be

replaced by a matrix representing the power and return via sets and their mutual inductances. The voltages can be assumed to be the same across these groups as the region in which they are placed are electrically small. The current distribution amongst the members in the groups depends on the patterns chosen, but as an approximation, if uniform current is assumed amongst the vias in each group, then the average values of each sub-matrix can be used. If the average value of the matrix $\mathbf{X}$ is defined as,

$$\langle \mathbf{X} \rangle \triangleq \frac{1}{N^2} \sum_{j=1}^{N} \sum_{i=1}^{N} X_{ij} \ , \tag{5.19}$$

where, X_{ij} is an element of the matrix $\mathbf{X}$. Thus the KVL system of equations for the general case for decaps on the top side is given as,

$$j\omega \begin{bmatrix} \mathbf{L_{11}} & \mathbf{M_{12}} & \mathbf{M_{13}} & \mathbf{M_{14}} \\ \mathbf{M_{21}} & \mathbf{L_{22}} & \mathbf{M_{23}} & \mathbf{M_{24}} \\ \mathbf{M_{31}} & \mathbf{M_{32}} & \mathbf{L_{33}} & \mathbf{M_{34}} \\ \mathbf{M_{41}} & \mathbf{M_{42}} & \mathbf{M_{43}} & \mathbf{L_{44}} \end{bmatrix} \begin{bmatrix} \mathbf{I_1} \\ \mathbf{I_2} \\ \mathbf{I_3} \\ \mathbf{I_4} \end{bmatrix} = \begin{bmatrix} \mathbf{V_1} \\ \mathbf{V_2} \\ \mathbf{V_3} \\ \mathbf{V_4} \end{bmatrix}, \tag{5.20}$$

and the L_{Planes} is approximately given by,

$$L_{Planes,Approx1} \approx \langle \mathbf{L_{11}} \rangle + \langle \mathbf{L_{22}} \rangle - 2\langle \mathbf{M_{12}} \rangle - \frac{\left(\langle \mathbf{M_{13}} \rangle - \langle \mathbf{M_{14}} \rangle - \langle \mathbf{M_{23}} \rangle + \langle \mathbf{M_{24}} \rangle \right)^2}{\langle \mathbf{L_{33}} \rangle + \langle \mathbf{L_{44}} \rangle - 2\langle \mathbf{M_{34}} \rangle} \ . \tag{5.21}$$

This is an approximate solution, which assumes that the currents through the vias are uniform in each group. This assumption is not rigorously true, but allows to write a simple expression for the inductance contribution from this piece of geometry with using matrix inverse. To solve rigorously without any assumptions on the current distribution amongst the vias in a group, matrix inverse method, similar to the L_{Decap}, can be used to calculate the reduced inductance matrix as,

$$\begin{bmatrix} L_{11} & M_{12} & M_{13} & M_{14} \\ M_{21} & L_{22} & M_{23} & M_{24} \\ M_{31} & M_{32} & L_{33} & M_{34} \\ M_{41} & M_{42} & M_{43} & L_{44} \end{bmatrix}_{4\times 4} = \left\{ \left(\sum_{\substack{\text{Grouped}\\ \text{Rows}}} \sum_{\substack{\text{Grouped}\\ \text{Columns}}} \begin{bmatrix} \mathbf{L_{11}} & \mathbf{M_{12}} & \mathbf{M_{13}} & \mathbf{M_{14}} \\ \mathbf{M_{21}} & \mathbf{L_{22}} & \mathbf{M_{23}} & \mathbf{M_{24}} \\ \mathbf{M_{31}} & \mathbf{M_{32}} & \mathbf{L_{33}} & \mathbf{M_{34}} \\ \mathbf{M_{41}} & \mathbf{M_{42}} & \mathbf{M_{43}} & \mathbf{L_{44}} \end{bmatrix}_{N\times N}^{-1} \right)^{-1} \right\}, \tag{5.22}$$

and (5.18) can used to find L_{Planes} rigorously. Further approximations can be used to reduce the number of terms in (5.21), by assuming the mutual terms are proportional to the distance between the vias. So the mutual terms between the vias at the IC and decap vias can be neglected, but this shows a bigger error compared to the rigorous solution.

$$L_{Planes,Approx2} \approx \langle \mathbf{L_{11}} \rangle + \langle \mathbf{L_{22}} \rangle - \frac{\left(\langle \mathbf{M_{13}} \rangle + \langle \mathbf{M_{24}} \rangle \right)^2}{\langle \mathbf{L_{33}} \rangle + \langle \mathbf{L_{44}} \rangle}. \tag{5.23}$$

For one IC power via surrounded by four return vias, the L_{Planes} is calculated using the approximations in (5.21) termed Approx1 and in (5.23) termed Approx2, and compared to the rigorous method with (5.22) and (5.18), and shown in the Figure something.

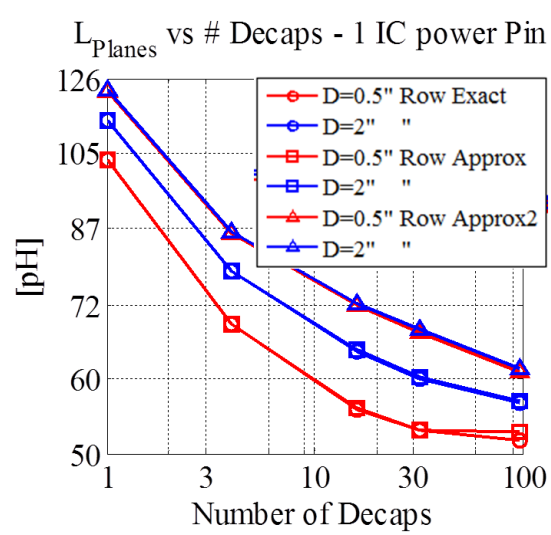


Figure 5.9. Comparison of the approximate analytical formulation with the exact solution for the Row pattern of decaps placed on the top side with the cavity thicknesses 2 mils for both upper and lower cavity and two distances between the IC region and decaps.

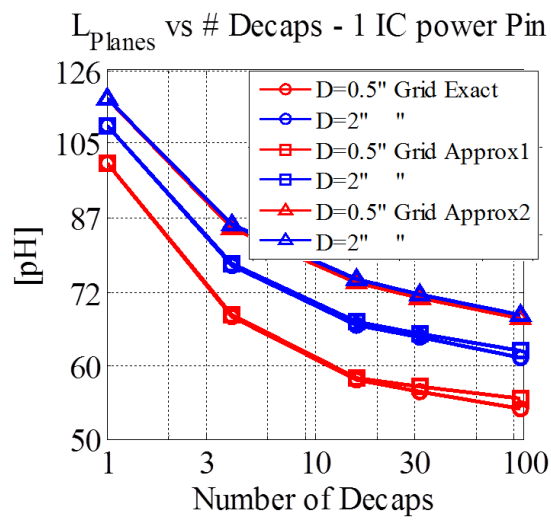


Figure 5.10. Comparison of the approximate analytical formulation with the exact solution for the Grid pattern of decaps placed on the top side with the cavity thicknesses 2 mils for both upper and lower cavity and two distances between the IC region and decaps.

Similarly for the case with decaps placed on the bottom of the board away from the IC region, the KVL system of equations is same as (5.13) but the definition of L_2 is different as shown in Figure 5.8 for the case with decaps on the bottom side. The voltage and current relationships change for this case and are redefined as,

$$I_1 = I_2 = -\left(I_3 + I_4\right), \tag{5.24}$$

and,

$$V_3 = V_4 \text{ and } V_{Planes} \triangleq \left(V_1 + V_2 - V_3\right). \tag{5.25}$$

The inductance for the planes is given as,

$$L_{Planes} = L_{11} + L_{22} - \frac{\left\{\begin{array}{l}\left[\left(M_{13}+M_{23}\right)-\left(M_{14}+M_{24}\right)\right]^2 + 2\left(M_{13}+M_{23}\right)\left(L_{44}-M_{34}\right) \\ +2\left(M_{14}+M_{24}\right)\left(L_{44}-M_{34}\right)+M_{34}^2 - L_3 L_4\end{array}\right\}}{L_{33}+L_{44}-2M_{34}}. \tag{5.26}$$

This can be extended to a general case, using the average value of each sub –matrix as,

$$L_{Planes,Approx1} = \langle \mathbf{L_{11}} \rangle + \langle \mathbf{L_{22}} \rangle - \frac{\left\{ \begin{array}{l} \left[\left(\langle \mathbf{M_{13}} \rangle + \langle \mathbf{M_{23}} \rangle \right) - \left(\langle \mathbf{M_{14}} \rangle + \langle \mathbf{M_{24}} \rangle \right) \right]^2 \\ +\mathbf{2} \left(\langle \mathbf{M_{13}} \rangle + \langle \mathbf{M_{23}} \rangle \right) \left(\langle \mathbf{L_{44}} \rangle - \langle \mathbf{M_{34}} \rangle \right) \\ +\mathbf{2} \left(\langle \mathbf{M_{14}} \rangle + \langle \mathbf{M_{24}} \rangle \right) \left(\langle \mathbf{L_{33}} \rangle - \langle \mathbf{M_{34}} \rangle \right) \\ +\langle \mathbf{M_{34}} \rangle^2 - \langle \mathbf{L_3} \rangle \langle \mathbf{L_4} \rangle \end{array} \right\}}{\langle \mathbf{L_{33}} \rangle + \langle \mathbf{L_{44}} \rangle - 2 \langle \mathbf{M_{34}} \rangle} . \tag{5.27}$$

The approximate formula for L_{Planes}, if the mutual terms between distant vias are neglected, is

$$L_{Planes,Approx2} = \langle \mathbf{L_{11}} \rangle + \langle \mathbf{L_{22}} \rangle - \frac{\left\{ \begin{array}{l} \left[\langle \mathbf{M_{13}} \rangle - \langle \mathbf{M_{24}} \rangle \right]^2 + \mathbf{2} \langle \mathbf{M_{13}} \rangle \langle \mathbf{L_{44}} \rangle \\ +\mathbf{2} \langle \mathbf{M_{24}} \rangle \langle \mathbf{L_{33}} \rangle + \langle \mathbf{M_{34}} \rangle^2 - \langle \mathbf{L_{33}} \rangle \langle \mathbf{L_{44}} \rangle \end{array} \right\}}{\langle \mathbf{L_{33}} \rangle + \langle \mathbf{L_{44}} \rangle - 2 \langle \mathbf{M_{34}} \rangle} . \tag{5.28}$$

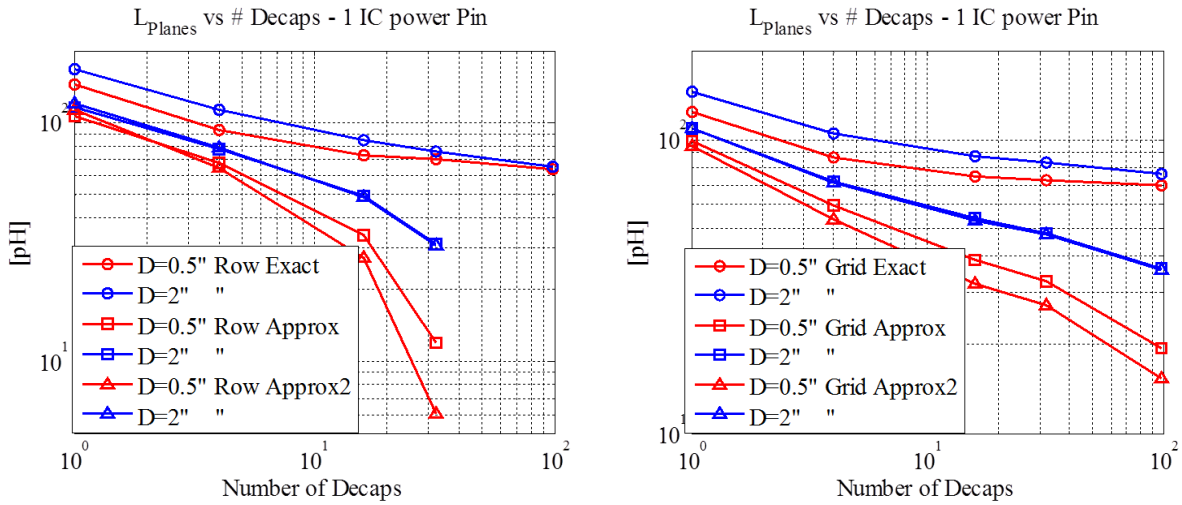
For a stack up with upper and lower cavities both 2 mils in thickness, the L_{Planes} is calculated using (5.27) and (5.28), and compared to the exact reduction methodology to see the effect of the approximations. The results are shown in Figure 5.11.

5.5. MODELLING RESULTS AND ANALYSIS

The circuit model extracted from cavity model and the PPP tool [34]are used to extract the inductance from one cavity simulation for a particular pattern of power and power-return vias. The cavity thickness used is 2 mils for these trends but the results are scalable to cavity thickness as the cavity model formulation shows that the inductance values are proportional to the height of the cavity.

Figure 5.12 shows the inductance contribution of L_{IC} vs the number of IC power pins for the patterns discussed in Section 5.3. The alternating grid converges fastest compared to the row pattern or grouped pattern. The number of IC power pins and pattern is controlled by the IC manufacturer or package design groups, but given a choice, the

alternating pattern shows faster reduction in L_{IC} with increase in number of power vias. A similar conclusion was observed in [12]. The cases were repeated with additional patterns in this paper for completeness.



(a) (b)

Figure 5.11. Comparison of the approximate analytical formulation with the exact solution for the Row and Grid patterns of decaps placed on the bottom side with the cavity thicknesses 2 mils for both upper and lower cavity and two distances between the IC region and decaps.

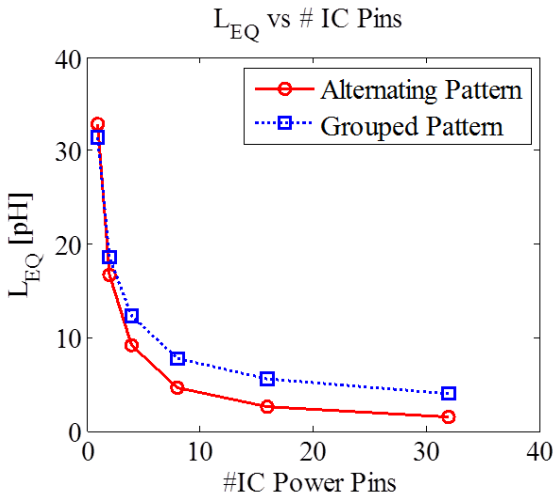


Figure 5.12. L_{IC} vs number of IC power vias for different IC power pin patterns

The comparison of the L_{Planes} vs number of capacitors for different patterns, and different number of IC power vias is shown in Figure 7 and Figure 8, where the family of curves for different IC power via number are shown in Figure 7, and comparison of the placement pattern inductance convergence is shown in Figure 8 for a fixed number of IC power vias. The L_{Decaps} may decrease with the increase in the number of decaps, if the pattern is chosen such that the mutual terms between opposing current are dominant. On the contrary, it could also decrease slower if the pattern is such that the mutual terms between the vias carrying current in same direction dominate the response.

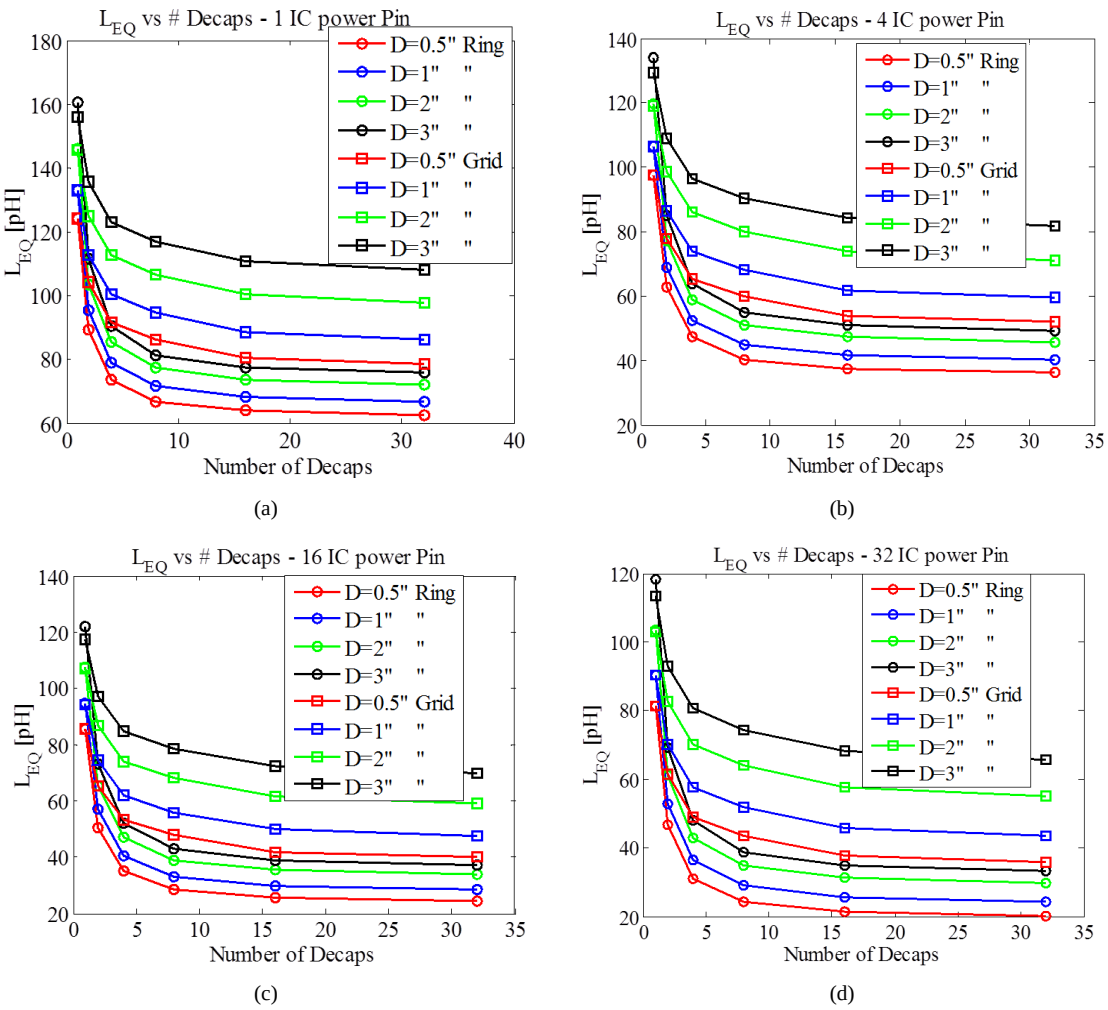


Figure 5.13. L_{Planes} trend with number of capacitors is shown for different number of IC pins:(a) 1 IC power pin, (b) 4 IC power pins (c) 16 IC power pins, and (d) 32IC power pins.

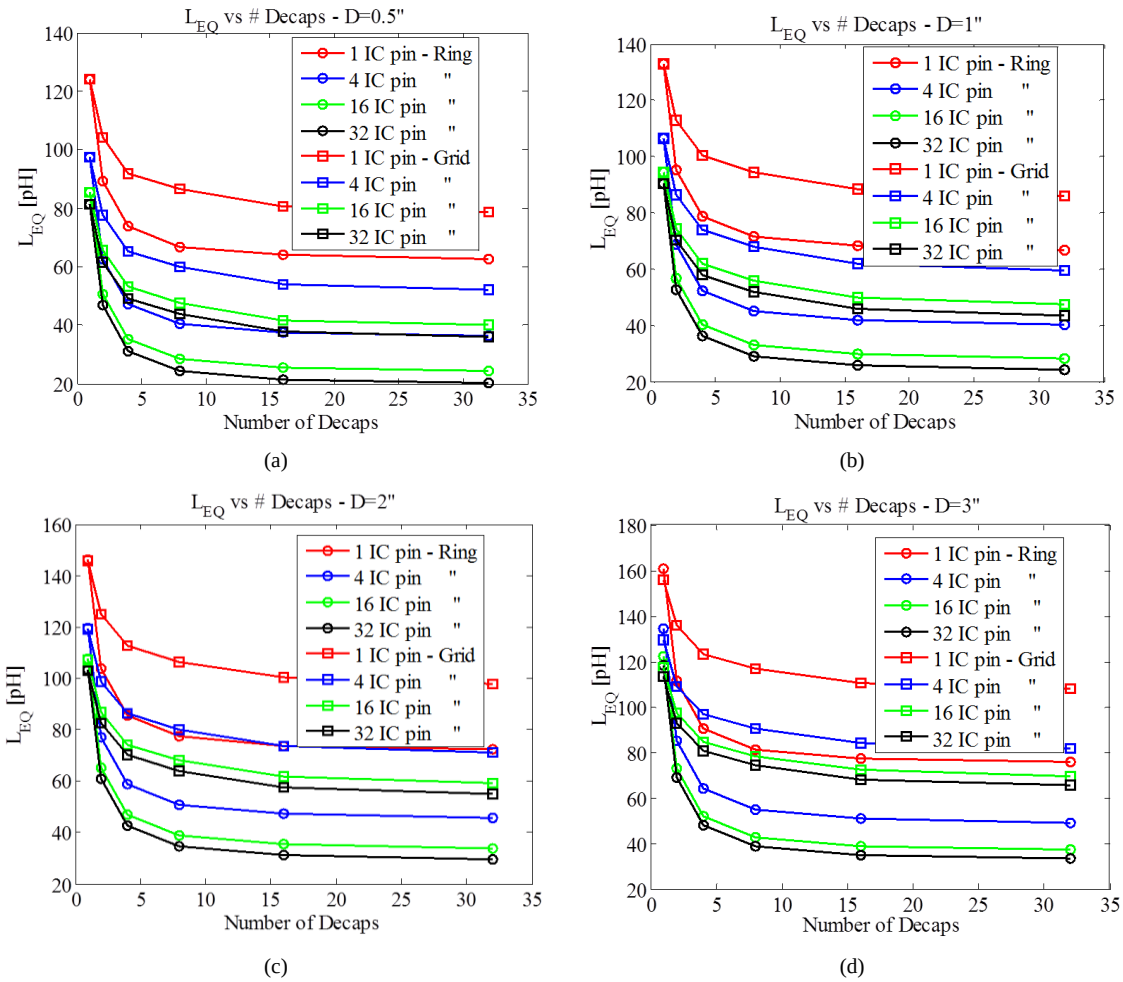


Figure 5.14. L_{Planes} trend with number of decaps is shown for different distances from the IC to decaps:(a) D=0.5”, (b) D=1” (c) D=2”, and (d) D=3”

5.6. DISCUSSIONS

The paper proposes an approach to minimize the equivalent inductance seen by the IC in the input impedance of the PCB PDN. The advantage of this method is that the equivalent inductance can be minimized by choosing geometry details particular to a design or within the limits of availability in a design. Here the scalable trends provided in Section IV help calculate the impact on the overall design down to the total equivalent inductance value.

The principle behind the approach is that the L_{EQ} will converge to a minimum value eventually as the designer adds more capacitors to improve the design. This

minimum value that the L_{EQ} will reach is the L_{IC}. The nature of the convergence of L_{EQ} to L_{IC} is a function of the placement pattern. If the pattern takes advantage of mutual inductance between the IC and decap vias and among the decap vias, then it converges faster, and if not, then it will converge slower. A part of future work is to quantify the fastest and slowest convergence using analytical form for best case and worst case current distribution on the planes and via placements. Each will have a number of capacitors required to converge within a few percent of the L_{IC} and these will form the bounds for number of capacitors needed for convergence.

A recommended procedure to use this approach is to firstly minimize the L_{IC} and then to choose the fastest converging decap placement pattern within design constraints. Once the pattern is chosen, the number of decaps needed for achieving L_{EQ} within a certain percent of L_{IC} can be found using the trends in the previous section. If one particular pattern is not used but a combination of different patterns are used, then several parts of L_{EQ} occur in parallel, and still an estimate can be found for the L_{EQ}, bar some error due to the mutual terms between different patterns not considered herein.

The methodology banks heavily on the segmentation approach. As long as the segmentation is valid this approach will work. When a number of different patterns and distances are used to place the decaps, the equivalent inductance has to be computed using the circuit modelling tool. Predicting the L_{EQ} value from the trends will have an assumption than the various patterns used will not interact, which may not be entirely true.

5.7. CONCLUSION AND FUTURE WORK

The paper provides a methodical approach to choose the patterns and number of the decaps based on quantitative analysis of the equivalent inductance of the design. The curves in the paper are scalable to cavity thicknesses, and hence provide flexibility to estimate parts of L_{EQ}, for a custom stack up. The approach can be used with high layer count structures and low layer count structures, in the same manner as the performance criteria remains the equivalent inductance which will impact the input impedance of the PDN.

The formulation in Section 5.4 to find simple expressions for the convergence of L_{Decap}, L_{Planes} and L_{IC} in terms of number of capacitors as a function of the geometry used, was not very successful. This is because several approximations were made to avoid matrix inverse and preserve the analytical formulation. These approximations or assumptions are based on the uniform current distribution among the vias in each region of the geometry. As the current distribution is not always uniform, and mostly dependent on the pattern and mutual inductance, the formulations do not follow the exact solution with the matrix inverse. Some future work is being done to curve fir the results to the same variables to find the simple formulas which designers can use easily. The curve fitting approach involves solving for the inductance components for a reasonable variable space and then fitting results with one or two variables at a time.

In this approach, the design choices are driven by current path based physics and not driven by rules of thumb or large full wave simulations. Thus the designer makes informed decisions, knowing or expecting the improvement or degradation of performance of the design.

6. STATISTICAL ANALYSIS OF CROSSTALK IN HIGH SPEED LINKS

6.1. INTRODUCTION

Data rates in high speed digital communication channels are increasing rapidly and with them the required timing margins are decreasing. With smaller bit periods and smaller operation voltages, the tolerable timing and noise margins are reducing. There are many sources of disturbances contributing to the tolerance margins. These margins have to account for inter symbol interference (ISI), reflections, jitter, noise from power distribution networks and crosstalk. An important task during the design phase of the system is to find and mitigate the noise from such sources.

Crosstalk forms a critical part of the budget, and if ignored, can lead to design failures. For printed circuit board (PCB) designs, many rules of thumb have been developed with regards to routing the signals, distances between victims and aggressors, use of stitching vias, etc [35]. But these are best practices which have been developed with experience and do not provide an exact number on the possible crosstalk between the channels. Also, many real designs may require these rules to be violated to enable certain routing densities or to manage the PCB real-estates [36]. In these cases, the impact of the real world compromises is not clearly known. In some cases, the difference between two choices in design on the PCBs is not quantitatively known, but these are made based on qualitative trends, known from ‘rules of thumb’ or proven physics.

In real designs, there are a number of sources contributing to the total crosstalk at a receiver. The sources may be neighboring traces on the routing layers, or neighboring vias in the connectors, or the integrated circuit (IC) via fields, or some noise coupling through plane-pairs penetrated by the routing vias. Due to the nature of the problem, some critical sources are identified and the design is optimized to minimize their impact. The choice of these critical sources is made based on full wave solutions or prior experience of the designers. The real impact may not be reflected as the simulations do not account for the data, or signals used in the real applications.

The most common method used to quantify the crosstalk is using scattering parameters (S parameters) to quantify the coupling in the frequency domain [35]. The decisions are commonly based on the coupling parameter at the fundamental frequency,

and the harmonics of the data rate on the aggressor channel. The main assumption here is that majority of the aggressor signal energy is at this fundamental frequency and its harmonics, which may not be true unless the aggressor carries a clock signal. The crosstalk is a function of the S parameters and the frequency content of data on the aggressor channel. As the common communication channels carry aperiodic data, a broad frequency band has to be considered to analyze the crosstalk. Thus, it is difficult to make a decision based on crosstalk S parameters alone, as the frequency content of the real signal is not always known and may change over time.

More rigorous time domain simulations require long PRBS sequences used to test with many aggressor sources or the actual data sequences. When using the conventional or traditional eye diagram for analysis, with the victim channel carrying its own data modelled with a PRBS sequence, the effect of crosstalk is buried in the victim channel's response and cannot be distinguished from the other non-ideal effects on the victim channel. Making design choices is difficult, as the difference in performance between the designs might not be clearly observable. But the aggregate effect of crosstalk from many aggressor sources may still cause the channel to fail, even if individual contributions to cross talk are not noticeable, which shows that these decisions are important.

Thus, it would make sense to evaluate the effect of crosstalk alone on the eye diagram at the victim, and base the design decisions about the aggressors on the distribution and the maximum crosstalk value observed in the eye diagram. This is the solution proposed, herein, to analyze the waveforms generated in a unit interval (UI) at the victim due to each aggressor individually and then to observe the combined effect of multiple aggressors together. As the victim's receiver port waveforms would not look like an eye when only the crosstalk is observed, it will be referred to as the crosstalk UI in the text hereon.

There are several methods to find the eye diagram at the victim analytically which account for the source and load conditions and the transmission-line effects modelled [37-39]. There are also several statistical methods to find the eye diagram [36], [40-42], which use either an impulse response, a step response or a one bit response convolved with the bit stream representing the input data to calculate the output waveforms at the victim's receiver. These output waveforms can be used to plot the eye diagram. There are

several variations in the method to find the eye diagram, depending on the choice of basis functions, an impulse response, a step response or a pulse response, and the choice of the input sequences, a PRBS sequence, or a kind of 'Monte Carlo' approach with all possible N –bit combinations, or just choosing a few worst case scenarios to get the corner cases. Such methods can be extended to find and analyze the crosstalk UI.

Herein, the crosstalk UI is generated using the pulse response or single bit response technique shown in [42], [40] for calculating the eye diagrams for through channels. The single bit response method is used with the aggressor–victim pair to get the crosstalk UI waveforms. The waveforms are calculated for all bit combinations at the input and then plotted together in a UI of the receiver to generate the crosstalk UI. If the victim's through channel pulse response is used, this would lead to one UI of the conventional eye diagram. This method can be extended to multiple aggressors can be calculated, and a brute force method can be used to calculate the total crosstalk waveforms for all bit combinations at all aggressors. The crosstalk UI is used to calculate the probability distribution of crosstalk at each time slice in the crosstalk UI. A faster method to calculate the probability distribution function at each time sample from the pulse-responses is shown which can also be extended to multiple aggressors. The probability distributions can be used to calculate the probability of crosstalk being more than or less than a tolerable value.

The main contribution of the paper is to use the single bit response method to calculate the crosstalk distribution due to several aggressors from the measured or simulated crosstalk S-parameters between the victim and the aggressors. The paper illustrates how to generate the probability distributions from the pulses responses of the aggressors and to convolve them to obtain the total crosstalk distribution which accounts for all possible input bit combinations at all aggressors. Results from this methodology have been validated by transient simulation results. Some discussions are included to clearly identify the limitations and possible applications.

6.2. METHODOLOGY

The goal to find the crosstalk distribution in the unit interval can be accomplished without having to setup a long time domain measurement, with PRBS generators, or long

simulations. Both, the simulations and measurements get complicated if many aggressor ports are to be considered at a time. The proposed approach is to start with a frequency domain characterization (measurements or simulation) to find the network parameters and find the time domain pulse response which can be used to find the crosstalk UI. Also, the frequency domain S parameters can be obtained more reliably in measurements, due to the availability of accurate calibration techniques, and high precision measurement devices. Simulations also can be setup in the variety of commercial tools available. Once the network parameters are available, these can be used flexibly for any combination of ports, and various loading conditions, without having to re-run the simulations or measurements. The following sub-sections provide the methodology used to generate the crosstalk UI for multiple sources, details about the crosstalk probability distribution and the crosstalk cumulative probability distribution in the unit interval.

6.2.1. Pulse Response. The S-parameter of an aggressor victim pair can be obtained from simulation or measurements. The S parameters are used to find the transfer function for the crosstalk, and can be transformed to time domain using the inverse Fourier transform to obtain an impulse response. For a single aggressor-victim system, the transfer function can be written in terms of the S parameters as,

$$H(\omega) = S_{ij}, \tag{6.1}$$

where, $H(\omega)$ is the transfer function, and S_{ij} is the S parameter representing the crosstalk between the ith and jth ports. Herein, it is assumed that all the other ports are terminated with the reference impedance, which is usually the case with the transmitter and receivers being matched to the lines. If there are non-ideal terminations at other ports of the system, then the reflections from these terminations will change the transfer function, so a SPICE-like circuit solver can be used to calculate the transfer function, for specific load conditions. The impulse response can be found from the transfer function as,

$$h[n] = \mathrm{IFFT}\left(H(\omega)\right) \tag{6.2}$$

There are many considerations, and data conditioning steps required in the inverse fast fourier transform (IFFT), depending on the time step required for the impulse response, which in turn depends on the time step required in the final UI waveforms. Some windowing and extrapolation may also be required to get a causal impulse response which is free of numerical noise due to the transform. The required impulse response may increase the signal processing burden. To avoid these problems, the pulse response may be directly obtained from any commercial tool using the S-parameters, as these processing steps have been studied well in literature [43], [44], and are not the primary focus of this work.

The impulse is convolved with a pulse shape $p[k]$ to get a pulse response as,

$$x[n] = \sum_i p[n-i]h[i]. \tag{6.3}$$

Figure 6.1 shows an example pulse response for a through channel, and the pulse response for a crosstalk channel.

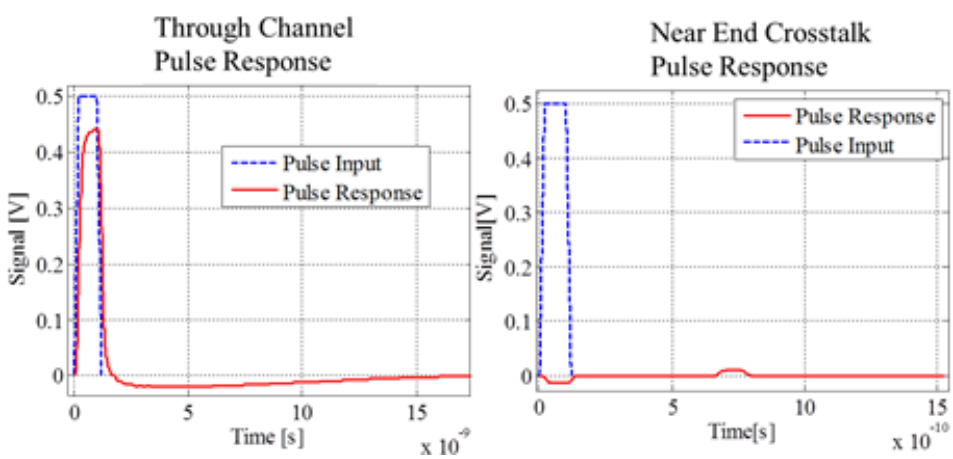


Figure 6.1. Example pulse response when through channel transfer function is used, and when a crosstalk transfer function is used.

6.2.2. Crosstalk Unit Interval. The crosstalk to be determined is the voltage at the victim port due to a digital input signal at the aggressor. The input bit stream at the aggressor can be decomposed into a series of shifted and scaled copies of the same pulse, shown in the Figure 6.1. The pulses overlap to achieve the resulting edges of the waveform. Assuming the system is linear and time invariant, the superposition theorem holds and so the response of an input bit stream can be recreated using individual time shifted and scaled pulse responses (which form the input bit stream). The shift, scale (by 1 or -1) and add is like convolving the pulse response with a stream of impulses, with magnitudes 1 or -1 to represent the bits.

The limitation of this procedure is that all the pulses should have the same rise and fall times. If the edges are asymmetric, then a different set of basis can be defined to span such input bit streams[41], or the step response methods could also be employed [45].

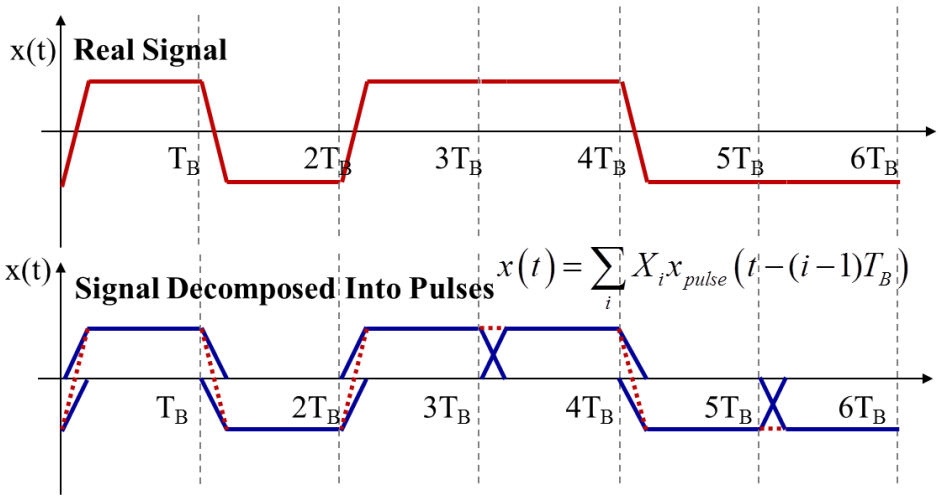


Figure 6.2. Pulse definition used to generate a pulse response, is designed such that a series of shifted pulses can reproduce original bit streams shown as the real signal.

If the pulse response is N bit long, then the output at the receiver port, due to the aggressor input, can be recreated by a combination of N input bits and one-UI-long

segments of the pulse response, as shown in Figure 6.3. Consider an N bit long pulse response $x[n]$, with an input bit stream $\mathbf{B}$ defined as,

$$\mathbf{B} = B_1 B_2 ... B_N, | B_i = 1 \text{ or } 0, \tag{6.4}$$

and, the input pulse stream defined as,

$$\mathbf{X} = X_1 X_2 ... X_N, \ | X_i \triangleq \begin{cases} 1, \text{if } \ B_i = 1 \\ -1, \text{if } \ B_i = 0 \end{cases}. \tag{6.5}$$

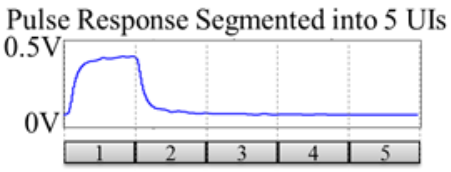
The output waveform at the victim port can be found using the pulse response as,

$$y[n] = \sum_{i=1}^{N} X_i x\left[(i-1)n_B + n\right], \quad n = 1, 2, ... n_B, \tag{6.6}$$

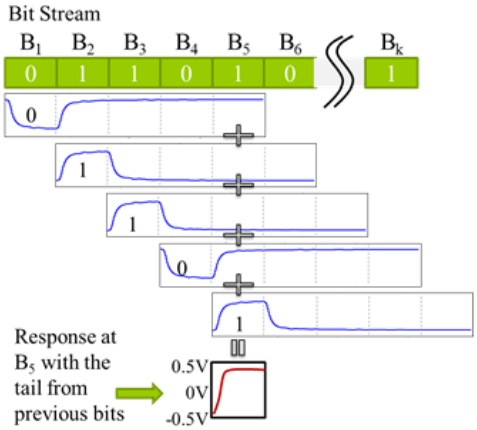
where, n_B is the number of samples in one UI or bit period, so depends on the sampling frequency. Here, the nth sample in every one UI segment gets added together and scaled by the bit value as defined in (6.5). An output waveform can be found for every combination of the input bit sequence $\mathbf{B}^k$, thus the response to the kth sequence or combination, is given as,

$$y^k[n] = \sum_{i=1}^{N} X_i^k x\left[(i-1)n_B + n\right], \ \forall \ n = 1, 2, ... n_B. \tag{6.7}$$

2^N combinations of N bits are possible with unique output waveforms at the receiver. For crosstalk analysis, the pulse response may be very long and requires a large number of combinations to characterize fully.



(a)



(b)

Figure 6.3. (a) Pulse response of a through channel is segmented into 5 UIs, (b)Pulse response used to recreate the output waveform of a bit stream using the segments and bit values to scale the response segments.

All the output waveforms corresponding to each bit combination can be plotted together to generate the crosstalk UI. If the same process is used with a through channel pulse response, half the eye diagram (only one UI) will be created, which can be repeated and concatenated to create the conventional eye diagram with a width of two UIs. For example, the one UI eye is shown in Figure 6.4 for the through channel pulse response shown in Figure 6.1. In case of a through channel, the tail of the pulse response depends on the ISI in the channel, and longer tail implies more ISI. The number of waveforms used to form the eye depends on the pulse response length. The eye diagram obtained from this method is compared to the FEMAS [46] calculation of eye diagram using a PRBS9.

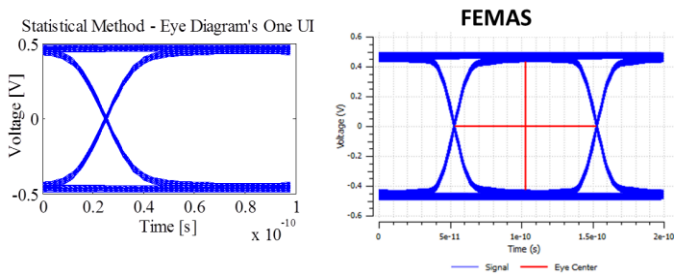


Figure 6.4. Eye diagram's one UI from the output waveforms for all combinations of bit stream for a through channel validated with FEMAS[46].

6.2.3. Crosstalk PMF UI. The probability mass function is the discrete probability distribution function used herein to associate the value of crosstalk with a probability of occurrence based on the crosstalk UI generated in the previous sub-section. The crosstalk UI is composed of all the crosstalk waveforms associated with every input bit combination at the aggressor. For the purpose of analysis, all input bit combinations at the aggressor can be assumed to have uniform probability distribution (equal probability). The same probability of occurrence is associated with the corresponding output waveforms in the crosstalk UI. The crosstalk UI can be converted into a crosstalk probability mass function (PMF) UI, by using quantization or binning on the voltage axis, to convert the possible crosstalk values into a discrete set. The x-axis, associated with the time samples, is already discrete in nature.

Crosstalk PMF UI is divided into time samples along the x-axis and discrete voltage values along y-axis, with each unique voltage-time combination associated with a probability of occurrence. Analogous to an image with pixels, where each pixel has a value of color associated with it, the crosstalk PMF UI is a matrix with time and voltage axis forming abscissa and ordinate, and a probability value associated with each position. The quantized waveforms can be saved into this matrix and each pixel probability can be incremented by 1/ (2^N) when the waveform includes at that pixel, where N is the number of bits used for the waveforms. The PMF of the crosstalk at the voltage level *v* and time sample *n* can be represented as,

$$f\left(v,n\right)=\Pr\left(y^k\left[n\right]=v\right) \quad \forall k=\{1,2,3,...,2^N\}. \tag{6.8}$$

The resulting matrix can be observed using a 3D plot with the probability forming the z-axis or 2D plot with the probability represented by a color grade. Figure 6.5 illustrates a crosstalk UI converted into a crosstalk PMF UI.

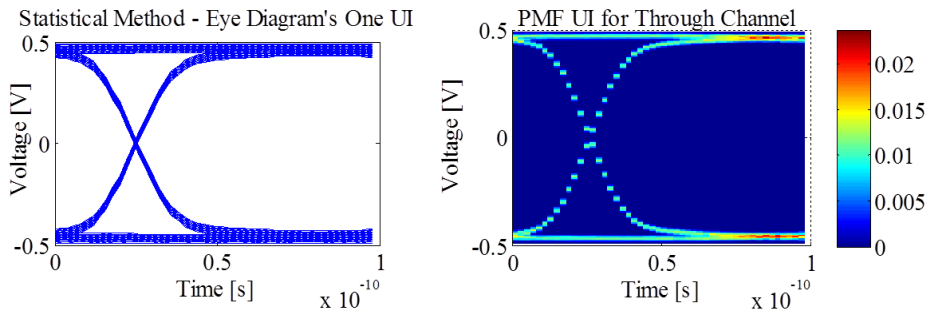


Figure 6.5. Crosstalk UI converted to a crosstalk PMF UI, where a through channel is used to illustrate instead of crosstalk for ease of understanding

Above method is the brute force method in which the occurrences at each pixel are counted after evaluating each waveform. But this method is time and resource consuming, as 2^N waveforms have to be evaluated. Another intuitive method can be used where the pulse response samples are considered as random variables R_n which can take values $x[n]$ or $-x[n]$ with an equal probability of ½, to represent the occurrence of one or zero bit respectively. The crosstalk value at each sample in the UI, given in (6.7), can be represented by the random variable Y_n, expressed as a sum of the random variables R_n as,

$$Y_n = R_n + R_{n+n_B} + \cdots + R_{n+(N-1)n_B} \,\big|\, n = 1, 2, \cdots, n_B \,. \tag{6.9}$$

Then the probability mass function at the nth time sample in the UI can be written as a convolution of the independent probability mass functions of the random variables in (6.9). Thus, if p_n^R and p_n^Y are the probability mass functions of R_n and Y_n, respectively, then,

$$p_n^Y = p_n^R \otimes p_{n+n_B}^R \otimes \cdots \otimes p_{n+(N-1)n_B}^R \,\Big|\, n = 1, 2, 3, \cdots, n_B \,, \tag{6.10}$$

where,

$$p_n^R = \begin{cases} 1/2 & \big| R_n = \pm x[n] \\ 0 & \end{cases} \quad \Big| n = 1, 2, 3, \cdots, Nn_B \,. \tag{6.11}$$

The evaluation of the crosstalk PMF UI, p_n^Y, can be done directly from the pulse response $x[n]$.

6.2.4. Crosstalk UI for Multiple Aggressors. The crosstalk calculation can be extended to the multiple aggressors' case by simply adding the crosstalk responses from each aggressor at every bit combinations. The method is explained in Figure 6.6, considering two aggressors. But this method can be extended to any number of aggressors. If N_1 bits are used for one aggressor and N_2 bits for the other aggressor, leading to $2^{(N_1+N_2)}$ bit combinations, which are all the possible combinations of the bits from both aggressors. The crosstalk calculation at the nth sample in the UI for the kth bit combination is given by,

$$y_n^k = \begin{bmatrix} \sum_{i=1}^{N_1} X_i^k x_1\left[(i-1)n_B + n\right] \\ + \sum_{i=1}^{N_2} X_{N_1+i}^k x_2\left[(i-1)n_B + n\right] \end{bmatrix}, \forall n = 1, 2, \ldots n_B \tag{6.12}$$

where, and are the pulse responses of the two aggressors, and, is the input bit stream's i^{th} bit in the kth combination of bits defined in (6.4) and (6.5).

If the time skew between the two aggressors is known then it can used in the crosstalk calculation. The lagging aggressor's pulse response can be shifted to account for this skew. For more than two aggressors, the time skew information can be used for each aggressor to delay the respective pulse responses. The total crosstalk, with a skew of δ samples between the two aggressors, is given by,

$$y_n^k = \begin{bmatrix} \sum_{i=1}^{N_1} X_i^k x_1\left[(i-1)n_B + n\right] \\ + \sum_{i=1}^{N_2} X_{N_1+i}^k x_2\left[(i-1)n_B + n - \delta\right] \end{bmatrix}, \forall n = 1, \cdots, n_B. \tag{6.13}$$

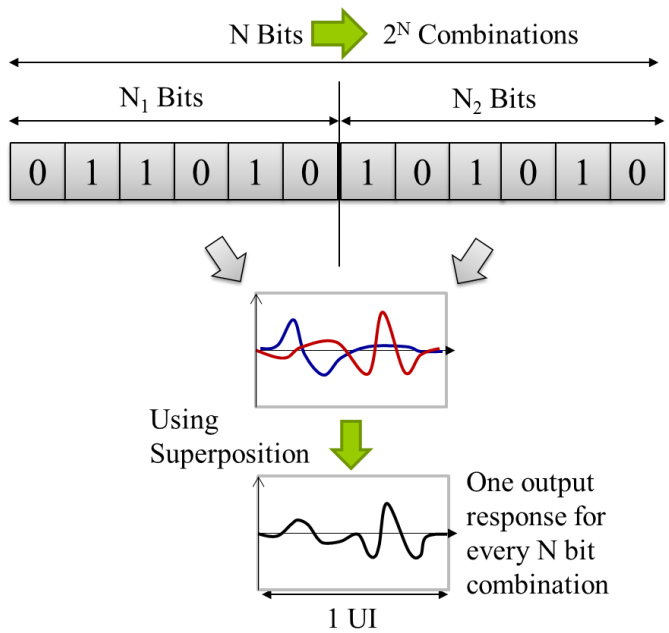


Figure 6.6. Crosstalk waveform obtained from two aggressors using superposition.

The time skew information is difficult to precisely calculate, and it may change over time. So a number of time skew values swept from 0 to one UI may be used to find the worst case possibilities. Say m aggressors are present and p steps of time skew are considered between the sources at each aggressor, then the original simulation can be repeated p(m-1) times to exhaust all the possibilities. This brute force method to exhaust all possibilities might be too resource intensive and time consuming. A better way would be to observe the individual crosstalk profile for each aggressor and identify the critical aggressors. Then the combinations of the critical aggressors can be used to identify the worst case possibilities and crosstalk profiles for different time skews.

Considering all the aggressors together requires $2^{(N1+N2+\ldots+Nk)}$ combinations of bits to be used to find all the UI waveforms for total crosstalk for one time skew case. This is not very practical when the total number of bits becomes very large. On the other hand, the crosstalk UI calculation for each aggressor requires 2^{Ni} combinations, which depends on the pulse response length (N_i bits) of the ith aggressor, but is very small compared to all the aggressors considered together. Depending on the application, if the crosstalk UI is not the final objective then some post processing of individual crosstalk UIs of the aggressors to get a probability distribution and then incorporating into one UI might prove efficient. This is shown in the following sub-sections.

6.2.5. Crosstalk PMF UI for Multiple Aggressors. When there are multiple aggressors, one approach is to transform the total crosstalk UI into crosstalk PMF UI. Using the method illustrated in previous sub-section each ith aggressor's pulse response is used with N_i bits and all possible combinations of the total number of bits are used to find corresponding total crosstalk waveforms which form the crosstalk UI. The total crosstalk has to be calculated considering the time skew, if any, between the aggressors. As discussed before, when the total number of bits is large, the time and resources required to compute the response to all the possible combinations is very large.

Alternatively, the individual crosstalk UIs from each aggressor can be converted to the individual crosstalk PMF UIs and then convolved together to get total crosstalk PMF UI. The convolution is performed between with the vertical slices of each aggressor's crosstalk PMF UI at corresponding time samples. As the convolution of two PMFs considers all combinations of the two independent events [7], all combinations of aggressor input waveforms (input bit patterns) are covered in this process. Also, if there is some time skew to be considered between the aggressors, then the lagging aggressor's crosstalk PMF UI can be shifted in a cyclic manner along time axis to get the effect of time skew. The total crosstalk PMF UI, p^T, of a system with two aggressors, can be found by convoluting the individual crosstalk PMF UIs, p^{Y_1} and p^{Y_2}, at each time slice as,

$$p_n^T = p_n^{Y_1} \otimes p_n^{Y_2}, \forall n = 1, \cdots, n_B. \tag{6.14}$$

If there are k aggressors with time skews between the aggressors of δ_i time samples for the ith aggressor, then the convolution in (6.14) is used with a cyclic time shift as,

$$p_n^T = p_{n-\delta_1}^{Y_1} \otimes p_{n-\delta_2}^{Y_2} \cdots \otimes p_{n-\delta_k}^{Y_k}, \forall n = 1, \cdots, n_B. \tag{6.15}$$

The crosstalk PMF UI calculation can be performed individually for all k aggressors using (6.10) and then the convolution, as shown in(6.15), would take relatively less time compared to considering all aggressors together to calculate total crosstalk UI. One more calculation step can be saved if (6.10) and (6.11) are substituted in (6.15) to get the total crosstalk PMF UI directly from the individual pulse responses.

The time required for the convolution of k aggressors with n_B time samples per UI each, depends on the number of discretization levels used along the voltage axis and the number of time skew combinations required. To reduce the time required for multiple convolutions due to large number of aggressors (k crosstalk PMF UIs to be convolved) a Fourier transform could be used for all the slices, changing the convolutions to multiplications. As the time skews (if any) would only shift the slices around in a cyclic manner, all possibilities of time skew can also be performed in the transformed domain. This can reduce the time required to implement this procedure significantly. This is part of future work to be explored to increase the time efficiency of the method.

6.2.6. Cumulative Mass Function (CMF). As the limit within which the crosstalk occurs is more relevant from the designer's point of view, the PMF can be converted into a cumulative distribution function (CDF) of crosstalk for all values less than or more than a certain voltage level at each time sample in the UI. The crosstalk CDF UI can be found by adding the probabilities cumulatively along the random variable. Here, the random variable is voltage of crosstalk and extends from UI minimum voltage level to UI maximum voltage level. The CDF is found for each time sample using two options, to start at zero voltage level and add probabilities moving towards the maximum and minimum voltage levels, or to start at the maximum or minimum voltage levels and add the probabilities moving inwards to zero. These can be interpreted as CDF and complimentary CDF (CCDF), but both functions are calculated in the half space

about the zero volt value on the random variables. The UI is divided by a line of symmetry about zero volts, both show maximum probability of 0.5 at the end of the scale in the direction of addition. Qualitatively, CDF represents the probability of absolute crosstalk value being less than a value at each time sample, and the CCDF represents the probability of absolute crosstalk value being more than a voltage value. The functions can be mathematically expressed as, F^T for the CDF,

$$F^T\left(v',n\right)=\begin{cases}\sum\limits_{\forall v\in[0,v_{\max}]} p_n^T\left(v\le v'\right)\\ \sum\limits_{\forall v\in[v_{\min},0]} p_n^T\left(v\ge -v'\right)\end{cases}, \tag{6.16}$$

and $\overline{F}^T$ for the CCDF,

$$\overline{F}^T\left(v',n\right)=\begin{cases}\sum\limits_{\forall v\in[0,v_{\max}]} p_n^T\left(v\ge v'\right)\\ \sum\limits_{\forall v\in[v_{\min},0]} p_n^T\left(v\le -v'\right)\end{cases}, \tag{6.17}$$

where, p_n^T is the total crosstalk PMF UI for the system at the nth time sample.

Each function may be useful for a particular application. At the same time, they are complimentary to each other, so one can be found from the other by subtracting the values from 0.5. If the objective of the application is to find the probability of crosstalk being less than a certain value, the CDF is more suitable. It gives the probability in the design for crosstalk less than a voltage value. The CCDF function is more suitable to find the probability being more than a certain value. If the crosstalk budget is known, the CCDF shows the probability for a system to fail (bit error), for that crosstalk budget.

6.3. VALIDATON AND APPLICATIONS

The proposed method has been validated with some examples in the following sub-sections. The validation uses FEMAS[46], which uses a complete transient analysis with a PRBS sequence to generate an eye diagram. To compare with the same number of samples in a UI, enough to observe a smooth transition, at practical data rates, requires a high sampling frequency. To achieve this, most tools require some post processing on the

S parameters, which may involve extrapolation procedure. To have the same extrapolation and other post processing effects used in FEMAS, the pulse response is exported from FEMAS and used with the proposed algorithm.

6.3.1. Multi-Conductor Transmission Line Example. Multi-conductor transmission line geometry is used in FEMAS cross-section analysis toolset, to generate the S parameters and eye diagrams. The geometry is shown in Figure 6.7, which shows a cross-section with 4 stripline traces forming the example geometry. The two differential pair example is chosen to get one victim port and two aggressor ports from NEXT and FEXT ports. Though this transmission line system may not be very realistic, it is used here just to verify the algorithm.

The differential S parameters for the NEXT and FEXT are shown in Figure 6.8(a). These S- Parameters are obtained from FEMAS, by cross-section analysis of the geometry shown in Figure 6.7, using a 2D FEM algorithm. The pulse responses corresponding to these crosstalk S-parameters, are shown in Figure 6.8(b). Both the pulse responses use a pulse definition corresponding to a 10 GHz signal and 20 ps rise and fall time. The time steps used are 2ps which allow 50 samples in each UI. The pulse response is obtained from FEMAS, to get the same data processing effects when comparing the crosstalk UI.

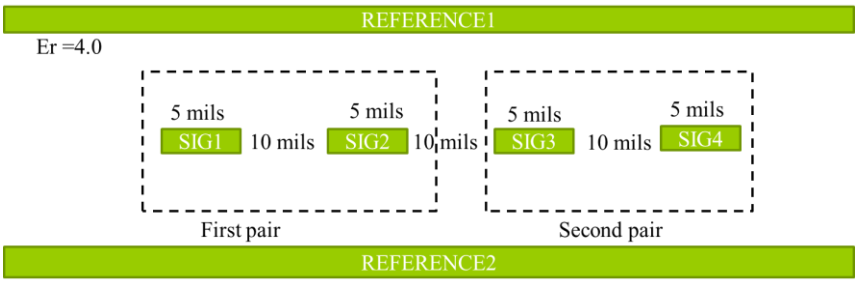


Figure 6.7. Cross-sectional geometry of the multi-conductor test case with four coupled stripline traces forming two differential links

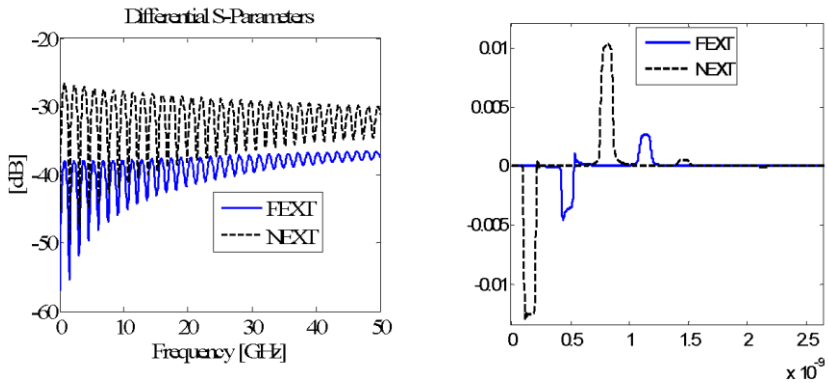


Figure 6.8. (a) FEXT and NEXT S parameters for two differential links (b) The pulse responses corresponding to the FEXT and NEXT of two differential links.

The S-parameter data is available till 50 GHz, but the sampling rate for a 2 ps step in the UI needs the frequency content up to half the sampling rate of 500 GHz. So it is required to extrapolate to 250 GHz, or use smaller number of samples and interpolate to 2 ps step in the time domain. The pulse response used here is exported from FEMAS to get the same data processing used to achieve the sampling rate.

As symmetric stripline geometry in homogeneous media is chosen here, the crosstalk seems to originate from a mismatch at the terminations and multiple reflections. The levels are low but due to the propagation delays of several UIs, the number of bits used at aggressor for calculation is large. Figure 6.9 shows the comparison of the crosstalk UI generated form the algorithm and from FEMAS. These results are generated using 16 bits as the combination length, which covers the complete tail of the pulse response. These crosstalk UI are converted to crosstalk PMF UI and shown in Figure 6.10.

The crosstalk PMF UI can be converted into the crosstalk CDF UI using the second method explained in the previous section. The NEXT crosstalk CDF UI and FEXT crosstalk CDF UI are shown in Figure 6.11 and Figure 6.12, respectively, using the two different methods. The crosstalk is from one aggressor line, so practically can have one active transmitter at a time. But to check the algorithm for combinations of sources, the two PMFs can be combined to get a total crosstalk PMF. These results are

for zero time skew between the aggressors' sources, shown in Figure 6.13 and Figure 6.14.

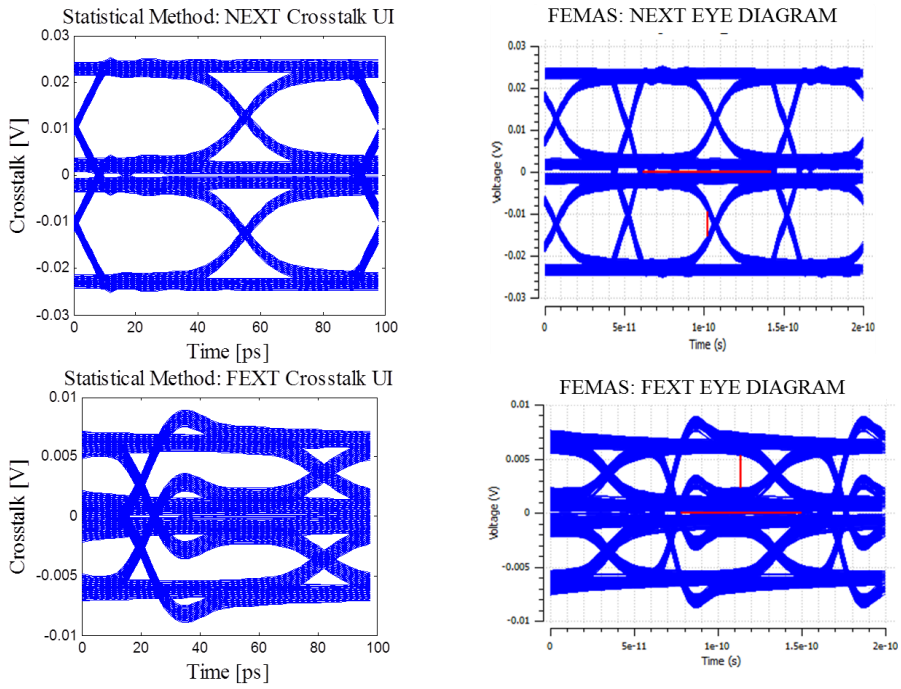


Figure 6.9. FEXT and NEXT crosstalk UI generated using 16 bit input sequences at the aggressor compared with FEMAS results of eye diagram using transient analysis and PRBS7.

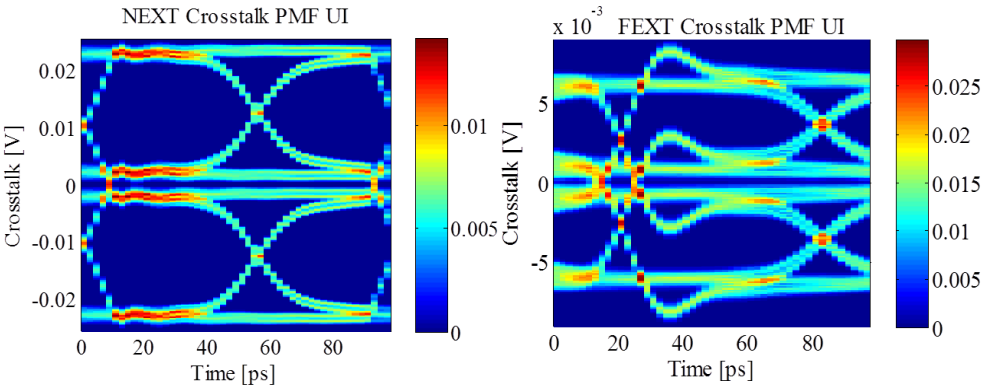


Figure 6.10. FEXT and NEXT crosstalk PMF UI generated using 16 bit input sequences at the aggressor.

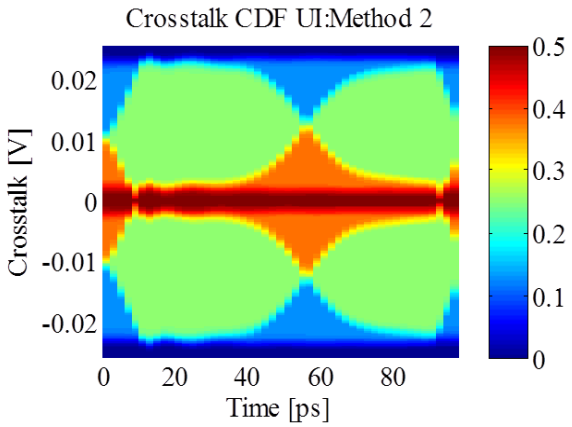


Figure 6.11. NEXT crosstalk CDF UI generated using 16 bit input sequences at the aggressor

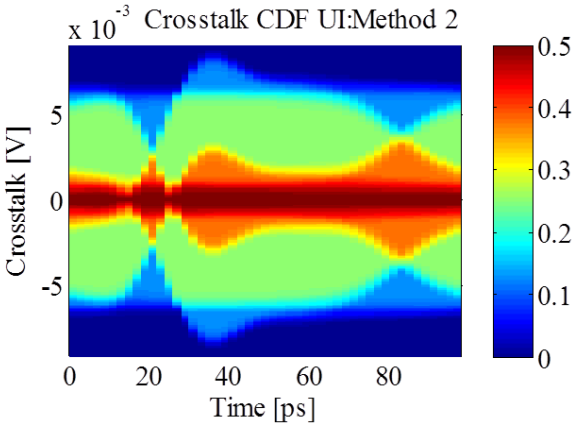


Figure 6.12. FEXT crosstalk CDF UI generated using 16 bit input sequences at the aggressor.

6.3.2. Backplane Connector Example. The proposed methodology can be used with the backplane connectors which typically have many aggressors for each victim link. The connector channels are mapped as shown in Figure 6.15, where the victim link at the center is considered and the links around it are considered as near-end aggressors. The S-parameters for the connector are used from [47], where the authors had measured the S parameters till 25 GHz. In order to avoid extrapolation of the S – parameters, a lower data rate of 1Gbps was chosen here, so the Nyquist frequency for the UI calculation is in-band.

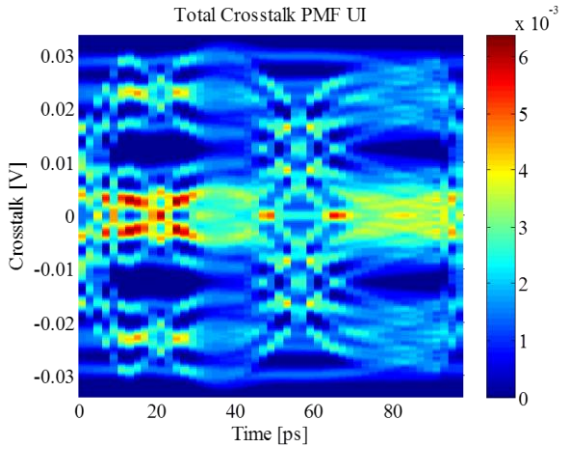


Figure 6.13. FEXT and NEXT used to get a total crosstalk PMF UI generated using 16 bit input sequences individually and then convoluted together with zero time skew between the sources.

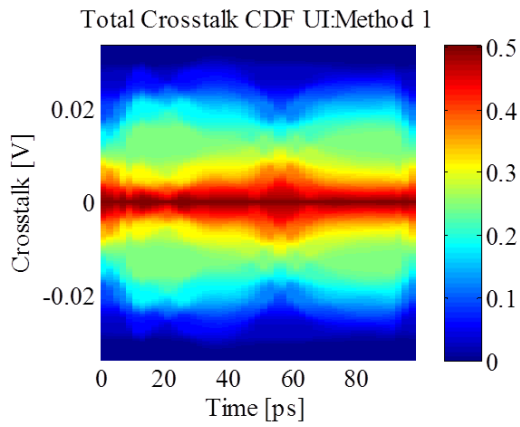


Figure 6.14. FEXT and NEXT used to get a total crosstalk CDF UI generated using total crosstalk PMF UI shown in Figure 6.13.

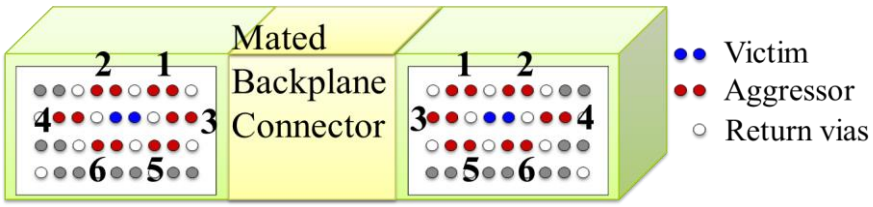
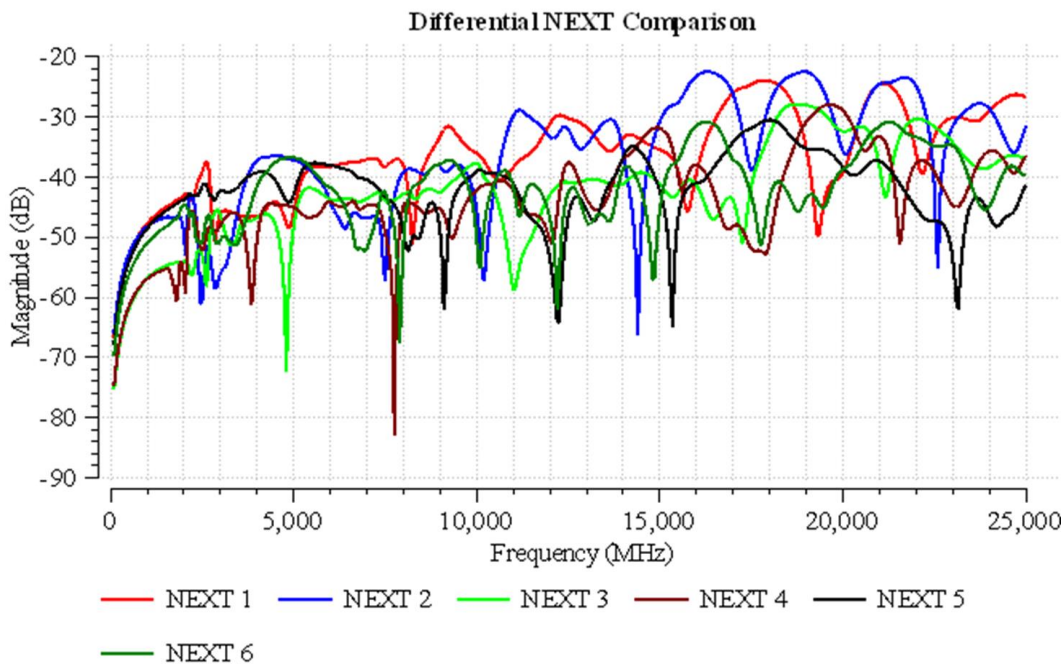


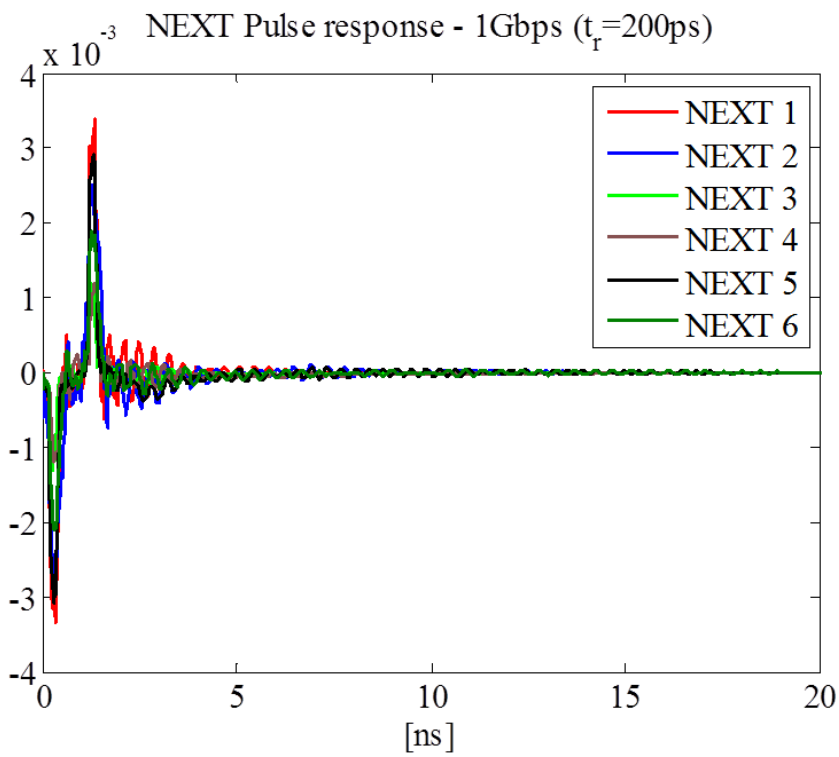
Figure 6.15. Backplane connector pin map of links for two parts of the connector.

The S-parameters for the near end crosstalk terms are shown in Figure 6.16 with the pulse response for the corresponding aggressor-victim combinations. FEMAS was used to generate the pulse response from the S-parameter block using transient analysis with a pulse source. The near end crosstalk does not have any time skews between the aggressors, but the amplitudes and shapes differ significantly. These differences are expected as each aggressor is placed at a different position and distance with respect to the victim. The individual crosstalk UIs are obtained and compared with one UI of the eye diagrams generated from the transient analysis in FEMAS, as shown in the Figure 6.17.



(a)

Figure 6.16. (a) Backplane connector s-parameters for corresponding to the near-end crosstalk terms. (b) Pulse response of the near-end crosstalk parameters.



(b)

Figure 6.16. (a) Backplane connector s-parameters for corresponding to the near-end crosstalk terms. (b) Pulse response of the near-end crosstalk parameters (cont.)

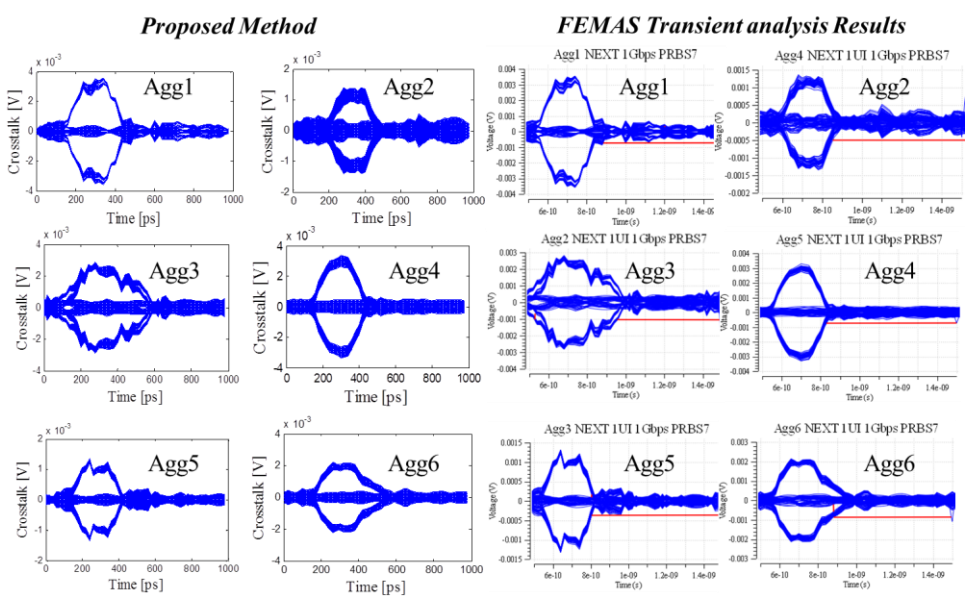


Figure 6.17. Comparison of the crosstalk UI from proposed method and the single UI of eye diagram generated using a transient analysis solver and PRBS7 source.

The individual crosstalk UIs can be converted to crosstalk PMF UI and then convolved together to form the total crosstalk PMF UI. Alternatively the total crosstalk PMF UI can be directly found from the individual pulse responses and then then converted to the crosstalk CDF UI. The Figure 6.18 shows the total crosstalk PMF UI and crosstalk CDF UI due to all 6 aggressors. To verify this last step, transient analysis was run in FEMAS with uncorrelated sources placed at Aggressor1 and Aggressor2, to get all the possible combinations of source bit sequences, and compared with the results from proposed method in Figure 6.19.

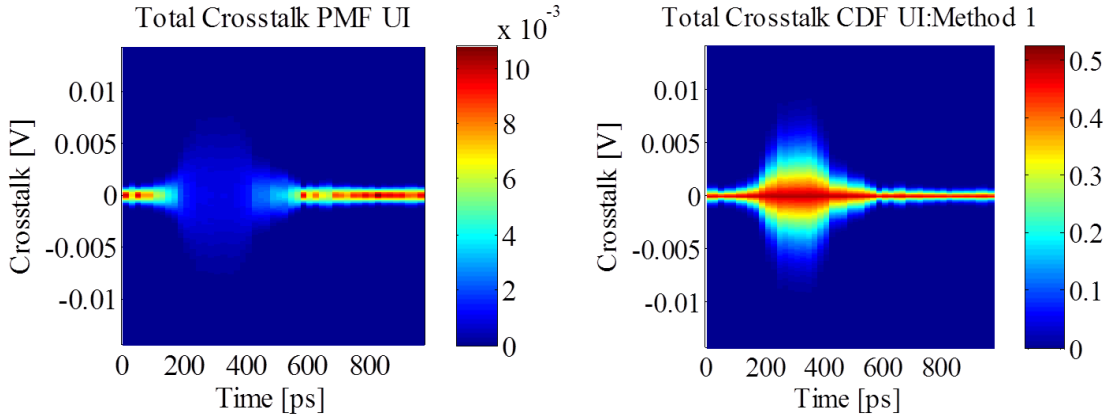


Figure 6.18. Total crosstalk PMF UI and total crosstalk CDF UI generated using the proposed methodology.

6.4. DISCUSSIONS

When there are multiple aggressors in the system, the proposed method requires the frequency domain S parameter characterization from simulation or measurements. These network parameters can be used with the said procedure to evaluate effect of individual aggressors using the crosstalk CDF UI. The critical sources can be used with different time skews to identify the worst case crosstalk and this can guide a strategy to mitigate the responsible sources. The two types of CDFs proposed are both complimentary to each other, and either can provide an insight into the possible crosstalk observable in the real system.

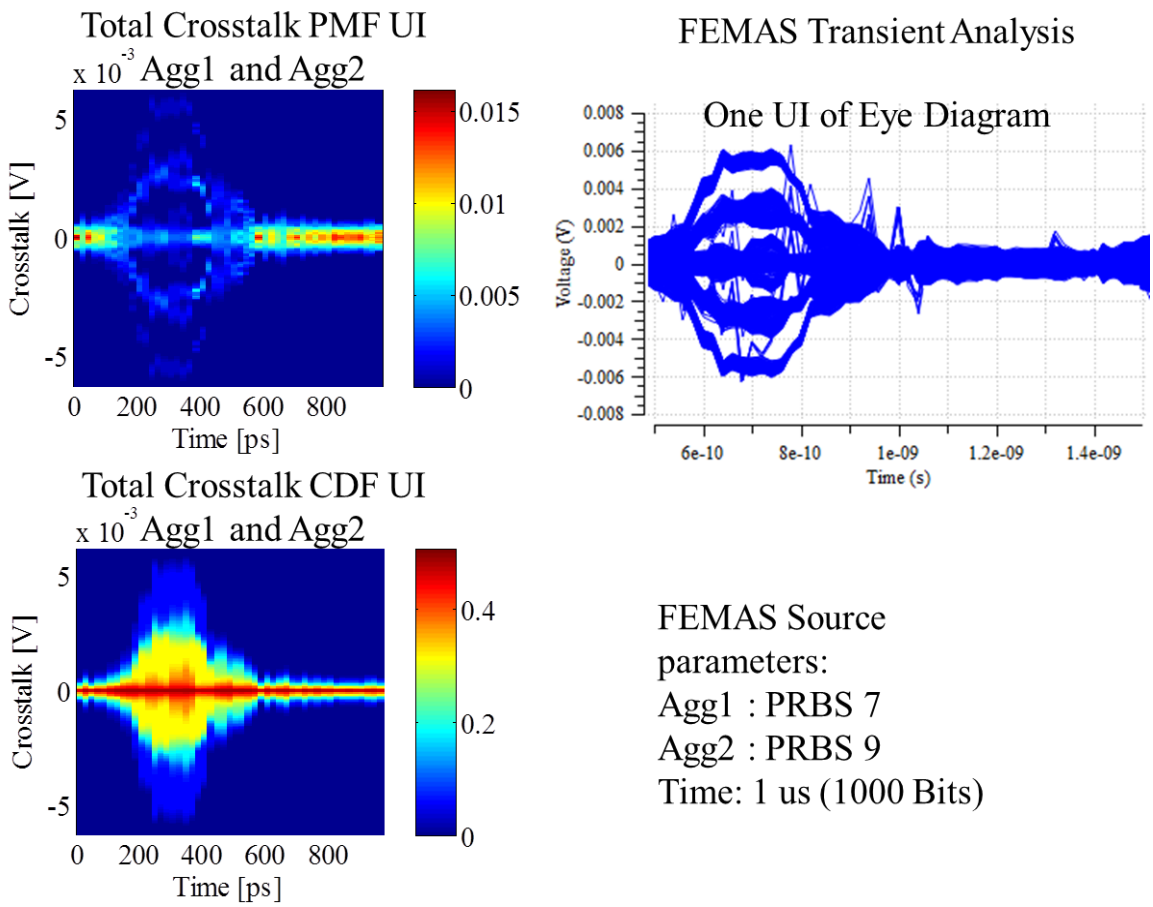


Figure 6.19. Total crosstalk PMF UI and total crosstalk CDF UI for Aggressor1 and Aggressor2 compared to one UI of eye diagram from FEMAS transient analysis.

The time skew between the sources used at each aggressor has a big effect on the total crosstalk UI, as it can add up or cancel the peaks of crosstalk in a UI. The effect of this time skew on total crosstalk has to be studied more with practical examples to demonstrate these effects. Further study for crosstalk connector and IC breakout region is planned where a number of aggressors is large and the propagation path has many discontinuities leading to a bigger impact of crosstalk on the channel eye diagram.

The PMF for crosstalk indicates the probability of crosstalk value in the UI. As most designers care about the maximum value of crosstalk in a design, only the envelope of maximum crosstalk value would be used. But in general where there are tradeoffs involved between designs, the probability associated with these occurrences of maximum

crosstalk may be considered. If the probability is very low for a particular maximum crosstalk value, the aggressor carrying such signal may be very unlikely, and could be avoided by software means for critical applications. These distributions are based on a deterministic approach to get the exact waveforms for crosstalk at the victim receiver. Then looking at a confidence or probability value for the crosstalk being less than a certain threshold would be more representative.

In real systems another factor that can affect the low crosstalk systems is the random noise effect. This has not been incorporated in the system, but can be added in later by convoluting a gaussian noise profile with the total crosstalk PMF UI, at each time slice of the UI. Another factor from the real systems is the random jitter in aggressor data, which can also be incorporated into the system by adding random delays in the waveform calculation of each aggressor crosstalk UI. This can also be extended to a deterministic jitter injection. These factors can be incorporated with some work, but do not prove to be the big control factors in the design as the primary issue is the magnitude of the crosstalk.

6.5. CONCLUSIONS

A solution was proposed to make better or informed design decisions with regards to signal routing and a criterion was proposed to evaluate the design. This method can estimate the individual and aggregated effect of many crosstalk sources in a system in time domain from the crosstalk S-parameters. The crosstalk UI calculation was validated using a transient analysis in a link path modeling tool. These crosstalk UI results were used to calculate the PMF and CDF of the UI. The CDF can be used to evaluate the design based on crosstalk above or below a certain value occurring with a calculable probability which can be setup as the tolerance of the system.

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