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Integration of energy storage components with cascaded H-bridge multilevel converters

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INTEGRATION OF ENERGY STORAGE COMPONENTS WITH CASCADED H-BRIDGE MULTILEVEL CONVERTERS

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ABSTRACT

In recent years, multilevel converters have gained considerable attention in medium-voltage motor drive and grid applications. This popularity is owed to their reduced voltage stress on the semiconductor devices used in their structure. In addition, multilevel converters generate near sinusoidal outputs with low harmonic distortions. Other advantages of such converters include inherent modularity and low dv/dt stresses. In general, multilevel power electronic converters are classified into three main topologies: diode-clamped, flying-capacitor, and cascaded H-bridge.

A cascaded H-bridge multilevel converter is created when several H-bridge cells are placed in series. Each H-bridge cell must be fed by a stiff voltage source. In earlier implementations, every one of these voltage sources had to contribute to the overall power supplied to the load. Later, it was demonstrated that under certain operating conditions, one can replace all but one of these sources with energy storage devices, e.g., capacitors. In other words, the entire power can be supplied by only one source. The replacing capacitors must only maintain a constant dc voltage supplying zero net power. Although this approach benefits from cost reductions, balancing the voltages across the replacing capacitors turns out to be a challenge.

In this thesis, the operating conditions under which the capacitor voltage regulation is feasible are first analytically investigated. The results show that the amplitude of the output voltage as well as the power factor of the load current determines the regulation range when the staircase modulation method is employed. In order to extend the regulation range for the replacing capacitors, a new control scheme—phase shift modulation—is proposed. This method is more robust when compared to existing methods. In this method, the main H-bridge cell of the multilevel converter operates at the fundamental frequency and the auxiliary cells run at the PWM frequency. Finally, the sigma-delta modulation method has been utilized to extend the capacitor voltage regulation range. This method benefits from simplicity in implementation in comparison to PWM techniques. The analytical and simulation results prove the effectiveness of the proposed approaches. They are also consistent with the results of the experiment.

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1. INTRODUCTION

Power electronic converters can be found wherever there is a need to modify the electrical energy form such as voltage, current, or frequency. Their power range is from some milliwatts as in a cell phone to hundreds of megawatts as in a HVDC transmission system. Industry has begun to demand higher power equipment. A continuous race to develop higher voltage and higher current power semiconductors to drive high power systems still goes on. Furthermore, the total harmonic distortion (THD) of the output voltage and the influence of the electromagnetic interference (EMI) need to be limited. For these reasons, multilevel converters have emerged as the solution for such applications.

The elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase or PWM voltage waveform. Solar cells, fuel cells, batteries, and ultra-capacitors are the most common sources used as the multiple dc voltage sources

A multilevel converter has several advantages over a conventional two-level converter which can be briefly summarized as follows.

One can not only generate output voltages with very low distortion but also can reduce the dv/dt stresses.

Multilevel converters produce smaller common mode voltage.

Multilevel converters can operate at both fundamental switching frequency and high PWM switching frequency which can decrease the switching loss and has less computational burden.

Modularity.

In general, multilevel converters are categorized into diode-clamped, flying capacitor, and cascaded H-bridge multilevel topologies. This thesis is focused on the cascaded H-bridge converters using a single dc source. It is composed of three papers. Some limitations on previous work will be discussed and two new control methods, the phase shift modulation technique and the unbalanced-voltage-level sigma-delta modulation technique are devised and introduced in these papers. Their contribution is to

balance the voltage across the capacitors as well as generate an output voltage with less total harmonic distortion.

In early implementations, each cell of the cascaded H-bridge multilevel converters was supplied by an independent dc source. However, only one cell needs to be supplied by a real dc power source and the remaining cells can be supplied with capacitors. Voltage regulation of the replacing capacitor is then a key issue. Previous works used switching state redundancy for the capacitor voltage regulation. In conventional methods, the existence of redundant switching states has been assumed to be adequate for the capacitor voltage regulation. However, the output current of the converter as well as the time duration of the redundant switching states greatly impact the charging and discharging patterns of the replacing capacitors. Different switching angles and different loads like a resistive load or a motor will generate different results which may cause the voltage of the capacitor not to be balanced.

A new control method named phase shift modulation technique is described in paper two to improve the capacitor voltage regulation. This method is more robust and has less of a computational burden. In this method, the main converter runs at the fundamental frequency and the auxiliary converter operates at the high PWM frequency. The output voltage is a combination of the voltage of the main converter and auxiliary converter in order to track the desired sinusoidal waveform. The idea of phase shift modulation is to keep the width of opening period of the main converter constant and then shift the rectangular waveform to right or left, so there is a time delay or advance between the main converter waveform and the desired sinusoidal signal. The capacitor will be charged during the right shift or discharged during the left shift periods. Therefore, through the right and left shifts, the voltage of the capacitor can be balanced.

Another control method, the unbalanced-voltage-level sigma-delta modulation technique, is described in paper three. This method also improves the capacitor voltage regulation. In previous work, the ratio between the main and auxiliary voltage sources has been selected to be either 2:1 or 3:1, which leads to some limitations on the capacitor voltage regulation. In the third paper, the voltage ratio of 4:1, which can simplify the control task, is proposed and successfully implemented. Furthermore, sigma-delta modulation (SDM) is proposed for voltage regulation across the replacing capacitors in

the auxiliary cell by replacing the binary quantizer with an N-level quantizer corresponding to the number of the levels of the multilevel converter. The modulator design task requires appropriate selection of the amplifier gain, the saturation limits of the integrator block, the sampling frequency, and the threshold of the hysteresis loop. The design principle of these parameters will be given and the analysis of the advantages of 4:1 ratio will be discussed. Unbalanced-voltage-level sigma-delta modulation technique can be easily implemented in digital control since almost all the signals are digital signals.

Paper

1. Cascaded H-Bridge Multilevel Converters - A Reexamination

Abstract- Multilevel power electronic converters have gained popularity in high-power applications due to their lower switch voltage-stress and modularity. Cascaded H-bridge converters are a promising breed of multilevel converters which generally require several individual dc voltage sources. Recently, the existence of a redundant switching state has been proposed to be utilized to replace the individual dc voltage sources with capacitors except for the one with the highest voltage level. Redundancy in the charge and discharge modes of the capacitors is assumed to be adequate for their voltage regulation. However, the effects of the output current of the converter as well as the time duration of the redundant switching states have been neglected. In this paper, the impacts of the connected load to the cascaded H-bridge converter as well as the switching angles on the voltage regulation of the capacitors are studied. This study proves that voltage regulation is only attainable in a much limited operating conditions that it was originally reported.

Key words-cascaded H-bridge converters; multilevel converters, voltage regulation

I. Introduction

Multilevel power electronic converters are mainly utilized to synthesize a desired single- or three-phase voltage waveform. The desired output voltage is obtained by combining several individual dc voltage sources [1]. Solar cells, fuel cells, batteries, and ultra-capacitors are the most common sources used. The main advantages of such converters are the low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency, the capability to operate at higher voltages, and modularity [2]. In general, multilevel converters are categorized into diode-clamped, flying capacitor, and cascaded H-bridge topologies [1, 3-5].

Diode-clamped multilevel converters are used in conventional high-power ac motor drive applications like conveyors, pumps, fans, and mills. They are also utilized in oil, gas, metals, power, mining, water, marine, and chemical industries. They have also been reported to be used in a back-to-back configuration for regenerative applications [6]. Flying capacitor multilevel converters have been used in high-bandwidth high-switching frequency applications such as medium-voltage traction drives [7]. Finally, cascaded H-bridge multilevel converters has been applied where high-power and power-quality are essential, e.g., static VAR generation (SVG) [8], active filter and reactive power compensation applications [9], photovoltaic power conversion [10], uninterruptible power supplies, and magnetic resonance imaging.. Furthermore, one of the growing applications for multilevel motor drives is electric and hybrid power trains. Normally, electric and hybrid vehicles use batteries to drive an electric motor. In high-power rating large vehicular motor drives (>250 kW), multilevel converters are suitable due to their high volt-ampere ratings. Multilevel converters can also solve the existing problems

associated with some of the present two-level PWM adjustable-speed motor drives since they can reduce the common-mode voltage causing the bearing leakage current [6].

Fig. 1 shows the circuit topology of the cascaded H-bridge multilevel converter [1]. The converter consists of n series-connected H-bridge cells which are fed by independent voltage sources. Depending on the conduction status of four switches S_1, S_2, S_3, and S_4 in each cell, as depicted in Fig. 2, each converter cell can generate three different voltage levels of $+V_n$, 0, and $-V_n$. The outputs of H-bridge cells are connected in series such that the synthesized voltage waveform is the sum of all of the individual cell outputs. The output voltage is given by

$$V_a = V_{a1} + V_{a2} + ... + V_{an} \tag{1}$$

where the output voltage of cell H1 is labeled Va1 and the output voltage of cell H_n is denoted by V_{an}. Letter ‘a’ is used for phase a in case a three-phase converter is considered.

In early implementations [11-14], each H-bridge cell was supplied by an independent dc source. However, it has been shown that only one cell needs to be supplied by a real dc power source and the remaining cells can be supplied with capacitors replacing their dc sources [12, 15]. Voltage regulation of the replacing capacitor is then a key issue. The proposed method in [15] uses the switching state redundancy for the capacitor voltage regulation. The existence of redundant switching states has been assumed to be adequate for the capacitor voltage regulation. However, the output current of the converter as well as the time duration of redundant switching states greatly impact the charging and discharging patterns of the replacing capacitors.

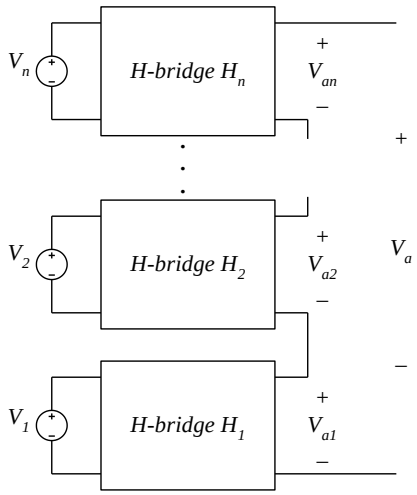


Fig. 1. The structure of a cascaded H-bridge converter

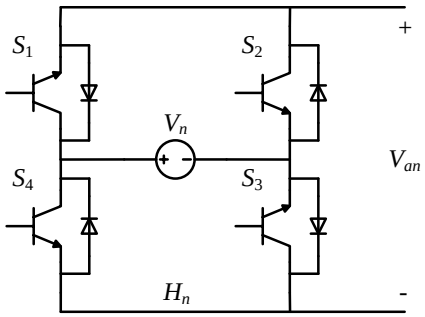


Fig. 2. The structure of an H-bridge converter cell

In this paper, the impact of the electric load connected to H-bridge multilevel converters as well as the switching angles on voltage regulation of the replacing capacitors will be studied. This study proves that voltage regulation is only achievable in a much limited conditions that it was originally reported [15]. In Section II, the principles of operation of multilevel H-bridge converters and switching angles are briefly

introduced. In Section III, multilevel H-bridge converters are used to drive two different types of load. Voltage regulation in each case is studied using simulation results. In Section IV, the hardware experiment results are given. Finally, Section V draws the conclusions based on the presented results and provides an overall evaluation of single-dc-source multilevel converters.

II. Cascaded H-Bridge Multilevel Converter

In this section, without loss of generality, a cascaded multilevel converter with only two H-bridge cells is considered. V_1 and V_2 in Fig. 1 are stiff voltages such as batteries, fuel cells, photovoltaic cells, capacitors, or ultra-capacitors. Here, they will all be referred to as voltage sources even though they may not be a real source.

Effective number of output voltage levels S depends on the ratio between the dc sources V_1 and V_2 as shown in Table 1. For example, for a two-cell converter (n=2), output voltage V_{a1} is either $-V_1$, 0, or $+V_1$ while the output voltage of H_2 can be either $-V_2$, 0, or $+V_2$. Accordingly, the output voltage of the converter in different cases is shown in Table 2.

Table 1. Relationship Between the Number of Voltage Levels and the Number of Sources

Voltage levels (i=2,…, n)	Number of levels S	Redundancy
Independent	3^n	0
$V_{a(i-1)} = V_{ai}$	2n+1	3^n-(2n+1)
$V_{a(i-1)} = 2V_{ai}$	2^{n+1}-1	3^n-(2^{n+1}-1)

Table 2. Output Voltage of a Multilevel Converter with Two Cells

V_{a1}	V_{a2}	V_{an} (V_1 and V_2 are independent)	V_{an} ($V_1=V_2=V_{dc}$)	V_{an} ($V_1=V_{dc}=2V_2$)
V_1	V_2	V_1+V_2	$2V_{dc}$	$3V_{dc}/2$
V_1	0	V_1	V_{dc}	V_{dc}
V_1	$-V_2$	V_1-V_2	0	$V_{dc}/2$
0	V_2	V_2	V_{dc}	$V_{dc}/2$
0	0	0	0	0
0	$-V_2$	$-V_2$	$-V_{dc}$	$-V_{dc}/2$
$-V_1$	V_2	$-V_1+V_2$	0	$-V_{dc}/2$
$-V_1$	0	$-V_1$	$-V_{dc}$	$-V_{dc}$
$-V_1$	$-V_2$	$-V_1-V_2$	$-2V_{dc}$	$-3V_{dc}/2$

As it can be observed from Table 2, if $V_1=V_2$, the output voltage has only five (5) levels; therefore, the total harmonic distortion of the output voltage is higher than when V_1 and V_2 are independent. Regarding redundancy, in case $V_1=V_{dc}=2V_2$, the output voltage level at $V_{dc}/2$ can be generated in two different ways. One is to choose $V_{a1}=V_{dc}$ and $V_{a2}=-V_{dc}/2$. In this case, V_2 will be charged for positive output currents. The second way is to choose $V_{a1}=0$ and $V_{a2}=V_{dc}/2$. In this case, V_2 will be discharged for positive output currents. A similar argument can be made when the desired output voltage is

$-V_{dc}/2$. Therefore, the output voltage will have seven levels as illustrated in Fig. 3 [10]. θ_1, θ_2, and θ_3 are the switching angles ($0 < \theta_1 < \theta_2 < \theta_3 < \pi/2$).

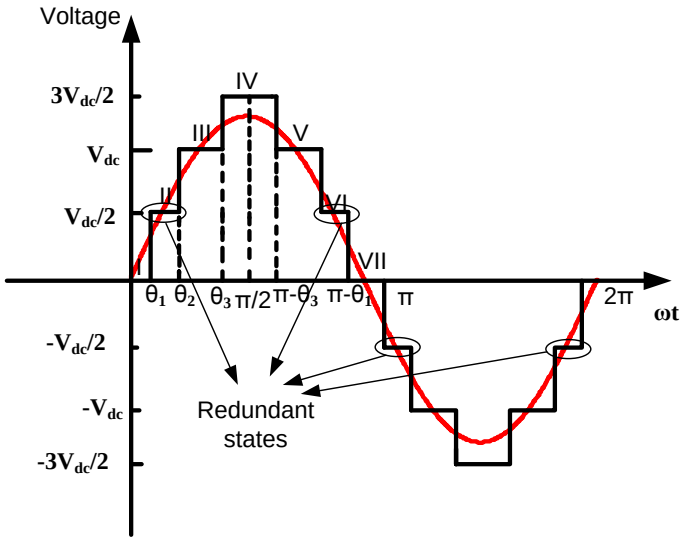


Fig. 3. Output voltage waveform of a 7-level cascaded H-bridge converter

The existence of the redundant states can be used to replace V_2 with a capacitor and provide voltage regulation across its voltage [15]. Also, a technique to regulate the voltage of the replacing capacitor is described in [12]. For highest and lowest output voltage levels $V_{an}=3V_{dc}/2$ and $-3V_{dc}/2$ there is no redundancy available for capacitor voltage balancing. In these two states, the capacitor will always be discharged. So these states have been ignored in [12]. The compromise is that it would result in an only 5-level operation and therefore increased total harmonic distortions. Another approach to balance the voltage of the capacitor is to use the redundant states and select the appropriate switching angels which will be described here.

III. Cascaded H-Bridge Multilevel Converter Working with Different Loads

The Fourier series expansion of the output voltage waveform which is shown in Fig. 3 is [15].

$$V_a(\omega t) = \frac{4}{\pi}\frac{V_{dc}}{2}\sum_{n=1,3,5}^{\infty}\frac{1}{n}(\cos(n\theta_1)+\cos(n\theta_2)+\cos(n\theta_3))\sin(n\omega t) \tag{2}$$

If the amplitude of the fundamental harmonic of phase *a* is desired to be $V_{a,1}$, by choosing appropriate values for the angles, one can eliminate the 5th and 7th order harmonics [12]. The third harmonic will be automatically cancelled in a balanced three-phase system. Therefore,

$$\begin{aligned}&\frac{4}{\pi}\frac{V_{dc}}{2}(\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)) = V_{a,1}\\ &\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3) = 0\\ &\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3) = 0\end{aligned} \tag{3}$$

In order to solve the system of equations in (3), several approaches, including resultant theory, have been proposed [15, 17]. In addition to the discussed methods, one can use MATLAB nonlinear solvers to solve this nonlinear system of equations. This method can be used without dealing with complexity of previously proposed methods [15, 17]. The solutions of the angles using MATLAB solver is depicted in Fig. 4 where modulation index *m* is defined to be $V_{a,1}/(4V_{dc}/2\pi)$. As it is shown in this figure, when *m* is between 1.488 and 1.852, solving the equations leads to two sets of answers. In other word, in this range creating the required *m* and eliminating the 5th and 7th harmonics is possible by two sets values for θ_1, θ_2, and θ_3.

Based on the nature of the load, the switching scheme may or may not be able to regulate the voltage across the replacing capacitor. The existence of redundant switching

states has been assumed to be adequate for capacitor voltage regulation [18, 19]. However, output current of the converter as well as the time duration of redundant switching states greatly impact the charging or discharging patterns of the replacing capacitor. In the following sub-sections, capacitor voltage regulation has been re-examined for two cases of resistive and inductive. For the following demonstrations, V_{dc} is considered to be 100 V and the replacing capacitor is chosen to be 100 μF. The control objective is to regulate the capacitor voltage at 50 V (V_{dc}/2).

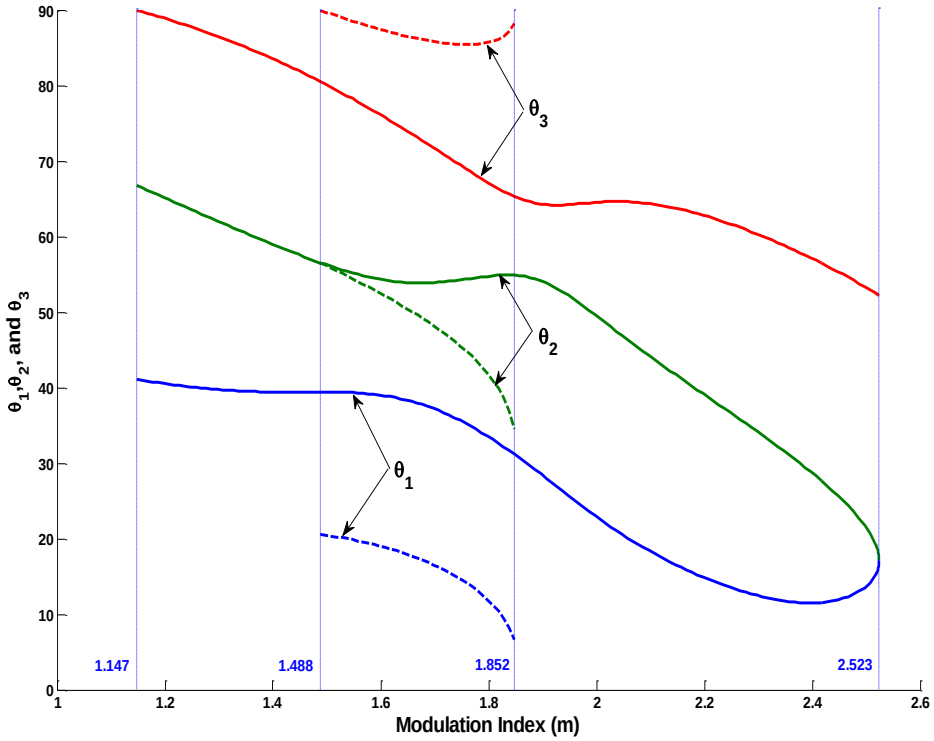


Fig. 4. Solution for the switching angles

1. Multilevel converter is used to drive a resistive load

Case A: If modulation index *m* is desired to be 1.2, the switching angles should be θ_1=40.5º, θ_2=65.1º, and θ_3=88.9º. The simulation results for the replacing capacitor voltage and output voltage waveform are depicted in Figs. 5 and 6, respectively. As it can be observed from the simulation results, the regulation of the capacitor voltage is feasible if θ_3 is very close to $\pi/2$.

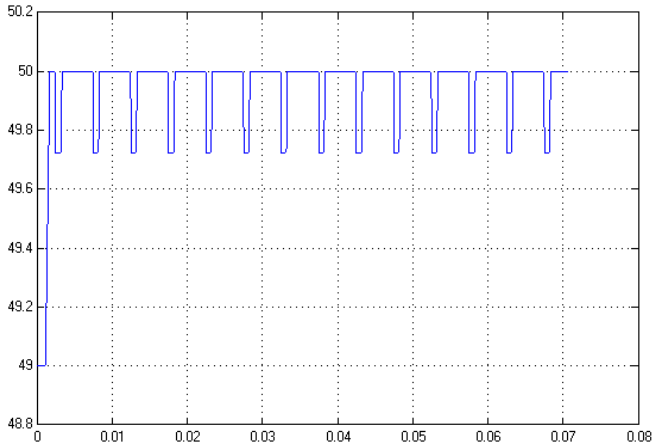


Fig. 5. Capacitor voltage is regulated at 50 V (Case A) (time in *s* and voltage in *V*)

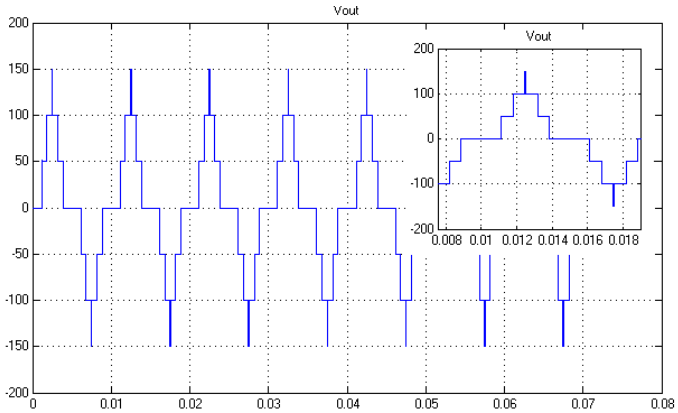


Fig. 6. The output voltage of the seven-level multilevel converter (Case A) (time in *s* and voltage in *V*)

*Case B***:** If a larger modulation index is desired, e.g., m=2.4, the switching angles should be selected to be θ_1=11.5º, θ_2=28.7º, θ_3=57.1º. With this set of angles, the capacitor charging time is less than its discharging time. Therefore, the voltage of the capacitor will not sustain a constant level and will decrease continuously. This can be seen in Fig.7 and 8. Therefore one cannot regulate the capacitor voltage in this case.

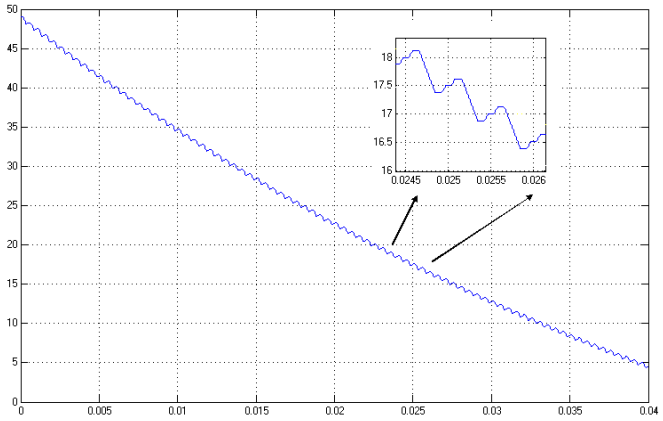


Fig. 7. Capacitor voltage in case B (time in *s* and voltage in *V*)

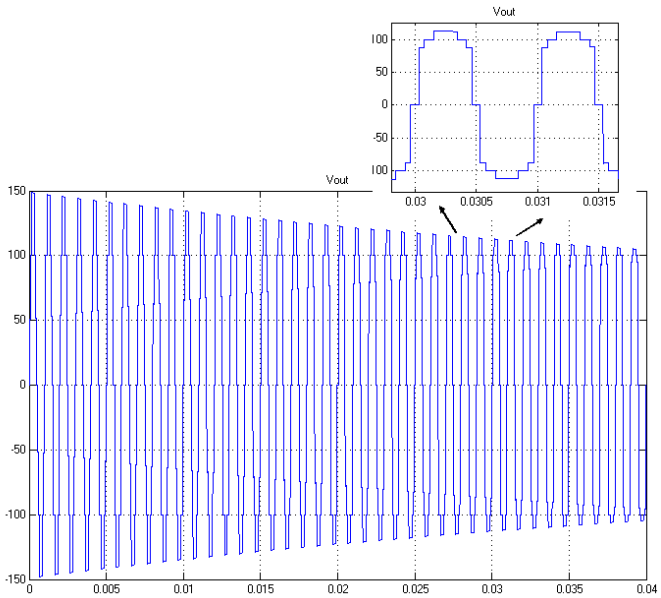


Fig. 8. Output voltage Waveform in case B (time in *s* and voltage in *V*)

Based on Fig. 3, one fourth of the period can be divided into the following subintervals

I	$0 < \omega t < \theta_1$	no capacitor charge or discharge
II.	$\theta_1 < \omega t < \theta_2$	capacitor charge or discharge depending on the capacitor voltage
III.	$\theta_2 < \omega t < \theta_3$	no capacitor charge or discharge
IV.	$\theta_3 < \omega t < \pi-\theta_3$	capacitor discharge
V.	$\pi-\theta_3 < \omega t < \pi- \theta_2$	no capacitor discharge
VI.	$\pi - \theta_2 < \omega t < \pi-\theta_1$	capacitor charge or discharge depending on the capacitor voltage
VII.	$\pi - \theta_1 < \omega t < \pi$	no capacitor charge or discharge

In order to achieve capacitor voltage regulation, the capacitor discharge in subinterval IV must be less than the capacitor charge in subintervals II and VI. Assuming that the initial voltage of the capacitor is $V_{dc}/2$, one can express the capacitor voltage in subinterval II as

$$V_c(\omega t) = V_{dc} - \frac{1}{2}V_{dc}e^{-\frac{\omega t-\theta_1}{\omega^*\tau}} \tag{4}$$

where $\tau=R*C$. R is the load resistance. Final value of the capacitor voltage at the end of subinterval II is

$$V_c(\theta_2) = V_{dc} - \frac{1}{2}V_{dc}e^{-\frac{\theta_2-\theta_1}{\omega^*\tau}} \tag{5}$$

Therefore, one can say the capacitor voltage in subinterval II has increased by

$$\Delta V_c(T_2) = \frac{V_{dc}}{2}(1 - e^{-\frac{\theta_2 - \theta_1}{\omega^* \tau}}) \tag{6}$$

where T_2 is the duration of subinterval II. In subinterval III, capacitor is not involved and obviously $V_c(\theta_3) = V_c(\theta_2)$. For the fourth subinterval, one can write

$$V_c(\omega t) = -V_{dc} + 2V_{dc} e^{-\frac{\omega t - \theta_3}{\omega \tau}} - \frac{V_{dc}}{2} e^{-\frac{\omega t + \theta_2 - \theta_1 - \theta_3}{\omega \tau}} \tag{7}$$

Final value of the capacitor voltage at end of the fourth subinterval is

$$V_c(\pi - \theta_3) = -V_{dc} + 2V_{dc} e^{-\frac{\pi - 2\theta_3}{\omega \tau}} - \frac{V_{dc}}{2} e^{-\frac{\pi + \theta_2 - \theta_1 - 2\theta_3}{\omega \tau}} \tag{8}$$

where T_4 is the duration of subinterval IV. Then the capacitor voltage drop in subinterval IV is

$$\Delta V_c(T_4) = -2V_{dc} + 2V_{dc} e^{-\frac{\pi - 2\theta_3}{\omega \tau}} - \frac{V_{dc}}{2} e^{-\frac{\pi + \theta_2 - \theta_1 - 2\theta_3}{\omega \tau}} + \frac{1}{2} V_{dc} e^{-\frac{\theta_2 - \theta_1}{\omega^* \tau}} \tag{9}$$

In subinterval V, capacitor is not involved and obviously $V_c(\pi\text{-}\theta_2) = V_c(\pi\text{-}\theta_3)$. During subinterval VI, if capacitor is charged, then one can describe the voltage across the capacitor as

$$V_c(\omega t) = V_{dc} + (-2V_{dc} + 2V_{dc} e^{-\frac{\pi - 2\theta_3}{\omega \tau}} - \frac{V_{dc}}{2} e^{-\frac{\pi + \theta_2 - \theta_1 - 2\theta_3}{\omega \tau}}) e^{-\frac{\omega t - \pi + \theta_2}{\omega \tau}} \tag{10}$$

In subinterval VII, capacitor is not involved and obviously $V_c(\pi) = V_c(\pi\text{-}\theta_1)$. One can describe the final value of the capacitor voltage as

$$V_c(\pi) = V_{dc} + (-2V_{dc} + 2V_{dc} e^{-\frac{\pi - 2\theta_3}{\omega \tau}} - \frac{V_{dc}}{2} e^{-\frac{\pi + \theta_2 - \theta_1 - 2\theta_3}{\omega \tau}}) e^{-\frac{\theta_2 - \theta_1}{\omega \tau}} \tag{11}$$

or

$$V_c(\pi) = V_{dc} - 2V_{dc}e^{-\frac{\theta_2-\theta_1}{\omega\tau}} + 2V_{dc}e^{-\frac{\pi-2\theta_3+\theta_2-\theta_1}{\omega\tau}} - \frac{V_{dc}}{2}e^{-\frac{\pi+2\theta_2-2\theta_1-2\theta_3}{\omega\tau}} \tag{12}$$

Therefore, the capacitor voltage has increased in subinterval VI by

$$\begin{aligned}\Delta Vc(T_6) = {} & 2V_{dc} - 2V_{dc}e^{-\frac{\theta_2-\theta_1}{\omega\tau}} + 2V_{dc}e^{-\frac{\pi-2\theta_3+\theta_2-\theta_1}{\omega\tau}} - \frac{V_{dc}}{2}e^{-\frac{\pi+2\theta_2-2\theta_1-2\theta_3}{\omega\tau}} \\ & - 2V_{dc}e^{-\frac{\pi-2\theta_3}{\omega\tau}} + \frac{V_{dc}}{2}e^{-\frac{\pi+\theta_2-\theta_1-2\theta_3}{\omega\tau}}\end{aligned} \tag{13}$$

where T_6 is the duration of subinterval VI. For successful capacitor voltage regulation, one needs to have

$$\left|\Delta V_c(T_4)\right| \le \left|\Delta V_c(T_2)\right| + \left|\Delta V_c(T_6)\right| \tag{14}$$

The constraint on the switching angles that must be satisfied can be described as

$$\begin{aligned}& 2V_{dc} - 2V_{dc}e^{-\frac{\pi-2\theta_3}{\omega\tau}} + \frac{V_{dc}}{2}e^{-\frac{\pi+\theta_2-\theta_1-2\theta_3}{\omega\tau}} - \frac{1}{2}V_{dc}e^{-\frac{\theta_2-\theta_1}{\omega^*\tau}} \le \frac{V_{dc}}{2}(1-e^{-\frac{\theta_2-\theta_1}{\omega^*\tau}}) + \\ & 2V_{dc} - 2V_{dc}e^{-\frac{\theta_2-\theta_1}{\omega\tau}} + 2V_{dc}e^{-\frac{\pi-2\theta_3+\theta_2-\theta_1}{\omega\tau}} - \frac{V_{dc}}{2}e^{-\frac{\pi+2\theta_2-2\theta_1-2\theta_3}{\omega\tau}} - 2V_{dc}e^{-\frac{\pi-2\theta_3}{\omega\tau}} + \frac{V_{dc}}{2}e^{-\frac{\pi+\theta_2-\theta_1-2\theta_3}{\omega\tau}}\end{aligned} \tag{15}$$

Equation (15) can be simplified to

$$\frac{1}{2} - 2e^{-\frac{\theta_2-\theta_1}{\omega\tau}} + 2e^{-\frac{\pi-2\theta_3+\theta_2-\theta_1}{\omega\tau}} - \frac{1}{2}e^{-\frac{\pi+2\theta_2-2\theta_1-2\theta_3}{\omega\tau}} \ge 0 \tag{16}$$

Since the capacitor for the auxiliary converter is chosen to be a big capacitor, we can make some assumption to simplify equation (16) and achieve a simpler formula. If we assume that time of each subinterval of the output voltage waveform is less $\tau=R^*C$ by expansion of exponential terms of the equation (16) and using only two first term of the series equation (16) can be simplified as

$$-\theta_1+\theta_2+3\theta_3>\frac{3\pi}{2} \tag{17}$$

The predictions of (16) and (17) on capacitor voltage regulation agree with the simulation results. Using (16) or (17) one can identify the regulation regions (see Fig. 9). In this figure regulate-able range is shown in solid lines while unregulated-able part is depicted in dashed lines.

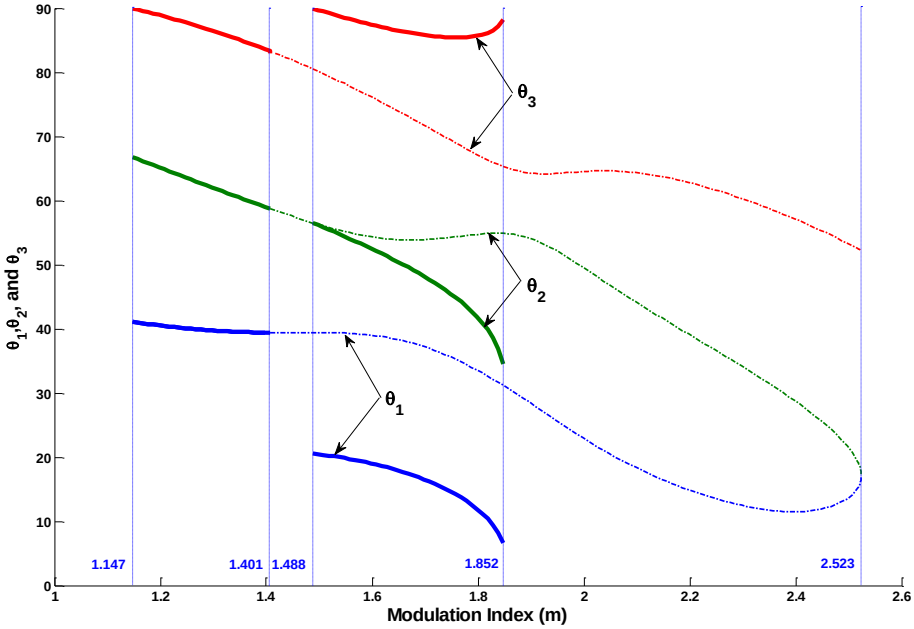


Fig. 9. Voltage regulation region when load is resistive

2. Multilevel converter is used to drive an inductive load

In this case, a three-phase Y-connected H-bridge cascaded multilevel converter was used to drive and induction motor (see Fig. 10) [21-23]. Simulation results for the output

voltage, output current, and capacitor voltage are depicted in Figs. 11, 12, and 13, respectively. In these results, per-phase L is 2 mH and per-phase R is 10Ω. As it can be observed, the capacitor voltage is regulated.

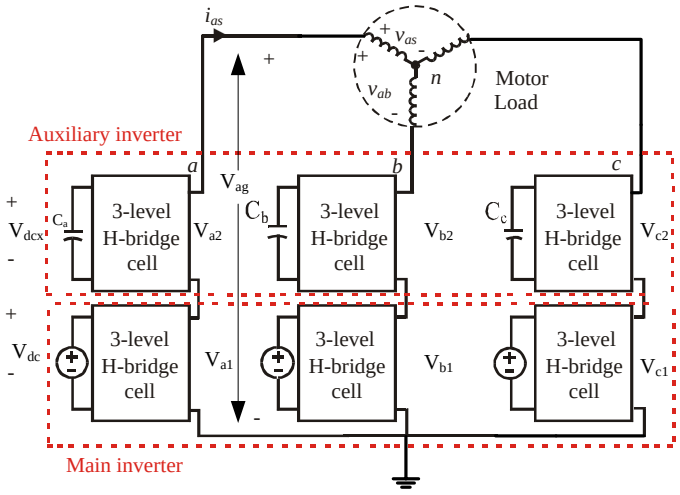


Fig. 10. Block diagram of the system when an inductive three-phase load is considered.

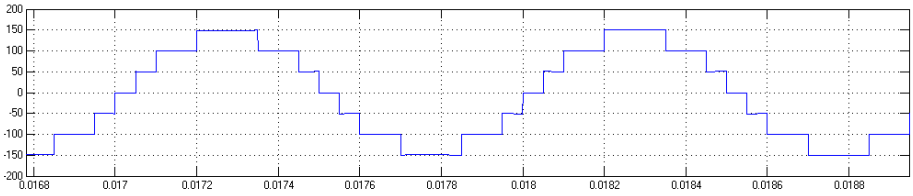


Fig. 11. Output voltage waveform of the seven-level multilevel converter driving an induction motor (time in *s* and voltage in *V*)

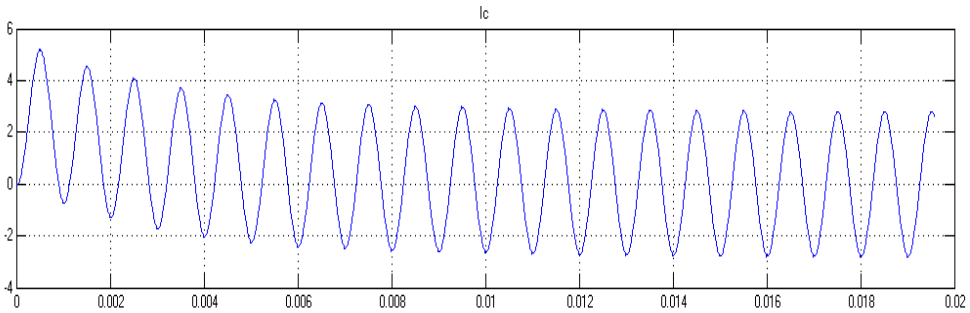


Fig. 12. Output current waveform of the seven-level multilevel converter driving an induction motor (time in *s* and current in *A*)

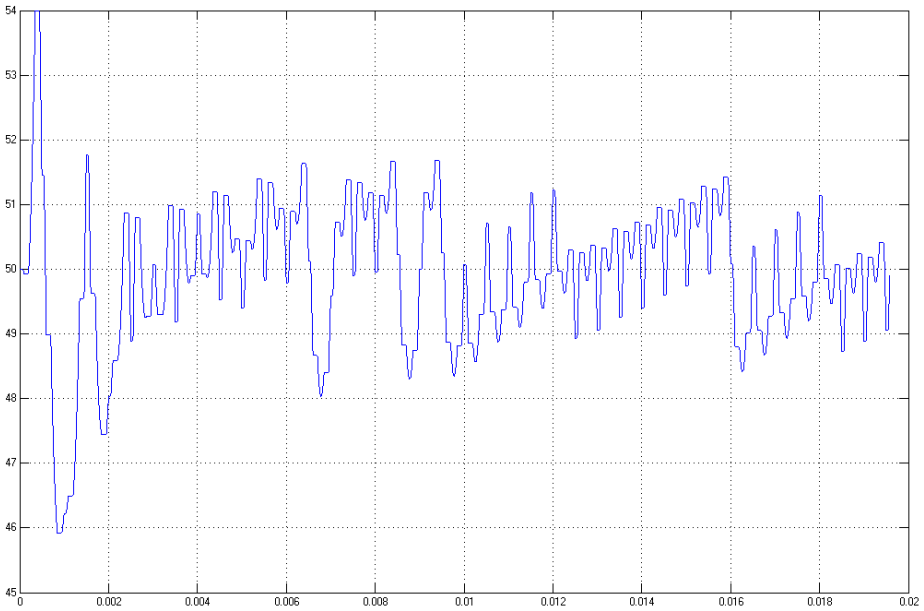


Fig. 13. Regulated capacitor voltage waveform (time in *s* and voltage in *V*)

The inductor motor as the load resembles a resistor in series with an inductor. In order to study the effect of power factor on the capacitor voltage regulation, the overall impedance of the load is kept to be constant at 9 Ω per phase. Then different values for the power factor were considered. Ultimately, for each value for the power factor, the entire range of modulation index *m* was investigated for capacitor voltage regulation.

The results are depicted in Fig. 14. One can observe that when the load is more like an inductive load (low power factor); the regulation region will extend to almost the entire region. However, the power factor is very low which means the efficiency is low. Normally the power factor of the motor is above 0.8 where the capacitor voltage regulation region faces limitations.

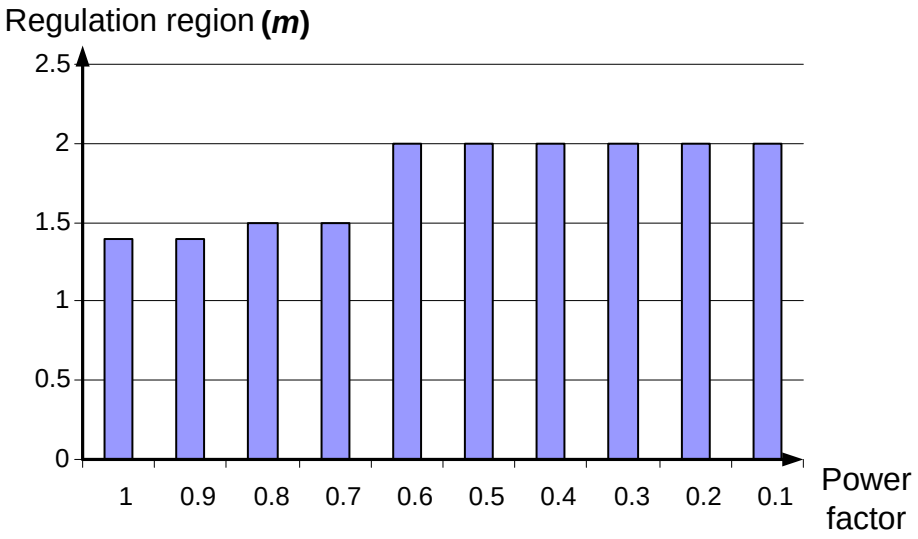


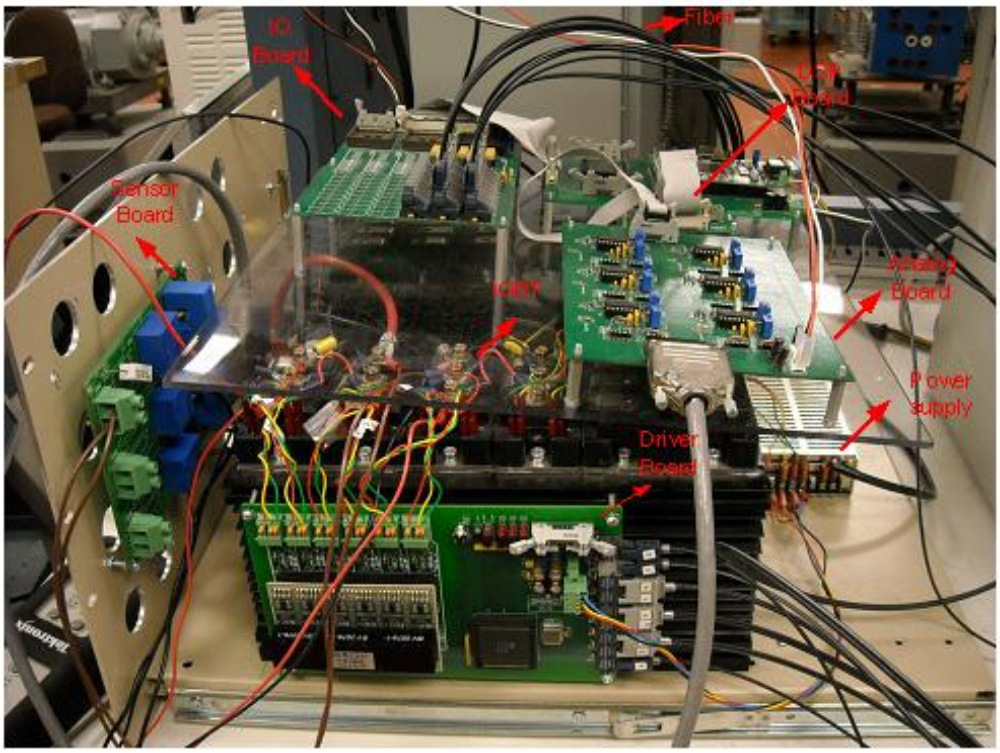
Fig. 14. Effect of power factor on the capacitor voltage regulation

IV. Experiment Results

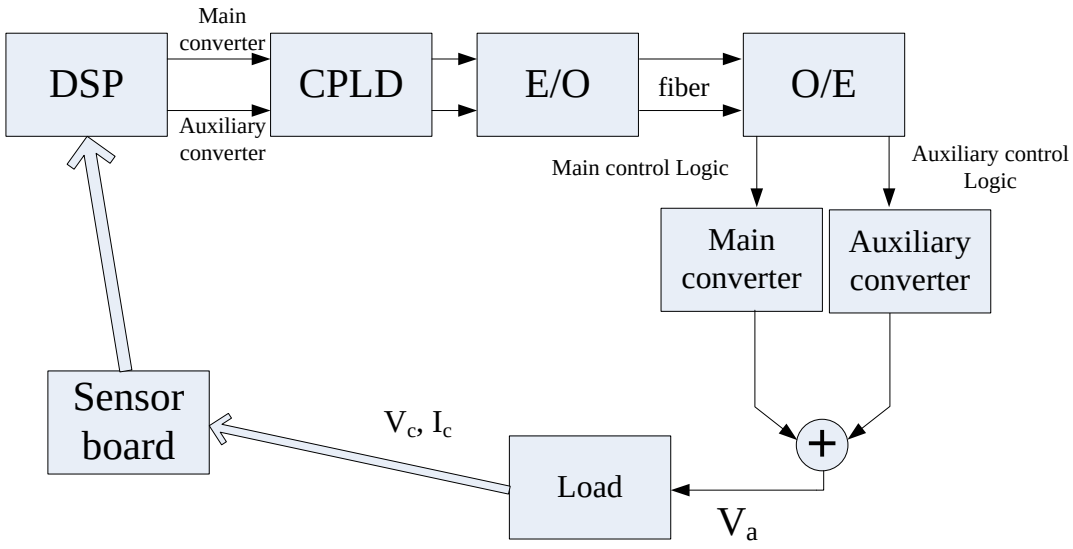
In order to verify the simulation and analytical results, a low-voltage low-power hardware prototype of the system was developed as depicted in Fig.15. Two cascaded H-bridge cells feed a resistive load (2.2 kΩ). The main cell is fed by a 20 V dc source. A 2.1 mF capacitor is used as the source for the auxiliary cell. The voltage of the capacitor is expected to be regulated at 10 V. This level is half of the main cell voltage. The

control scheme is programmed in a TI-TMS3202812 digital signal processor (DSP) and CY37128P84 complex programmable logic device (CPLD) which is connected to drive CM75DU-24F the Insulated-gate bipolar transistors (IGBT) through optical fiber. Furthermore, the sensor board is used to monitor the voltage of the capacitor and then feedback to DSP thought voltage shift.

Two data sets are provided here. First, in test I, θ_1, θ_2, θ_3 were selected to be 40 º, 65 º, and 89 º, respectively. In this case, capacitor voltage regulation is expected to happen. Fig. 16(a) depicts the variations of the capacitor voltage during the test. At point A, capacitor voltage is about 6 V which is lower than 10 V. Therefore, based on the control rules, charging opportunities for the capacitor are selected. Point B indicates when capacitor voltage is about 10 V. As it can be observed, capacitor charging was successfully performed. Figs. 16(b) and 16(c) depict the output voltage at points A and B, respectively. In test II, θ_1, θ_2, θ_3 were selected to be 12 º, 28 º, and 56 º, respectively. In this case based on the analytical and simulation analysis, capacitor voltage regulation is not doable. As Fig. 17(a) depicts, the capacitor starts with being charged at 10 V. Even though the controller selected charging states for the capacitor, its voltage drops to 0 V (see point D in Fig. 17(a)). Figs. 17(b) and 17(c) depict the output voltage at points C and D, respectively. As it can be observed, the output voltage waveform gradually deteriorates as the capacitor gets discharged. The hardware experimental results agree with the theory.



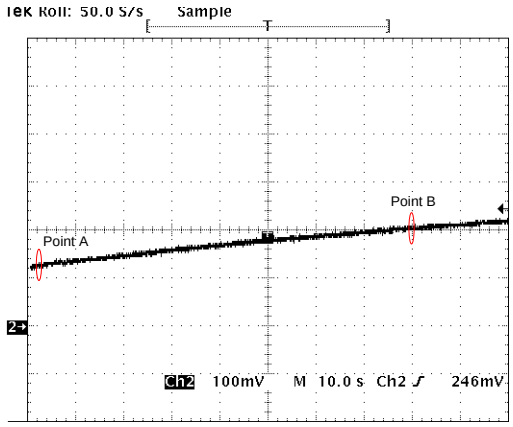
(a)



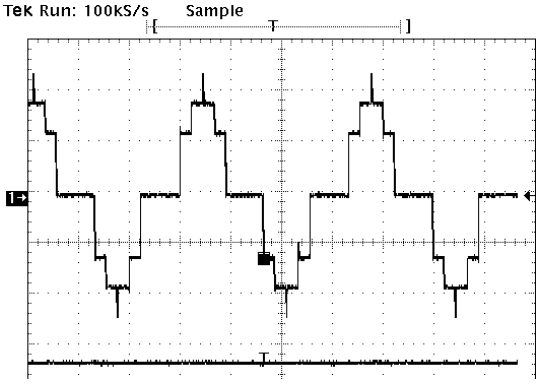
(b)

Fig. 15(a). Hardware implement of Cascaded H-bridge converters

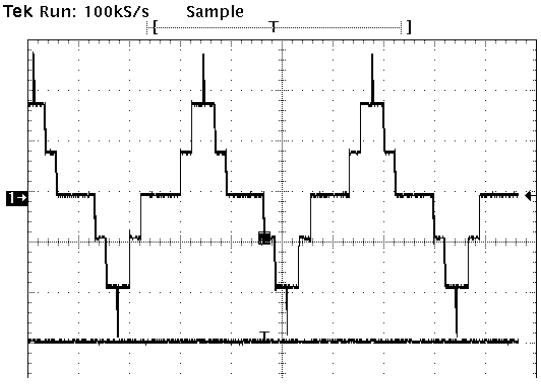
(b). Hardware diagram of Cascaded H-bridge converters



(a)



(b)

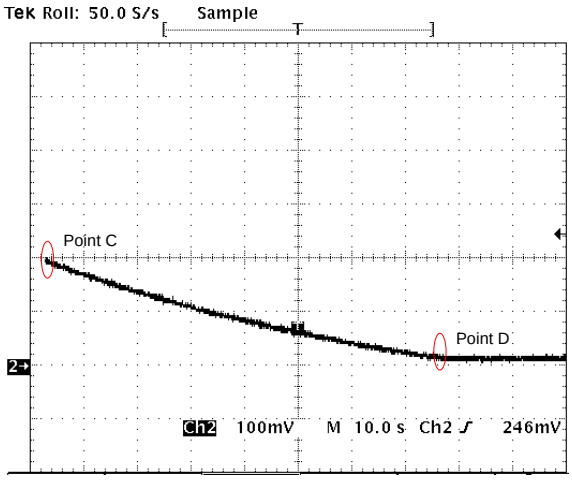


(c)

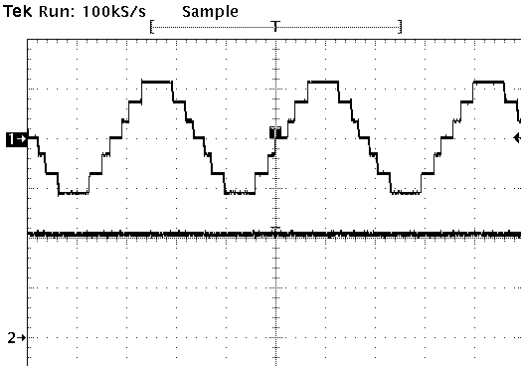
Fig. 16(a). Capacitor voltage in test I

(b). Output voltage waveform at point A

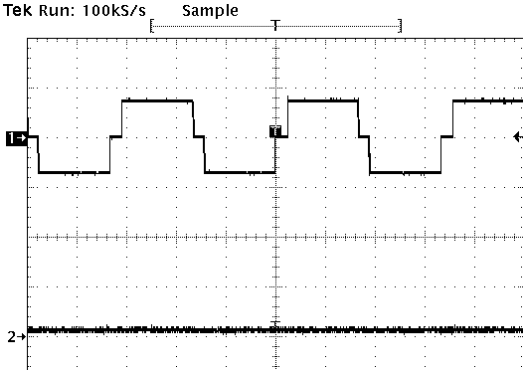
(c). Output voltage waveform at point B



(a)



(b)



(c)

Fig. 17(a). Capacitor voltage waveform in test II

(b). Output voltage waveform at point C

(c). Output voltage waveform at point D

V. Conclusion

A single-dc-source cascaded H-bridge multilevel converter driving different loads has been analyzed in this paper. Only a staircase output voltage is considered. According to the analysis, capacitor voltage regulation is not attainable in all load situations. The effects of the variations of switching angles and the power factor on the voltage regulation of the replacing capacitor are studies. The analytical, simulation, and hardware results agree with each other.

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Paper

2. A New Control Method for Single-DC-Source Cascaded H-Bridge Multilevel Converters Using Phase-Shift Modulation

Abstract—Cascaded H-bridge converters are a promising breed of multilevel converters which generally require several dc sources. Using phase-shift modulation, a new control method for cascaded H-bridge multilevel converters with only one independent dc source per phase is presented in this paper. The rest of the dc sources are replaced with capacitors. Unlike conventional approaches, the proposed method has a wide voltage regulation range for the replacing capacitors in the H-bridge converter cells.

Index Terms-cascaded converters; H-bridge cell; multilevel converter

I. INTRODUCTION

In multilevel power electronic converters, the desired output voltage is synthesized by combining several separate dc voltage sources. Solar panels, fuel cells, batteries, and ultra-capacitors are the most common independent sources used [1, 2]. These converters have single- and three-phase applications. The output voltage in such converter is usually composed by staircase or pulse width modulation schemes. The main advantages of multilevel converters are low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency, capability to operate at high voltages, and modularity. In general, multilevel converters are categorized into diode-clamped, flying

capacitor, and cascaded H-bridge multilevel topologies [3, 4]. The applications of diode-clamped multilevel converters include high-power ac motor drives in conveyors, pumps, fans, and mills [5]. Flying capacitor multilevel converter has been used in high-bandwidth high-switching frequency applications such as medium-voltage traction drives [6]. Finally the cascaded H-bridge multilevel converter has been applied to high-power and high-quality applications such as static VAR generation (SVG) [7], active filters, reactive power compensators [8], photovoltaic power conversion [9], uninterruptible power supplies, and magnetic resonance imaging. Furthermore, one of the growing applications for multilevel power electronic converters is in electric drive vehicles where the traction motor is driven by batteries. Multilevel inverters can also solve the existing problems associated with some of the present two-level PWM adjustable-speed drives since they can reduce the common mode voltage causing the bearing leakage current [10].

Fig. 1 shows the block diagram of a three-phase cascaded H-bridge inverter system. The load is considered to be an induction motor. As it can be observed, the inverter consists of main and auxiliary H-bridge cells in each phase. In early implementations [10, 12, 13], each H-bridge cell was supplied by an independent dc source. Later, it was shown that only one cell needs to be supplied by a real dc power source and the remaining cells could be supplied with capacitors [11, 14]. The proposed method in [14] uses the switching state redundancy for capacitor voltage regulation. However, studies show that voltage regulation of capacitors is not as easy as it was initially predicted [15]. The existence of redundant switching states has been assumed to be adequate for capacitor voltage regulation. However, output current of the inverter as well as the time

duration of redundant switching states greatly impact the charging or discharging patterns of the replacing capacitors.

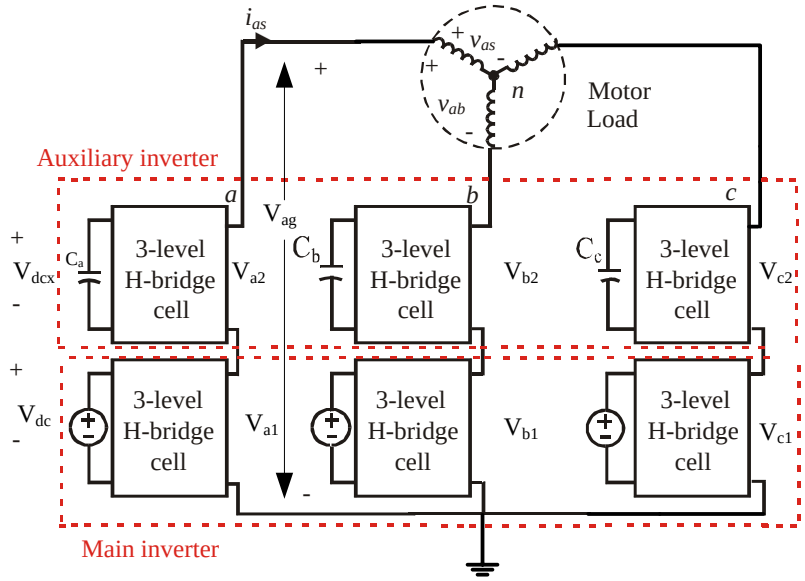


Fig. 1. Block diagram of a three-phase cascaded H-bridge converter

This paper proposes a new control method applicable to single-dc-source cascaded H-bridge multilevel converters to improve their capacitor voltage regulation. The proposed method, phase-shift modulation, is more robust and has less computational burden. In this method, the main converter switches at the fundamental frequency and the auxiliary converter switches at the PWM frequency. The working theory of the cascaded H-bridge multilevel converter is briefly introduced in Section II. In Section III, the application of phase-shift modulation is described. Simulation results and harmonic analysis are also presented in this section. The experimental results are presented in Section IV. The

concluding remarks and overall evaluation of the proposed method are included in Section V.

II. MULTILEVEL H-BRIDGE CONVERTER - FUNDAMENTALS OF OPERATION

The structure of the main and auxiliary cells is very similar and the only difference is that the main converter uses a battery while the auxiliary converter uses a capacitor (see Fig. 1). Fig. 2 shows the circuit diagram of a general H-bridge cell. Parameter *n* is either 1 or 2 labeling the main or auxiliary converters. Depending on the conduction status of switches S_1, S_2, S_3, and S_4, each converter cell can generate three different voltage levels of $+V_n$, 0, and $-V_n$. H-bridge cells in each phase are connected in series; hence, the synthesized per-phase voltage waveform is the sum of all individual cell outputs. The output voltage of phase *a* can be described as (see Fig. 1)

$$V_{ag} = V_{a1} + V_{a2} \tag{1}$$

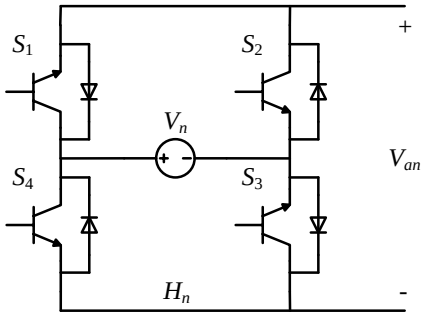


Fig. 2. Circuit diagram of the main and auxiliary H-bridge cells

In motor drive applications, the desired output voltage waveform of a cascaded H-bridge multilevel converter is a sinusoidal waveform which can be described as

$$V_{ag,ref} = V_{ag,amplitude}\sin(\omega_e t) \tag{2}$$

where ω_e is the electrical angular frequency. Fig. 3 describes how the desired output voltage waveform is synthesized using the main and auxiliary converter cells. The main converter cell is supplied by V_{dc} and generates a rectangular waveform, which is at the same frequency with the reference. Equation (3) describes the relationship between the amplitude of the desired output voltage and the dc voltage level of the main converter cell.

$$V_{ag,amplitude} = \frac{4V_{dc}}{\pi}\cos(\alpha), \tag{3}$$

where phase shift α (or conduction angle of the main converter cell) is denoted in Fig. 3. The remaining part of the output voltage, the second trace in Fig. 3, which is described in (4), is synthesized by the auxiliary cell at a higher frequency using a PWM technique (see Fig. 4).

$$V_{a2} = V_{ag} - V_{a1} \tag{4}$$

In a three-phase system, the third harmonic will automatically be canceled [16-20].

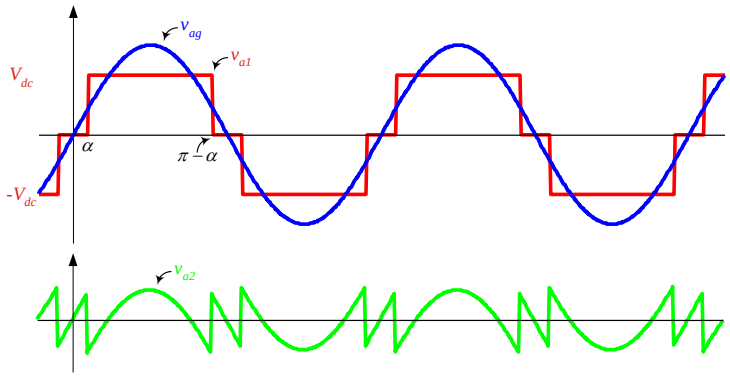


Fig. 3. Desired output voltage waveforms of the main and auxiliary cells

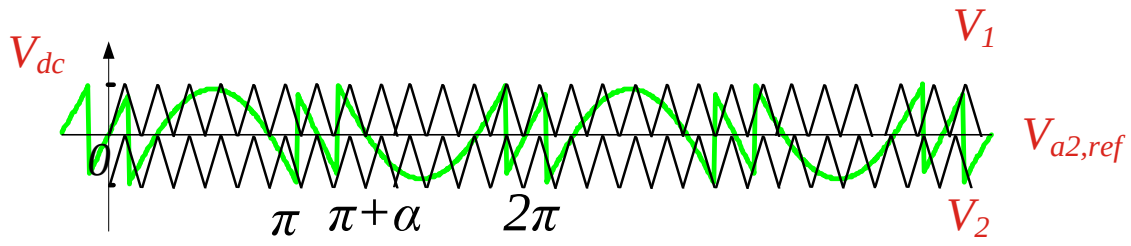


Fig. 4. Sub-harmonic PWM (SHPWM) technique

In order to force the output voltage of the auxiliary cell to track the reference signal shown in the second trace in Fig. 3, the sub-harmonic PWM (SHPWM) technique is used. The control principle of the SHPWM method is to use several triangular carrier signals. Here, the output voltage of the auxiliary converter has 3 levels; therefore, two triangular carriers of the same frequency f_c, as depicted in Fig. 4, are used. The control logic can be described as

1. If $V_1 < V_{a2,ref}$, the output is +1* V_{dcx}
2. If $V_2 < V_{a2,ref} < V_1$, the output is 0
3. If $V_{a2,ref} < V_2$, the output is -1* V_{dcx}

where V_1 and V_2 indicate the modulating signals. If the main cell is fed by a 200-V dc source and the auxiliary cell is fed by a 100-V, the output voltage has 7 levels which are ±300V, ±200V, ±100V and 0.

III. APPLICATION OF PHASE-SHIFT MODULATION

Voltage regulation of the capacitor in the auxiliary cell is a challenging task [7, 10, and 11]. In the proposed method, capacitor voltage regulation is achieved by adjusting the active and reactive power that the main converter injects to the system. The main converter injects only active power if α is chosen by (3). By shifting the voltage waveform synthesized by the main converter (see Fig. 5), one could also inject some reactive power, which can be used to charge or discharge the capacitor on the auxiliary cell. The phase-shift modulation technique is used to find the required phase shift. The control diagram of the system is shown in Fig. 6.

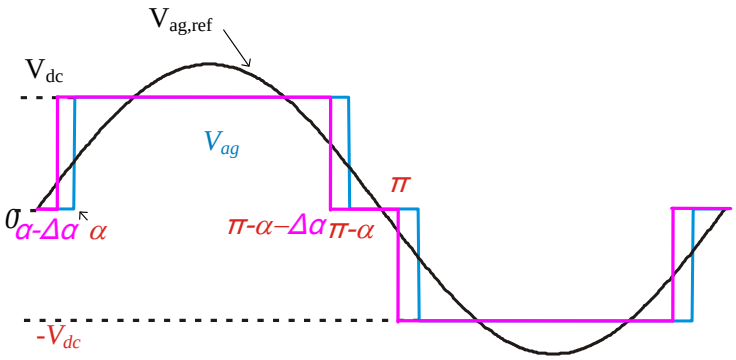


Fig. 5. α shifted to the left

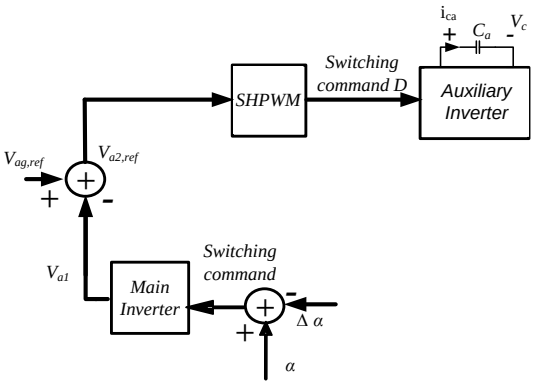


Fig. 6. Control diagram of the system

Each phase of the Y-connected load is assumed to be comprised of a resistor in series with an inductor. This type of load covers all of the operating modes of an induction machine. Here the power factor is considered to be variable from 0 to 1 for both lagging and leading situations and the amplitude of the load current is assumed to be constant at 50 A. Having the voltage information and the values for the current and power factor, the values of the load resistor and inductor (or capacitor) can easily be calculated.

Fig. 7(a) shows how the average current across the capacitor in auxiliary cell H_{a2} is affected by $\Delta\alpha$ for different values of the power factor. The average capacitor current is labeled with $<i_{ca}>$. Here, the load is considered to be inductive and the amplitude of the current is kept at a constant level. It is clear that for inductive loads the average capacitor current and $\Delta\alpha$ are almost linearly related. Therefore, one can regulate the voltage of the capacitor by adjusting $\Delta\alpha$ within an appropriate range. In Fig. 7(b), instead of the amplitude of the output current, the output power is kept constant. Similar relationship can be observed.

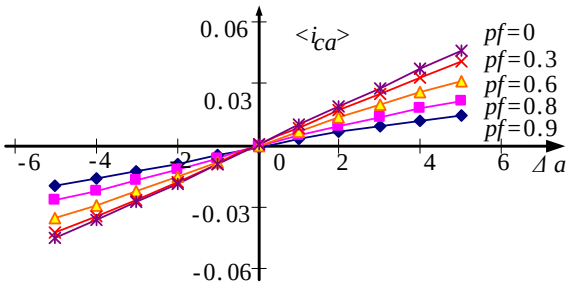


Fig. 7 (a). Relationship between the average capacitor current and $\Delta\alpha$ when load is inductive and the amplitude of the output current is constant (50 A)

(b). Relationship between the average capacitor current and $\Delta\alpha$ when power factor is 0.8, load is inductive, and the output power is constant (4 kW)

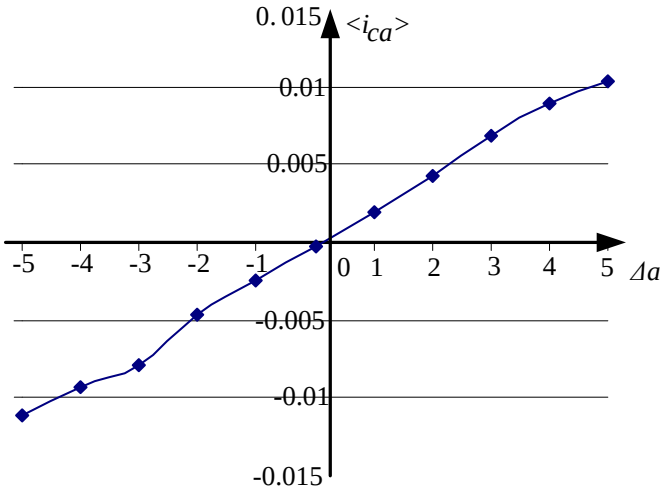


Fig. 7. (Continued)

In order to verify these results, simulations have been carried out. The simulation results with a 0.866 leading power factor are depicted in Fig. 8. In Fig. 8(a), $\Delta\alpha = -1^{\circ}$ and therefore the capacitor voltage decreases which indicates capacitor discharge. In Fig. 8(b), $\Delta\alpha = +1^{\circ}$thus capacitor voltage increases which indicates capacitor charge. Hence, one can regulate the voltage of the capacitor by adjusting $\Delta\alpha$ appropriately.

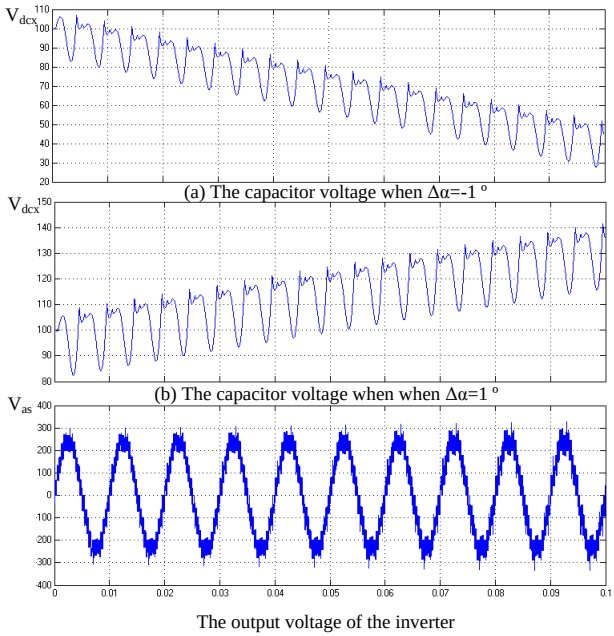


Fig. 8. Simulation results of open-loop phase-shift modulation (time in *s*)

Based on the discussion above, one can devise a closed-loop control system for capacitor voltage regulation as depicted in Fig. 9. $\Delta\alpha$ is adjusted to regulate the capacitor voltage in auxiliary cells. Simulation results of the closed loop phase-shift system, with an induction motor as load, are depicted in Fig. 10. From Fig. 10, it can be observed that the variations of $\Delta\alpha$ are very small. Therefore, it will not generate drastic harmonic distortions. The frequency spectrum of the output voltage is presented in Fig. 11. From the figure, one can observe that the 3rd harmonic is 0 and the 5th harmonic is very small compared with the fundamental component.

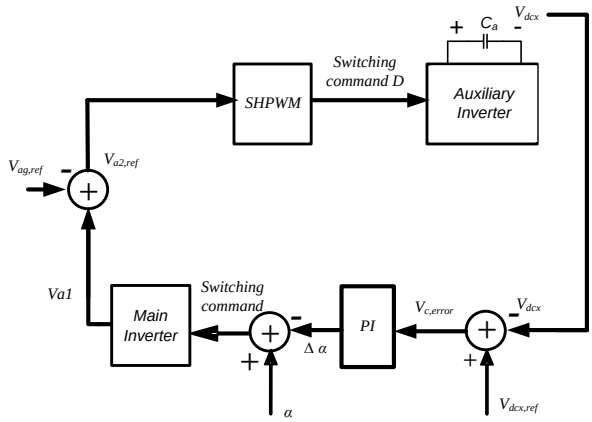


Fig. 9. Closed-loop control block diagram of the system

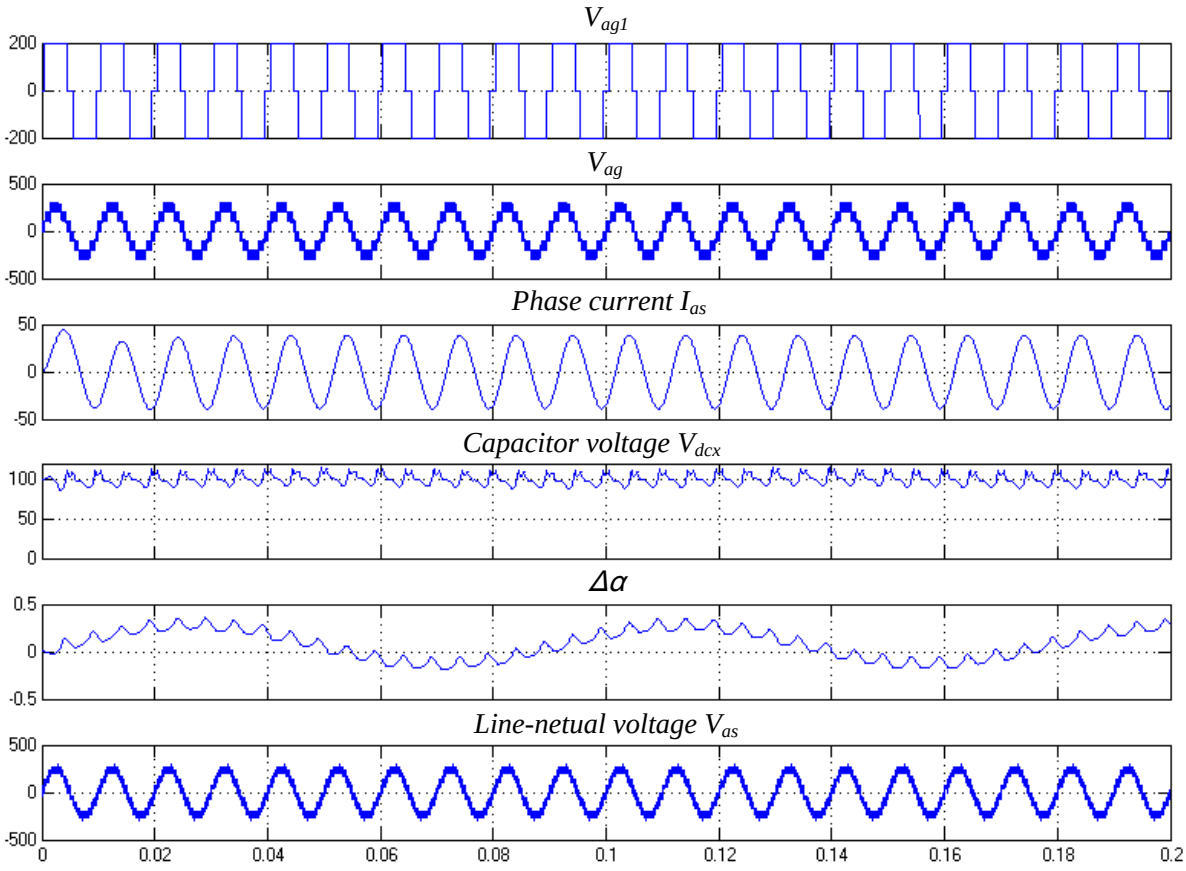


Fig. 10. Simulation results of the closed-loop phase-shift modulation (time in *s*)

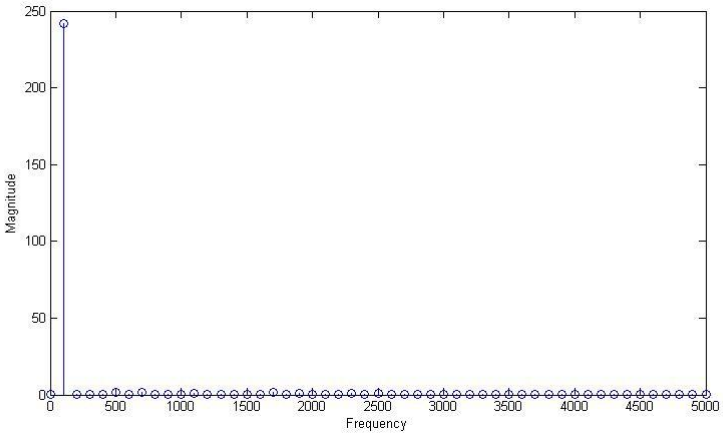
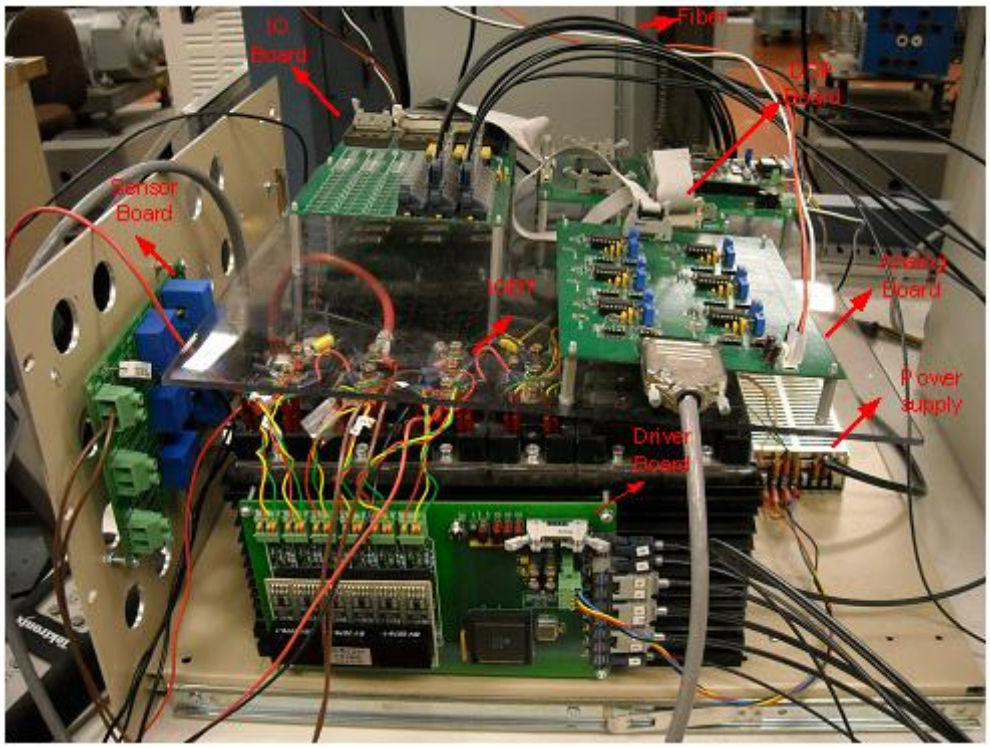


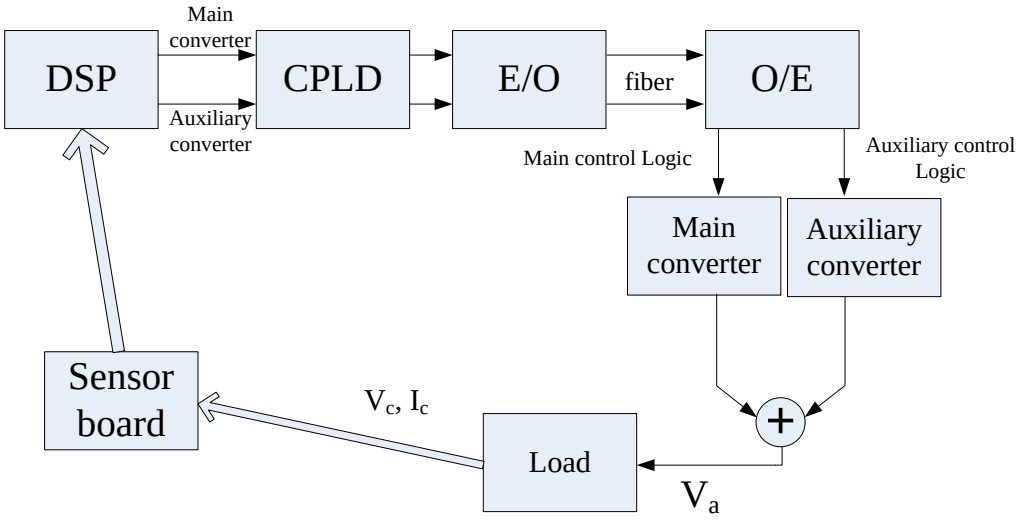
Fig. 11. Spectrum of the output voltage

IV. EXPERIMENT RESULT

In order to verify the simulation results, a low-voltage low-power hardware prototype of the system was developed as depicted in Fig. 12(a) and (b). Two cascaded H-bridge cells feed a load which is a 39 Ω resistor in series with a 15 mH inductor. The main cell is fed by a 20 V dc source. A 2.1 mF capacitor is used as the source for the auxiliary cell. The fundamental frequency is 60Hz and high PWM frequency is 6 kHz. The voltage of the capacitor is expected to be regulated at 10 V which is half of dc source used in the main cell. The control scheme is programmed in a TI-TMS3202812 digital signal processor (DSP) and CY37128P84 complex programmable logic device (CPLD) which is connected to drive CM75DU-24F the Insulated-gate bipolar transistors (IGBT)_through optical fiber. Furthermore, the sensor board is used to monitor the voltage of the capacitor and then feedback to DSP thought voltage shift.



(a)

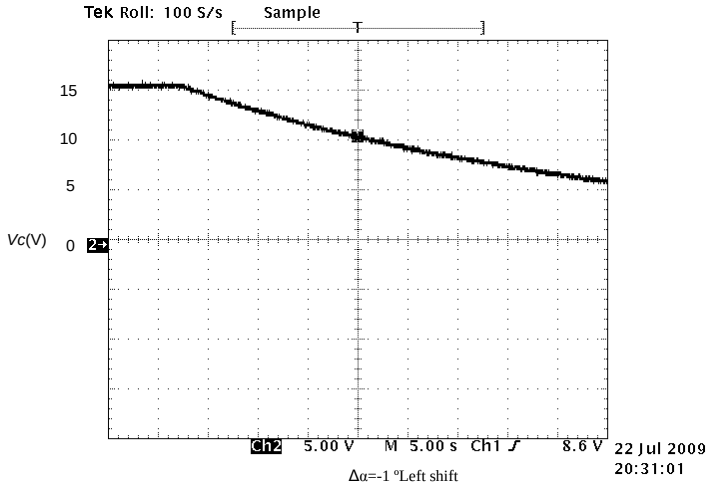


(b)

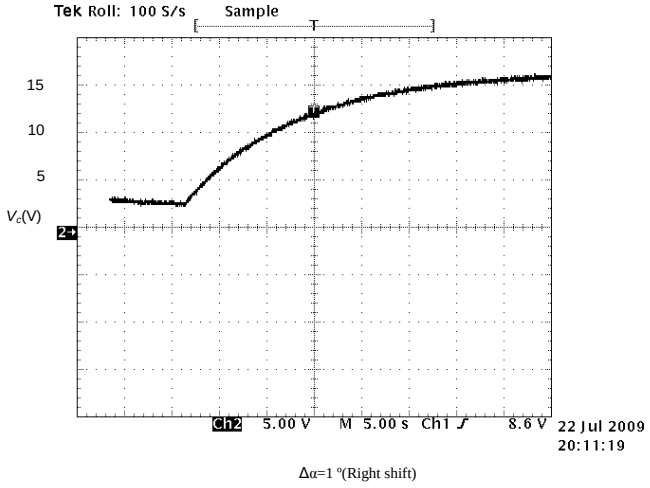
Fig. 12(a). Hardware implement of cascaded H-bridge converters

(b). Hardware diagram of cascaded H-bridge converters

Figs. 13(a) and 13(b) show the open-loop charging and discharging patterns of the capacitor voltage. In Fig. 13(a) the capacitor is discharged sine $\Delta\alpha$ is chosen to be negative. Whereas, $\Delta\alpha$ is selected to be positive which leads to the charging of the capacitor in Fig. 13(b). These results can be compared with the simulation results presented in Fig. 8.



(a)



(b)

Fig. 13(a). The voltage of capacitor for a left shift which leads to discharge

(b). The voltage of capacitor for a right shift which leads to charge

Figures 14, 15, and 16 present the closed-loop response of the system. The output voltage waveforms of the main and auxiliary H-bridge cells are depicted in Fig. 14. It can be observed that the main cell operates at the fundamental frequency while the auxiliary cell operates at the PWM frequency. The output voltage waveform of the cascaded cells is depicted in Fig. 15. This waveform is basically the sum of the two traces in Fig. 14. Figure 16 shows that capacitor voltage regulation has been successfully conducted.

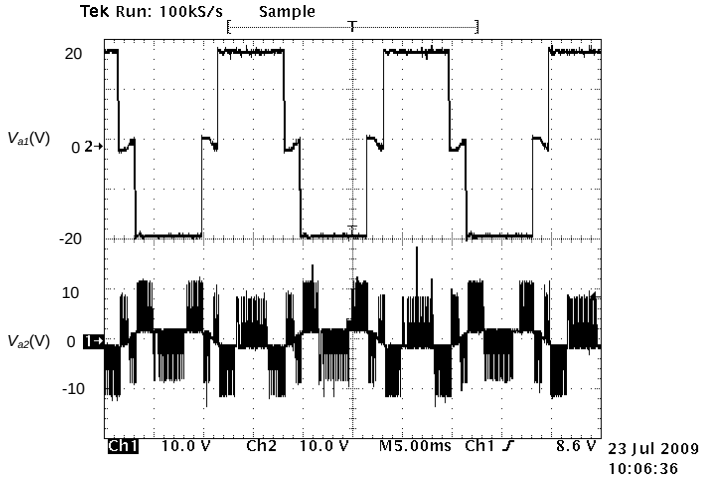


Fig. 14. Output voltage waveform of the main and auxiliary converters when the control loop is closed

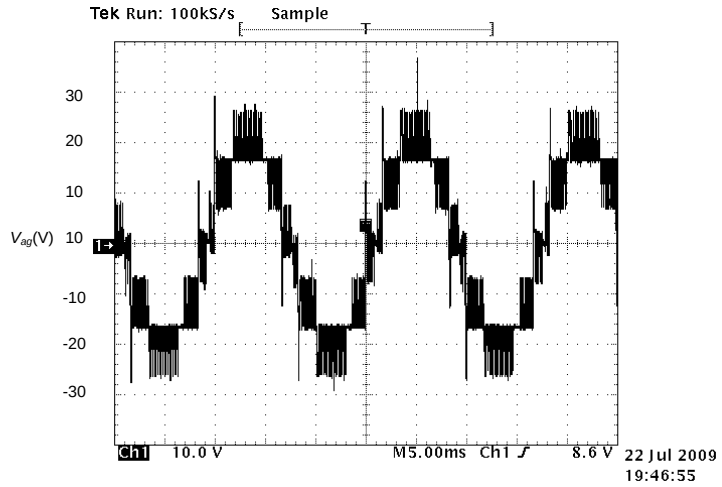


Fig. 15. Output voltage waveform of phase *a* (V_{ag}) when the control loop is closed

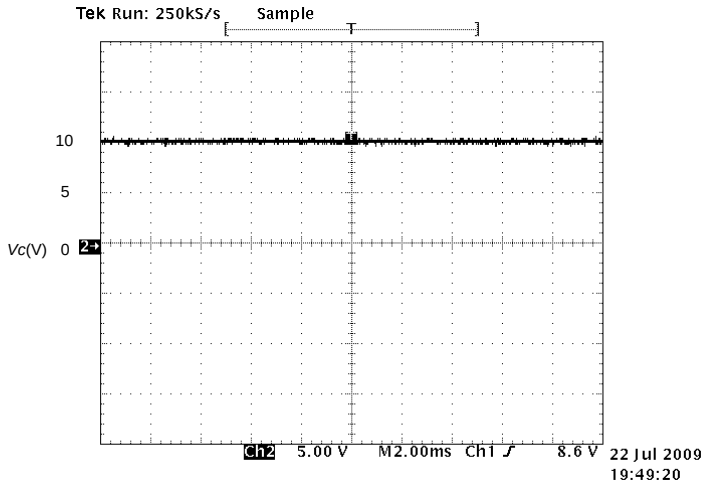


Fig. 16. Regulated voltage of the capacitor when the control loop is closed

V. CONCLUSIONS

A single-dc-source cascaded H-bridge multilevel converter driving an electric motor has been analyzed. A new control method, phase-shift modulation, is used to achieve

voltage regulation for the capacitors replacing the independent dc sources in the auxiliary H-bridge cells. The main H-bridge cells operate at the fundamental frequency while the auxiliary cells run at the PWM frequency. The proposed approach has less computational burden and benefits from a more robust capacitor voltage control scheme. The experimental results agree with the simulation and analytical results. The results show that the regulation of the capacitor voltage is achievable without deteriorating the total harmonic distortion.

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Paper

3. An Improved Cascaded H-Bridge Multilevel Converter Controlled by a Unbalanced Voltage Levels Sigma-Delta Modulator

Abstract- Multilevel converters are proven to be viable solutions for automotive motor drive applications. Cascaded H-bridge converters are a promising breed of multilevel converters which generally require several independent dc sources. Replacement of all but one of the dc sources with capacitors in cascaded H-bridge multilevel converters, which leads to single-dc-source cascaded converters, has recently gained popularity. However, very few efforts have been made to address the challenging problem of voltage regulation in the replacing capacitors. In this paper, the applicability of a new voltage control technique on providing voltage regulation across the replacing capacitors is examined. The proposed method is named unbalanced-voltage-level sigma-delta modulation technique. In addition, a new voltage ratio which simplifies the control tasks in H-bridge cells is introduced. Analytical and simulation results prove the effectiveness of the proposed scheme.

Keywords—Delta-Sigma modulation; H-bridge multi-level converter

I. INTRODUCTION

Multilevel power electronic converters are mainly utilized in dc-ac applications including automotive motor drives, static VAR compensators [1], and uninterruptible power supplies. They are usually the converter of choice the high-power medium-voltage range. Their main advantages are low harmonic distortion of the generated output voltage, low electromagnetic emissions, high efficiency, capability to operate at high voltages, and modularity. In general, multilevel converters are categorized into diode-clamped, flying capacitor, and cascaded H-bridge topologies [2]. Figure 1 shows the block diagram of a three-phase cascaded H-bridge converter. As it can be observed, the converter consists of main and auxiliary H-bridge cells in each phase. The structures of the main and auxiliary cells are very similar (see Fig. 2). Depending on the conduction status of switches S_1, S_2, S_3, and S_4, each converter cell can generate three different voltage levels which are $+V_n$, 0, and $-V_n$. H-bridge cells in each phase are connected in series; hence, the synthesized per-phase voltage waveform is the sum of all individual cell outputs. The output voltage of phase *a* can be described by the following equation (see Fig. 1)

$$V_{ag} = V_{a1} + V_{a2} \tag{1}$$

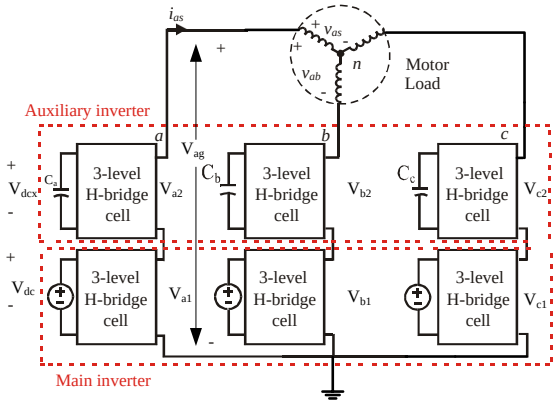

Fig. 1. Block diagram of a three-phase cascaded H-bridge converter

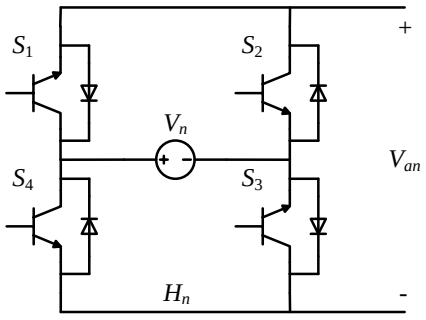

Fig. 2. Circuit diagram of an H-bridge cell

In early implementations [3-5], each H-bridge cell was fed by an independent dc source. Later, it was shown that only one cell needs to be supplied by a real dc power source and the remaining cells could be supplied with capacitors [6, 7]. However, studies show that the voltage regulation of the replacing capacitors is not an easy task [8]. In previously reported works [6, 7], the ratio between the main and auxiliary voltage sources has been selected to be either 2:1 or 3:1, which leads to some limitations on the capacitor voltage regulation. In this paper, the voltage ratio of 4:1, which simplifies the control

task, is proposed and successfully implemented. Furthermore, sigma-delta modulation (SDM) is proposed for voltage regulation across the replacing capacitors in the auxiliary cells. In previous applications, SDM has successfully been applied to synthesize voltage waveforms in discrete pulse modulated system such as resonant dc link converters [9, 10].

The application of the SDM technique and appropriate selection of the voltage ratio between the H-bridge cells are the main contributions of this paper. In Section II, SDM and its principles of operation are briefly introduced. Utilization of SDM in controlling multi-level converters with two independent dc sources as well as the selection of parameters are discussed in Section III. Voltage ratio selection is discussed in Section IV. Application of SDM to single-dc-source cascaded H-bridge multilevel converters is discusses in Section V. Simulation results are also presented in this section. Concluding remarks and overall evaluation of the proposed method are included in Section V.

II. SIGMA DELTA MODULATION (SDM)

The block diagram of a conventional two-level SDM is shown in Fig. 3. V_{ref} represents the desired output voltage, V_o is the synthesized output voltage, and f_s represents the sampling frequency of the system. The modulator encodes reference signal V_{ref} into a two-level output (V_o). The output and its reference are fist compared to find the error. The error signal then passes through a gain block and an integrator. Finally, it is quantized and forms the output signal. Under normal operating conditions, output signal has to track the input signal with zero average error.

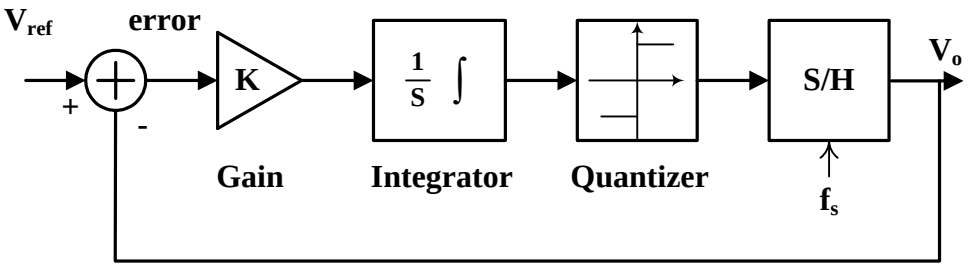

Fig. 3. Block diagram of a two-level sigma-delta modulator

The SDM method can easily be extended to synthesize a multilevel waveform by replacing the binary quantizer with an N-level quantizer corresponding to the number of the levels of the multilevel converter. The block diagram of the new SDM is depicted in Fig. 4. The modulator design task requires appropriate selection of amplifier gain *K*, the saturation limits of the integrator block, and sampling frequency f_s. Here, a brief analysis of the system performance is studied using the static transfer characteristics of a uniform quantizer as illustrated in Fig. 5.

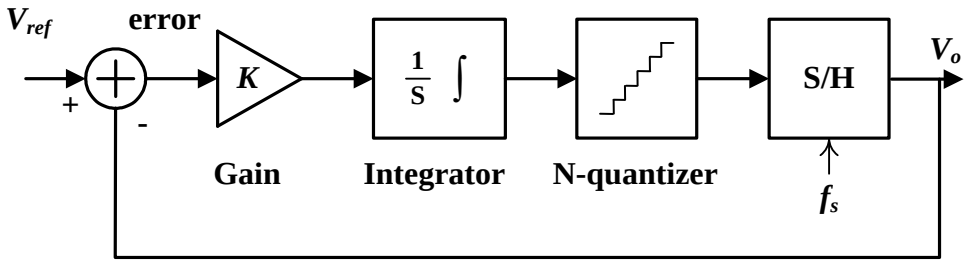

Fig. 4. Block diagram representation of a multilevel sigma delta modulator

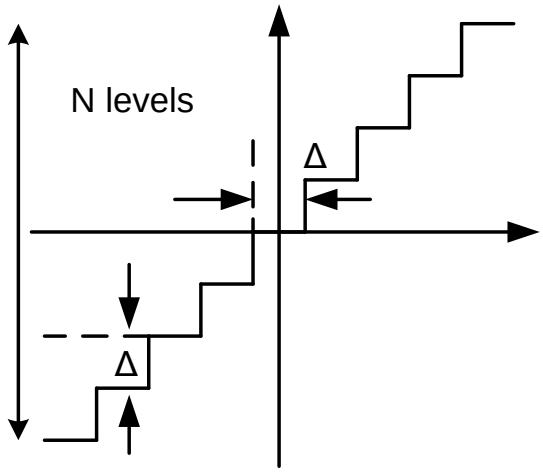

Fig. 5. Static transfer characteristics of a uniform quantizer

Normally, the static transfer characteristics of the uniform N-level quantizer features all the step widths and step heights which are equal in magnitude representing equal dc bus levels. As may be seen, each step width and the corresponding step height are of magnitude Δ. For a normalized uniform quantizer with *N* number of levels the relation between *N* and Δ will be

$$\Delta(N-1)=2 \tag{2}$$

The optimum selection of gain *K* and modulation frequency f_s will be determined by

$$K / f_s \le 1 \tag{3}$$

III. Using SDM to Drive a Multi-Level Converter with Two DC Sources

Previously, each H-bridge cell was fed by an independent dc source such as a battery. The control diagram for this case is depicted in Fig. 6. The reference voltage is a sinusoidal waveform, and the output voltage is expected to track the reference voltage.

The output of the hysteresis block is either +1 or -1. This signal is then sampled at the modulation frequency rate. The adjustable parameters are gain *K*, saturation limits of the integrator *S*, sampling frequency f_s, and threshold of the hysteresis loop *H*. Tracking characteristics of the synthesized output voltage depends on the appropriate selection of the above mentioned parameters. For instance, for $H = 0.01$, $f_s = 5$ kHz, $S = \pm 0.05$, and $K = 10$ one would be able to get the output voltage that is depicted in Fig. 7. On the other hand, for $H = 0.0005$, $f_s = 5$ kHz, $S = \pm 0.5$, and $K = 10$. The results are not satisfactory (see Fig. 8).

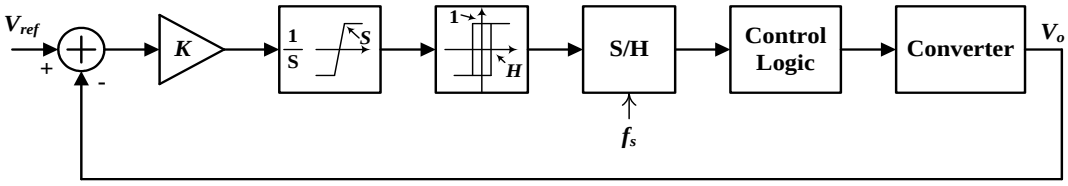

Fig. 6. Control block diagram of SDM driving multi-level converter

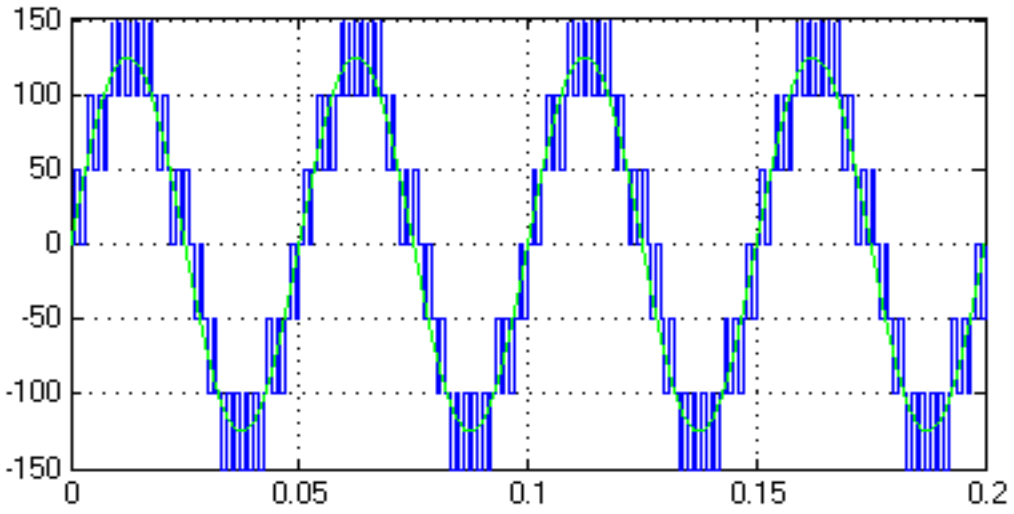

Fig. 7. The output voltage waveform when the modulator parameters are well-selected(time in *s* and voltage in *V*)

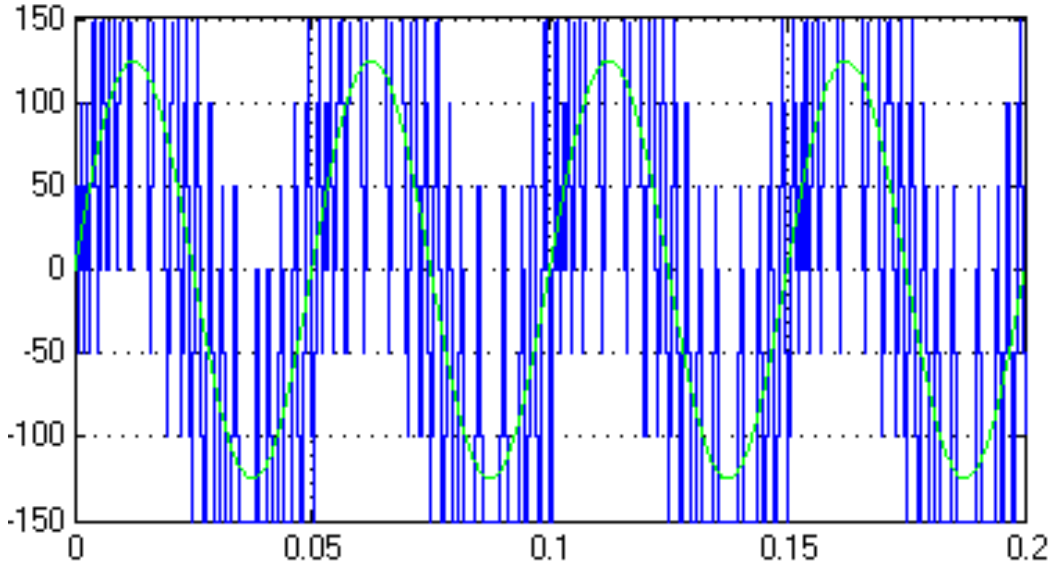

Fig. 8. The output voltage waveform when the modulator parameters are not well-selected(time in *s* and voltage in *V*)

High sampling frequency is preferred to guarantee that the loop is fast enough to track the reference signal. Studies carried out show that the sample frequency needs to be at least 30 times the fundamental frequency. For gain *K* and the saturation limits of the integrator block, simulations show that small values for gain *K* (e.g. 0.1) do not result in a good tracking response. However, values of 1 and larger are satisfactory. Saturation limits of the integrator black have a similar affect like gain *K*.

IV. Voltage Ratio Selection

As mentioned earlier, it has been proven that only one dc source is needed in a multilevel converter and others can be replaced with capacitors. In that case, the challenge is to regulate the voltage of the replacing capacitors [8]. Two approaches have

been introduced in the literature which are the redundancy-based [7, 11-13] and level reduction [6] methods. These two approaches both impose new limitations on the system. The redundancy-based method only works for a very limited load range [8] and the level reduction method gives up on two of the output voltage levels; therefore, it leads to higher harmonic distortion.

Usually, the voltage ratio of the main and auxiliary converters is selected to be 2:1 [7]; therefore, output voltage has only seven levels, as depicted in Fig. 9. In this case, V_{dc} is the voltage level of the main cell and $V_{dc}/2$ is that of the auxiliary cell.

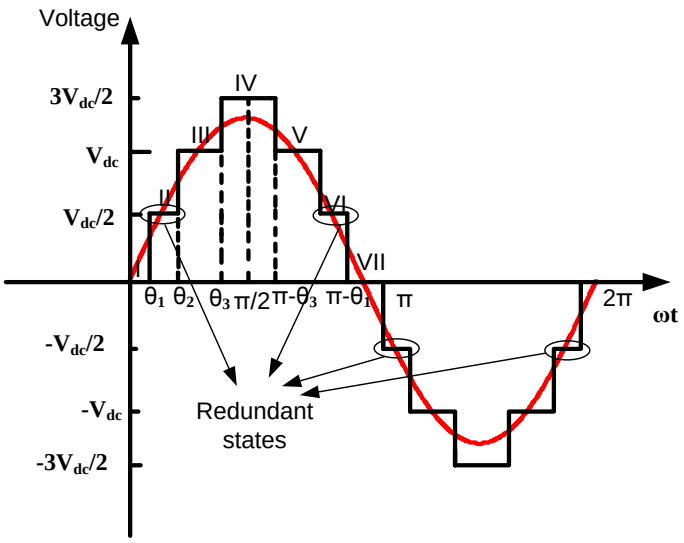

Fig. 9. Output voltage redundancy for 2:1 ratio

Based on Fig. 9, one fourth of the period could be divided into the following subintervals

I. $0 < \omega t < \theta_1$ no capacitor charge or discharge

II. $\theta_1 < \omega t < \theta_2$ capacitor charge or discharge depending on the capacitor voltage

III. $\theta_2 < \omega t < \theta_3$ no capacitor charge or discharge

IV. $\theta_3 < \omega t < \pi-\theta_3$ capacitor discharge

V. $\pi-\theta_3 < \omega t < \pi- \theta_2$ no capacitor discharge

VI. $\pi - \theta_2 < \omega t < \pi-\theta_1$ capacitor charge or discharge depending on the capacitor voltage

VII. $\pi - \theta_1 < \omega t < \pi$ no capacitor charge or discharge

In order to balance the capacitor voltage, subinterval IV should be very short otherwise the capacitor voltage will continuously decrease since the discharge times will be longer than charge times [8]. To overcome this disadvantage, the voltage ratio is proposed to be 4:1, as depicted in Fig. 10. In this case, there is no redundancy and therefore output voltage has nine levels. The capacitor is discharged when output voltage is at level 1 while it is charged when output voltage is at level 3. Therefore one fourth of the period could be divided into the following subintervals.

I. $0 < \omega t < \theta_1$ no capacitor charge or discharge (level 0)

II. $\theta_1 < \omega t < \theta_2$ capacitor discharge (level 1)

III. $\theta_2 < \omega t < \theta_3$ capacitor charge (level 3)

IV. $\theta_3 < \omega t < \theta_4$ no capacitor charge or discharge (level 4)

V. $\theta_4 < \omega t < \pi- \theta_4$ capacitor discharge (level 5)

VI. $\pi - \theta_4 < \omega t < \pi-\theta_3$ no capacitor charge or discharge (level 4)

VII. $\pi - \theta_3 < \omega t < \pi - \theta_2$ capacitor charge (level 3)

VIII. $\pi - \theta_2 < \omega t < \pi - \theta_1$ capacitor discharge (level 1)

IX. $\pi - \theta_1 < \omega t < 2\pi$ no capacitor charge or discharge (level 0)

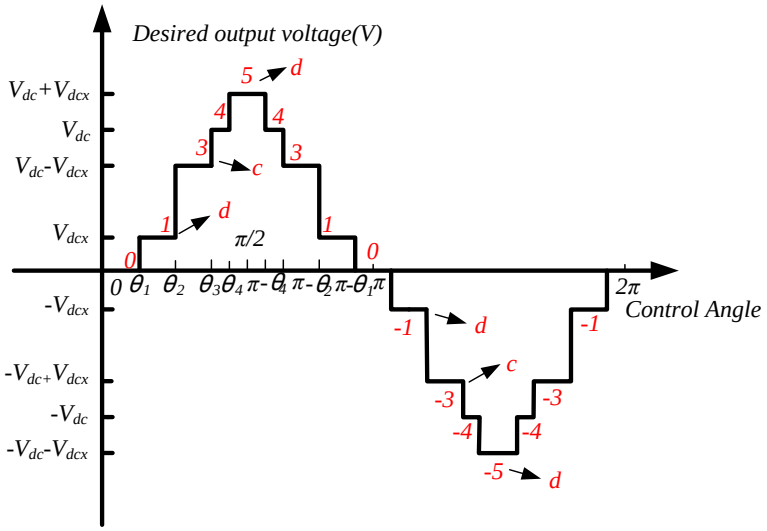

Fig. 10. Output voltage for 4:1 ratio (V_{dc} = 4 * V_{dcx})

By comparing modes II and III, one would observe that capacitor is discharged when output voltage (and hence output current) is smaller and charged with a larger current. This way, there is a higher chance to successfully balance the capacitor voltage as opposed to the 2:1 case.

V. SDM Applied to the Multilevel H-Bridge Converter

Instead of the conventional stair-case modulation, SDM is proposed to push the undesired harmonic components of the output voltage to higher frequencies (see Fig. 11). V_{ref} is the reference signal which is sinusoidal.

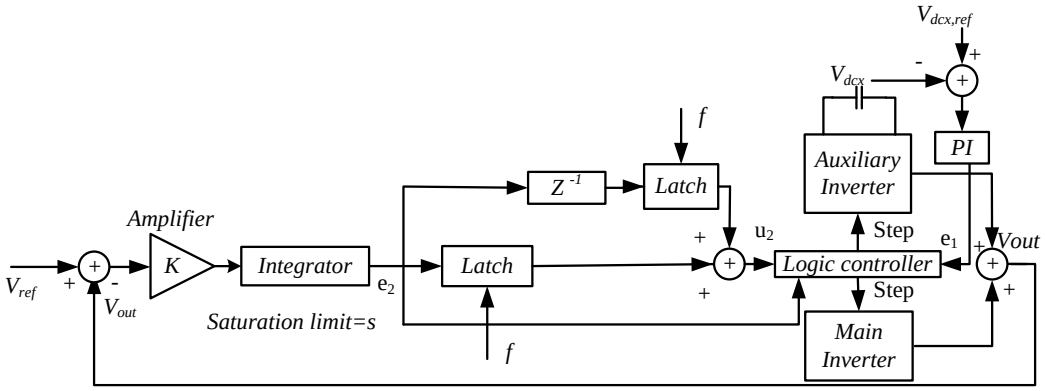

Fig. 11. Proposed sigma-delta modulation applied to the multilevel converter

The output voltage of the converter (V_{out}) is compared with reference signal V_{ref} and the resulting error is fed in to the integrator. The output of this block is named e_2 which is one of the control signals of the logic controller. The other is generated based on how well-regulated the capacitor voltage is. These two error signals are then quantized into one of the two possible levels 1 or -1 depending on their polarity. Next, a simple logic circuit decides on which switch has to be turned ON. This logic is shown in Table 1 where u_2 is the previous status of the output voltage stage and the 'discrete step' is the next stage of the output voltage and x means do not care. The output of the logic controller block has 9 levels which are 0, ±1, ±3, ±4, ±5. Accordingly, the output of the converter is 0, $\pm V_{dcx}$, $\pm(V_{dc}-V_{dcx})$, V_{dcx}, $\pm V_{dc}$, $\pm(V_{dc}+V_{dcx})$.

Table 1 Control Logic of the Logic Controller

u_2	e_2	e_1	Discrete step
Level 0	1	x	Level 1
Level 0	-1	x	Level -1
Level 1	1	1	Level 3
Level 1	1	-1	Level 1
Level 1	-1	x	Level 0
Level 3	1	1	Level 3
Level 3	1	-1	Level 4
Level 3	-1	1	Level 3
Level 3	-1	-1	Level 1
Level 4	1	x	Level 5
Level 4	-1	x	Level 3
Level 5	-1	x	Level 4
Level -1	1	x	Level 0
Level -1	-1	1	Level -3
Level -1	-1	-1	Level -1
Level -3	1	1	Level -3
Level -3	1	-1	Level -1

Table1. (Continued)

u_2	e_2	e_1	Discrete step
Level -3	-1	1	Level -3
Level -3	-1	-1	Level -4
Level -4	1	x	Level -3
Level -4	-1	x	Level -5
Level -5	1	x	Level -4

Figure 12 depicts the output voltage waveform of the converter. As it can be observed, SDM modulation is successful in tracking the sinusoidal reference signal. Figure 13 shows the capacitor voltage in the auxiliary H-bridge cell where the amplitude of V_{ref} is 131 V, the fundamental frequency is 100 Hz, the gain of the controller (K) is 10, the saturation limits of the integrator are ±0.005, the sampler frequency is 10 kHz, the threshold of the hysteresis loop is 0.0001. The value of the capacitor is 1 mF and the load is a 10-Ω resistive load. It is obvious that capacitor voltage is well regulated. Selection of a larger capacitor would result in a lower voltage ripple.

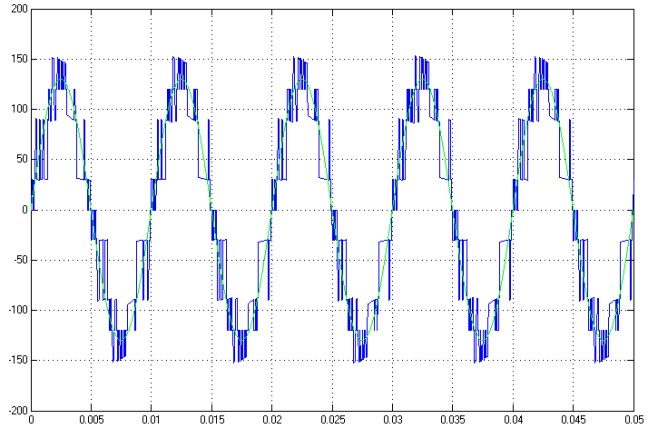

Fig. 12. Output voltage waveform of the cascaded H-bridge multilevel converter and its reference(time in *s* and voltage in *V*)

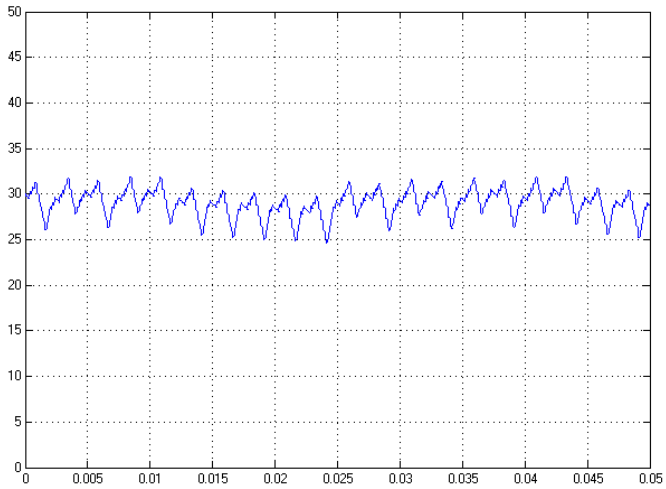

Fig. 13. Regulated voltage across the capacitor in the auxiliary cell(time in *s* and voltage in *V*)

Generally, the problem associated with the SDM method is the presence of high harmonics at the output. In the proposed method, since a 4:1 voltage ratio is selected,

undesired harmonics at the output are suppressed. Figure 14 shows the frequency spectrum of the output voltage where the THD is equal to 0.87%. One can further improve the THD by using high order modulators such as interpolative modulators [14], cascaded modulators [15-17] and adaptive modulators [18-20].

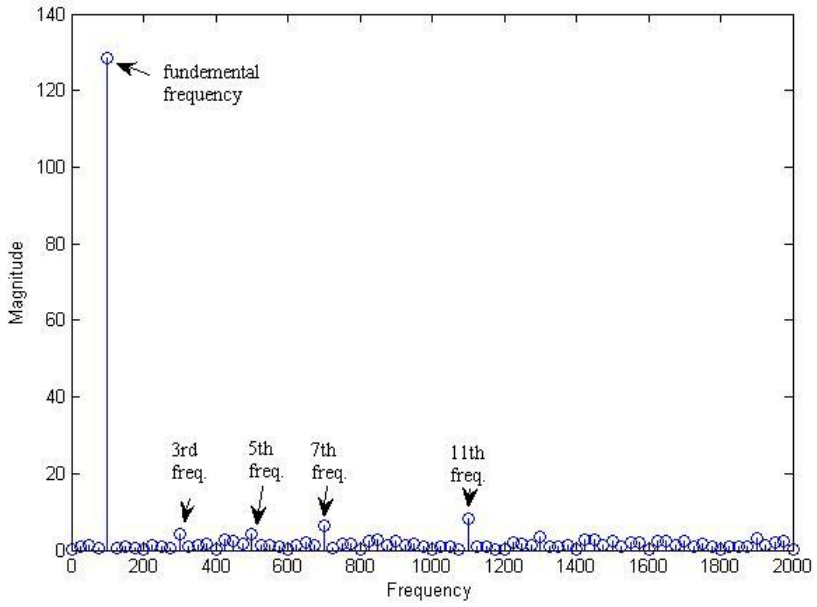

Fig. 14. The frequency spectrum of the output voltage

VI. CONCLUSIONS

A cascaded H-bridge multilevel converter, which requires only one dc source, driving a three phase motor has been analyzed in this paper. The converter is proposed to have a voltage ratio of 4:1 which leads to nine output voltage levels. In order to provide sinusoidal tracking characteristics, sigma-delta modulation technique is employed. Simulation results show that voltage regulation for the replacing capacitors is feasible.

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2. CONCLUSION

The single-dc-source cascaded H-bridge converter was investigated in this thesis. The voltage regulation of the capacitor is a key issue. Using the existing methods based on the switching state redundancy does not achieve capacitor voltage regulation. The effects of the variations of switching angles and the power factor on the voltage regulation of the replacing capacitor are studied here. An equation which describes how to choose appropriate values of the switching angles was derived. By applying this equation, one can eliminate the 5th and 7th harmonics of the output voltage. In addition, one can balance the voltage of the capacitor under different load conditions. The simulation and experimental results are consistent with each other.

Also, a new control method, phase-shift modulation technique, was used to achieve voltage regulation for the replacing capacitor. The main H-bridge cell operates at the fundamental frequency while the auxiliary cell runs at the high PWM frequency. The proposed approach has less computational burden and benefits from a more robust capacitor voltage control scheme. The experimental results agree with the simulation and analytical results. The results show not only the regulation of the capacitor voltage is achievable but also the total harmonic distortion is small.

Another control method named unbalanced-voltage-level sigma-delta modulation technique was also proposed to improve the capacitor voltage regulation. The voltage ratio of 4:1 which can improve the output voltage quality and simplify the control task of the capacitor voltage regulation was proposed and successfully implemented. Furthermore, sigma-delta modulation was proposed for voltage regulation across the replacing capacitors in the auxiliary cell by replacing the binary quantizer with an N-level quantizer corresponding to the number of the levels of the multilevel converter. The design principles of the selection of the amplifier gain, the saturation limits of the integrator block, the sampling frequency, and the threshold of the hysteresis loop were provided. The unbalanced-voltage-level sigma-delta modulation technique can be easily implemented in digital control which is easy to be programmed and benefits from high flexibility and reliability.