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BGA footprints modeling and physics based via models validation for power and signal integrity applications

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BGA FOOTPRINTS MODELING AND PHYSICS BASED VIA MODELS

VALIDATION FOR POWER AND SIGNAL INTEGRITY APPLICATIONS

by

GIUSEPPE SELLI

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This dissertation has been prepared in four papers for publication in the style used at the University of Missouri-Rolla. *The original intent to submit the four articles separately will not be followed up, also, the venue where to submit the articles has not been finalized at the time of the submittal of this thesis. Finally, in order to meet the formatting requirements of the University and avoid unaesthetic misalignments and shifts in the figures and paragraphs, some words are sometimes repeated or removed from the unformatted original version.*

ABSTRACT

Modelling and simulating the multi-scale nature of a power distribution network (PDN) is essential to ensure the correct functioning of the devices connected to it. Simple parallel-plate sections constitute the core of these PDN geometries, together with sections where a large number of holes and vias are present, as in the case of a BGA footprint. Employing a divide-and-conquer approach allows for the modelling of these geometries separately, i.e., 3-D full wave solvers for the sections with holes and vias, and a cavity model approach, for the simple parallel-plate structures. Also, equivalent circuit models can be obtained for time-domain and frequency-domain SPICE simulations. The circuit extraction features of the cavity model method can be applied on the parallel-plate geometries, while, a black-box circuit-extraction approach can be applied on the 3-D simulation results of the complex structures. Concise physics based models for vias are also presented in here. These models are built by employing few circuit elements, i.e., transmission lines to account for signal propagation on striplines, via-to-antipad capacitances to account for displacement currents between the via barrels and the antipad rims and, finally, parallel-plate impedances to account for the return paths associated with the vias. The effectiveness of these concise models resides in the possibility to rearrange the same circuit elements in order to model different via configurations. The models are finally run in a SPICE-like environment allowing for the possibility to carry out what-if scenarios due to the one-to-one correspondence between circuit elements and geometry features.

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INTRODUCTION

Modelling and simulating the multi-scale nature of a power distribution network (PDN) is essential to ensure the correct functioning of the devices connected to it. Simple parallel-plate sections constitute the core of these PDN geometries, together with sections where a large number of holes and vias are present, as in the case of a BGA footprint. The employment of 3-D full wave simulators is then necessary, since specific design requirements need to be met over the frequency range of interest, and fast analytical approaches are available only for simple parallel-plate geometries, but not for those parts with many holes and vias. However, the PDN features often vary from the order of inches/cm to the order of mils/μm, hence, 3-D full-wave modelling is cumbersome and time-consuming. Employing a divide-and-conquer approach allows for the modelling of these geometries separately, i.e., 3-D full wave solvers for the sections with holes and vias, and a cavity model approach, for the simple parallel-plate structures. Also, equivalent circuit models can be obtained for time-domain and frequency-domain SPICE simulations. The circuit extraction features of the cavity model method can be applied on the parallel-plate geometries, while, a black-box circuit-extraction approach can be applied on the 3-D simulation results of the complex structures. In both modelling strategies, the reconstruction is carried out by ensuring voltage and current continuity along the boundaries where the segments are recombined. Concise physics based models for vias are presented in this article. These models are built by employing few circuit elements, i.e., transmission lines to account for signal propagation on striplines, via-to-antipad capacitances to account for displacement currents between the via barrels and the antipad rims and, finally, parallel-plate impedances to account for the return paths

associated with the vias. The via-to-antipad capacitance is calculated from a closed-form expression fitted on a large set of values, which are obtained from 2D static simulations. On the other hand, the parallel-plate impedances are calculated from well-known formulas found in the literature. Finally, a parallel combination of two 100Ω transmission lines is employed to model the stripline-to-via transitions. The effectiveness of these concise models resides in the possibility to rearrange the same circuit elements in order to model different via configurations. Also, the circuit elements are all calculated based on board geometry specifications and material parameters extracted from measured data. The models are finally run in a SPICE-like environment allowing for the possibility to carry out what-if scenarios due to the one-to-one correspondence between circuit elements and geometry features. The simulation results are ultimately validated by means of measurements on ad-hoc test sites realized with the purpose of capturing very precisely the physics of via transitions.

1. MODELING OF BGA FOOTPRINTS FOR POWER INTEGRITY ON MULTILAYER PRINTED CIRCUIT BOARDS FROM FIRST PRINCIPLE AND CIRCUIT MODEL EXTRACTION

ABSTRACT

Modelling and simulating the multi-scale nature of a power distribution network (PDN) is essential to ensure the correct functioning of the devices connected to it. Simple parallel-plate sections constitute the core of these PDN geometries, together with sections where a large number of holes and vias are present. The employment of 3-D full wave simulators is then necessary, since specific requirements need to be met over the frequency range of interest, and fast analytical approaches are available only for simple parallel-plate geometries, but not for those parts with many holes and vias. However, the PDN features often vary from the order of inches/cm to the order of mils/μm, hence the 3-D modelling efforts are cumbersome and time-consuming. Employing a divide-and-conquer approach allows to model the geometries separately, i.e., 3-D full wave solvers for the sections with holes and vias, and the Cavity Model approach for the simple parallel-plate structures. Also, equivalent circuit models can be are obtained. The circuit extraction feature of the Cavity Model method can be applied on the parallel-plate geometries, while, a black box approach can be applied on the 3-D simulation results of the complex sections.

1.1 INTRODUCTION

The analysis of power integrity issues is a fundamental aspect in high-speed system designs [1.1]-[1.5]. Ensuring the delivery of timely amount of charges as well as

avoiding noise coupling is an enormous design challenge, especially when BGA-packaged components are utilized. Modeling the interface between the board and the BGA package (balls, holes, and vias) can be carried out within 3D full-wave tools. However, the computational effort is usually time-consuming, since the small features of that interface increases the size of the models and the computational effort, given the difference in scale with respect to the planes. Conversely, closed form expressions for self and transfer parallel-plate impedances are readily available for simple planar structures [1.6]-[1.10] and the segmentation method can be used to combine elementary rectangular or triangular shapes to obtain more realistic ones.

Two modeling strategies are applied on a power distribution network and described in this article. The first one utilizes self and transfer-impedances obtained from both a 3-D full wave FEM simulator and the Cavity Model approach. The second strategy combines circuit models obtained by means of a black box approach and the circuit model extraction feature of the Cavity Model method. The results achieved with the two modeling strategies are compared and validated against 3-D full wave simulations. Firstly, the power delivery network of interest is cut into five adjacent pieces, the center section contains a BGA footprint with holes and vias, while the remainder four consist of simple parallel-late geometries with several external ports. The center part is finely simulated within a 3D full wave FEM simulator and an equivalent circuit model is extracted from the simulation results by means of a black box approach [1.11]-[1.12]. On the other hand, Z-parameter data as well as equivalent circuit models are obtained for the reminder four sections by means of the Cavity Model approach. Finally, all the parts are combined back together by using matrix algebra or properly connecting the circuit

models. Fundamental is the presence of the internal ports that allow the continuity of voltages and currents along the cuts. The advantage of this type of approach resides in focusing the 3-D full wave analysis only on the most complex part, also, the simulation results as well as the equivalent circuit models of the BGA section can be recycled in other PDN designs. The modeling strategies are illustrated in this article as explained hereafter. In the second section, the geometry under investigation is described in details. In the third and fourth sections, respectively, the first modeling strategy and the second modeling strategies are outlined in terms of their implementation and compared with full wave simulation results. In the fifth section, some details are given regarding the two modeling approaches and finally some conclusions are drawn in the sixth section

1.2   DESCRIPTION OF THE GEOMETRY UNDER INVESTIGATION

The two-plate geometry of interest is initially extracted from the multilayer structure of Fig. 1.1. Only the GND-1.5V pair of planes, highlighted in the dashed box, is investigated. Both planes are also called, respectively, bottom and top plane. The BGA package shown in Fig. 1.1 is provided only to describe all the possible pin connections and explain the rationale of the hole patterns.
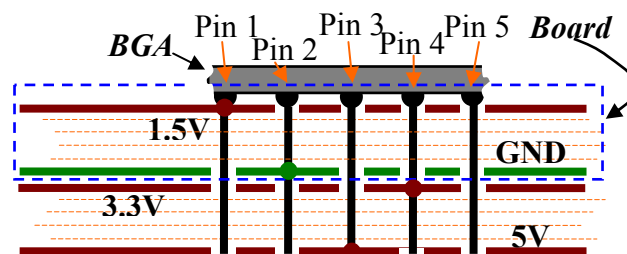
Fig. 1.1. Stack-up of the multilayer board under investigation. The power delivery network of interest corresponds to the GND-1.5V pair.

A detailed description of the power delivery network of interest is given in Fig. 1.2 (a), (b) and (c). The board has a rectangular shape of 10 cm by 8 cm and it is divided into five rectangular patches so that the center part labeled 3, where an IC footprint is located, is surrounded by four other sections. Two simple discrete ports are located on the section labeled 1 and one simple discrete port is located on the section labeled 5. The location of these ports is chosen to investigate the effect of the BGA footprint on the transfer impedance between Port 1 and Port 6 and between Port 1 and Port 7. The four sections surrounding the center one are rectangular parallel-plate geometries, which can be characterized by means of the Cavity Model approach, both in the format of tables of values or as equivalent circuit representations [1.6]-[1.10]. A close up of the cut out corresponding to the BGA footprint is shown in Fig. 1.2. The footprint corresponds to the center part of a real BGA packaged IC with all the pins assigned. However, only the central 15 by 15 connections out of the total 25 by 25, are represented in the 3D full wave model, to reduce the simulation complexity. The hole patterns on the top or on the bottom layer correspond, respectively, to the pins connected to the bottom or top layer. Also, when a pin is connected to the 3.3V plane or the 5V plane, antipads are present on both the GND plane and the 1.5V plane. Only four ports are defined within this geometry and a close up of the port model is shown in Fig. 1.2 (b).

The port model takes into account the entire interconnect from the IC package down to the top or bottom layer. Several elements constitute this interconnect, i.e., the balls of the BGA package, offset with respect to the vias, small sections of μ-strip lines, pads and vias. All the curved surfaces and volumes are replaced by parallelepipeds and the short μ-strip line sections are laid out perpendicularly to the sides, whereas, in reality,

they are along a diagonal direction. The distance between the 1.5 V and the GND plane is approximately 21 mils, the balls are cubes of 24 mils side, the vias have a cross-section
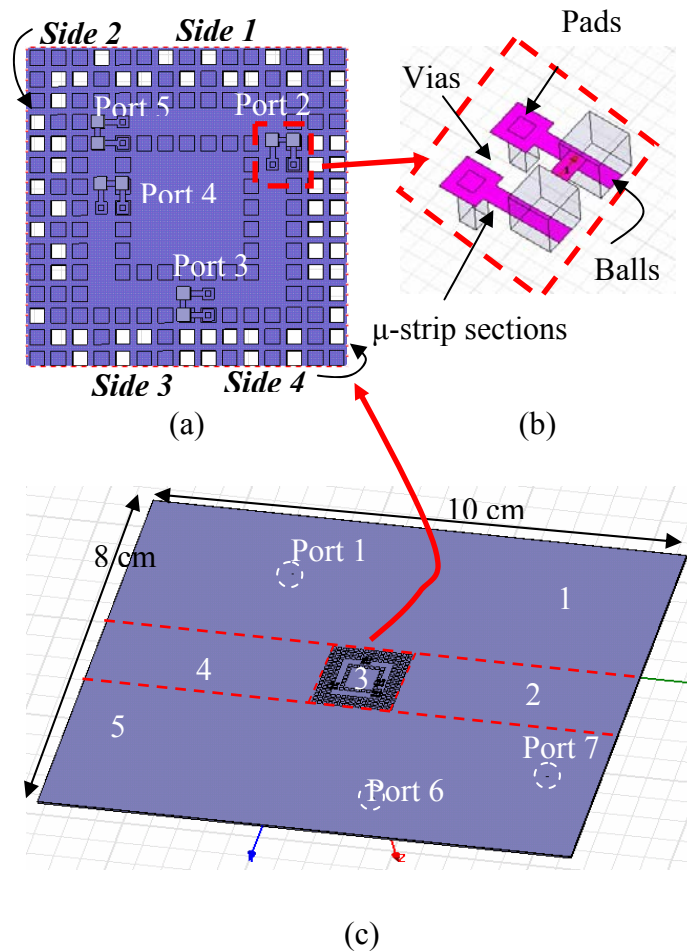
Fig. 1.2. Detailed description of the power delivery network of interest. (a) Close up of the BGA footprint. (b) Close up of the port model. (c) Overall view.

of 10 mils by 10 mils and they measure 25 mils from the bottom layer, the antipad hole are 28 mils by 28 mils and the distance between the center of two adjacent antipad is 40 mils. Finally, the pad are 22 mils by 22 mils and the length of the μ-strip lines from the edge of the antipad to the edge of the ball is 22 mils. Differently from the surrounding

rectangular sections, the center part cannot be described in terms of closed form expressions or simple equivalent circuit models. Hence, a 3-D full wave FEM simulator is employed to characterize the geometry in terms of a table of values and a black box approach is employed to extract an equivalent circuit model from the above table of values.

1.3 HOW THE SECTIONS ARE RECOMBINED IN TERMS OF THEIR EQUIVALENT Z-PARAMETER MATRICES

The divide-and-conquer approach outlined in the introduction is carried out by employing the concept of the segmentation method [1.3] -[1.4]. This procedure has been extensively used in power delivery applications in combination with the Cavity Model approach [1.6]-[1.10]. The application of the procedure is described in Fig. 1.3 for an irregular parallel-plate geometry with two external ports. The irregularly-shaped geometry is first partitioned into two regular patches. Closed form expressions are now available for the two patches and a number of internal ports are created along the edges where the two patches were connected at a distance usually dependent upon the maximum frequency of interest.

The Cavity Model approach in then employed to calculate two matrices of Z-parameter data associated with the external Port 1 plus the internal Ports Ai and Port 2 plus the internal Ports Bi. It is common to locate the sub-networks corresponding to the external ports in the left top part of the whole matrices $(Z_{11}$ or $Z_{22})$ and the sub-networks of internal ports in the right bottom part $(Z_{AiAi}$ or $Z_{BiBi})$. The remainder right-bottom and left-top sections are then filled with transfer impedance between the external ports and the internal ports and vice-versa $(Z_{1Ai}, Z_{2Bi}, Z_{Ai1}, Z_{Bi2})$. Finally, the recombination of the

patches is carried out by enforcing continuity of voltages and currents at the corresponding internal ports and solving for the equivalent impedance matrix looking into the two external ports. In Fig. 1.3, the final matrix is just a two-by-two matrix, whose elements are functions of the full matrices of Z-parameters calculated for the two rectangular patches. It is interesting to note that the approach is independent on the way the Z-parameter matrix data are obtained.

STEP 1

Original Geometry   Split Geometry

STEP 2

$$\begin{bmatrix} Z_{11} & Z_{1Ai} \\ Z_{Ai1} & Z_{AiAi} \end{bmatrix} \qquad \begin{bmatrix} Z_{22} & Z_{2Bi} \\ Z_{Bi2} & Z_{BiBi} \end{bmatrix}$$

Internal Ports

$$V_1 = Z_{11}I_1 + Z_{1Ai}I_{Ai} \qquad V_2 = Z_{22}I_2 + Z_{2Bi}I_{Bi}$$
$$V_{Ai} = Z_{Ai1}I_1 + Z_{AiAi}I_{Ai} \qquad V_{Bi} = Z_{Bi2}I_2 + Z_{BiBi}I_{Bi}$$

STEP 3

$$V_{Ai} = V_{Bi} \quad \& \quad I_{Ai} = -I_{Bi} \quad \begin{cases} V_1 = Z_{11}{}^* I_1 + Z_{12}{}^* I_2 \\ V_2 = Z_{21}{}^* I_1 + Z_{22}{}^* I_2 \end{cases}$$

$$\begin{bmatrix} Z_{11}{}^* & Z_{12}{}^* \\ Z_{21}{}^* & Z_{22}{}^* \end{bmatrix} = \begin{bmatrix} Z_{11} - Z_{1Ai}Z_T Z_{Ai1} & Z_{1Ai}Z_T Z_{Bi1} \\ Z_{1Bi}Z_T Z_{Ai1} & Z_{22} - Z_{1Bi}Z_T Z_{Bi1} \end{bmatrix}$$

$$where \quad Z_T = \left(Z_{AiAi} + Z_{BiBi} \right)^{-1}$$

Fig. 1.3. Example of the segmentation procedure.

Hence, it is possible to combine impedance matrices obtained from different methods as long as the same frequency points are used and the internal ports are defined and modeled correctly. For instance, the procedure in Fig. 1.3 can be applied on the impedance matrices extracted with the Cavity Model approach for the patches labeled 1,2 4 and 5 of Fig. 1.2(c) and the impedance matrix obtained with a 3D-full wave FEM simulator for the section labeled 3 of Fig. 1.2(c). The same number of internal ports at corresponding positions are defined between each pair of touching edges. Simple discrete ports are used in the 3D full-wave FEM model, while internal ports are defined as regular port within the Cavity Model approach. The spacing between two adjacent internal ports is equal to $\lambda_{min}/10$, where λ_{min} corresponds to the maximum frequency of 5 GHz, hence, a total of 6 internal ports per side are utilized along the footprint cut-out. The results obtained with this modeling strategy are compared with simulation results obtained by modeling the entire board of Fig. 1.2 with a 3D full-wave FEM simulator only. The comparisons of the results are shown in Fig. 1.4 and Fig. 1.5 for the self impedances looking into Port 1 and Port 2 of Fig. 1.2(c), respectively. Larger discrepancies are observed in Fig. 1.4 due to the different modeling of Port 1. In the first strategy, the Cavity Model approach is utilized to model Port 1, while a discrete port is utilized in the 3-D full wave FEM simulator. On the other hand, Port 2 is modeled in the same exact fashion in both cases, since it is located inside the BGA footprint section. Finally the transfer impedances between Port 1 and Port 2 and between Port 1 and Port 6 are compared in Fig. 1.6 and Fig. 1.7, respectively. Discrepancies between the different simulation results start to appear above 4 GHz. The accuracy of the first modeling approach is dependent upon the number of internal ports employed. Fewer ports make the
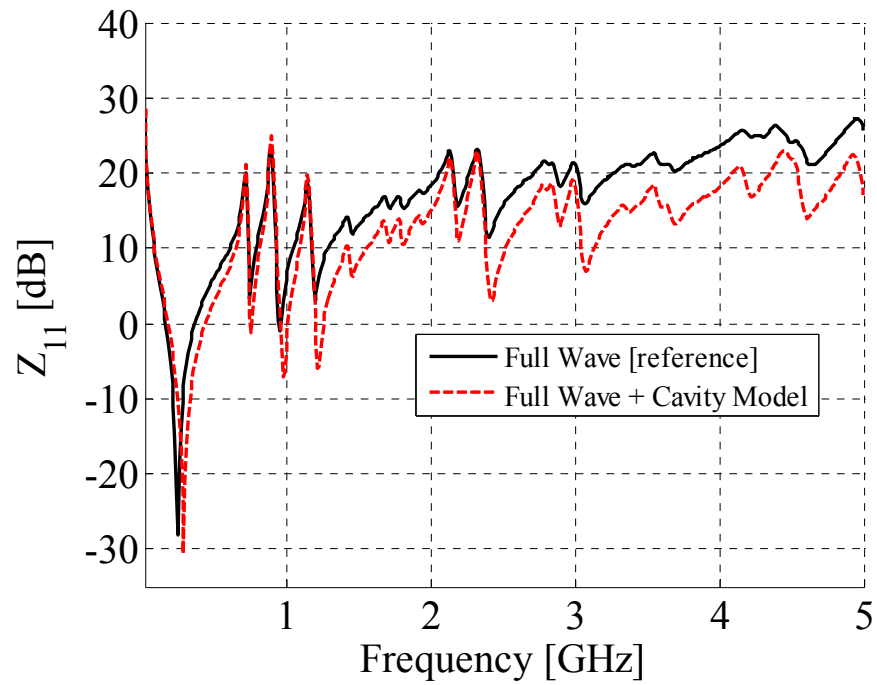
Fig. 1.4. Self-impedance comparison at Port 1 between the first modeling strategy and full wave simulation results.
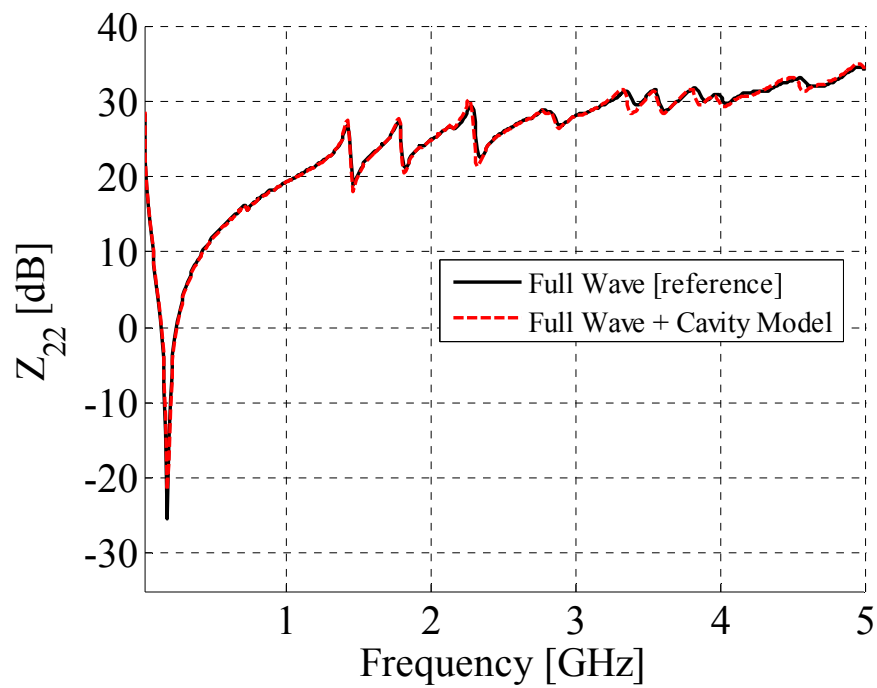
Fig. 1.5. Self-impedance comparison at Port 2 between the first modeling strategy and full wave simulation results.
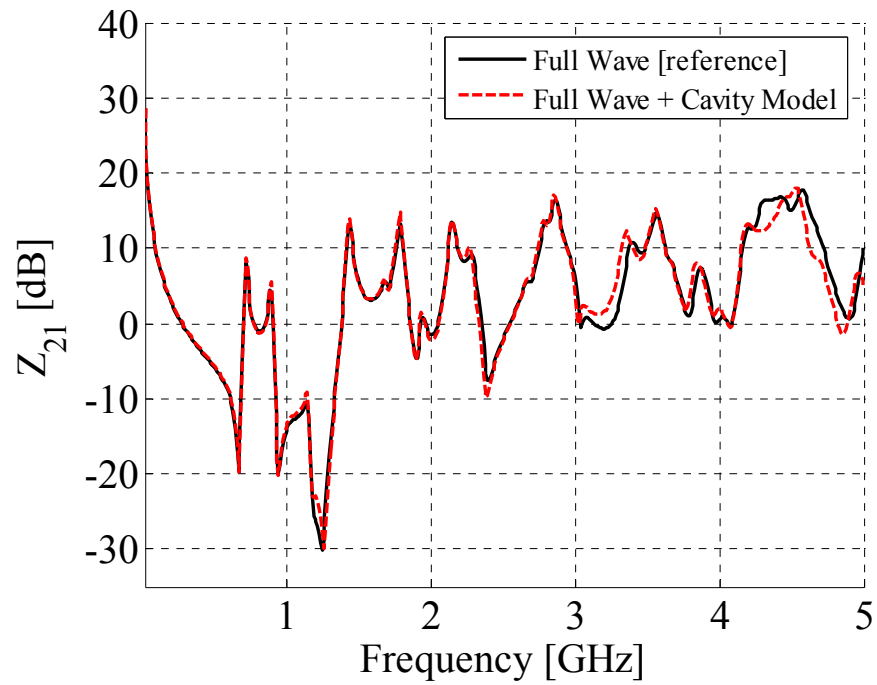
Fig. 1.6. Port 1 to Port 2 transfer impedance comparison between the first modeling strategy and full wave simulation results.
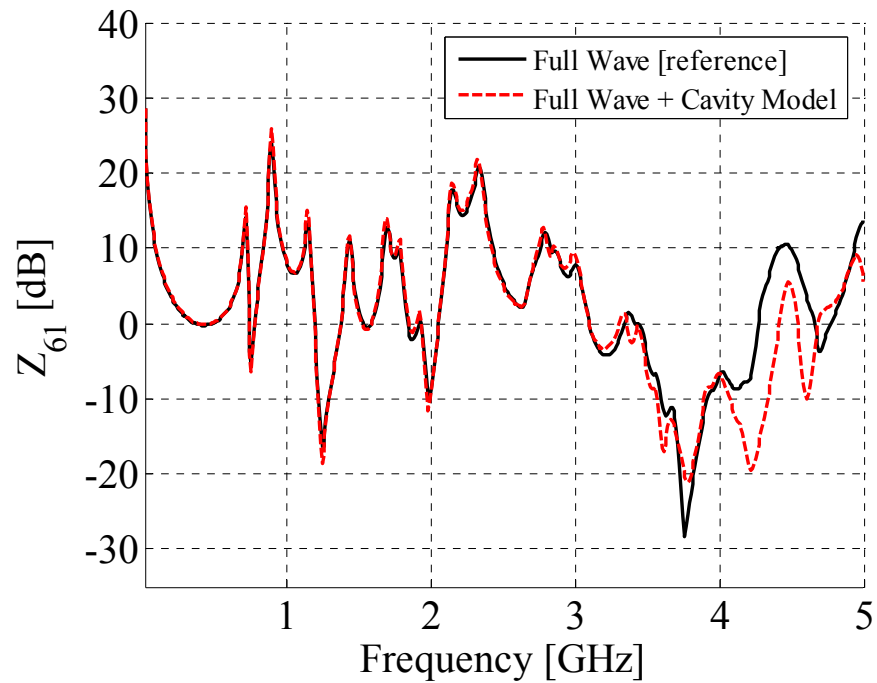
Fig. 1.7. Port 1 to Port 6 transfer impedance comparison between the first modeling strategy and full wave simulation results.

procedure less complex, but the continuity of the voltages and currents can occur only a few points, where the currents are crunched, hence, modeling artifacts are introduced. On the other hand, the employment of many ports improves the accuracy of the results, but the complexity of the segmentation procedure increases significantly. The employment of ten ports per wavelength has been empirically shown to be a good trade-off and further details will be discussed in section five regarding the number of internal ports and the distance of the internal ports from the perimeter of the BGA footprint.

1.4   HOW THE SECTIONS ARE RECOMBINED IN TERMS OF THEIR EQUIVALENT CIRCUIT MODELS

The interesting advantage of the segmentation method outlined in the previous paragraph is that it applies also to equivalent circuit models. Instead of carrying out the procedure shown in Fig. 1.3, the circuit models for each section of Fig. 1.2(c) can be joined together by connecting the corresponding internal ports of different patches. The equivalent circuit models associated with each regularly-shaped parallel-plate patch, i.e., 1,2,4, and 5 are obtained by employing the following formulation [1.6]-[1.10],

$$Z_{ij}(\omega) = \frac{1}{j\omega C} + \sum_{i=1}^{M}\sum_{j=1}^{N}\frac{N_{mni}N_{mnj}}{\dfrac{1}{j\omega L_{mn}} + j\omega C + \dfrac{1}{R_{mn}}} + j\omega L_{ij}^{HM} \tag{1.1}$$

where the first term, and the term C in general, corresponds to the equivalent capacitance of the rectangular patch, the double summation consists of a set of resonant R-L-C circuits corresponding to the resonant frequencies of the patch within the frequency range of interest and the last term is the higher order inductance L^{HM}. All the modes, whose resonant frequencies are beyond the highest frequency of interest, contribute to this term. Finally, the quantities N_{mni}, N_{mnj} and L^{HM}_{ij} are functions of the positions of the

ports with respect to the left bottom corner of the patch and port dimensions. On the other hand, a black box approach can be employed to extract an equivalent circuit representation from the simulated Z-parameter data. A circuit model for the center BGA footprint is extracted by means of IdEM, Identification of Electrical Macromodel [1.11]-[1.12], a tool developed within the EMC Laboratory of the Polytechnic University of Torino. Once the equivalent circuit models of the five sections of the geometry in Fig. 1.2(c) are obtained, the corresponding internal ports on the patches sharing a common side are connected. A frequency sweep is finally performed within a SPICE based tool by feeding with a 50 Ω voltage source Port 1 and monitoring the currents and voltages at all the ports, Fig. 1.8.

The comparison between the full wave simulation results and the SPICE simulation results are shown in Fig. 1.9, Fig. 1.10 and Fig. 1.11 for the input impedance looking into Port 1, the transfer impedances between Port 1 and Port 2, and the transfer impedance between Port 1 and Port 6, respectively. The same accuracy is practically observed and the same considerations as the previous modeling approach can be drawn. By virtue of the formulation, the same results are achieved when comparing the SPICE simulation results of the equivalent circuit models and the table of values both obtained with the Cavity Model approach. Also, the SPICE simulation results of the models extracted with IdEM reproduce well the set of data fed to the approach itself according to [1.11]-[1.12]. In reality, some differences are observed when comparing the circuit formulation and the close-form formulation of the Cavity Model approach, particularly noteworthy, the former employs fixed-value resistances to represent the losses, while the latter enjoys a frequency dependent expression [1.6]-[1.10]. However, this second
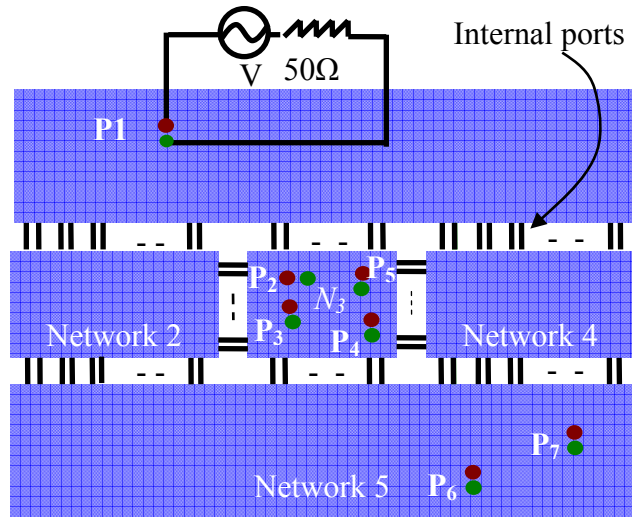
Fig. 1.8. Sketch of the overall equivalent circuit model obtained by connecting the cavity model equivalent circuit models for Networks 1, 2, 4 and 5 with the circuit Network 3 obtained by applying a black box approach on full wave data.
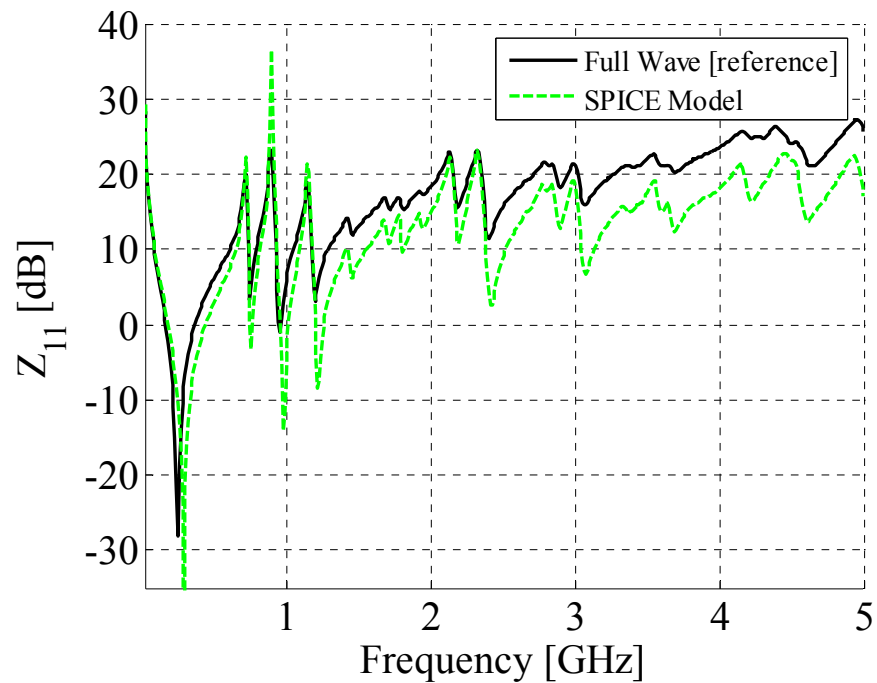
Fig. 1.9. Self-impedance comparison at Port 1 between the second modeling strategy and full wave simulation results.
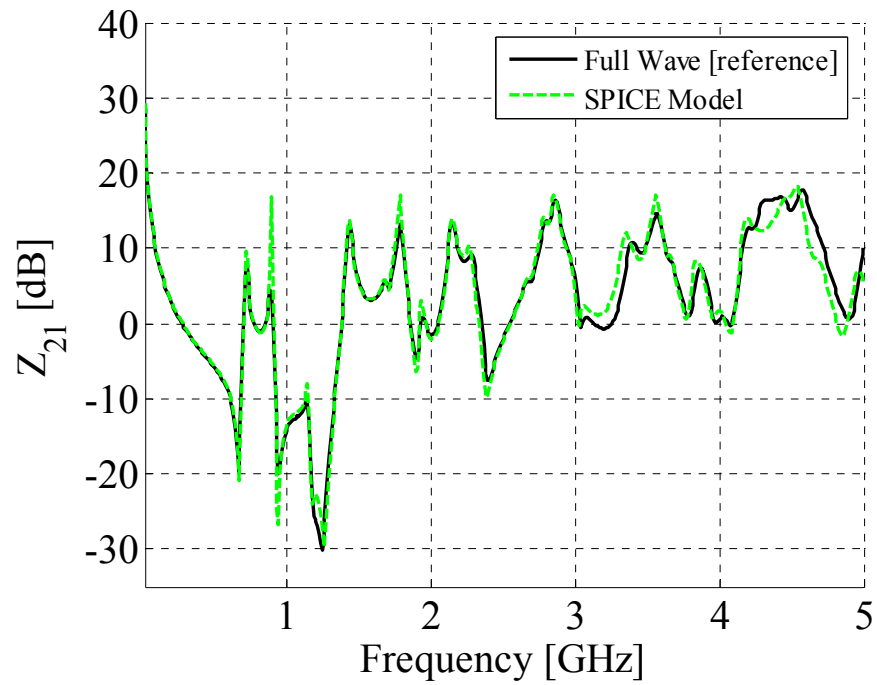
Fig. 1.10. Port 1 to Port 2 transfer impedance comparison between the second modeling strategy and full wave simulation results.
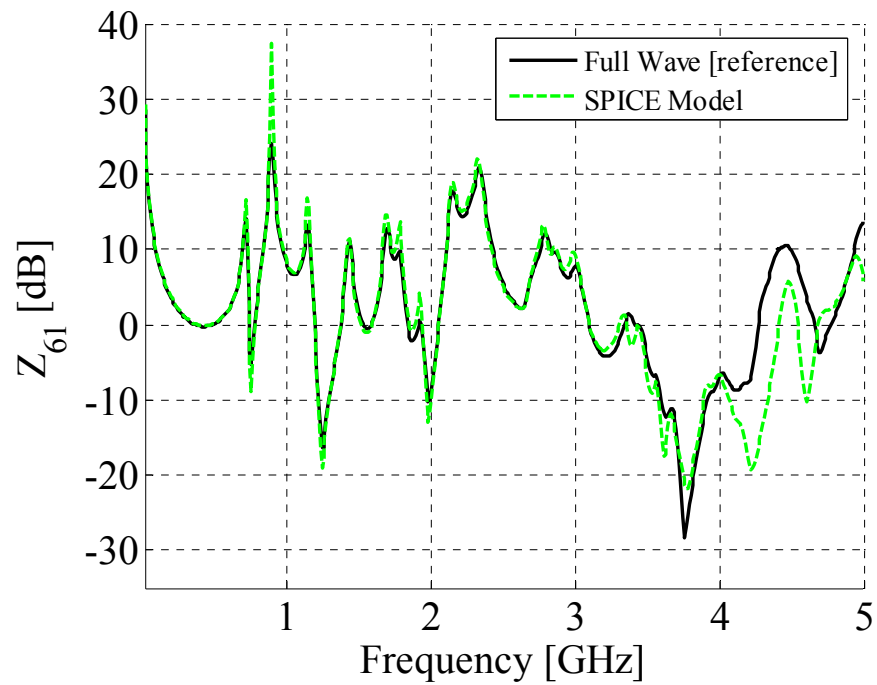
Fig. 1.11. Port 1 to Port 6 transfer impedance comparison between the second modeling strategy and full wave simulation results.

modeling approach allows both time domain and frequency simulations, hence, the investigation of power delivery issues can be performed in a complete fashion.

1.5   MODELING ISSUES: PORTS PER WAVELENGTH, CUTTING DISTANCE AND COMPUTATIONAL TIME

Before drawing some conclusions regarding the approaches presented in this article, further details should be discussed regarding the effects of the number of ports per wavelengths, the rationale in the choice of the distance between the perimeter of the BGA and the internal ports and, finally, the computational effort of the various modeling strategies. The number of internal ports per wavelength is usually the result of a the trade-off between accuracy and complexity. Several attempts on trial geometries were performed prior to the investigation of the geometry in Fig. 1.2, in order to estimate the most suitable number of ports per wavelength in the frequency range up to 5 GHz. Fig. 1.12 shows the comparison between the Z_{21} transfer impedance obtained with the 3D-full wave FEM simulator only and the first modeling approach with 5 ports per wavelength and 10 ports per wavelength. Five ports per wavelength are barely enough to obtain accuracy in the results up to approximately 700 MHz, while 10 ports per wavelength ensure a good correlation up to the maximum frequency of interest. Finally, the transfer impedance Z_{61}, Fig. 1.11, shows the worst agreement among the curves shown in section III, Z_{11} in Fig. 1.4 is manly affected by port modeling issues. However, the correlation between the reference behavior and the first modeling approach with 10 ports per wavelength is accurate at least up to 4 GHz. The second important issue to be discussed is the rationale behind the choice the distance from the BGA perimeter shown in Fig. 1.2, red dashed line surrounding the center part of the overall board geometry shown,
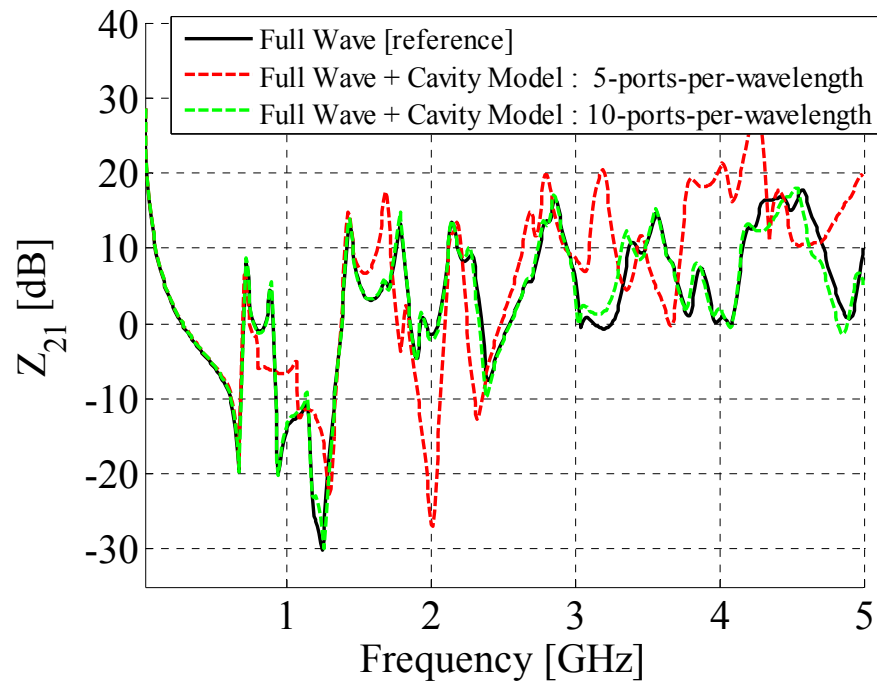
Fig. 1.12. Comparison of the hybrid modeling approach as a function of two number of internal ports per wavelength vs. the reference full wave simulation results.

to the points where to locate internal ports. These ports must be used to enforce continuity of voltages and currents between simple parallel-plate sections, where only TM_{zmn0} modes are present, and a BGA footprint section, where more complex field distributions are present. The results showed in the previous paragraph are all carried out by locating the internal ports 1-plane separation away, 21 mils, from the BGA perimeter. In fact, as long as the internal ports within the BGA section are away enough from the perimeter of the footprint, mainly the TM_{zmno} modes are supported, while all the others evanesce very rapidly. The variation of the fields as a function of the distance is investigated as it follows. Several field probes are located along side 2 and side 3 of the BGA footprint in Fig. 1.2 at increasing distance from the perimeter, i.e., zero, one, two and three plane separations away. The maximum values of the Ex and Ey fields are

recorded and divided by the maximum Ez field also recorded at the same locations. These two ratios as a function of the distance from the BGA footprint perimeter are reported in dB in Fig. 1.13 (a) and (b). Although a value greater than 42 mils or 2 times the plane separation would yield very accurate results, since there are practically no more Ey and Ex field components beyond this range, the ratios are both below -40 dB for all the distances, hence the Ez field can be considered to be always the dominant one. Hence, the conclusions drawn for the aforementioned geometry are considered to be valid.

(a) (b)
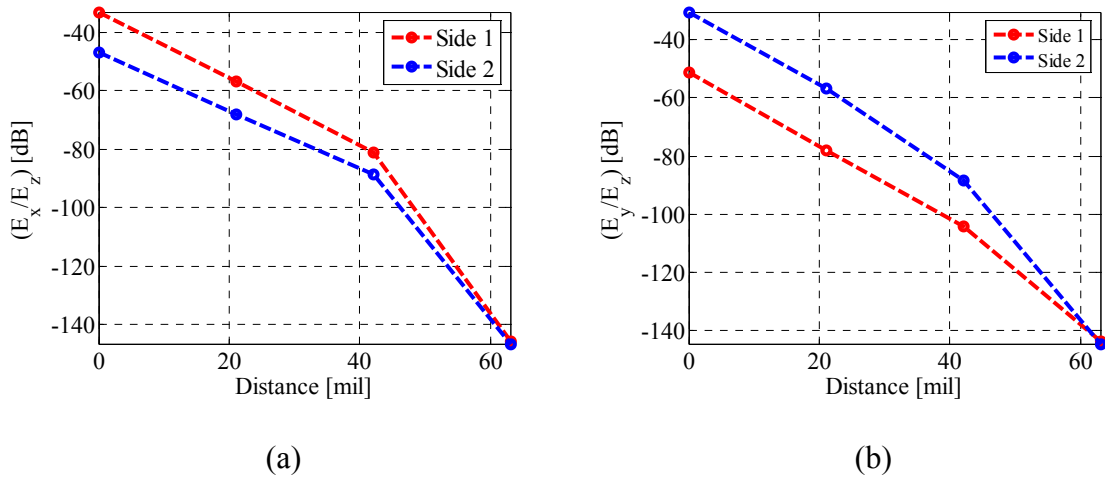
Fig. 1.13. Ratio of the maximum E_x and E_y fields over the maximum E_z field as a function of the distance from the perimeter of the BGA at two different sides. (a) E_x over E_z. (b) E_y over E_z.

A final discussion needs to be carried out regarding the computational effort associated with all the various pieces. For instance, the full wave model employed as the reference is characterized by the highest accuracy, but as soon as some of the parameters are changed, variations in the size and shape of the board, brand new simulations are required. Also the multi-scale features makes the computational effort time-consuming

On the other hand, the first modeling approach has the advantage that the center part can be recycled for as many shapes and sizes necessary or even utilized multiple times as long as the same number of ports per wavelength and type of cut-out is employed. This approach though is characterized by a lower accuracy, which is dependent on the frequency range of interest and the number of ports per wavelength utilized, but the full-wave computational effort is focused just on the center section. Finally, employing the second modeling procedure is even more versatile, since SPICE based tool can be utilized, time domain and frequency domain simulations can be performed and driver or receiver models also added. This second approach, though, is characterized by slightly less accuracy when compared to the first one, but this difference is practically negligible when comparing the corresponding simulation results of section III and section IV. Also the computational effort is slightly higher than the first one since the full-wave model for the center part needs to be run first, the black-box approach needs to be applied and only afterwards the SPICE simulation can be set up and run.

1.6   CONCLUSIONS

Two modeling strategies are presented in this article for investigating complex planar geometry. The first modeling approach has been shown to be viable and accurate, when compared to complete full wave simulations. It also has the advantage of reducing the computational burden by focusing the 3-D full-wave simulation just on a cutout corresponding to a section where many holes, vias and interconnects are present. Also, these simulation results can be reused if the shape of the surrounding parallel-plate geometry is changed as long as the same number and disposition of internal ports is maintained. The second modeling approach is also shown to be as accurate as the first

one, although the computational burden is slightly higher due to the additional extraction

procedure required. However, it is also more versatile, since it allows frequency and time

domain simulations for addressing power delivery issues in a complete fashion.

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2.   PHYSICS-BASED VIA MODELS WITH THE PARALLEL-PLATE IMPEDANCE INCLUDED: SINGLE-ENDED VIA MODELS

ABSTRACT

Concise physics-based models for vias are presented in this article. These models are built by employing few circuit elements, i.e., transmission lines to account for signal propagation on striplines, via-to-antipad capacitances to account for displacement currents between the via barrels and the antipad rims and, finally, parallel-plate impedances to account for the return paths associated with the vias. The via-to-antipad capacitance is calculated from a closed-form expression fitted on a set of values, which are obtained from 2D and 3D static simulations. On the other hand, the parallel-plate impedances are calculated from well-known formulas found in the literature. The effectiveness of these concise models resides in the possibility to rearrange the same circuit elements in order to model different via configurations. Also, the circuit elements are all calculated based on board geometry specifications and material parameters extracted from measured data. The models are finally run in a SPICE-like environment allowing for the possibility to carry out what-if scenarios due to the one-to-one correspondence between circuit elements and geometry features. The simulation results are ultimately validated by means of measurements on ad-hoc test sites realized with the purpose of capturing very precisely the physics of via transitions.

2.1.   INTRODUCTION

Vias in multilayer printed circuit boards and packages have been extensively investigated in the literature [2.1]-[2.15]. While the increase in complexity of on-board

systems have required the utilization of vias, since limited on-board space prevents from routing the links entirely on one layer, the increase of data rates makes the modeling of the vias as important as the modeling of their corresponding return paths. Moreover, vias are characterized by the same barrel radius and antipad radius, while the corresponding return paths are different and dependent upon many parameters. The characteristic discontinuity of the via plus its return path constitutes a limiting factor in the design performance, especially when the discontinuity itself is not modeled correctly and the link behavior cannot be predicted, at least within some bounds. Modeling just the via barrel is quite simple, while taking into account its return path is challenging, since all the possible paths leading the current back to the source need to be accounted for. Neglecting some of them may lead to an underestimation/overestimation of the performance, hence to incorrect designs and expectations. Alongside the numerous modeling attempts reported in the literature, frequency domain or time domain wave simulators, both commercial and in-house, have been shown to be capable of modeling a large variety of complex via configurations with the desired accuracy. The major drawback in the utilization of such tools is the computational effort, due to the different scales of the model features, i.e., from the few-mil scale up to the many-inch scale. It would be preferable to investigate the via geometries within SPICE or SPICE-like based tools, which are more versatile and can take into account driver and the receiver models. Employing black-box circuit models obtained from simulation data or measured data is also a viable solution, although these models suffer from the lack of one-to-one relationship between circuit elements and geometry features. The models presented in this article belongs to the category of physics-based models, for which it is possible to

establish a one-to-one correspondence between geometry features and circuit elements. In short, the models, whose topology has been presented in the literature [2.5],[2.11], combine the equivalent circuit representation of the signal propagating on a strip/μ-strip line and the signal propagating between a parallel plate configuration, i.e., via and its return path. Due to the skin-effect, the energy launched on the transmission lines is coupled into the parallel-plate configurations only through the via-antipad gaps, where it is possible to render, as a first order approximation, a capacitance. In order to explore the correctness of this approach, a confined environment is created around the signal vias, so that the return path is controlled and easily modeled by employing the Cavity Model approach. Measurements are utilized to validate the SPICE/SPICE-like simulation results of these physics-based via models. Several via test sites are laid out for this purpose on a 16-layer printed circuit board. Each via configuration is enclosed into a cage of ground vias in order to achieve the desired field containment. The recessed probe launch technique [2.16] and a VNA are employed in the measurement set-up. The topics in this article are unfolded, starting from the second paragraph as explained afterwards. The underlying approach and the basic constituting elements are introduced in the second section. Then, two full-via models are built and compared with measured data in the third section.. A zero and 1st order model approximation of the parallel plate impedance is employed instead of the complete formulation and the results are all compared in the fourth section. The assumptions and the limitations of the models are discussed in the fifth section and finally some conclusions are drawn in the sixth section. Vias in multilayer printed circuit boards and packages have been extensively investigated in the literature, since these elements account for the most complex features to be modeled.

2.2. SINGLE-ENDED VIA MODELING: THE PARALLEL-PLATE IMPEDANCE AND THE VIA-TO-ANTIPAD CAPACITANCE

Observations on the fields inside the via geometry can help constructing concise circuit models. An example of how these models can be devised, according to the approach described in [2.1]-[2.5], is shown in Fig. 2.1 (a), (b) and (c).
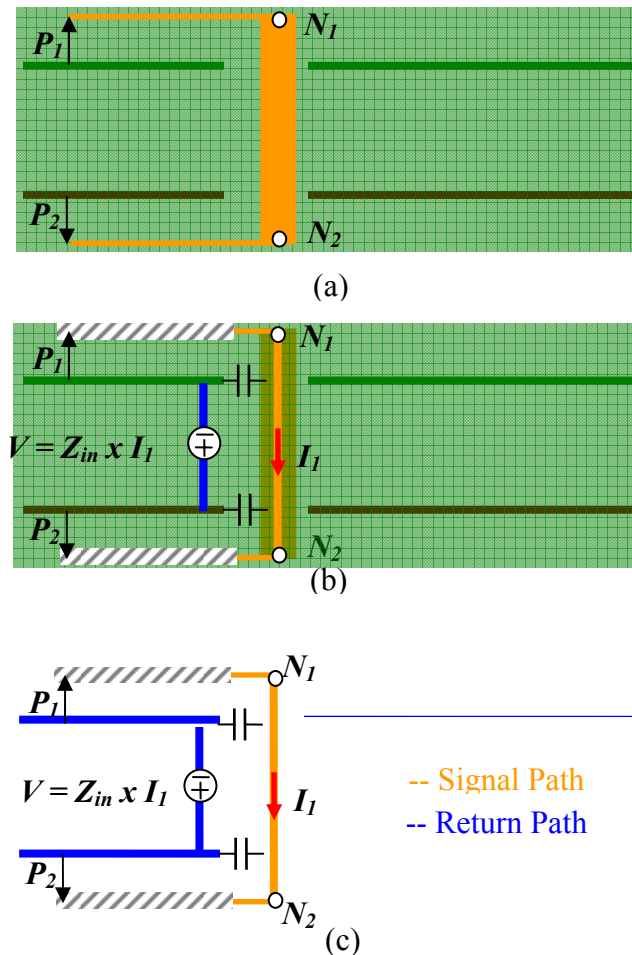
Fig. 2.1. (a) Geometry under investigation. (b) Geometry and corresponding circuit model. (c) Circuit model only.

The electromagnetic fields along the μ-strip lines primarily propagate in a TEM fashion, making a transmission line model the most suitable circuit representation. On the

other hand, the current flowing on the via barrel establishes transverse magnetic fields within the metal plates as a function of the characteristic geometrical features, such as transverse dimensions, plane separation, boundary conditions, dielectric properties, etc. This propagation is represented as a current controlled voltage drop on the return path associated with the via. Finally, the transition between the μ-strip and the parallel-plate excites complex field patterns. These are necessary to ensure the continuity of the fields as the signal goes through this transition. When looking at the current flow and the charge accumulation in this region, it appears straightforward to render a capacitance between the outer surface of the via barrel and the rim of the antipad hole, at least as a first order approximation.

In the modeling approach presented in this article, the parallel-plate impedance constitutes the first of the two fundamental elements employed to represent the via and its return path. Closed form expressions for the boundary value problem associated with a cavity is available in the literature for Perfect Magnetic Conductors (PMC), Perfect Electric Conductors (PEC) and Perfectly Matched Layers (PML), [2.4],[2.18]-[1.10]. Although it is common to consider only the first type of boundary conditions, when dealing with PCB geometries, far more complex field patterns are observed in the real board configurations, where the presence of many other vias also disrupt and attenuate the TM_{mn0z} field patterns. Employ PEC boundary conditions is more appropriate when many other vias are in proximity of a signal via and PML boundary conditions are more descriptive of the physics, when the amount of energy reflected at the boundaries is not important. The input parallel-plate impedance profiles shown in Fig. 2.2 are associated with the lateral dimensions and the port location specified in Fig. 2.2 for three
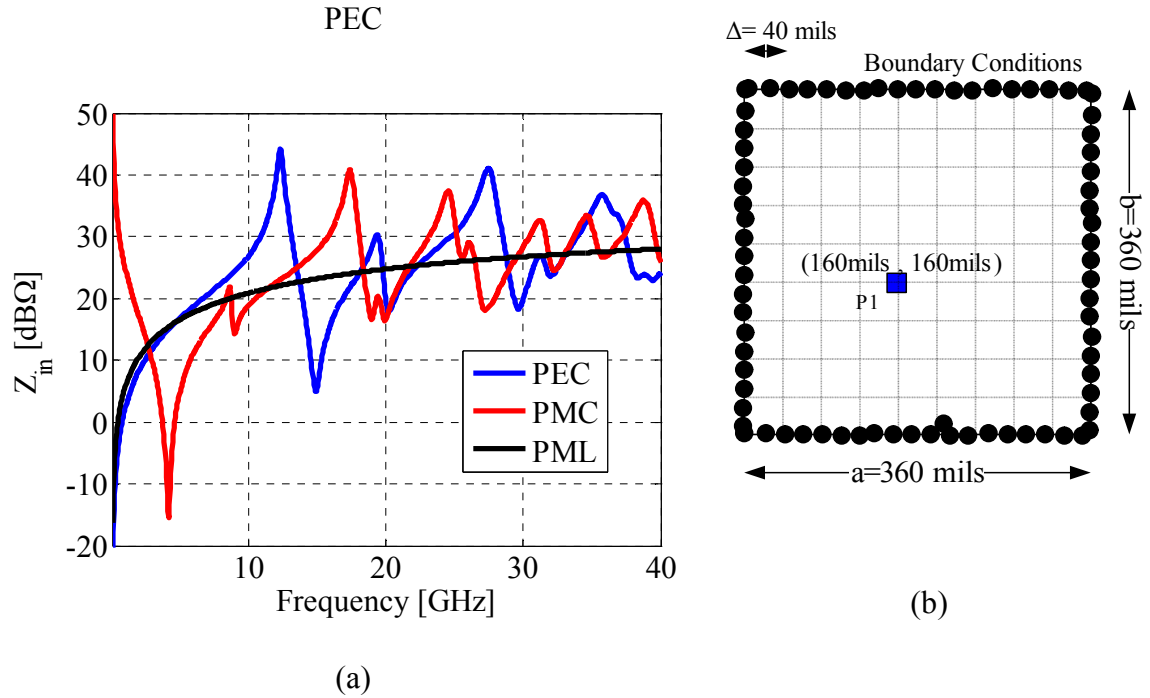
Fig. 2.2. (a) Example of the parallel-plate impedance associated with geometry in (b) for different boundary conditions. (b) Geometry under investigation.

different types of boundary conditions, perfect magnetic and open boundary conditions. More details regarding the choice of this particular geometry are given in the next paragraphs. The separation of the copper plate is approximately 12 mils and the dielectric material characteristics are extracted from measured data and coincide with those utilized later in the actual via modeling. Both frequency dependent permittivity and tangent delta are employed in the impedance closed-form expressions. The differences between the PEC and the PMC profiles are mainly due to the different spatial relationships of the two impedance formulas. The PEC formula contains sines, while the PMC one contains cosines. Also, the input port sees an open at DC in the PMC case and a short at DC in the PEC case. Finally, the PML case does not show any resonant behavior over the entire frequency range [2.4].

In the modeling approach presented in this article, the via-to-antipad capacitance constitutes the second of the two main elements employed to represent the via plus its return path. This circuit element is obtained by looking at the board stack-up and extracting a core geometry consisting of one solid metal plane with an antipad hole and a section of a via symmetrically placed inside the antipad hole, Fig. 2.3. This configuration is defined as core, because the multilayer stack-up can be built by stacking up several of these core elements, as shown in Fig. 2.3 (b). The symmetrical disposition of the via with respect of the antipad comes from the rationale employed to split up the multilayer configuration. Due to the equally-spaced plane pair, cutting along the midpoint between two planes corresponds to cut along a line where the normal component of the electric field is zero. Hence a very easy geometry is obtained which can be investigated by means of various approaches, Fig. 2.3 (a). Another location where the electric field is perfectly radial is along the line of symmetry shown as a red dash-dotted curve in Fig. 2.3. Each half geometry corresponds exactly to half of the capacitance extracted for the full configuration and the multilayer stack-up can also be seen as a combination of multiple half capacitances as well. This second approach, although equivalent to the first one, simplifies the stacking of multiple plane pair where different dielectric materials and different plane separations are present.

One of the method utilized to extract the capacitance values for the configuration Fig. 2.3, as a function of the various parameters, is a two dimensional Finite Difference method which is implemented by setting up the domain of interest and meshing the two dimensional geometry associated with the configuration characterized as in Fig. 2.3. By considering the radial symmetry which significantly characterize such geometry,
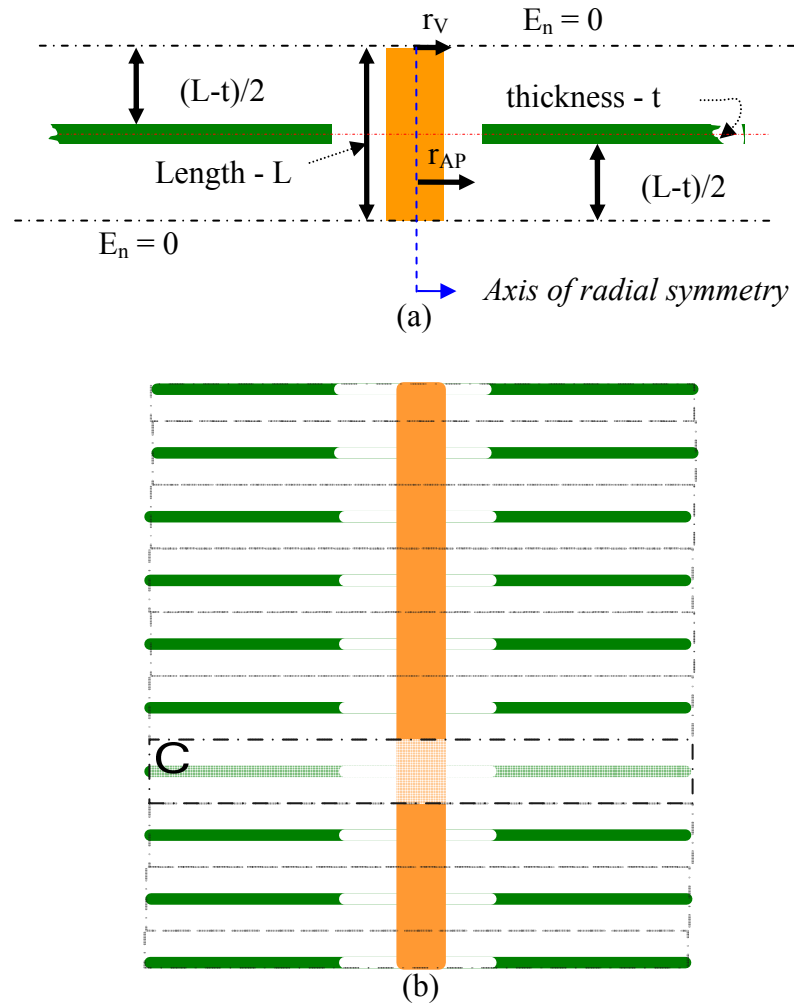
Fig. 2.3. (a) Core geometry constituting the multilayer geometry of interest. (b) Multilayer geometry of interest.

Laplace equation in polar coordinates can be set up and solved for the geometry obtained by cutting along the axis of radial symmetry the geometry in Fig. 2.3, as shown in Fig. 2.4. The capacitance of the geometry in Fig. 2.4 is numerically extracted and the final via-to-antipad capacitance is obtained by multiplying this value by 2π. Some values extracted with this approach are compared to the values extracted with a 3D static FEM solver and the comparison for three different via radii, as a function of the length, is shown in Fig. 2.5. The 2D FD cell employed is 0.5 mils by 0.5 mils and the external

radius, r_{EXT} in Fig. 2.4, is approximately 50 mils. This value is chosen in order to capture all the electric field lines going from the via barrel and terminating on the horizontal metal surface. The larger this value, the larger the computational domain, the more accurate the solution. The choice of the external radius is also required for setting up the static 3D FEM simulations. Further investigations as a function of r_{EXT} showed 200 mils to be a convergent value in these simulations and the capacitances reported in Fig. 2.5 are all extracted for an external radius equal to this value.
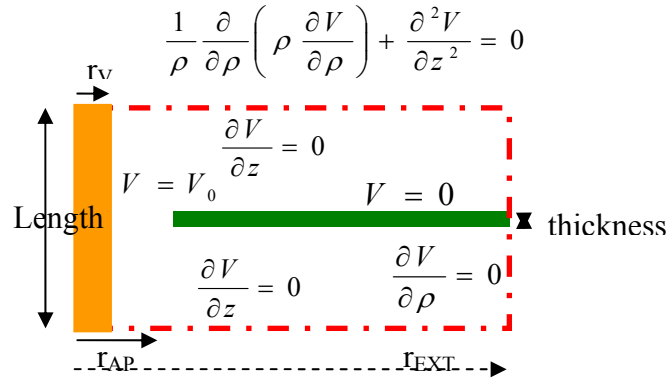
Fig. 2.4. Two dimensional surface where Laplace equation in polar coordinates is set up and solved.

An additional achievement has been the derivation of a closed-form expression for the via-to-antipad capacitance as a function of the length, the via radius, the antipad radius and a plane thickness of 1 mil. This expressions has been extracted by fitting a large set of values obtained with the 2D FD code by letting the via radius to span the range between 5 and 10 mils, the antipad radius to span between 15 and 25 mils, and the length between 4 to 18 mils. The expression is given in Eq.(1) and it is compared with the capacitance values extracted with the 2D FD code in Fig. 2.6. The maximum derivation

of the closed-form expressions with respect to the calculated values is within ±5%. Equation (2.1) is given as a function of the length over the natural logarithm of the ratio between the antipad radius and the via radius. This functional relationship is characteristic of a coaxial cable, and the geometry tends to a coaxial configuration as a limiting case, since the quadratic term can be neglected for small values of the ratio. For simplicity, the expression assumes relative permittivity equal to 1, the dimensions need to be input in mils and the capacitance values are given in femtoFarad.

$$C_{v2a} = -0.011 \left(\frac{L}{\ln\left(\frac{r_{AP}}{r_V}\right)} \right)^2 + 1.3983 \left(\frac{L}{\ln\left(\frac{r_{AP}}{r_V}\right)} \right) + 0.1412 \tag{2.1}$$
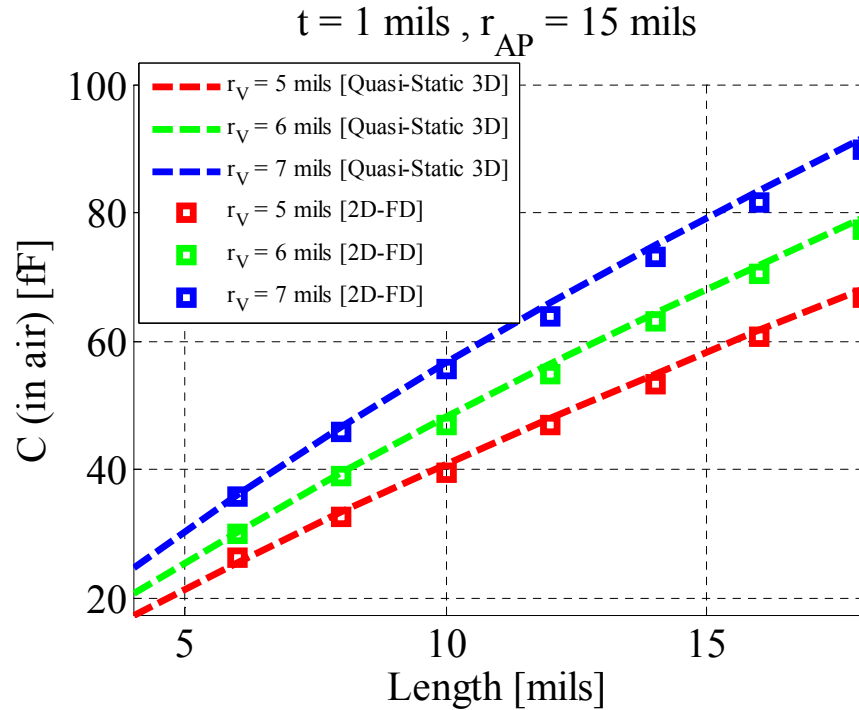
Fig. 2.5. 3D static FEM solver vs. 2D FD approach.
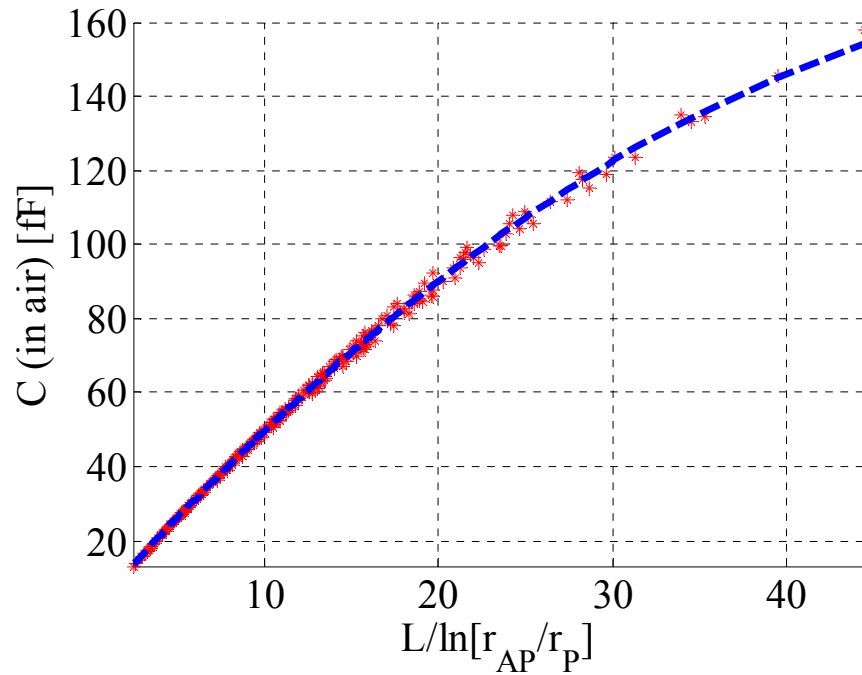
Fig. 2.6. Capacitance value comparison between 2D FD code and fitted closed-form expressions of Eq. (2.1).

2.3. BUILDING THE VIA MODELS AND COMPARISON WITH MEASURED DATA

After introducing the two fundamental elements, equivalent circuit models can be obtained for multilayer via configurations by following the example outlined in Fig. 2.1. The modeling is carried out by using a SPICE-like type of tool, ADS, and the simulation results are compared with real via geometries realized on a multilayer PCB and measured by employing the Recessed Probe Launch Technique [2.16]. Many test sites, such the ones shown in Fig. 2.7, are employed for validating the via models presented in this article and being investigated at the time of this article is being written. All the test sites realized for validating purposes although they are all not practical for an application point of view and cannot be used in real world-scenarios.

(a)   (b)
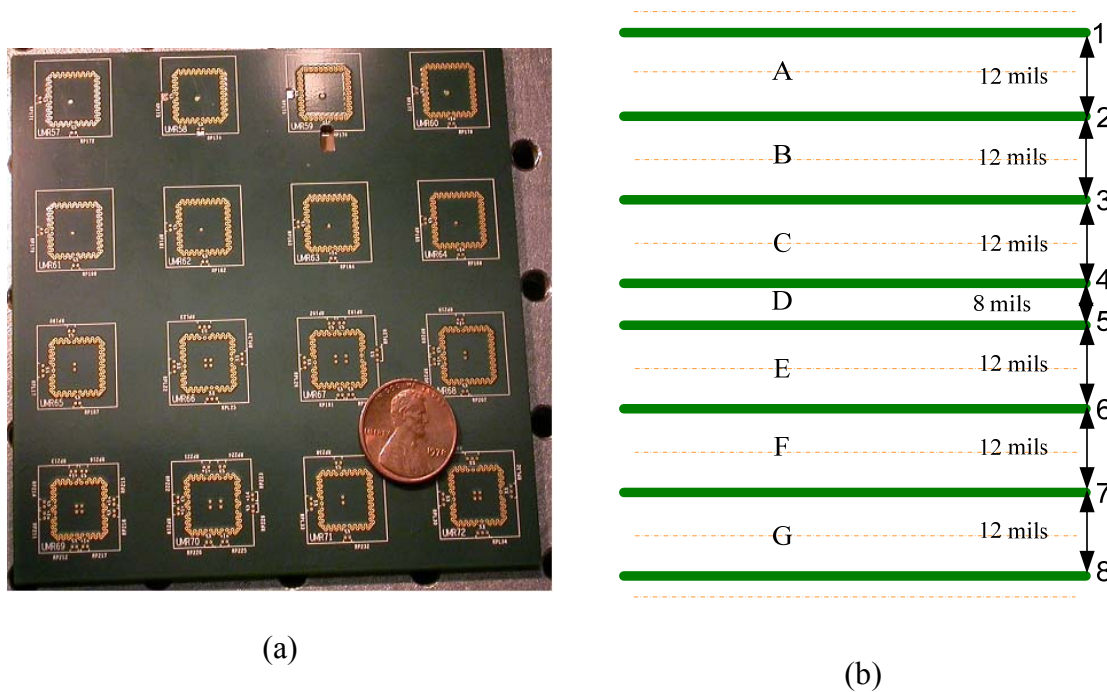
Fig. 2.7. (a) Sample of test sites realized on a 16-layer board. (b) Board stack-up.

Figure 2.7 show a sample set of these test sites, which are all laid out on a 16-layer board that has 8 solid planes, as shown in Fig. 2.7 (b). The solid planes are arranged to create 7 resonant cavities of 8 mils nominal height and 12 mils nominal height, for the center cavity and for all the remaining cavities, respectively. The nominal transverse dimensions of the ground cage of vias are - from via center to via center - 360 mils by 360 mils, while the via and antipad radii are 5 mils nominal and 15 mils nominal, respectively. An FR-4 type of material is employed as substrate and several test sites are utilized to extract the board material properties based on the work published in [2.17]. A mean permittivity value and a mean tangent delta value are also obtained by averaging over the frequency range the frequency-dependent parameters extracted. The frequency dependent values are used in the parallel-plate impedance calculations, whereas the mean

values are employed to calculate the via-to-antipad capacitances and in the lossy transmission line models. Additional destructive verifications allowed to discover a discrepancy between the real value and the nominal value of the via radius, which was found to be larger than 5 mils, i.e., approximately 7 mils. The deviations from the nominal values of all the dimensions of the via geometries are due to fabrication tolerances. A through via configuration is initially considered. This geometry consists of two stripline sections laid out between the top-most plane pair and the bottom-most plane pair. These two striplines are connected by means of a through hole via barrel perforating the entire stack-up. The PCB layout excerpt and the stack-up geometry of the through via are shown in Fig. 2.8 (a) and (b). The cavities, where the stripline are laid out, are not labeled because they are neglected in the equivalent circuit model and the location of the via with respect to the ground cage corresponds to the coordinates of P_1 in Fig. 2.2 (b). The ADS model is built by employing two 250 mils long lossy transmission line models, this length corresponds approximately to the length between each launching port located outside the ground cage and the through via. These models are implemented by employing a relative dielectric constant of 3.84 and a loss tangent of 0.033. Also, six capacitances of three different values are utilized, C_1, C_2 and C_3, respectively. These capacitances are obtained by using the fitted closed-form expression described in the previous paragraph. The first capacitance, C_1, is used to model the transition between the top-most cavity and the cavity B and the transition between the cavity F and the bottom-most cavity. The second capacitance, C_2, represents the transition between the cavities B and C and the cavities E and F. Finally, the third capacitance, C_3, is employed to model the transition between both the cavity C and D and between the cavity D and E.
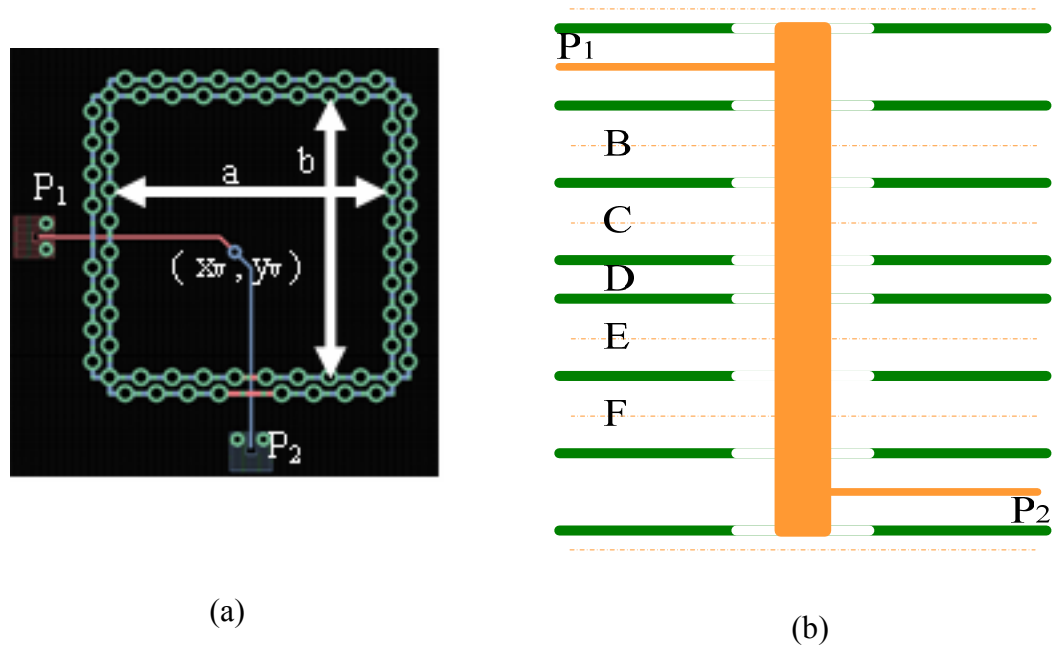
Fig. 2.8. (a) PCB layout excerpt of the through via. The coordinates (x_v, y_v) correspond to P_1 in Fig. 2.2 (b). (b) Stack-up of the through via geometry.

The capacitance C_1 is equal to the capacitance C_2 plus half of C_2, which corresponds to the capacitance associated with the half via between the top-most stripline and the top solid plane or, likewise, the half via between the bottom-most stripline and the bottom solid plane. The simulations are carried out and compared for several via radii, 5 mils, i.e., the nominal value, 6 mils and 7 mils. Three sets of capacitances are then obtained as a function of these via radii, a via antipad of 15 mils, a plane separation of 12 mils and 8 mils and a plane thickness of 1 mil. Also, the parallel-plate impedances are computed for a 12 mil and an 8 mil cavity with PEC boundary conditions. Both cavities are assumed to have lateral dimensions equal to the nominal via-center to via-center value, 360 mils by 360 mils, minus the via diameter, also, the coordinates of the signal via correspond to the coordinate of P_1 in Fig. 2.2 (b) and the impedances are calculated

by employing the frequency dependent material parameters extracted from measured data. Both the parallel-plate impedances are converted into S-parameter data in touchstone format and imported into ADS. The various circuit elements, summarized in Table 2.1, are finally connected as shown in Fig. 2.9, a frequency domain simulation is run from 50 MHz up to 40 GHz and compared to measured results. The measured data are acquired by hooking up a network analyzer to a pair of calibrated surface probes and the Recessed Probe Launch Technique [2.16] is utilized to obtain the S-parameters data. The S_{11} simulation results, given in Fig. 2.10, are actually characterized by an higher sensitivity to the variation of parameters due to the small values assumed. While, the transmission parameter of Fig. 2.11 shows a better agreement than the reflection parameter, especially when looking at the frequency range below 10 GHz.. For instance, by varying the value of the via radius, hence, the value of the via-to-antipad capacitance, no significant effects are observed in the transmission parameter S_{21}, while the low frequency profile of the reflection parameter S_{11} changes significantly. Prediction simulations, then, must be conducted as a function of geometry parameters since the exact dimensions are known just within factory tolerances   and the via configuration performances can be found just within some bounds. This problem, though, affects any modeling approach, whether full wave or circuit-based. The modeling approach described in the previous paragraph proposes to recycle the circuit elements utilized for the through via also for other via configurations, a stub via geometry for instance. The PCB layout excerpt of this configuration and the stack-up associated with it are shown in Fig. 2.12, respectively. The configuration consists of two striplines, laid out between the top-most pair of plane. These two striplines meet each other where a through via is left hanging.

Table 2.1. Summary of the elements employed in the model.

$Z_0 = 50\Omega$, Length = 250 mils, $\varepsilon_r = 3.84$, tg$\delta = 0.033$
Lossy TL model

	C_1 [fF]	C_2 [fF]	C_3 [fF]
5 mils	$87 = (1+\frac{1}{2})C_2$	58	50
6 mils	$102 = (1+\frac{1}{2})C_2$	68	59
7 mils	$120 = (1+\frac{1}{2})C_2$	80	69

Via-to-Antipad capacitance values employed

Example of parallel-plate impedances to be imported into a 1-Port S-parameter component in touchstone format

1-Port S-parameter data item (1 Port → 2 Nodes)
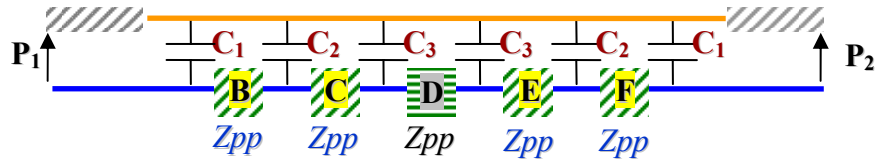
Fig. 2.9. Complete equivalent circuit model of the through via described in Fig. 2.8 based on the elements described above and summarized in Table 2.1.
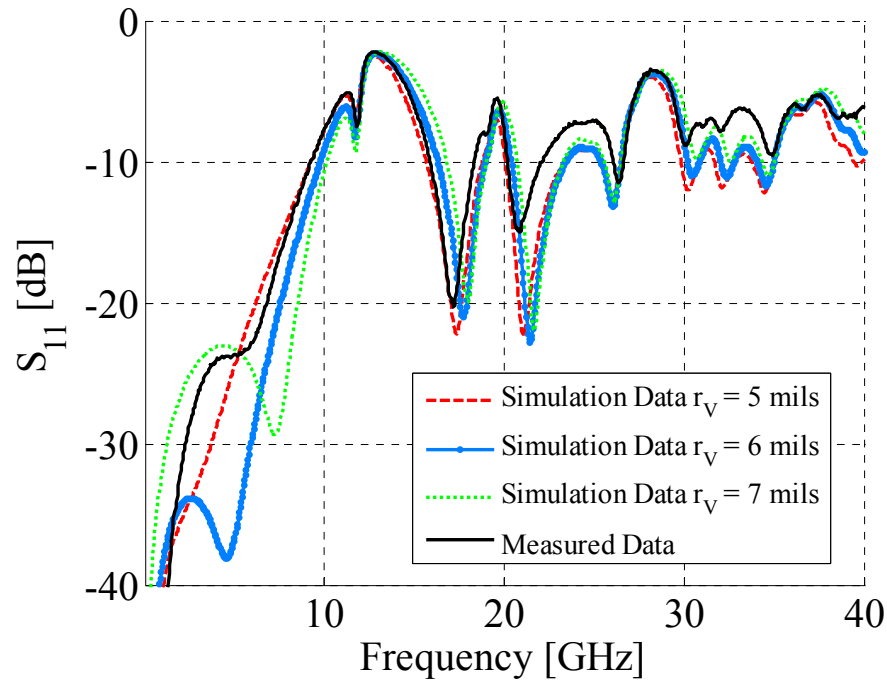
Fig. 2.10. Reflection parameter comparison between measured data and simulation results for the through via geometry shown in Fig. 2.9.

Again, the top-most cavity is not labeled because is to be neglected in the procedure. The equivalent circuit model associated with the stub via of Fig. 2.12 (a) and (b) is shown in. The circuit is realized by rearranging the circuit elements shown Fig. 2.9 to reflect the new geometry configuration. The only new element is C_4, which corresponds to the capacitance associated with the half via between the midpoint of cavity G and the bottom solid plane.
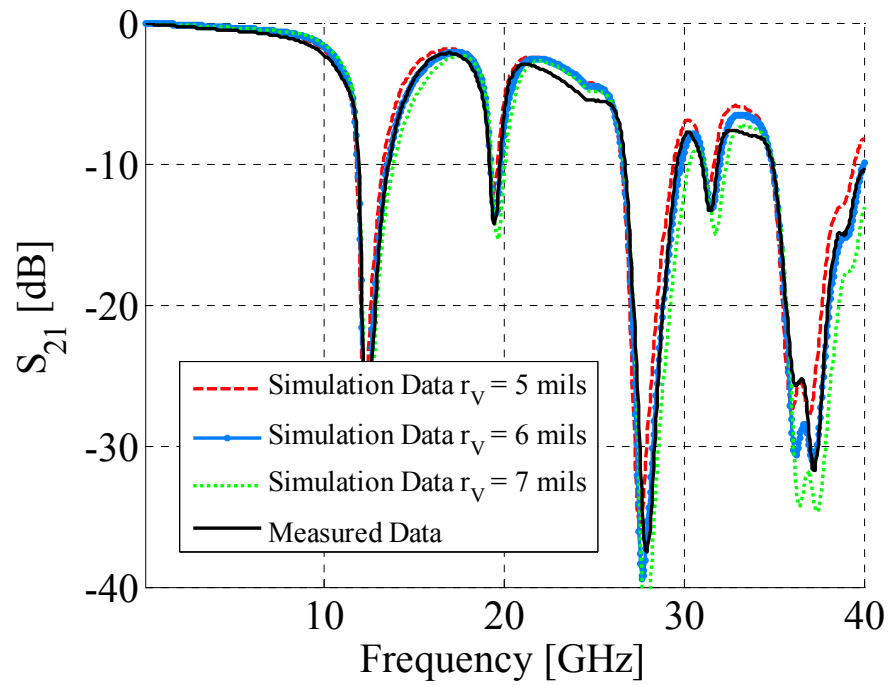
Fig. 2.11. Transmission parameter comparison between measured data and simulation results for the through via geometry shown in Fig 2.9.

(a)

(b)
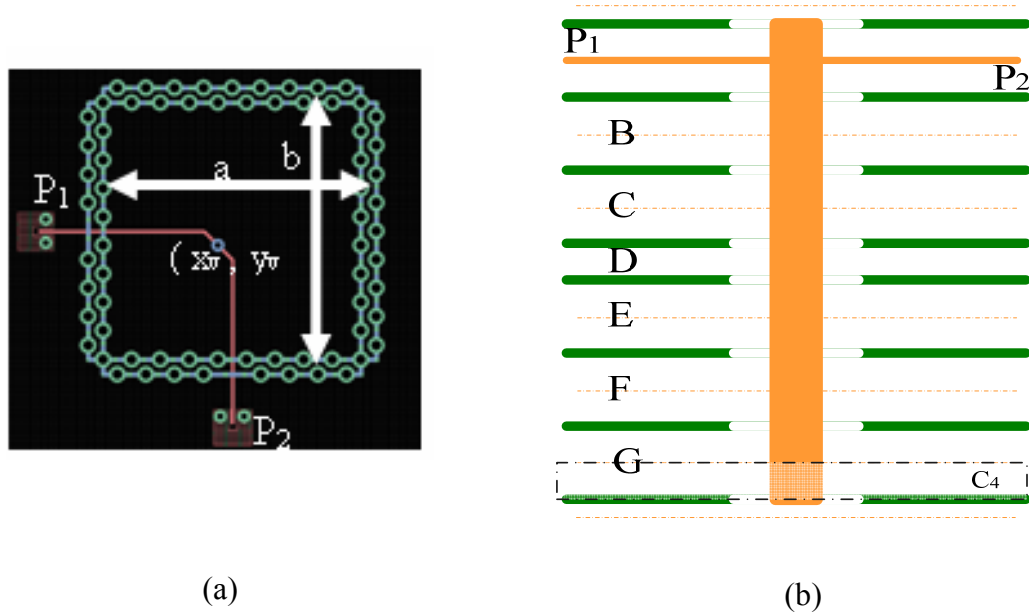
Fig. 2.12. (a) PCB layout excerpt of the stub via. The coordinates (x_v, y_v) correspond to P_1 in Fig. 2.2 (b). (b) Stack-up of the stub via geometry.
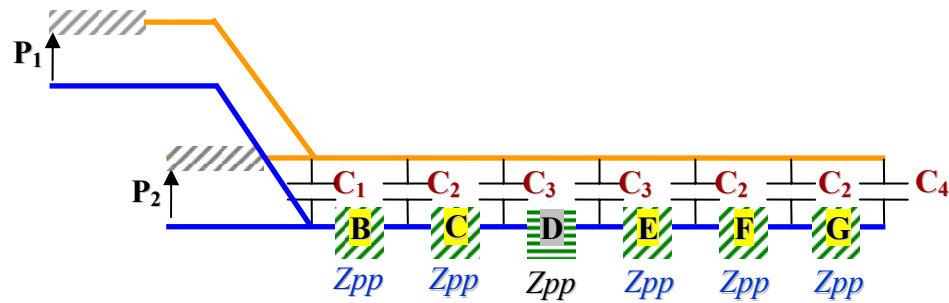
Fig. 2.13. Complete equivalent circuit model of the stub via described in Fig. 2.12 and based on the circuit elements described above and summarized in Table 2.1.

The values employed are 29 fF , 34fF and 40 fF for 5 mils, 6 mils and 7 mils via radius, respectively. These values are obtained by utilizing the closed form expression introduced in the previous section. The model-to-hardware correlation shown in Fig. 2.14 and Fig. 2.15 for both the transmission and reflection parameters indicates that the topology and the circuit elements are able to capture the physics of propagation also for this via configuration. Contrarily to the previous through via case, both S_{11} and S_{21} simulated parameters show the same agreement with the measured data. The reflection parameter in the low frequency range, though, is lar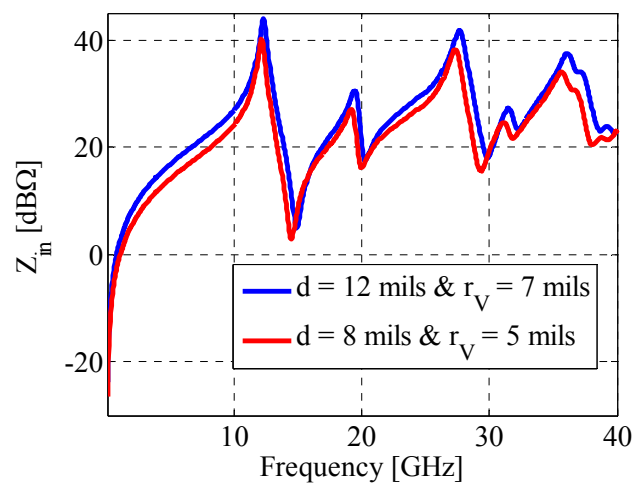ger than the corresponding parameter in the through via case. Also, the first large dip is observed at different frequencies, when comparing the S_{21} of Fig. 2.11 with the S_{21} of Fig. 2.15. The first minimum in Fig. 2.11 corresponds exactly to the first resonant frequency of the ground cage, as seen in Fig. 2.2 for the PEC case. In fact, the equivalent circuit model of the through via configuration consists of two transmission lines in series with several parallel-plate impedances. As soon as the value of the parallel-plate impedance reaches a maximum value, the transmitted signal sees a maximum value of impedance, hence a minimum in the S_{21} or a maximum in the S_{11} parameter is observed. On the other hand, the first
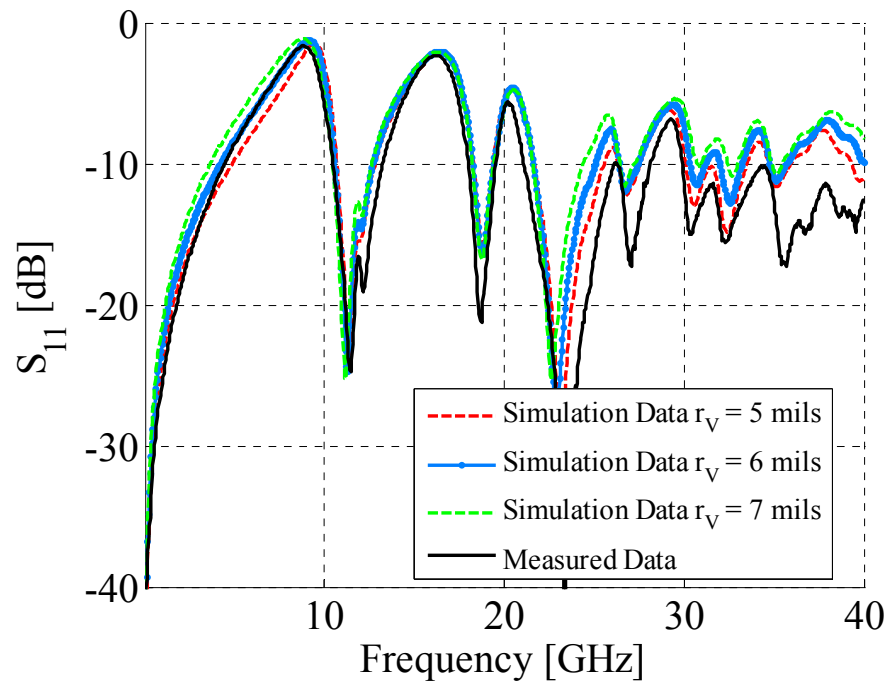
Fig. 2.14. Reflection parameter comparison between measured data and simulation results for the stub via geometry shown in Fig. 2.13.
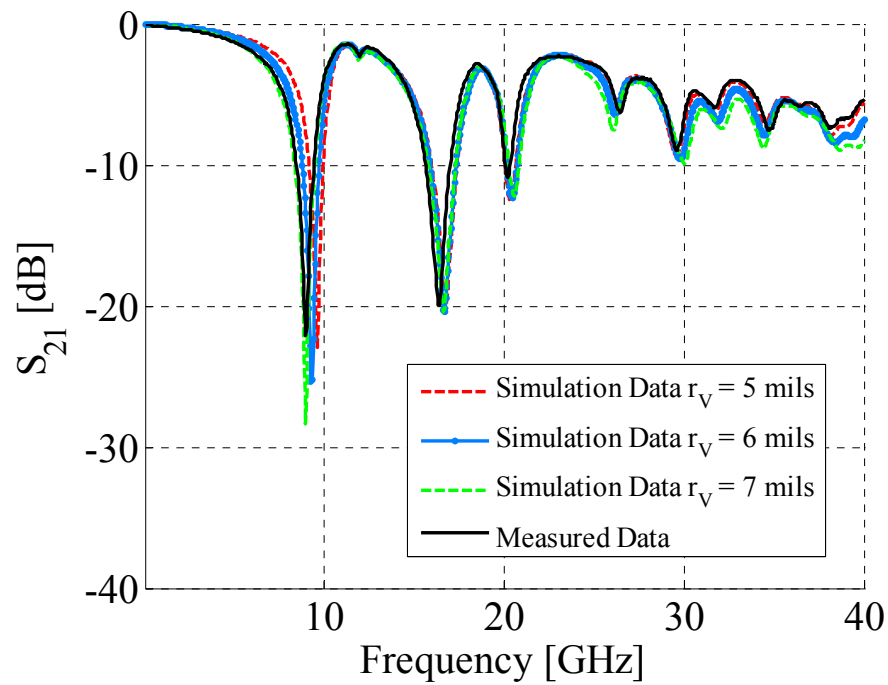
Fig. 2.15. Transmission parameter comparison between measured data and simulation results for the stub via geometry shown in Fig. 2.13.

minimum in the stub via configuration occurs earlier in frequency and it is due to the resonance between the equivalent inductive behavior of the parallel-plate impedance and the via-to-antipad capacitance. This inductive behavior doesn't consist of the asymptotic low frequency inductance only, but the first resonant mode must be accounted as well. Differently from the previous through via case, both the simulated S_{11} and the S_{21}, show larger differences as a function of the via radius. Hence, parameterized prediction simulations are more important for this configuration than for the previous one.

2.4.   CONSIDERATIONS ON THE CIRCUIT MODELS

Some of the issues and limitations associated with the circuit topology and circuit elements utilized in the modeling procedure need to be addressed now. Enforcing the same potential at every node of the signal path is one of the assumptions found in both the circuit models realized. Since no circuit elements are placed along this path, an instant propagation of voltages and currents are assumed from the output terminal of the first transmission line and the input terminal of the second transmission line. Another important assumption consist is neglecting the stripline-to-via transition, which is currently modeled by disregarding the parallel-plate impedances where the striplines are laid out. Neglecting these plane pair forces to neglect any noise coupled on them coming from the striplines or vice-versa, i.e., to disregard any noise excited between the planes and coupled onto the striplines. Such assumption cannot be justified, since the coupling between the signal path and the planes is clearly observed when looking at all the other plane pair. Another modeling deficiency consists in neglecting the hanging stubs found on the top-most part and the bottom-most part of the via configurations. These are both disregarded since the vias are cut right at the top and the bottom of the board, while in

reality the vias sticks out from both ends and pads are present at both ends, as well. Also, the ports are modeled as ideal ones, although the Recessed Probe Launch Technique [2.16] has some parasitics associated with it. An additional deficiency is associated with the cavity model approach itself [2.18]-[2.22], which is not accurate if the vias are very close one another or the via dimensions are not small compare to the wavelength.

2.5. ZERO AND FIRST ORDER MODEL APPROXIMATION FOR THE PARALLEL-PLATE IMPEDANCE

The model-to-hardware correlation reported for both the through via case and the stub via case is shown up to 40 GHz. In many applications, there is no need to span this wide frequency range. Moreover, it is possible to express the parallel-plate plane impedance in terms of its constituting circuit models [2.18]-[2.22] and discard those R-L-C resonant circuits that correspond to the modes falling outside the frequency range of interest. The circuit models given in Fig. 2.16 shows the topology comparison between the complete model, the original model with the parallel-plate impedance replaced with just the asymptotic inductance value and the original model with the parallel-plate impedance replaced with the asymptotic inductance value plus the first resonance circuit. A summary of the values employed in the circuit of Fig. 2.16 (b) and (c) are given in Table 2.2 and the impedance comparison is shown in Fig. 2.17. The comparisons of the S-parameter data obtained by simulating the complete circuit, the circuit with the zero order approximation for the parallel-plate impedance and the circuit with the 1st order approximation for the parallel-plate impedance are shown in Fig. 2.18 and Fig. 2.19. By employing just the asymptotic inductance value, there is no difference with respect to the complete formulation up to approximately 5 GHz. Whereas a perfect match is achieved

up to at least 13 GHz when employing the asymptotic value and the first resonance circuit. Since the two approximations of the parallel-plate impedance match with the complete formulation up to 5 GHz and 13 GHz, respectively, the S-parameter data also match up to these frequencies for the two corresponding simplified circuit
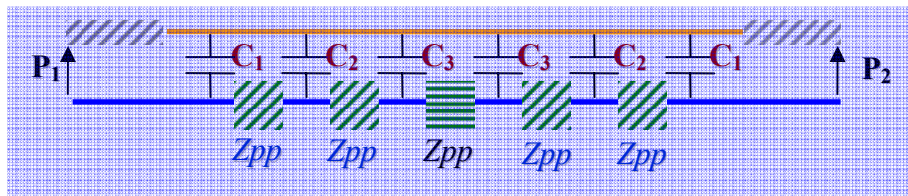
(a) Through via complete model
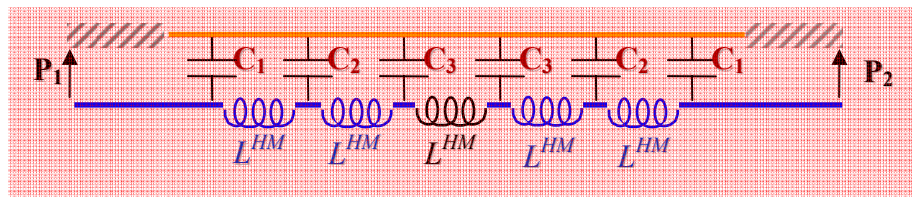
(b) Through via circuit with zeroth order approximation of Zpp
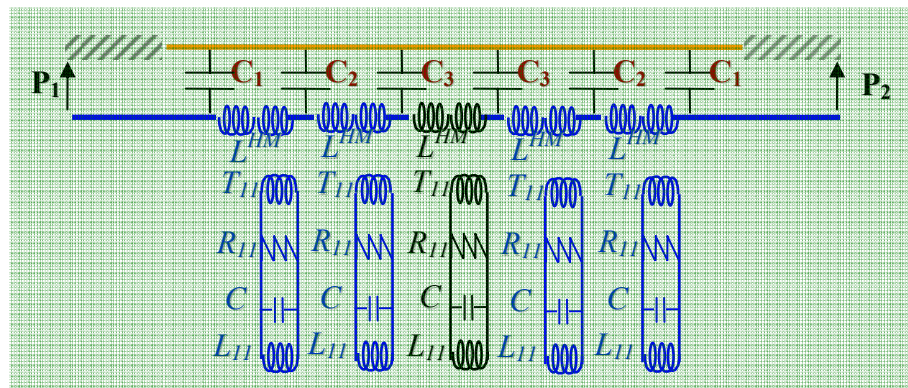
(b) Through via circuit with 1st order approximation of Zpp

Fig. 2.16. Through via configuration: (a) complete model as given in Fig. 2.9. (b) Through via circuit with zero order parallel-plate impedance approximation. (c) Through via circuit with 1st order parallel-plate impedance approximation.

Table 2.2. Summary of values employed in Fig. 2.16 (b) and (c).

zero[th] -	*12 mils*	$L^{HM} = 203pH$	→	
	8 mils	$L^{HM} = 135pH$	→	
1th **order**	*12 mils*	$L^{HM} = 132pH$	→	
		$T_{11} = 1.932$	→	
		$R_{11} = 28\Omega$	→	
		$L_{11} = 19\ pH$	→	
		$C = 12.9pF$	→	
	8 mils	$L^{HM} = 88pH$	→	
		$T_{11} = 1.932$	→	
		$R_{11} = 28\Omega$	→	
		$L_{11} = 43pH$	→	
		$C = 8.6.9pF$	→	

models of Fig. 2.16 (b) and (c). Finally, it needs to be mentioned that the choice of the simplified circuit needs to be carried out on a case-by-case basis. In fact, different dimensions or characteristic geometries or features can require the utilization of different R-L-C circuit models, i.e., the employment of different modes. Another important factor to be considered is the frequency range of interest since, different resonant circuit corresponding to different resonant modes associated with the geometry of interest might be required. The final choice need to be carried out on a case by case basis since the approach require the computation a priori of the circuit elements to be utilized.
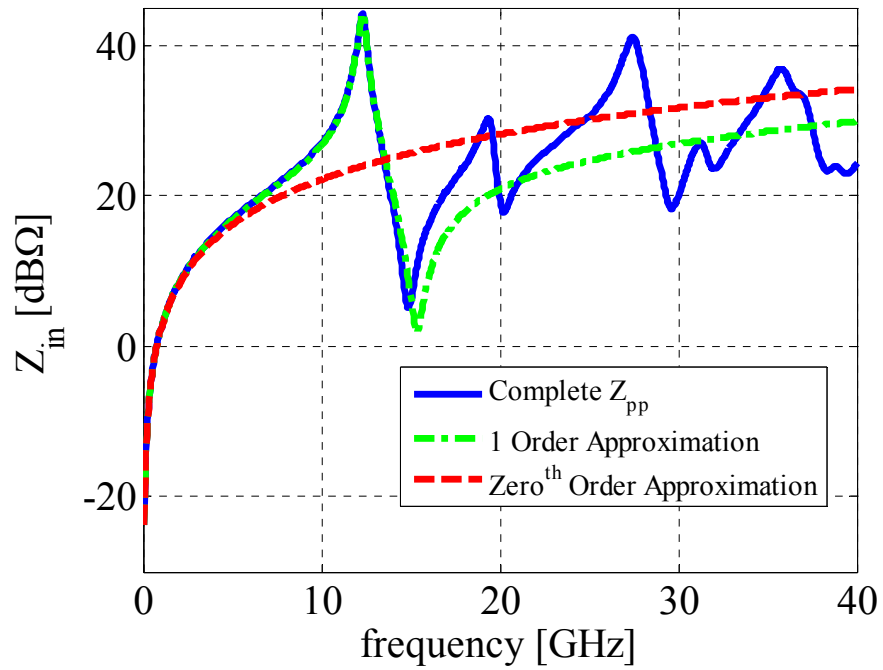
Fig. 2.17. Complete Zpp vs. 1st order approximation vs. zero order approximation
.
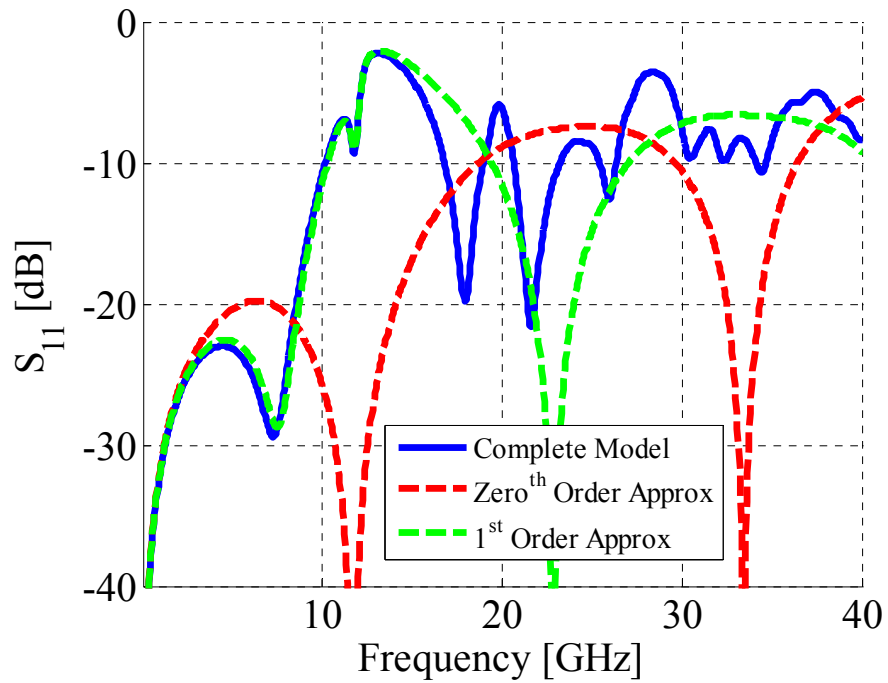
Fig. 2.18. S$_{11}$ parameter comparison for the through via.
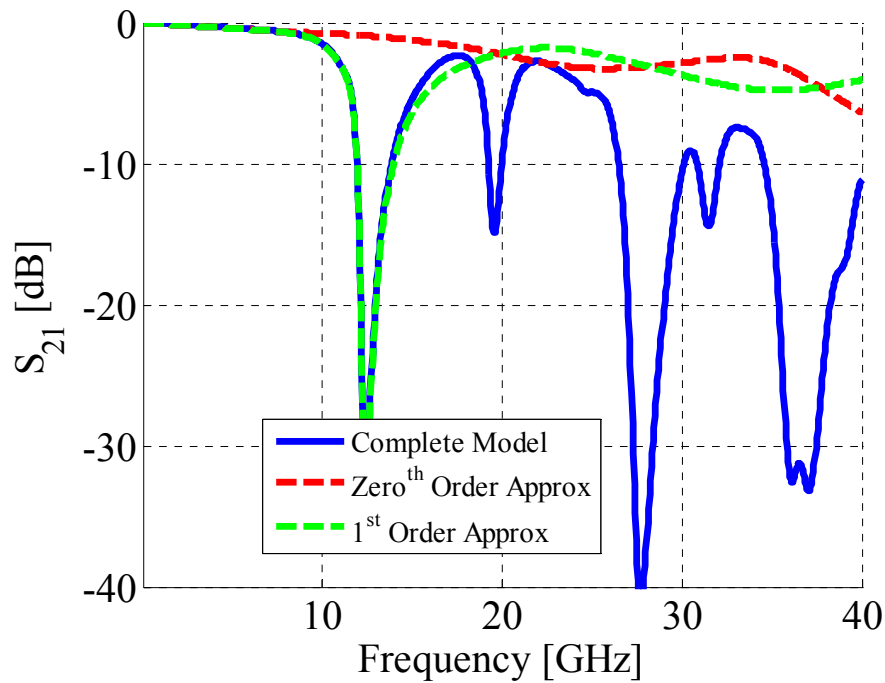
Fig. 2.19. S_{21} parameter comparison for the through via.

2.6. CONCLUSIONS

Physics based models have been presented in this article. The topology of these models, which has been discussed in the literature, are built from physical considerations on the field propagation and by employing circuit elements to represent it. Although the model-to-hardware correlation shows good agreement between the simulation results and measured data, several assumptions are made in the model building process and several important elements, which can be devised already, are neglected. Despite the inadequacies of the models, though, a first order modeling can be already carried out by employing few circuit elements and rearranging them according to the geometry to be considered, i.e., through via or stub via for instance. The major features of these models are the via-to-antipad capacitance, extracted by a fitting a curve on a wide set of data

values from 2D and 3D static simulations, and the parallel-plate impedance, which is calculated by using analytical closed-form expressions. The possibility to extract an equivalent circuit model for the parallel-plate impedance also highlights the possibility to further simplify the models, when a narrow frequency range is of interest.

The great advantage of these concise models is the possibility to carry out what-if scenarios by changing the geometrical parameters that have a one-to-one correspondence with the constituting circuit elements. However, further work is though required at least along three different directions: expand the modeling approach to two or more vias, improve the models by introducing the elements, hence the physics, neglected, take into account a more realistic parallel-plate environment rather than a ground via cage.

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3.   PHYSICS-BASED VIA MODELS WITH THE PARALLEL-PLATE IMPEDANCE INCLUDED: COUPLED VIAS, FULL-GROUND VIAS AND HALF-GROUND VIAS

ABSTRACT

Concise physics-based models for via pair are presented in this article. Three different types of vias are contemplated ,i.e., signal vias, vias not connected to any solid metal planes, full-ground vias, vias connected to all the solid metal planes, and half-ground vias, vias connected to every other solid metal planes. As already shown in [3.1], these models can be built by employing few circuit elements, i.e., transmission lines, capacitances, and, in this case, a two-by-two matrix of self and transfer parallel-plate impedances, calculated by known formulas found in the literature. The advantage of the modeling approach presented here and in consists in rearranging these circuit elements or changing the connections among them to represent several types of single-ended or via pair configurations. Closed-form expressions, both analytical and derived from curve fitting, are utilized to obtain these circuit elements from the dimensions specified in the board designs and material information extracted from measurements [3.1]. The models are finally validated by means of measured data on ad-hoc test sites realized on a 16-layer circuit board. The simulations of the models are carried out within a SPICE-like based tool.

3.1.   INTRODUCTION

The investigation of vias in multi-layer configurations, both PCB geometries and packages, have been widely studied and reported in the literature [3.1]-[3.16]. It is common to see many signal links jumping between layers and across plane pair in

multilayer PCB designs and vias are always utilized for this purpose. Noise is then coupled among these vias also depending upon the many parameters characterizing the parallel-plate structures. Modeling this coupling and predicting the amount of energy transferred from one signal link path to another is crucial for ensuring a correct design. The ultimate goal is to relate geometrical features to noise coupling and others quantities and, moreover, to carry out predictive simulations for achieving the optimal design of via configurations. Beside the many modeling approaches reported in the literature [3.1]-[3.16], frequency domain or time domain wave simulators, both commercial and in-house, have been shown to be capable of modeling a large variety of complex via configurations with the desired accuracy. The big disadvantage associated with these tools is the computational effort due to the different scales of the model features, from the few-mils scale up to the many-inches scale. On the other hand, it is preferable to have SPICE or SPICE-like models for such via configurations, which are more suitable for what-if scenario investigations and, also, can be easily combined with driver and receiver models. Black-box circuit modeling approaches offer a valid alternative, although these models suffer from the lack of one-to-one relationship between circuit elements and geometry features. Within these approaches, circuit models can be extracted either from measured data or simulated data, however the extraction approach needs to be repeated as anyone among the geometry parameters is changed.

The models presented in this article and in [3.1] belong to the category of physics-based models. The extension from single-ended configurations to paired configurations is straightforward and described in details in the following paragraphs. Different types of vias are considered, i.e., half-ground vias, i.e., connected to every other solid plane, full-

ground vias, i.e., connected to every metal layer or just signal vias, i.e., isolated from any solid plane. The transmission line models and via-to-antipad capacitances presented in [3.1] are also utilized in this article, while the major difference with [3.1] is the employment of a matrix of two-port parallel-plate impedances obtained with the Cavity Model approach [3.17]-[3.21]. One of the basic assumption consists in modeling the coupling between the vias just with the transfer parallel-plate impedance, while all the other possible coupling paths are neglected. Measurements are finally utilized to validate all the models. Several test sites are laid out for this purpose on a 16-layer printed circuit board. Each test site is enclosed into a cage of ground vias in order to achieve the desired field containment as in [3.1]. The Recessed Probe Launch Technique [3.22] and a VNA are employed in the measurement set-up. The extension of the modeling approach for single-ended via to via pair is described in details in the second paragraph. Then, complete via pair models are built and compared with measured data in the third paragraph. A zero and a 1st order model approximation of the two-by-two matrix of parallel plate impedances is utilized to build the via pair models and the simulation results are compared with the complete models in the fourth paragraph. Finally, several considerations on the models are carried out in the fifth paragraph and some conclusions are drawn in the last and sixth paragraph

3.2.   EXTENDING THE PARALLEL-PLATE IMPEDANCE CONCEPT TO TWO VIAS

The one-to-one correspondence between geometrical features and circuit elements employed in the case of single- ended via geometries, [3.1], is extended here to configurations consisting of via pair, Fig. 3.1(a), (b) and (c).
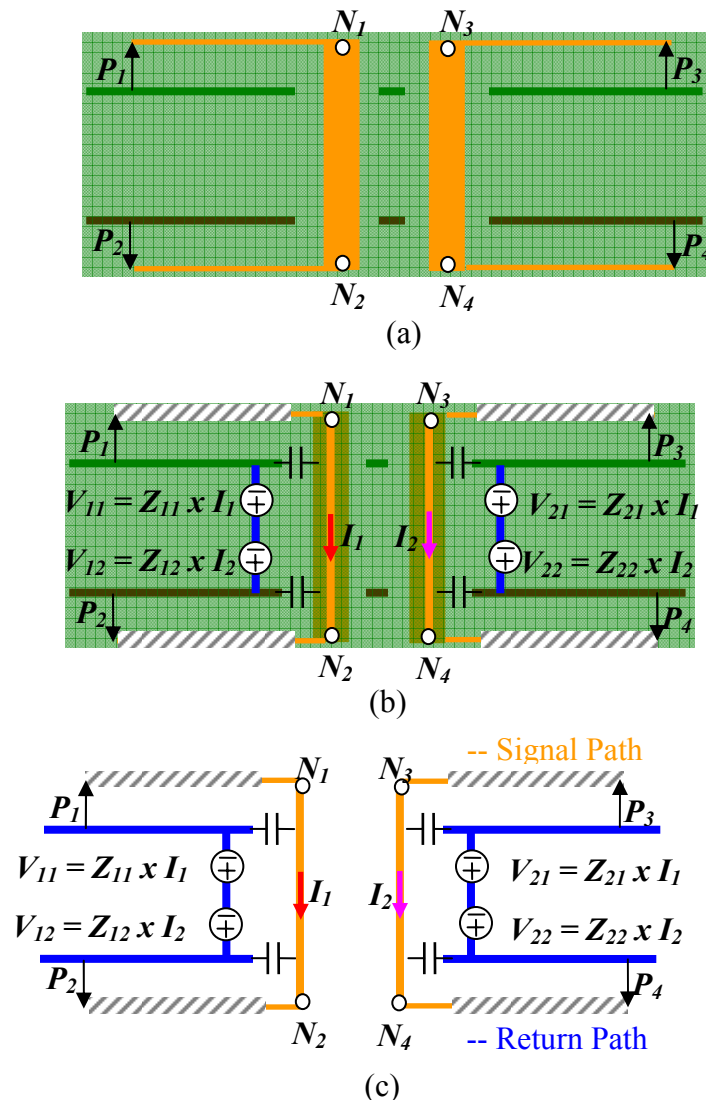
Fig. 3.1. (a) Geometry under investigation. (b) Geometry and corresponding circuit model. (c) Circuit model only.

Extending the same modeling approach proposed in [3.1]-[3.6] and [3.12] to the structure shown in Fig. 3.1, the equivalent circuit models in Fig. 3.1 (b) and (c) is obtained. Two coupled vias are accessed from four uncoupled μ-strip lines laid out on the top and bottom of a four-layer board. Considering striplines would not change the

topology, although some important considerations would have to be discussed regarding the stripline-to-via transitions. The μ-strip lines are represented by employing transmission line models, while the two vias are modeled by employing self and transfer parallel plate impedances. Each via is characterized by a via-to-antipad capacitance, similar to the one introduced for the single-ended cases in [3.1], while the modeling of the return path is carried out by inserting current-controlled voltage sources in the return branch of each via path. The sources are realized by using self and transfer parallel-plate impedances. The voltage drops V_{11} and V_{22} account for the effects of the return paths from the prospective of each via. The voltage drop V_{12} accounts for the amount of voltage coupled into the via on the left, when a current I_2 is observed in the via on the right. The reciprocal behavior is also described with the insertion of the voltage drop V_{21} in the return branch of the via on the right due to the current I_1. Nothing particular characterizes this via pair model, hence, the proposed approach could be extended to cases with more than two vias, [3.1]-[3.6] and [3.12]. Limitations and approximations associated with these models are discussed later in paragraph V.

The parallel-plate impedances constitutes one of the two main elements employed in the modeling approach presented in this article. When dealing with pair of vias, though, both the self and the transfer parallel-plate impedances are important. Both, in fact, contribute to characterize the signal return path, while the transfer impedance accounts for coupling.

The self and transfer parallel-plate impedances are shown in Fig. 3.2 for the geometry given in Fig. 3.2 (a), just for Perfect Electric Conductor boundary condition. The choice of this geometry resides in the availability of real test sites laid out on a

multi-layer printed circuit board and further details are given in the next paragraph.. The

separation of the copper plate is approximately 12 mils and the dielectric material

characteristics are extracted from measured data and coincide with those utilized later in

the actual via modeling. Both frequency dependent permittivity and tangent delta are

employed in the impedance closed-form expressions.

(a)

(b)
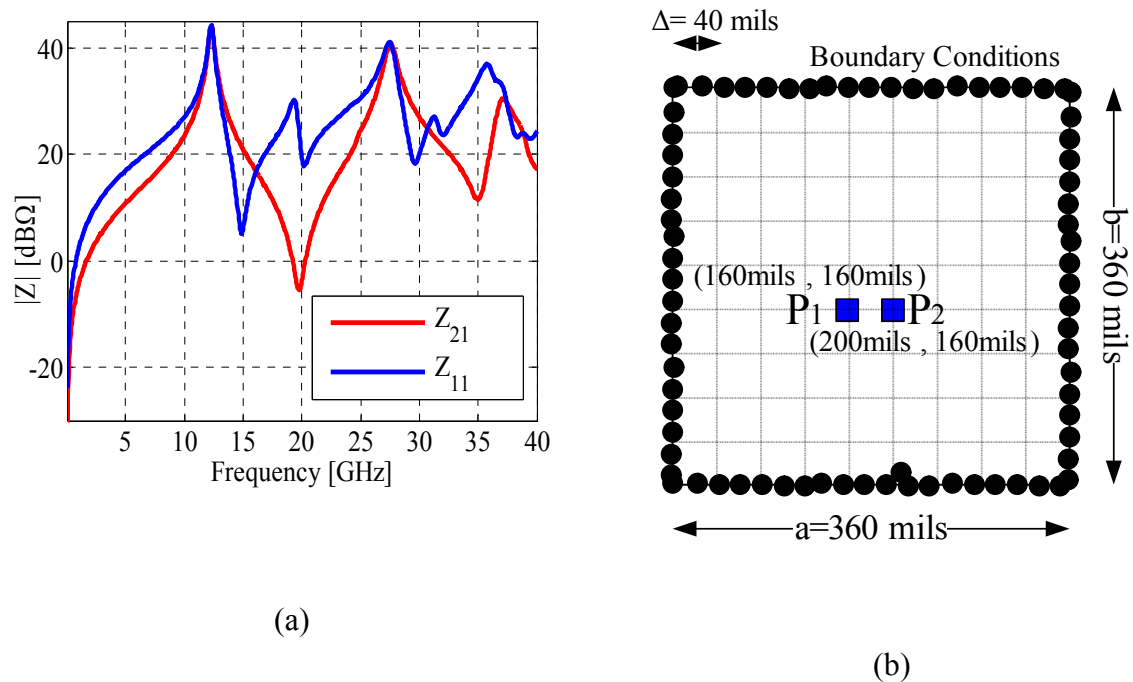
Fig. 3.2. (a) Example of the self and transfer parallel-plate impedance associated with the
geometry in (b). (b) Parallel-plate geometry modeled.

The circuit models described and correlated with measured data in [3.1] consisted

of just a single signal via, i.e., a via isolated from all the solid plane. However, a couple

of other types of vias can be devised, a full-ground via for instance, i.e., a via that is

shorted to all the solid planes as the one shown in Fig. 3.3. This type of via provides an

alternative path for the return current as the signal via couples energy to the plane-pair.

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Two signal vias, i.e., both isolated from the solid planes.

(b) One signal via and one full- ground via, i.e., connected to both solid plane.

One signal via and one half-ground via, i.e., connected to just one solid plane.
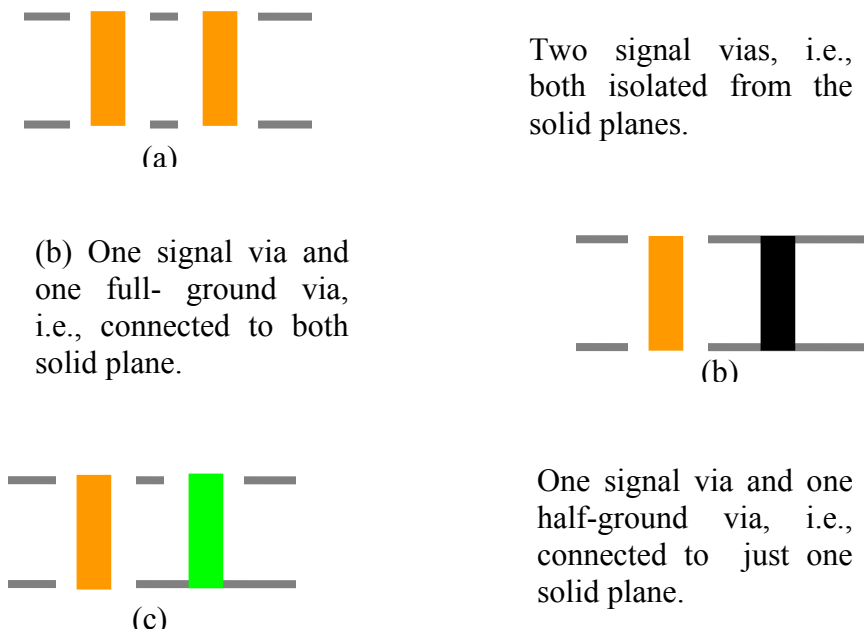
Fig. 3.3. (a) Example of two signal vias. (b) Example of a signal via plus a full-ground via. (c) Example of a signal via plus a half-ground via.

Although very convenient from a signal integrity prospective, employing these full-ground vias is never possible since some of the solid planes are held to a reference-ground voltage, i.e., ground planes, while others are held at different potentials, i.e., power planes. Connecting together just the layers held at a the same reference-ground potential is the next most convenient solution from a signal integrity prospective. The connecting vias are then called half-ground vias, if the ground planes alternate with power planes, as shown in Fig. 3.3(c). The three configurations in Fig. 3.3 (a), (b) and (c) can be represented in terms of the same parallel-plate impedance matrix. The main difference among them resides in the connection of the signal path to the corresponding return path. In presence of antipad, the via-to-antipad capacitance maintains the node on the signal path and the node on corresponding return path at different potentials, Fig. 3.1.

In presence of a short connection, those two nodes are held at the same potentials. It is interesting to compare the configuration in Fig. 3.3 (a) and Fig. 3.3 (b) for the geometry described in Fig. 3.2 (b), i.e., the self-impedance seen looking into the via at Port 1, when the other via is isolated from the planes or shorted to both planes. This comparison is shown in Fig. 3.4 and the presence of the ground via at P_2 of Fig. 3.1 (b) reduces the values of the impedance at low frequencies and shifts toward higher frequencies the modes characterized by even symmetry along both the x and y directions. Although very convenient from a signal integrity prospective, employing these full-ground vias is rarely possible, since the various planes are usually held at different potentials.
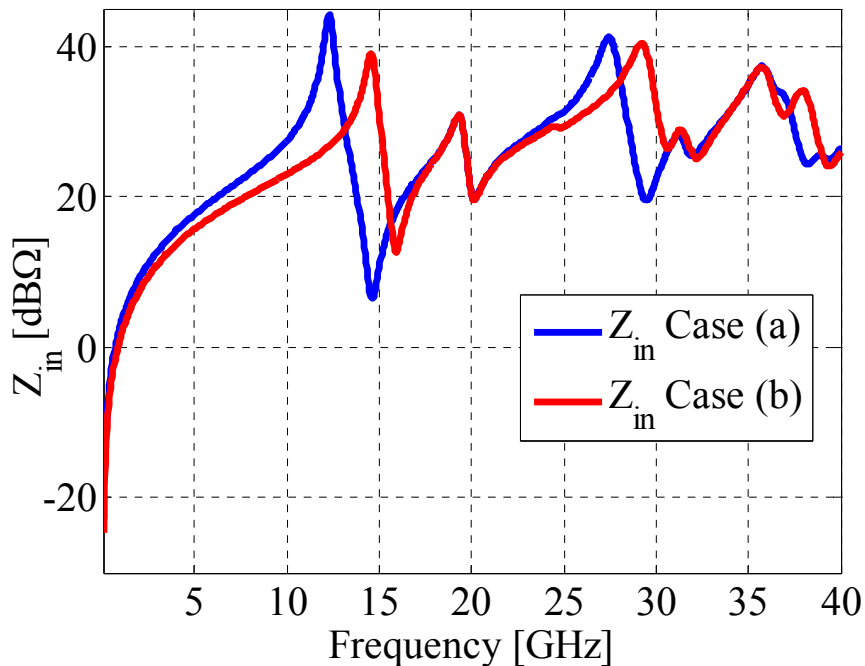
Fig. 3.4. Self-impedance comparison looking into the signal via corresponding to Port 1 of Fig. 3.2 (b) when the via at Port 2 is open, Z_{in} Case (a), and when the signal via is shorted to the planes, Z_{in} Case (b).

The impedance curve Z_{in} Case (a) corresponds to the Z_{11} in the parallel-plate impedance matrix of two vias, i.e.,:

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} Z_{in} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} \qquad (3.1)$$

On the other hand, the curve Z_{in} Case (b) is obtained by employing the same parallel-plate impedance matrix and enforcing the voltage on the ground via to be zero, i.e., $V_2 = 0$,

$$\begin{pmatrix} V_1 \\ 0 \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} \qquad (3.2)$$

Hence, the current on the ground via can be expressed in terms of the current flowing on the signal via,

$$I_2 = -\frac{Z_{21}}{Z_{22}} I_1 \qquad (3.3)$$

and a new expression of the parallel-plate impedance is obtained,

$$V_1 = \left(Z_{11} - \frac{Z_{21} Z_{12}}{Z_{22}} \right) I_1 = \left(Z_{inN} \right) I_1 \qquad (3.4)$$

3.3. BUILDING THE MODELS AND COMPARISON WITH MEASURED DATA

A coupled through via configuration is considered first, according to the stack-up given in Fig. 3.5, Fig. 3.6 (a) and (b). The geometry consists of a pair of uncoupled striplines laid out between the top-most planes and connected, by means of two through hole vias, to two uncoupled striplines laid out between the bottom-most planes. Following [3.1] and Fig. 3.1 (a), the elements required to build the equivalent circuit model are lossy single-ended transmission lines, via-to-antipad capacitances and a two-

by-two matrix of parallel-plate impedances. The procedure described in Fig. 3.1 is reiterated as many times as the number of plane pair requires it and the modeling is carried out by using a SPICE-like type of tool, ADS. Finally, the simulation results are compared with measured data. The measured data are obtained by utilizing a four port vector network analyzer.

(a)

(b)
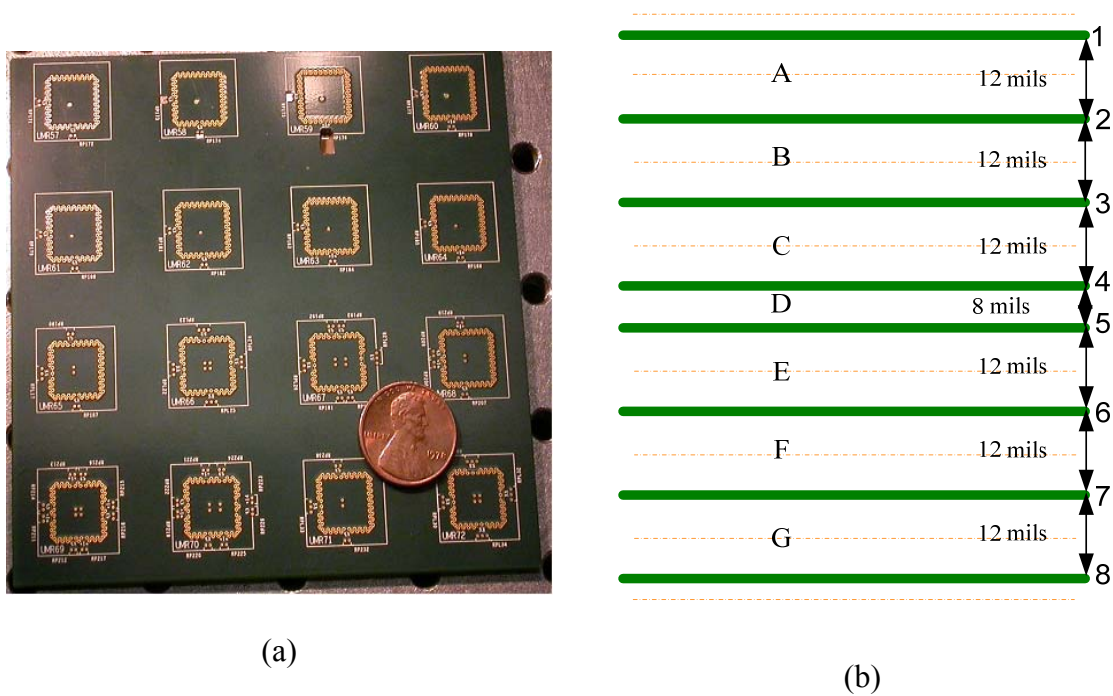
Fig. 3.5. (a) Sample of test sites realized on a 16-layer board. (b) Board stack-up.

Coupled through via geometries, alongside with many more others, are laid out and realized on a 16-layer PCB and measured by employing the Recessed Probe Launch Technique [3.22]. A sample set of the test sites realized and employed for model validation is shown in Fig. 2.7 (a) and (b). The solid planes are arranged to create 7 resonant cavities of 8 mils height and 12 mils height, for the center cavity and for all the

remaining cavities, respectively. The nominal via-center to via-center transverse dimensions of the ground via cage are 360 mils by 360 mils, while the via and antipad radii are 5 mils nominal and 15 mils nominal, respectively. An FR-4 type of material is employed as substrate and several test sites are realized to extract material properties based on the work published in [3.23]. A mean permittivity value and a mean tangent delta value are also obtained by averaging over the frequency range the frequency-dependent parameters extracted. The frequency dependent values are used in the parallel-plate impedance calculations, whereas the averaged values are employed to calculate the via-to-antipad capacitances and in the lossy transmission line models. Additional destructive verifications allowed to discover a discrepancy between the real value and the nominal value of the via radius, which was found to be larger than 5 mils, i.e., approximately 7 mils. The deviations of the via geometry dimensions from nominal values are due to fabrication tolerances. The PCB layout excerpt and the stack-up geometry of the coupled through via configuration are both shown in Fig. 3.6 (a) and (b). The cavities A and G are not labeled because they are neglected in the equivalent circuit model. More over, the positions of both vias with respect to the ground cage corresponds to those described in Fig. 3.2 (b). The final ADS models are built by employing four 250 mils lossy transmission line models, which correspond approximately to the length between each launching port located outside the ground cage and the signal vias. Two transmission lines correspond to the two uncoupled striplines laid out between the top-most pair of planes, while the other two correspond to those laid out between the bottom-most pair of planes. Twelve capacitances of three different values are employed, C_1, C_2 and C_3, respectively. These values are obtained by utilizing the fitted closed form

expressions and the stacking procedure described in [3.1]. The first capacitance, C_1, is used to model the transition between the top-most cavity and the cavity B and the transition between the cavity F and the bottom-most cavity. The second capacitance, C_2, represents the transition between the cavities B and C and the cavities E and F. Finally, the third capacitance, C_3, is employed to model the transition between both the cavities C and D and the cavities D and E. The capacitance C_1 is equal to the capacitance C_2 plus half of C_2, which corresponds to the half via above the top-most stripline and the top solid plane or, likewise, the half via below the bottom-most stripline and the bottom solid plane. The simulations are carried out and compared for three via radii, 5 mils, i.e., the nominal value, 6 mils and 7 mils. Three sets of capacitances are then obtained as a function of these geometrical features.
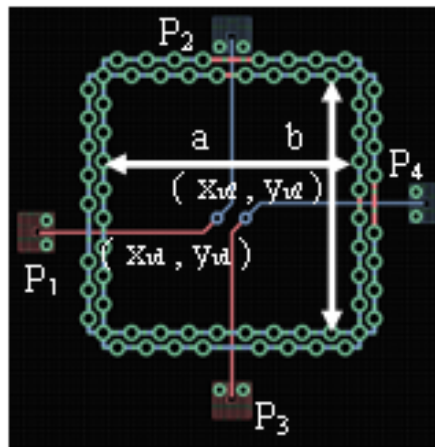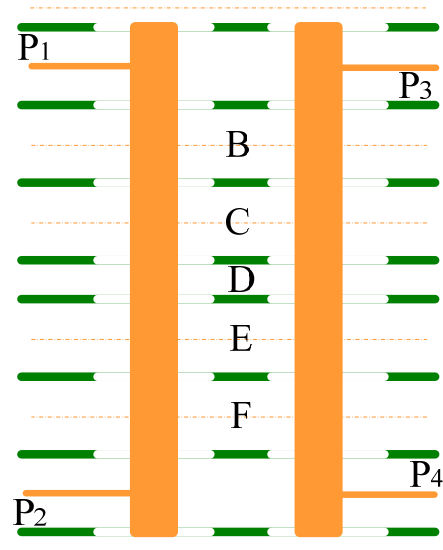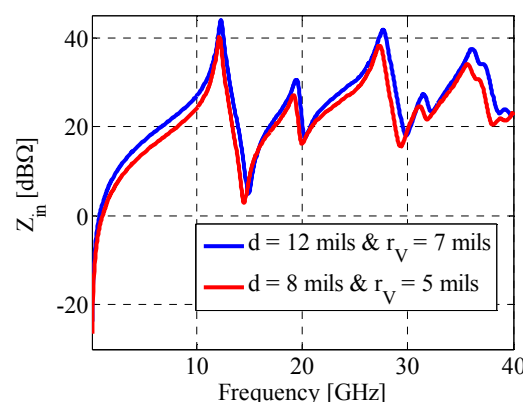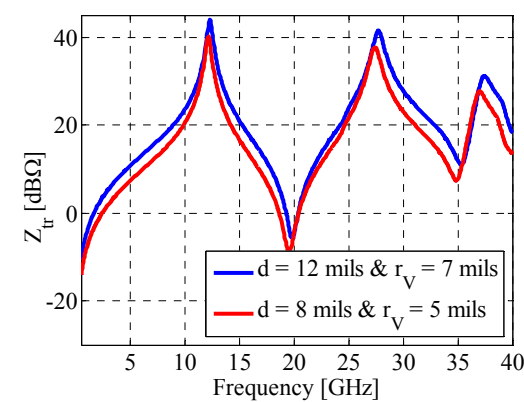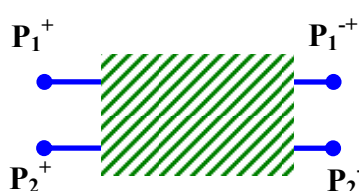
(a)   (b)

Fig. 3.6. (a) PCB layout excerpt of the coupled through via configuration. The coordinate sets (x_{v1}, y_{v1}) and (x_{v2}, y_{v2}) correspond to those shown in Fig. 3.2 (b). (b) Stack-up of the coupled through via geometry.

Both cavities have lateral dimensions equal to the via-center to via-center nominal value of 360 mils by 360 mils minus the via diameter and the coordinates of the two vias correspond to P_1 and P_2 in Fig. 3.2 (b). The parallel-plate impedances are computed by employing the frequency-dependent material parameters extracted from measured data and the two-by-two matrix of impedances is finally converted into a two-by-two matrix of S-parameter . data in touchstone format and imported into ADS All these elements, summarized in Table 3.1, are connected as shown in Fig. 3.7, a frequency domain simulation is run from 50 MHz up to 40 GHz and finally compared to measurements. The frequency dependent values are used in the parallel- plate impedance calculations, whereas the averaged values are employed to calculate the via-to-antipad capacitances and in the lossy transmission line models. Additional destructive verifications allowed to discover a discrepancy between the real value and the nominal value of the via radius, which was found to be larger than 5 mils, i.e., approximately 7 mils. The deviations of the via geometry dimensions from nominal values are due to fabrication tolerances. The PCB layout excerpt and the stack-up geometry of the coupled through via configuration are both shown in Fig. 3.6 (a) and (b). The cavities A and G are not labeled because they are neglected in the equivalent circuit model. More over, the positions of both vias with respect to the ground cage corresponds to those described in Fig. 3.2 (b). The final ADS models are built by employing four 250 mils lossy transmission line models, which correspond approximately to the length between each launching port located outside the ground cage and the signal vias. Two transmission lines correspond to the two uncoupled striplines laid out between the top-most pair of planes, while the other two correspond to those laid out between the bottom-most pair of planes.

Table 3.1. Summary of the elements utilized.

$Z_0 = 50\Omega$, Length = 250 mils, $\varepsilon_r = 3.84$, $tg\delta = 0.033$
Lossy TL model

	C_1 [fF]	C_2 [fF]	C_3 [fF]
5 mils	$87 = (1+\frac{1}{2})C_2$	58	50
6 mils	$102 = (1+\frac{1}{2})C_2$	68	59
7 mils	$120 = (1+\frac{1}{2})C_2$	80	69

Via-to-Antipad Capacitance Values Employed

Example of self and transfer parallel-plate impedances to be imported into a 2-Port S-parameter component in touchstone format

2-Port S-parameter data item (2 Ports → 4 Nodes)

The measured data are acquired by hooking up a network analyzer to four
calibrated surface probes and the recessed probe launch technique [3.22] is utilized for
obtaining the S-parameters.
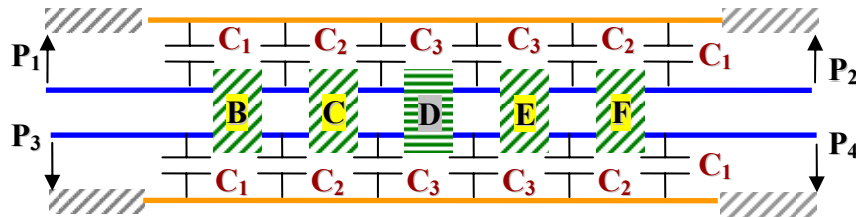
Fig. 3.7. Complete equivalent circuit model of the coupled through vias described in Fig.
3.6 and based on the elements described in Table 3.1.

The model-to-hardware comparisons of S_{11}, S_{21}, Near-end crosstalk and Far-end
crosstalk are shown, respectively, in Fig. 3.8, Fig. 3.9, Fig. 3.10 and Fig. 3.11. Despite
the conciseness of the circuits, the agreement between measured data and the simulation
results suggest that the major physics phenomena are captured. and the model constitutes
a solid starting point for adding, in terms of additional circuit elements, all the physics
neglected. Some differences are observed between the S_{11} simulation results as a function
of different via radii, especially below 10 GHz. As already found in [3.1], the reflection
parameter of through configurations is more sensitive to geometry variations due to the
small values assumed in this low frequency range. Variation of the via radius, hence,
variation of the via-to-antipad capacitance minimally affects the transmission, the Far-
end crosstalk and the Near-end crosstalk, while the S_{11} spans several dB and shows a
different frequency behavior below 10 GHz. Reflection, transmission, near-end and far-
end crosstalk, i.e., the signal coupled for instance from Port 1 to Port 3 and/or Port 4,
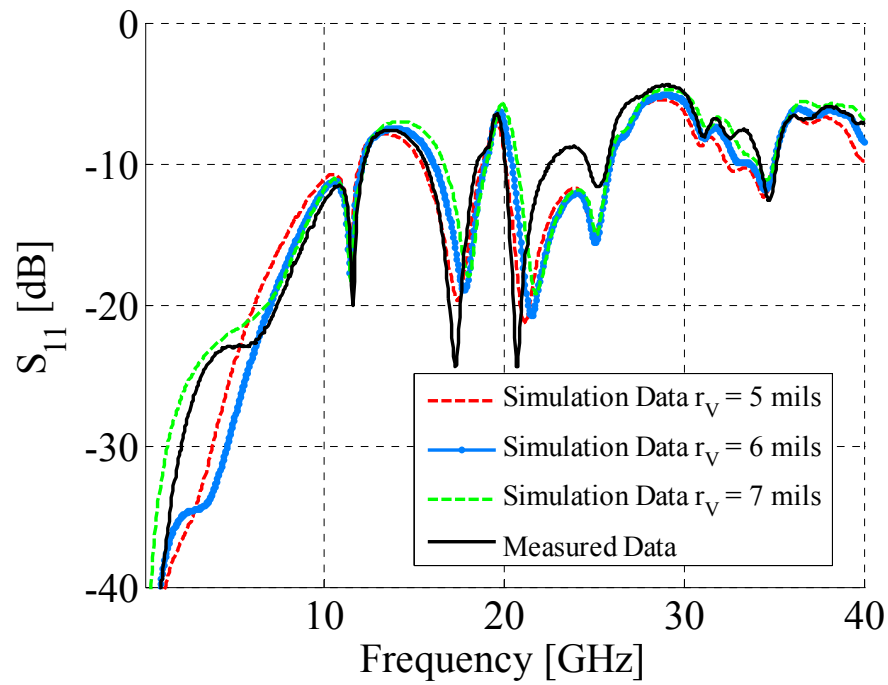
Fig. 3.8. Reflection parameter comparison between measured data and simulation results for the coupled through via geometry shown in Fig. 3.6.
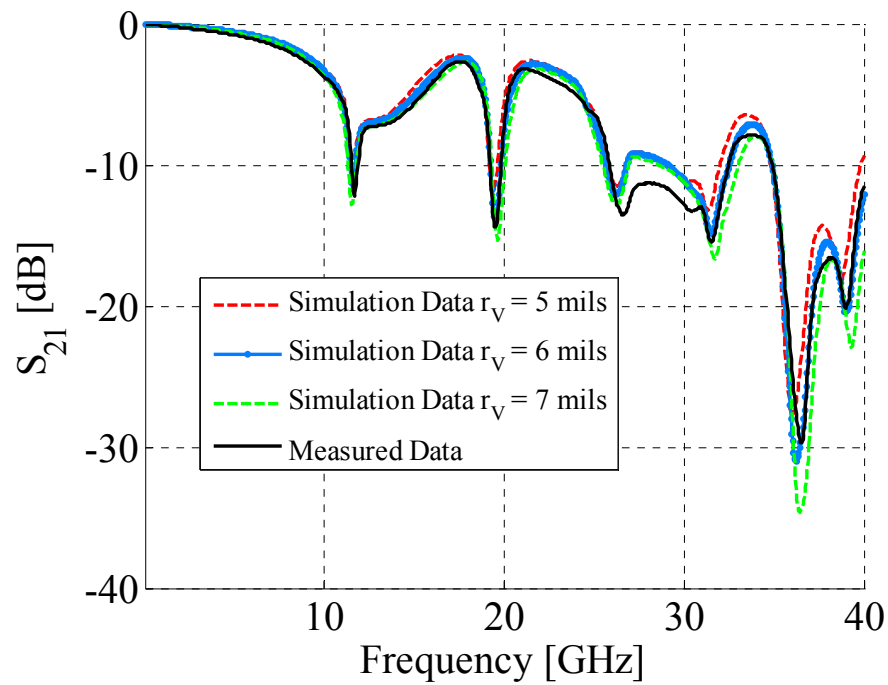
Fig. 3.9. Transmission parameter comparison between measured data and simulation results for the coupled through via geometry shown in Fig. 3.6.
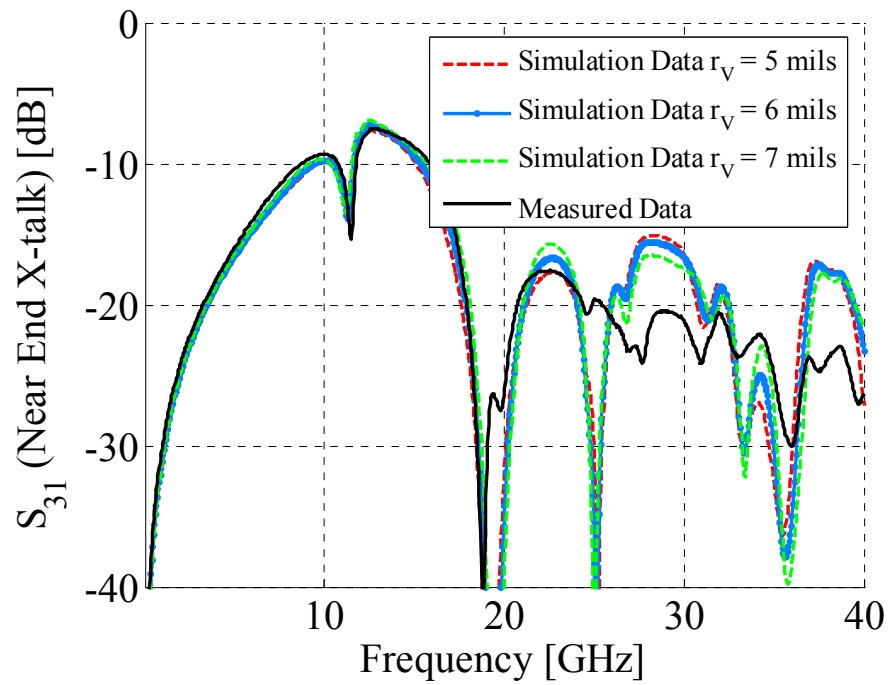
Fig. 3.10. Near-end crosstalk comparison between measured data and simulation results for the coupled through via geometry shown in Fig. 3.6.
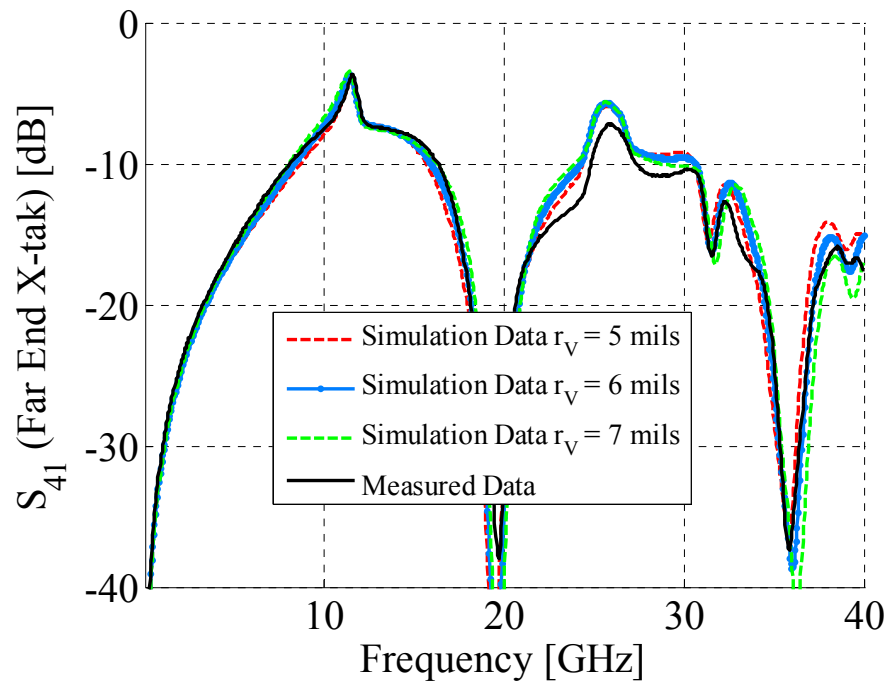
Fig. 3.11. Far-end crosstalk comparison between measured data and simulation results for the coupled through via geometry shown in Fig. 3.6.

comparison are shown in Fig. 3.8, Fig. 3.9, Fig. 3.10 and Fig. 3.11, respectively. When comparing the S_{21} in Fig. 3.9 with the S_{21} of the single-ended through via described in [3.1], many resemblances regarding the two frequency behaviors can be observed. From a topology prospective, both the single-ended and the coupled configuration has the via plus its return path in series with the transmission line models, hence maxima in the parallel-plate impedance corresponds to minima in the transmitted power. The first dip in Fig. 3.9 corresponds to the first cage resonance, Fig. 3.2 (a), but it is not as severe as the one reported in [3.1], since an additional via is present between the planes. This via is terminated into matched loads at both ends, where some of the energy coupled into the various parallel-plate configurations gets absorbed. It is important also to note the correlation between the transfer impedance and both the measured and simulated crosstalk results. Maxima and minima of the Z_{21} parallel-plate impedance, Fig. 3.2 (a), correspond to minimum and maximum values in both the Near-end and Far-end crosstalk in the frequency range up to 20 GHz. This is a direct consequence of the topology employed in Fig. 3.1, where the only coupling path is the transfer impedances located in the return path of each via. Further investigations are finally required to establish the reasons of the discrepancies observed between measured data and simulated data in the Near-end crosstalk comparison of Fig. 3.10 above 20 GHz.

The proposed modeling approach recycles the circuit elements employed above to build an equivalent model for a coupled stub via configuration. A PCB layout excerpt of this geometry and the stack-up associated with it are shown in Fig. 3.12 (a) and (b), respectively. The configuration consists of four uncoupled striplines all laid out between the top most pair of plane. The geometry is obtained within the same board where the

through configuration is also obtained. The major difference reside in the way the stripline are laid out. For instance, in the through configurations, they are laid out in the top most and the bottom most plane pair, while in the stub configuration, they are all laid out between the top most pair. The four section of stripline meet in pair where two vias are left hanging at the locations specified in Fig. 3.2 (b). The top-most cavity is not labeled because is neglected in the modeling procedure and the final circuit model is shown in Fig. 3.13. All the elements employed to build this new model are recycled from the one shown in Fig. 3.7 with the exception of C_4, which corresponds to the capacitance of the bottom half of each via in cavity G and the bottom solid plane. The values employed are 29 fF, 34fF and 40 fF for the 5mils, 6 mils and 7 mils via radius case, respectively. The model-to-hardware correlation for this geometry is shown in Fig. 3.14, Fig. 3.15, Fig. 3.16 and Fig. 3.17, for the reflection, the transmission, the Far-end crosstalk and the Near-end crosstalk, respectively. Despite the many assumptions, the agreement between the measured data and the simulation results suggest that the major physics phenomena are also captured for this configuration. Although larger discrepancies are observed in the model-to-hardware correlation when compared to the previous case, the circuit model in Fig. 3.13 constitutes a solid staring point for adding, in terms of equivalent circuit models, the physics neglected.

Contrarily to the previous through configuration, the differences just between the simulation results as a function of the via radius are more relevant. Prediction simulations, then, must be conducted as a function of geometry parameters since the exact dimensions are known just within factory tolerances and the via configuration performances can be predicted just within some bounds. It is also interesting to note the

(a)

(b)
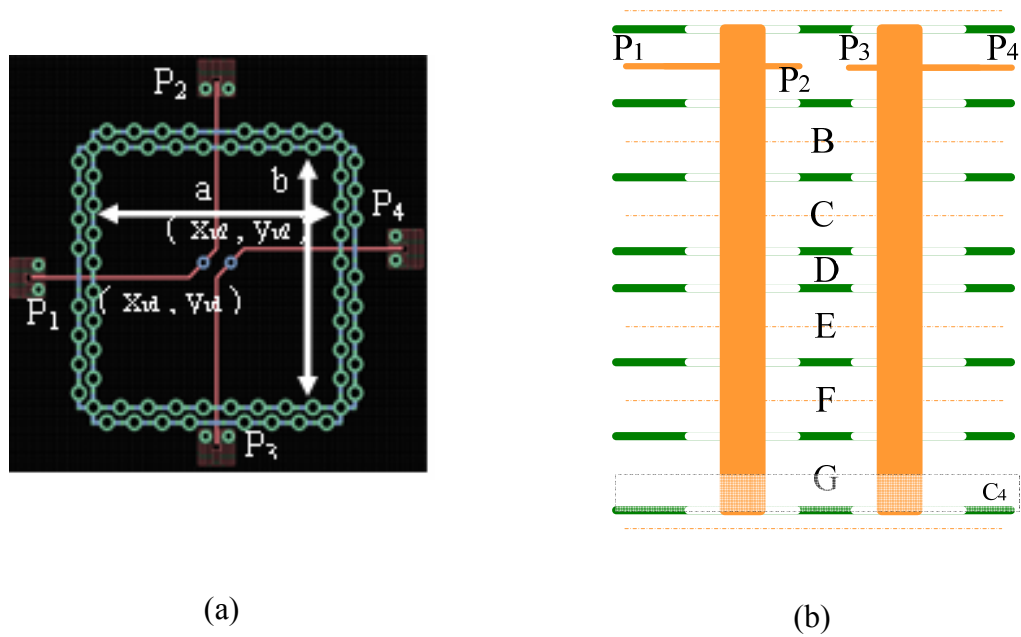
Fig. 3.12. (a) PCB layout excerpt of the coupled stub via configuration. The coordinate sets (x_{v1}, y_{v1}) and (x_{v2}, y_{v2}) correspond to those shown in Fig. 3.2 (b). (b) Stack-up of the coupled stub via geometry.

Fig. 3.13. Complete equivalent circuit model of the coupled stub via configuration based on the circuit elements described in Table 3.1.
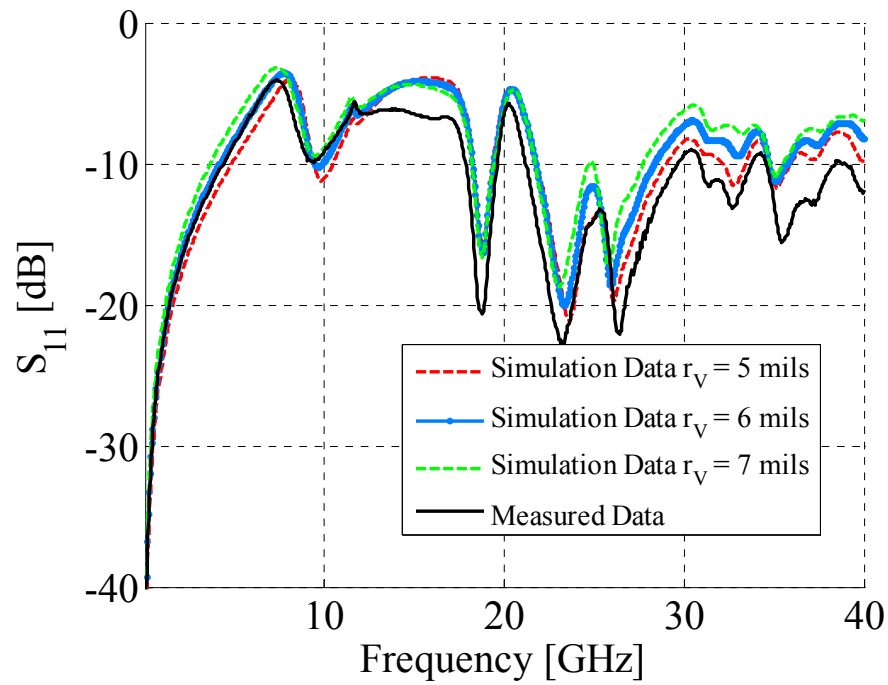
Fig. 3.14. Reflection parameter comparison between measured data and simulation results for the coupled stub via geometry shown in Fig. 3.12.
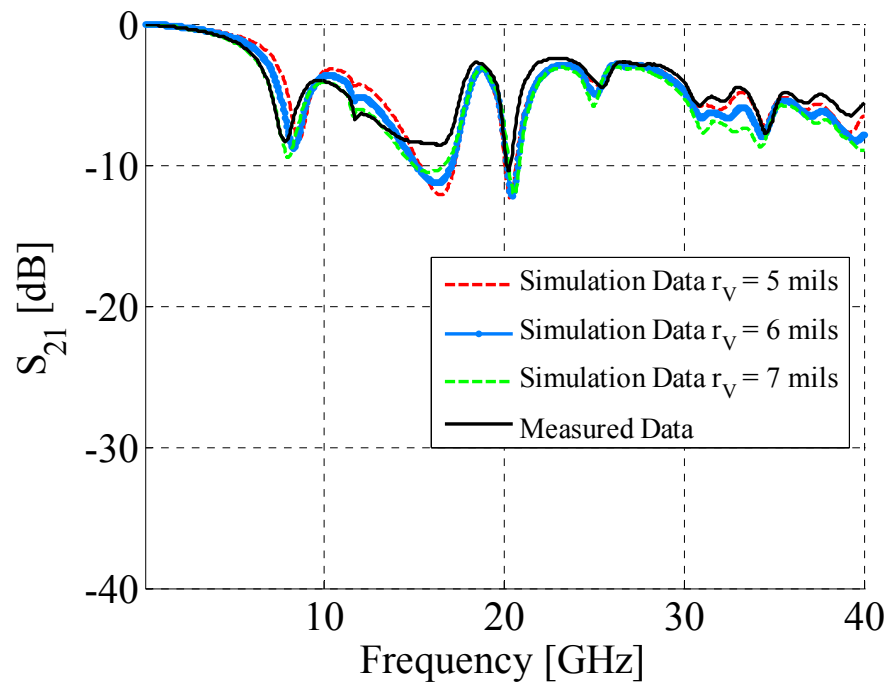
Fig. 3.15. Transmission parameter comparison between measured data and simulation results for the coupled stub via geometry shown in Fig. 3.12.
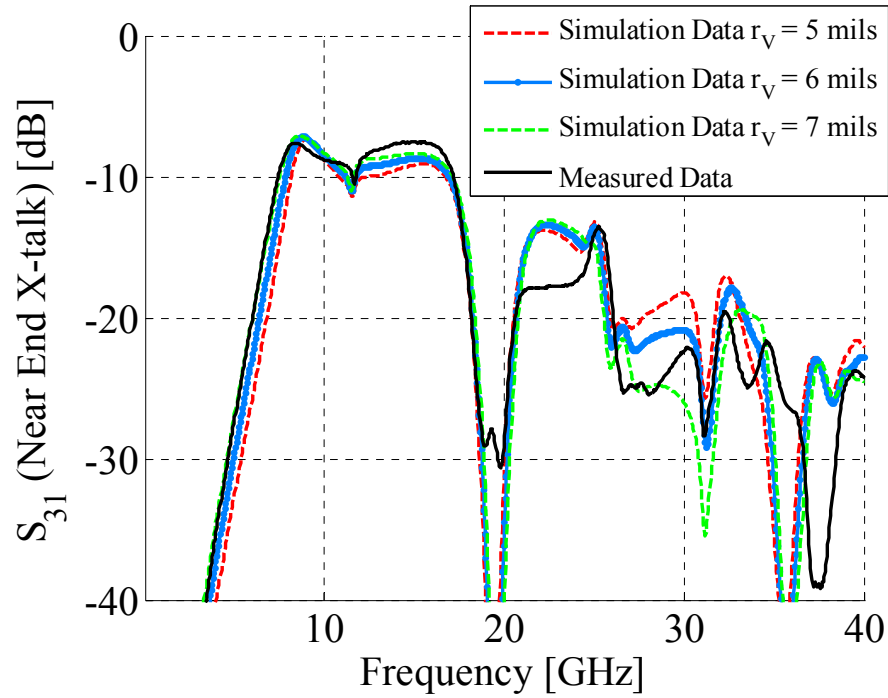
Fig. 3.16. Near-end crosstalk comparison between measured data and simulation results for the coupled stub via geometry shown in Fig. 3.12
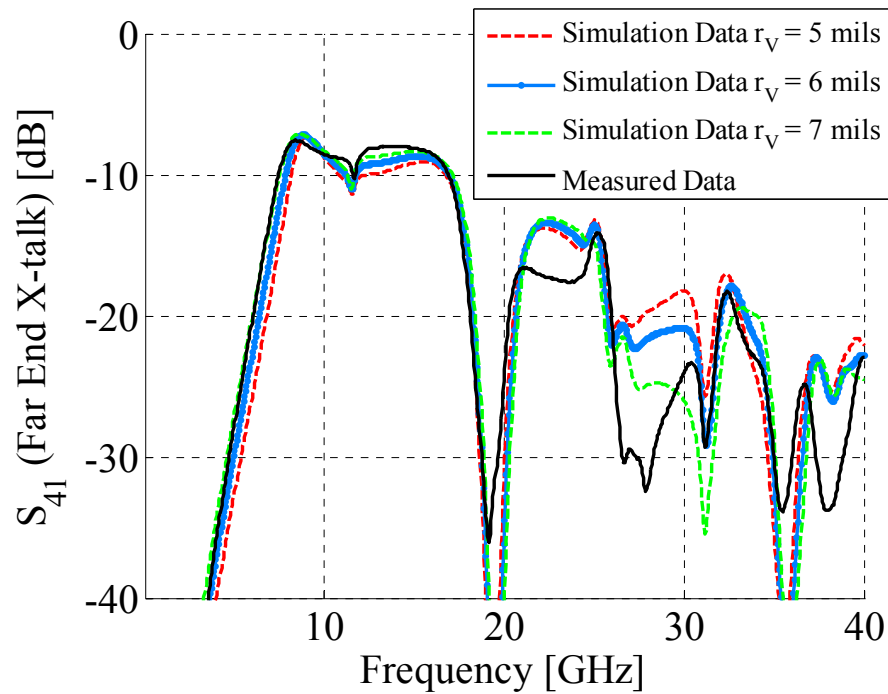
Fig. 3.17. Far-end crosstalk comparison between measured data and simulation results for the coupled stub via geometry shown in Fig. 3.12.

extreme similarities between the Near-End X-talk and the Far-End X-talk. Port 3 and Port 4 look exactly the same from the prospective of Port 1, since the transmission lines are all uncoupled and the only coupling between the two paths occur between the vias inside the planes. Finally, the same considerations of the previous paragraph can be repeated for this configuration as well, i.e., the reduction of some of the dips in the S_{21} of Fig. 3.15 with respect to the single-ended case [3.1] and the correlation of both the Near-end and Far-end crosstalk of Fig. 3.16 and Fig. 3.17 with the transfer impedance in Fig. 3.2 (a).

By changing the connections among the different elements constituting both the stub and the through coupled vias, different via pair geometries can be implemented. For instance, two additional geometries are investigated in this paragraph, a through single via plus a full-ground via and a stub single via plus a full-ground via, described and compared in details from Fig. 3.18 to Fig. 3.25. Both configurations consist of two sections of a stripline laid out between the top-most and the bottom-most pair of planes, in the case of the through via, or just between the top-most pair, in the case of the stub via. These two sections are conjoined together by a through hole via, in the through via case, or connected where a through hole via is left hanging, in the case of the stub via . The other via in both configurations is a through hole via, which is shorted to every solid plane, i.e., full-ground via. The positions of the two vias correspond those described in Fig. 3.2 (b), the geometries are given in Fig. 3.18 and Fig. 3.22, respectively, and the equivalent circuit models are given in Fig. 3.19 and Fig. 3.23, respectively. These models are built by looking at the corresponding coupled through and stub configurations shown in Fig. 3.7 and Fig. 3.13, respectively, and removing the sections of transmission lines from the second via path and shorting out all the capacitances between the signal nodes

and the corresponding return nodes associated with the second via. The model-to-hardware correlation of the through configuration is shown in Fig. 3.20 and Fig. 3.21 for the reflection and the transmission parameter, respectively, and three different via radius sizes. Contrarily to the comparison of the transmission data, the comparison of the reflection data shows large variations between the simulation results especially below 10

(a)

(b)
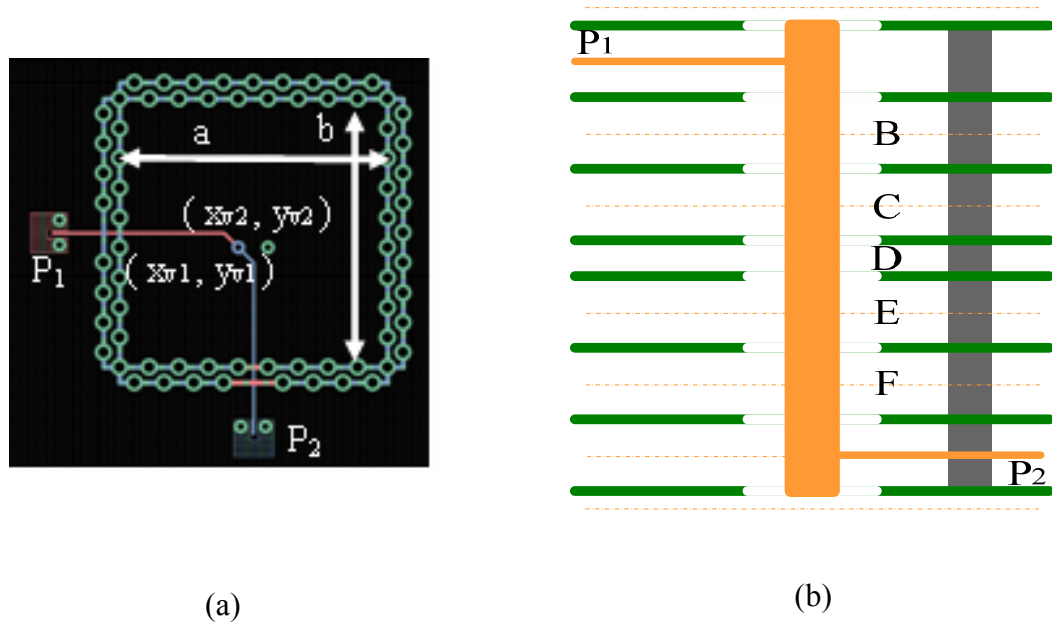
Fig. 3.18. (a) PCB layout excerpt of the through via plus full-ground via configuration. The coordinate sets (x_{v1}, y_{v1}) and (x_{v2}, y_{v2}) correspond to those shown in Fig. 3.2 (b). (b) Stack-up of the through via plus full-ground via geometry.
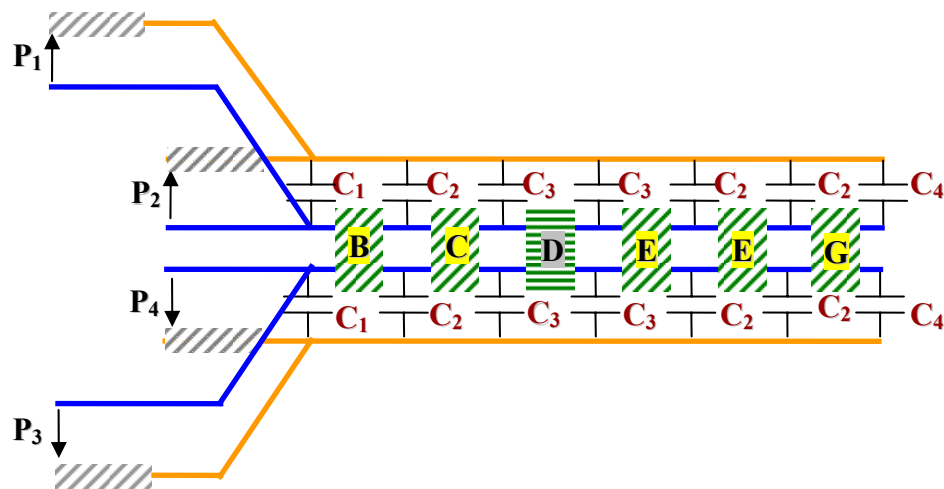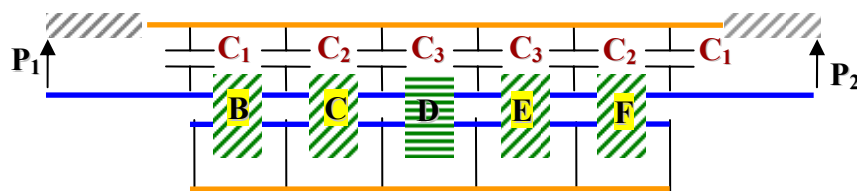

Fig. 3.19. Complete equivalent circuit model of the through via plus full-ground via configuration based on the circuit elements described in Table 3.1.
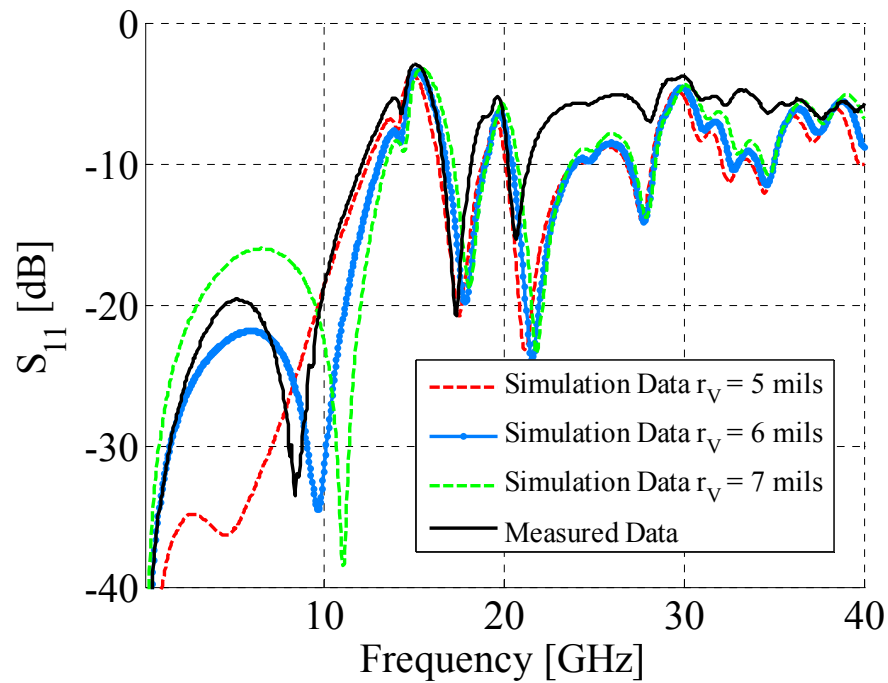
Fig. 3.20. Reflection parameter comparison between measured data and simulation results for the through via plus full-ground via geometry shown in Fig. 3.18.
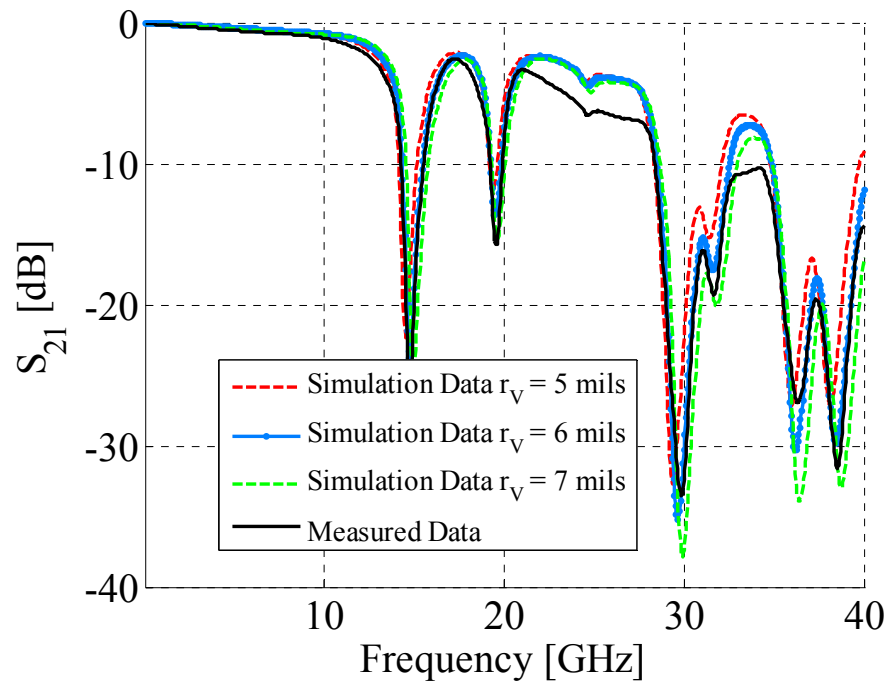
Fig. 3.21. Transmission parameter comparison between measured data and simulation results for the through via plus full-ground via geometry shown in Fig. 3.18.

GHz. Again, the discrepancies are mainly due to the higher sensitivity of the S11 to parameter variations, such as the via radius. It is also interesting to note that the first dip in S_{21} of Fig. 3.21 now occurs at a different frequency when compared to the

(a)   (b)

Fig. 3.22. (a) PCB layout excerpt of the stub via plus full-ground via configuration. The coordinate sets (x_{v1}, y_{v1}) and (x_{v2}, y_{v2}) correspond to those shown in Fig. 3.2 (b). (b) Stack-up of the stub via plus full-ground via geometry.
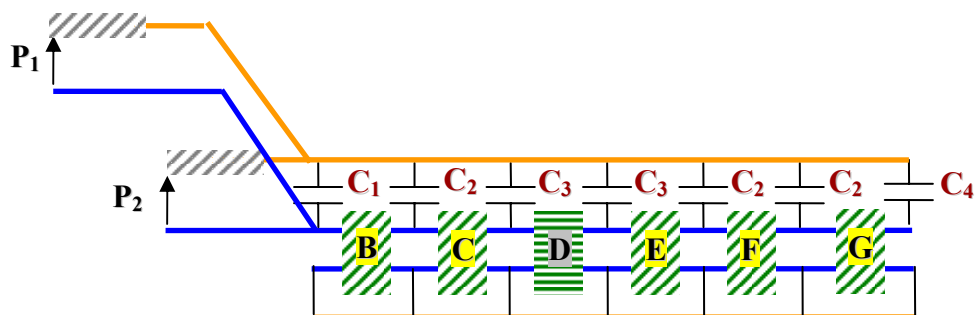
Fig. 3.23. Complete equivalent circuit model of the stub via plus full-ground via configuration based on the circuit elements described in.

corresponding single-ended through via case described in [3.1]. The parallel plate impedance has a different profile when a shorting pin is present and some resonances are shifted toward higher frequencies as shown in Fig. 3.4. Placing a full-ground via between the planes in proximity of the signal via, increases the pass band of the configuration. Locating this shorting post in close proximity of the signal via also reduces the value of the inductance and the decrease in this inductance influences the stub via configuration, since the first resonance in the transmission, Fig. 3.25, is due to the resonance between this elements and the via-to-antipad capacitance, which is the same with respect to the single-ended stub via configuration described in [3.1].

Fig. 3.24. Reflection parameter comparison between measured data and simulation results for the stub via plus full-ground via geometry shown in Fig. 3.22.

Fig. 3.25. Transmission parameter comparison between measured data and simulation results for the stub via plus full-ground via geometry shown in Fig. 3.22.

Hence, placing a full-ground in close proximity of the signal via increases the pass band of the configuration. The stub via plus full-ground via configuration is more sensitive to via radius variations, as also indicated in the single-ended case [3.1] and the coupled case above. A set of two additional geometries are finally considered in this paragraph, i.e., a through signal via plus an half-ground via and a stub signal via plus an half-ground via, described in details and compared from Fig. 3.26 to Fig. 3.33. The two geometries consist of two sections of stripline laid out between the top-most and bottom-most pair of planes, in the case of the through via, or just between the top-most plane pair, in the case of the stub via. These two stripline sections are connected by means of a through hole via, in the case of the through via, or connected together at a point where a through hole is left hanging, in the case of the stub via. The half-ground via is connected

to every other solid layer starting from the top-most one. Both via locations are specified Fig. 3.2 (b), the geometries are given in Fig. 3.26 and Fig. 3.30, respectively, while the equivalent circuit models are given in Fig. 3.27 and Fig. 3.31, respectively. As already shown for the full-ground via configurations, the circuit models with half-ground vias are obtained by looking at the corresponding coupled via cases and shorting the nodes across the capacitances where the second via is connected to the reference plane and by removing the transmission lines connected to the second via path. The incompleteness of these equivalent circuits models is clearly observed when relating the stack-up in Fig. 3.26 (b) and Fig. 3.30 (b) and the circuit models in Fig. 3.27 and Fig. 3.31. Neglecting the top most cavity, i.e., cavity A, forces the realizations of both circuits to have the half-ground vias terminated into the capacitance C_2 toward the second-from-the-top solid plane instead of being short circuited to the top solid plane. Despite the inconsistency of this assumption, the reflection and the transmission comparisons given in Fig. 3.28 and Fig. 3.29 show the same type of agreement and discrepancies observed in the previous via comparisons of Fig. 3.20 and Fig. 3.21. Specifically, large discrepancies in the S_{11} simulation results as a function of the via radius below 10 GHz. It is interesting to note also the additional feature present below the first large dip in the transmission parameter shown in Fig. 3.29. Being the half-ground via a sort of hybrid element between a signal via and a full-ground via, the dips in the S_{21} corresponds to both the resonance sets associated with the simple plane pair and the simple plane pair plus a shorting pin, both shown in Fig. 3.4.

The same type of agreement and discrepancies between measured results and simulation data are also found when comparing the signal stub via plus half-ground via,

i.e., Fig. 3.32 and Fig. 3.33, and the stub via plus full-ground via, i.e., Fig. 3.24 and Fig. 3.25. Again, the more complex behaviors of the configurations with half-ground vias indicate the presence of both sets of resonances contributing to generate the characteristic features of such geometries.
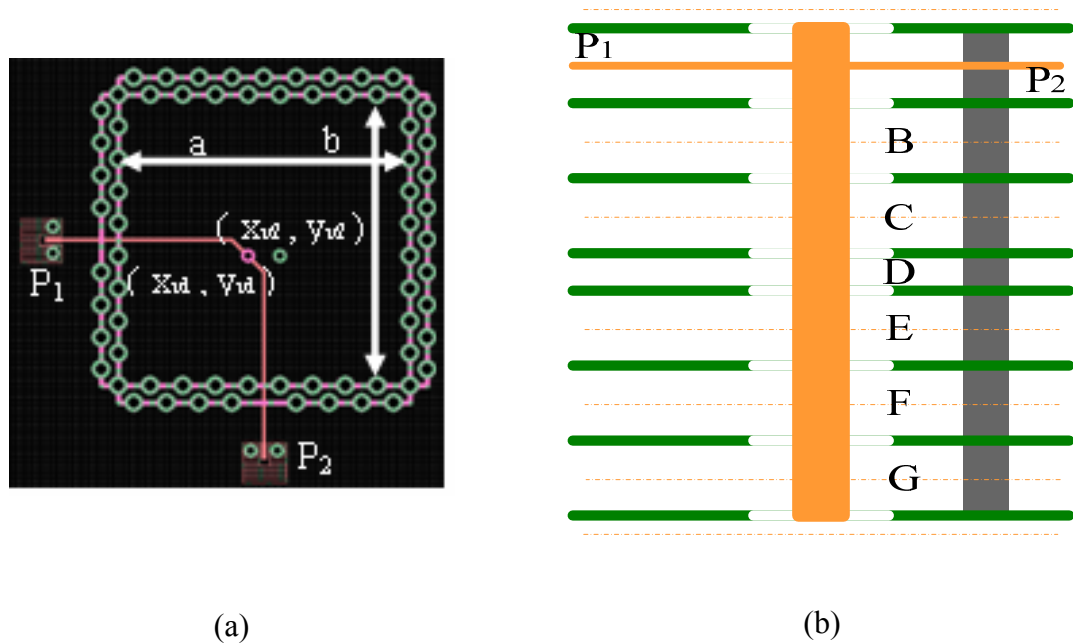

(a)

(b)
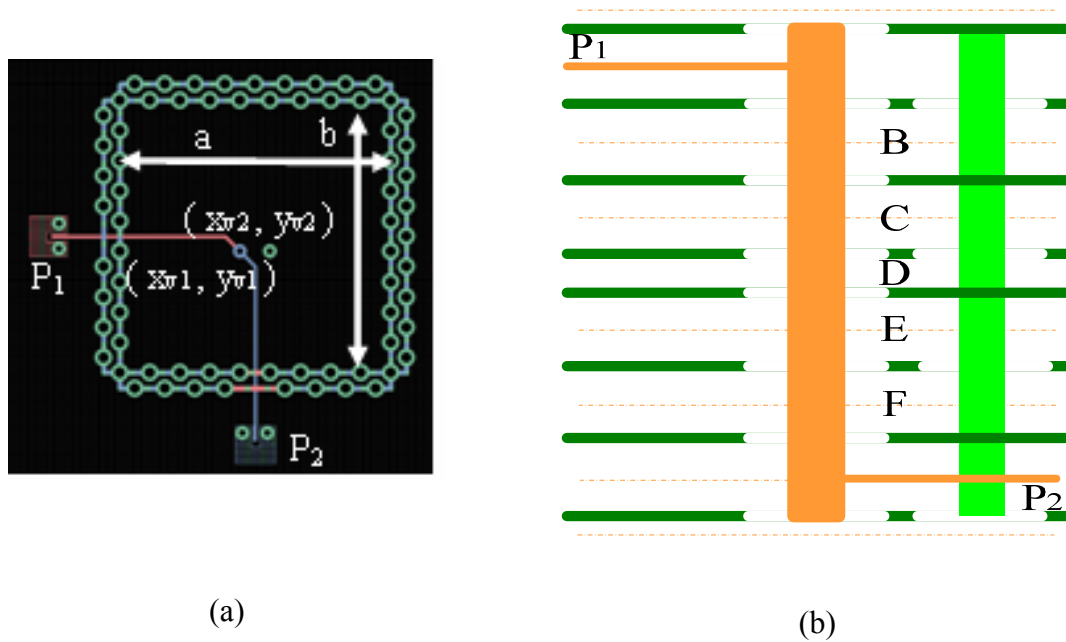
Fig. 3.26. (a) PCB layout excerpt of the through via plus half-ground via configuration. The coordinate sets (x_{v1}, y_{v1}) and (x_{v2}, y_{v2}) correspond to those shown in Fig. 3.2 (b). (b) Stack-up of the through via plus half-ground via geometry.
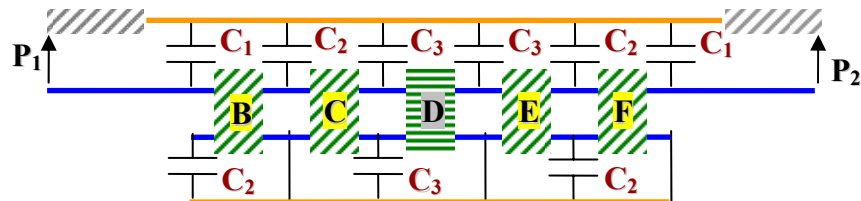
Fig. 3.27. Complete equivalent circuit model of the through via plus half-ground via configuration based on the circuit elements described in.
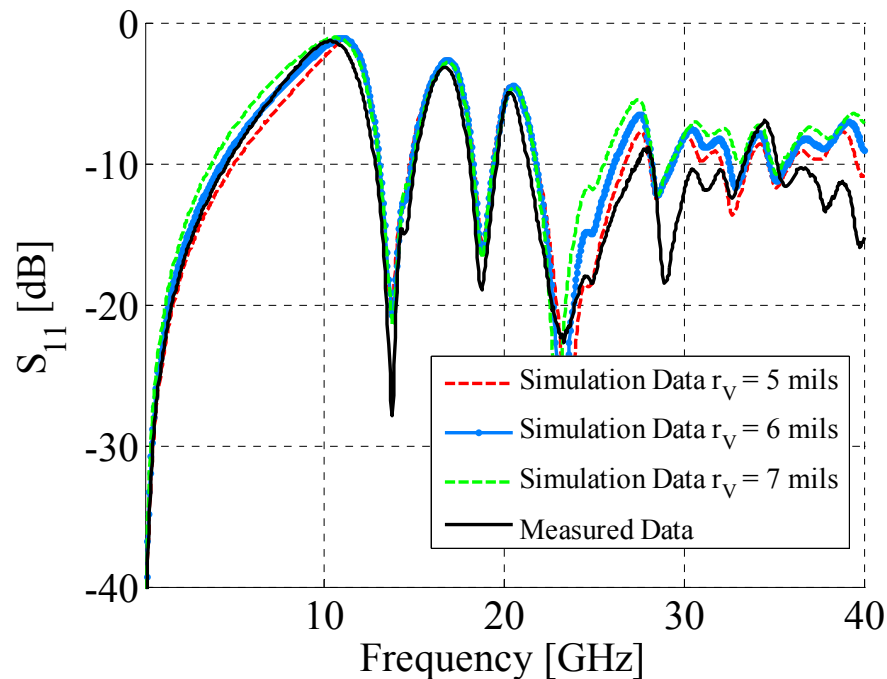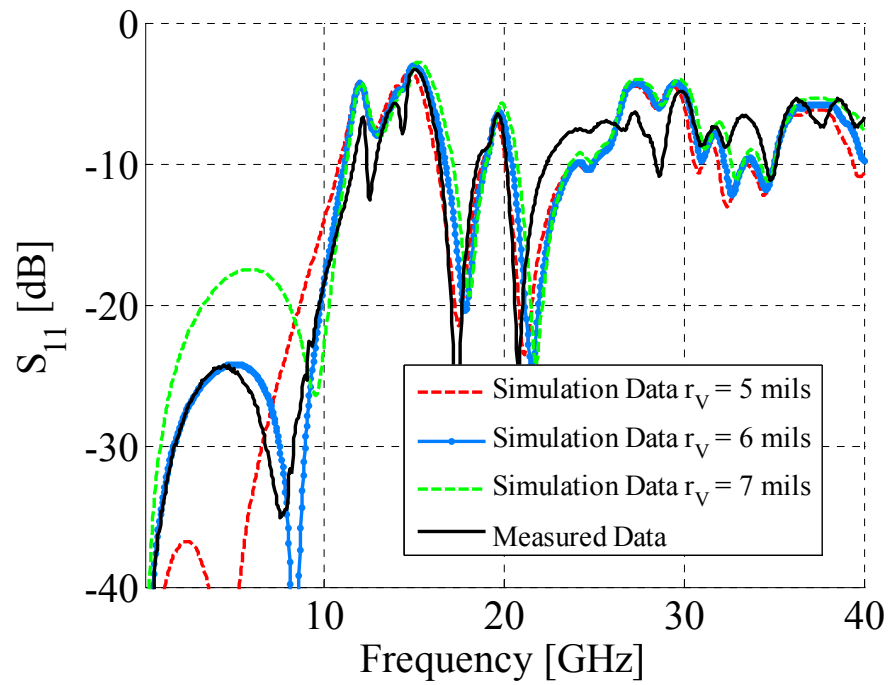
Fig. 3.28. Reflection parameter comparison between measured data and simulation results for the through via plus half-ground via geometry shown in Fig. 3.26.
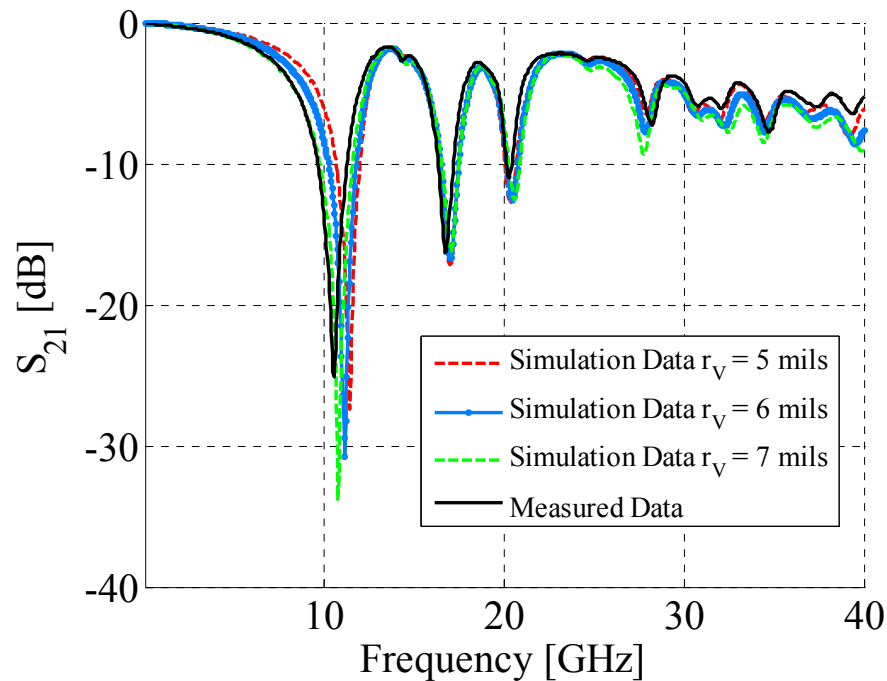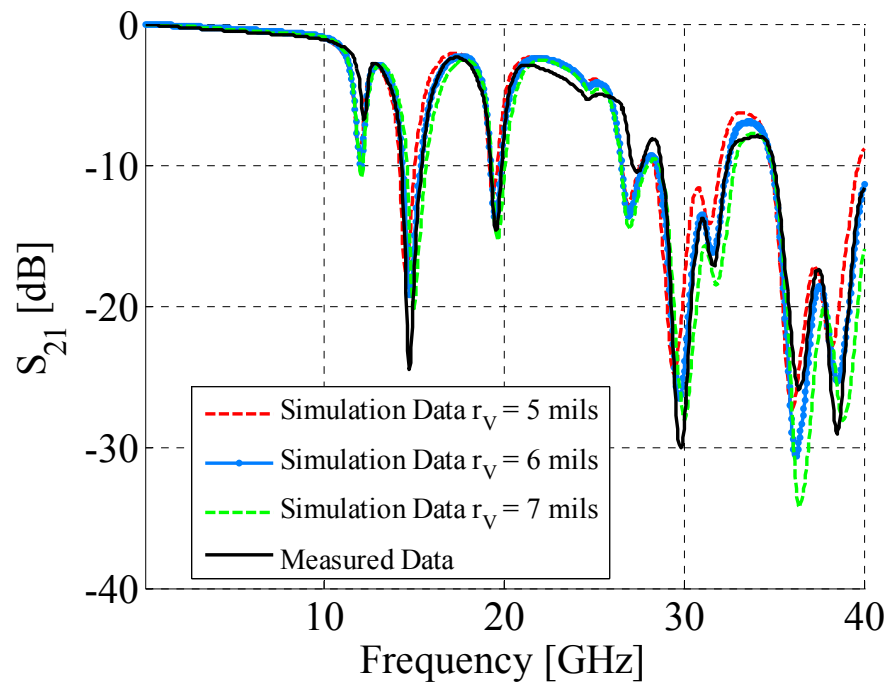

Fig. 3.29. Transmission parameter comparison between measured data and simulation results for the through via plus half-ground via geometry shown in Fig. 3.26.

The features associated with all the models discussed so far is the possibility to recycle the same circuit elements introduced for the coupled via configuration and by

(a)

(b)
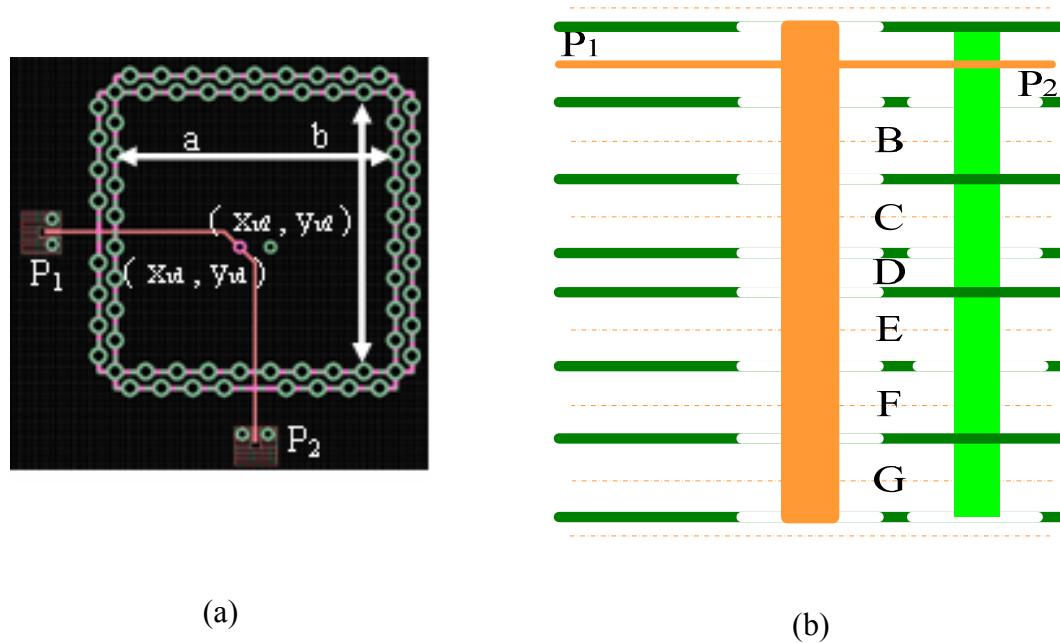
Fig. 3.30. (a) PCB layout excerpt of the stub via plus half-ground via configuration. The coordinate sets (x_{v1}, y_{v1}) and (x_{v2}, y_{v2}) correspond to those shown in Fig. 3.2 (b). (b) Stack-up of the stub via plus half-ground via geometry.
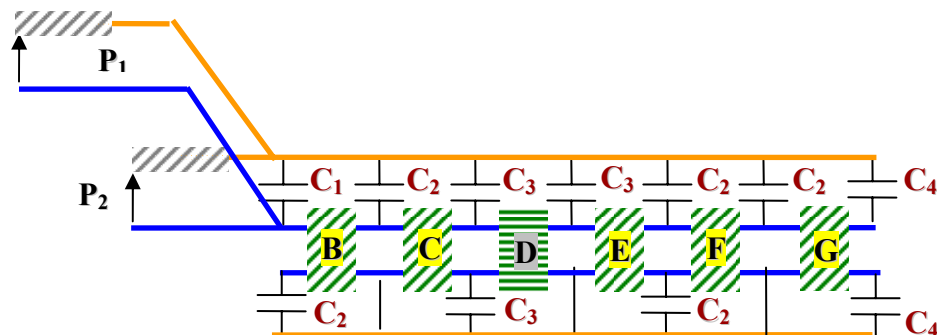
Fig. 3.31. Complete equivalent circuit model of the stub via plus half-ground via configuration based on the circuit elements described in.
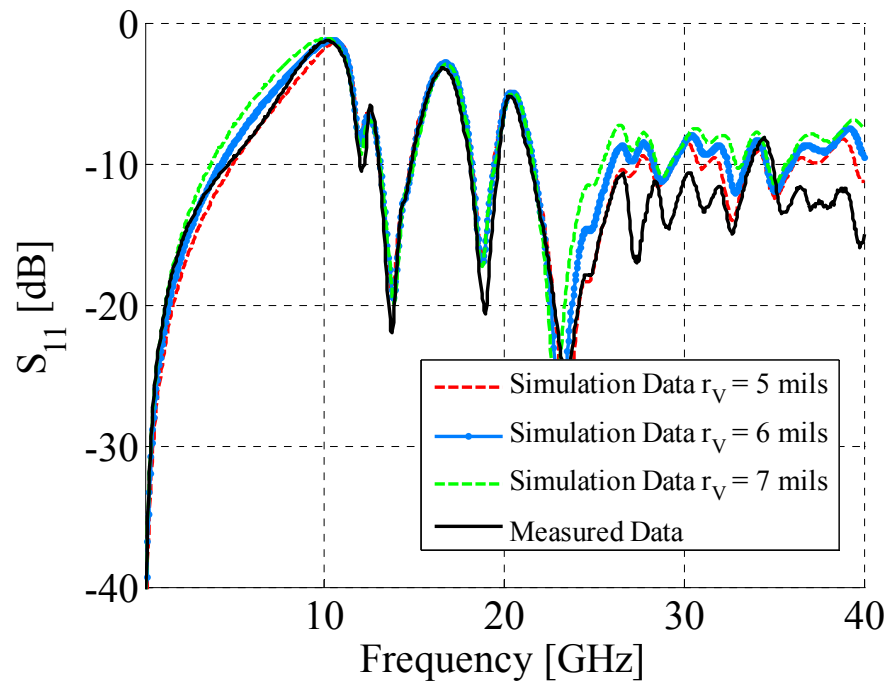
Fig. 3.32. Reflection parameter comparison between measured data and simulation results for the stub via plus half-ground via geometry shown in Fig. 3.30.
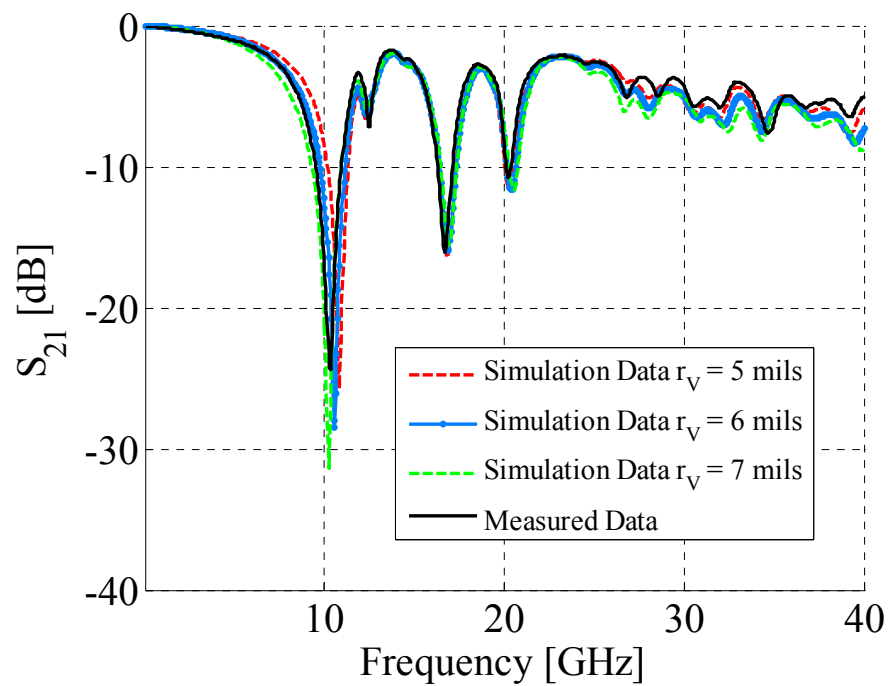
Fig. 3.33. Transmission parameter comparison between measured data and simulation results for the stub via plus half-ground via geometry shown in Fig. 3.30.

changing just the circuit topology represents the physics associated with all the different geometries treated in this paragraph. In fact, when a via is isolated from a solid plane a via-to-antipad capacitance is located between the two voltage potentials located on via and the solid plane, respectively. On the other hand, when a via is connected to one or more solid plane, the via-to-antipad capacitance is removed and the two points are shorted so that the same voltage potential is enforced on both via and the corresponding power plane. When looking at the definitions of the vias, three main groups of vias are introduced throughout this article, i.e., signal vias, full ground vias and half ground vias, the latter two are also called ground vias and power vias, respectively. The major differences consist in the way the vias are connect to the solid planes they penetrate. Signal vias are isolated from all the solid planes regardless of their potentials. The full ground vias or just ground vias are connected to all the solid planes, hence the planes must be held at the same potentials. Finally, the half ground vias or power vias correspond to through hole vias that are not connect to all the solid planes, since different plane can be held at different potentials.

3.4. CONSIDERATIONS ON THE CIRCUIT MODELS

Some of the issues regarding the incompleteness of the models have already been alluded in the previous paragraph. Also, the modeling approach presented in this article for two vias is still characterized by the same limitations and assumptions carried out for the single-ended configurations reported in [3.1]. For instance, neglecting the parallel plate impedance where the striplines are laid out, enforcing all the nodes on the signal path to be at the same potentials, neglecting the additional stub sections left hanging from the top and the bottom and modeling the launching structures as ideal are all assumptions

that degrade the model-to-hardware correlation of the via test sites More over, all the striplines are modeled as ideal lossy 50 Ω transmission lines with constant dielectric permittivity and loss tangent over the frequency range and also no skin effect loss is considered. Another important assumption, in the case of coupled vias, is neglecting all the possible coupling paths between the vias except the transfer parallel plate impedance, i.e., no additional elements are considered such as mutual inductances or capacitances and, finally, another modeling deficiency resides in the formulation of the cavity model. This formulation becomes less and less accurate as the vias get close one another or the via dimensions are not small compare to the wavelength.

3.5.   ZERO AND FIRST ORDER MODEL APPROXIMATION FOR THE PARALLEL-PLATE IMPEDANCE

The model-to-hardware correlation reported for the various via pair cases is shown from 50 MHz up to 40 GHz. This wide frequency range, though, is not always necessary and the interest can be restricted to a narrower band. Since the cavity model approach can be also formulated in terms of circuit elements [3.17]-[3.21], the self and transfer parallel-plate impedances can be viewed as a sequences of parallel R-L-C resonant circuits coupled to the external ports through ideal transformers, whose turn ratios account for the positions of the. Every resonant circuit corresponds to a resonant mode of the cavity, hence by restricting the frequency of interest, only the modes falling within this range can be considered, while all the other can be discarded. The circuit models shown in Fig. 3.34 (a), (b) and (c) correspond to the original implementation and two approximations valid in two narrow frequency bands for the configuration described in Fig. 3.6. The circuit model given in Fig. 3.34 (a) corresponds to the complete

implementation On the other hand, the circuit model in Fig. 3.34 (b) corresponds to the original model with the self and transfer parallel-plate impedances replaced with just the asymptotic self and mutual inductance values reported in Table 3.2.
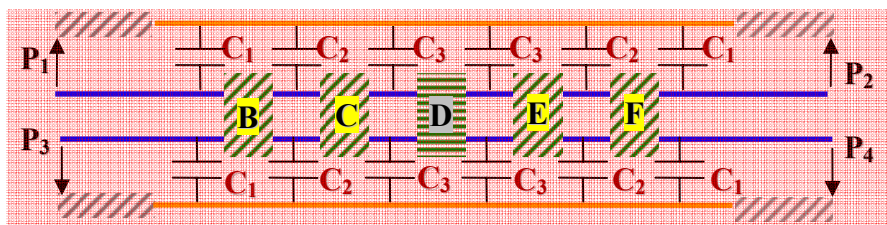
(a) Complete model
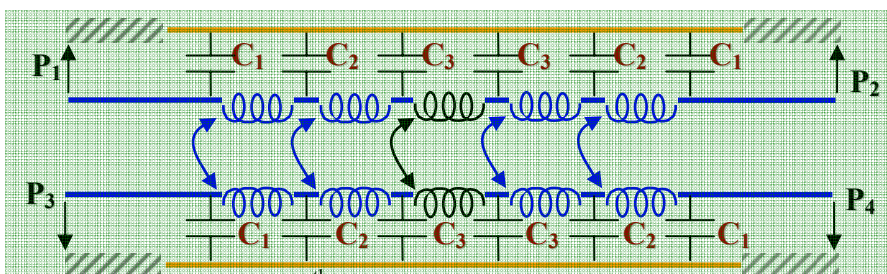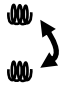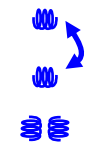
(b) Zeroth order approximation of Zpp
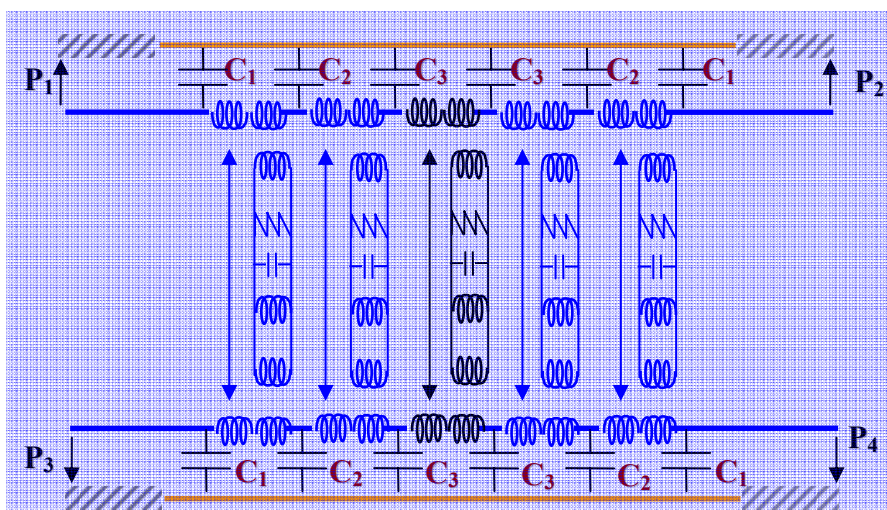
(c) First order approximation of Zpp

Fig. 3.34. Coupled through via configuration: (a) complete model as also shown in Fig. 3.7. (b) Zero order parallel-plate impedance approximation. (c) 1st order parallel-plate impedance approximation.

Table 3.2. Summary of values employed in Fig. 3.34 (b) and (c).

0th order	*12 mils*	$L_1^{HM} = 203pH$ $M_{12}^{HM} = 93pH$ $L_2^{HM} = 203pH$	
	8 mils	$L_2^{HM} = 135pH$ $M_{12}^{HM} = 62pH$ $L_2^{HM} = 135pH$	
1st order	*12 mils*	$L_1^{HM} = 203pH$ $M_{12}^{HM} = 93pH$ $L_2^{HM} = 203pH$ $T_{1\text{-}11} = T_{2\text{-}11} = 1.932$	
		$R_{11} = 43\Omega\ L_{11} = 19pH\ C = 8.6pF$	
	8 mils	$L_2^{HM} = 135pH$ $M_{12}^{HM} = 62pH$ $L_2^{HM} = 135pH$ $T_{1\text{-}11} = T_{2\text{-}11} = 1.932$	
		$R_{11} = 28\Omega\ L_{11} = 13pH\ C = 13pF$	

Finally, the circuit in Fig. 3.34(c) corresponds to the complete model with the self and transfer parallel-plate impedances replaced by the asymptotic self and mutual inductance values plus the first R-L-C resonant circuit. These circuit elements are also reported in Table 3.2. The comparisons of the self and transfer parallel-plate impedances utilized in the circuits in Fig. 3.34 (a), (b) and (c) are shown in Fig. 3.35 and Fig. 3.36, respectively. When employing just the self and mutual inductances, no differences with respect to the complete parallel-plate impedance is observed up to 5 GHz, whereas employing these values and the first resonant circuit allows for a perfect match up to at least 13 GHz. The S-parameter comparisons between the circuits shown in Fig. 3.34 are shown in Fig. 3.37, Fig. 3.38, Fig. 3.39, and Fig. 3.40.
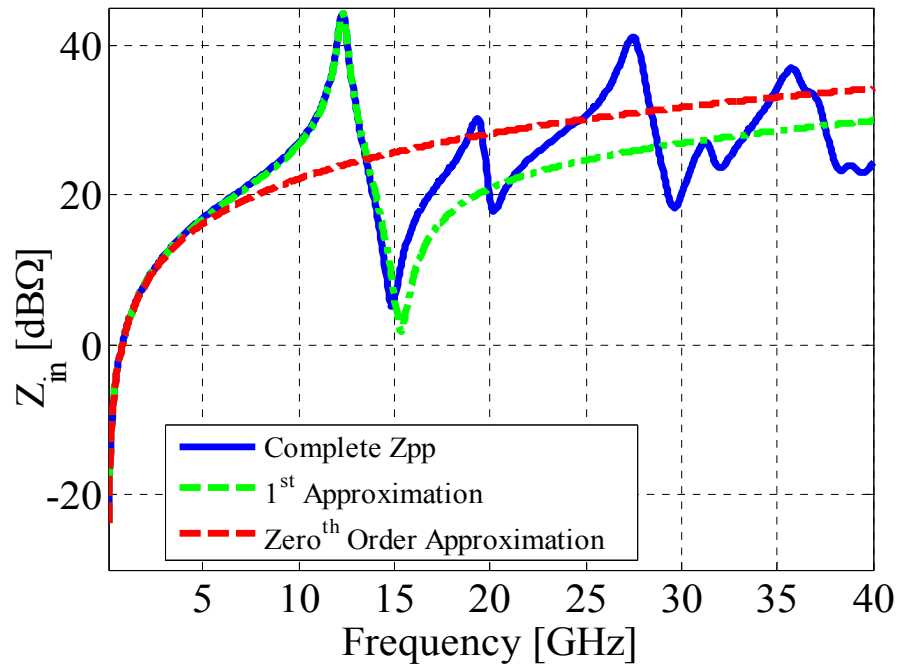
Fig. 3.35. Complete Z_{11} vs.first order approximation vs. zero order approximation.
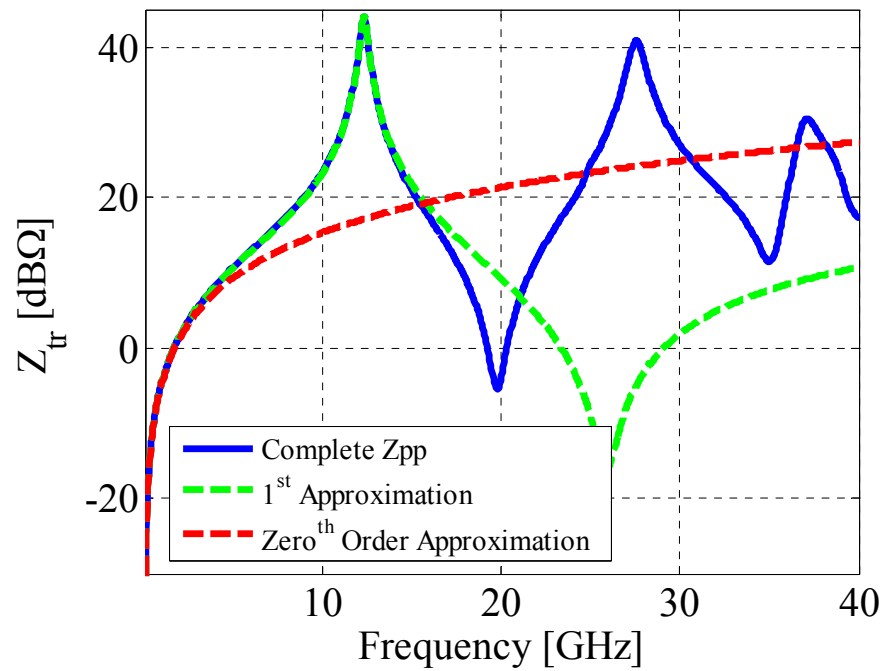
Fig. 3.36. Complete Z_{21} vs. first order approximation vs. zero order approximation.
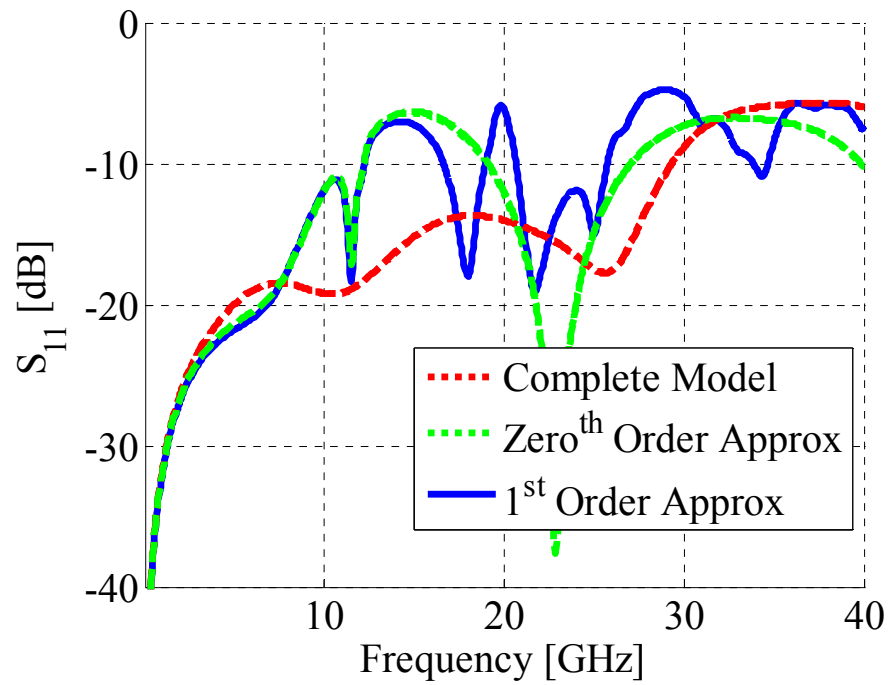
Fig. 3.37. S_{11} parameter comparison for coupled through vias.
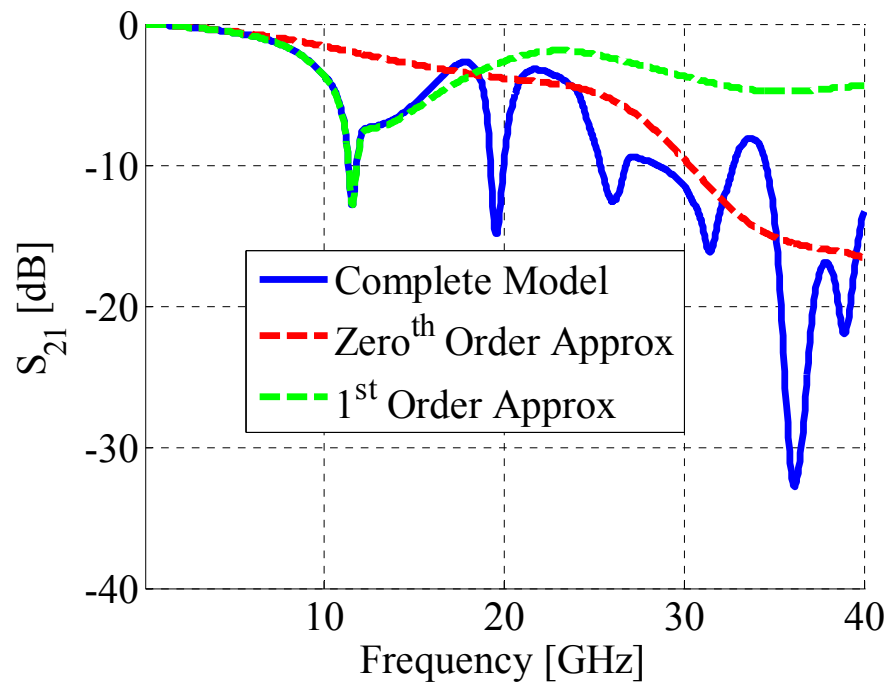
Fig. 3.38. S_{21} parameter comparison for coupled through vias.
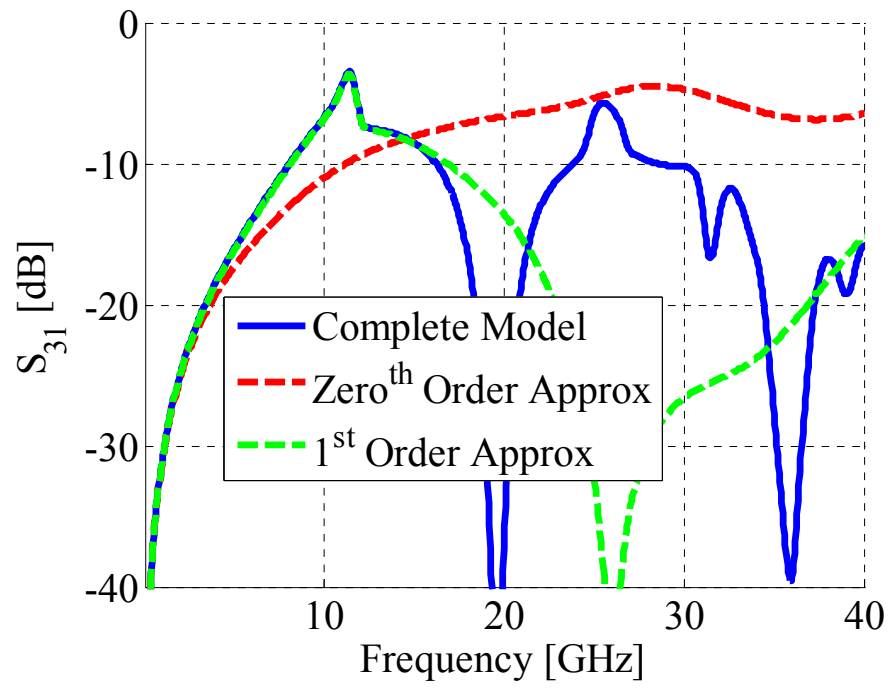
Fig. 3.39. S_{31} parameter comparison for coupled through vias.
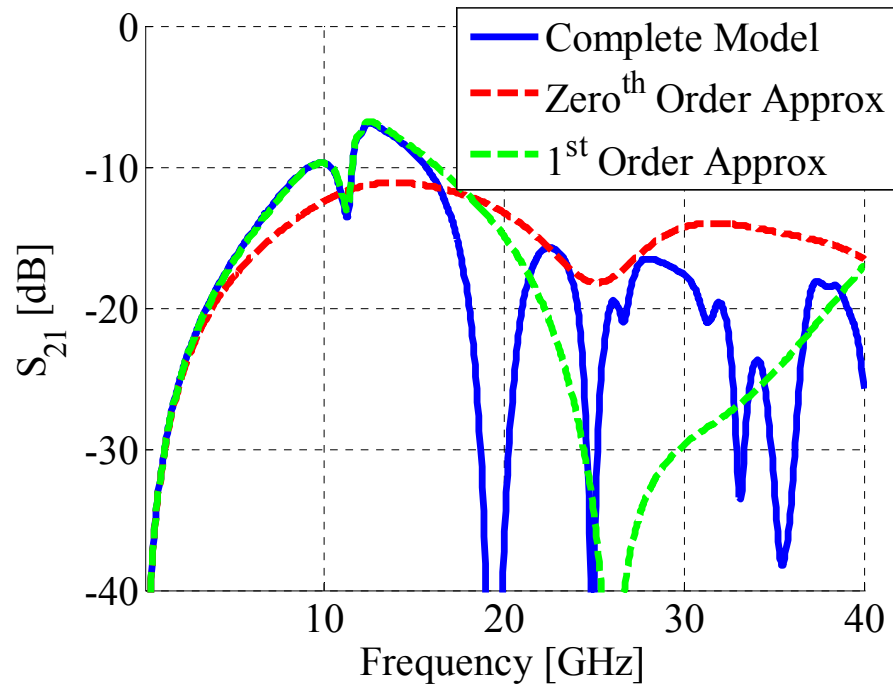
Fig. 3.40. S_{41} parameter comparison for coupled through vias.

3.6.   CONCLUSIONS

The modeling approach already presented in [3.1] for single-ended via configurations is extended to pair of vias in this article. The comparison of simulation results with measured data indicates that these models capture the major physics phenomena and constitute a solid starting point to add, in terms of additional circuit elements, the physics neglected. Few circuit elements are required, i.e., self and transfer parallel plate impedances, transmission lines and capacitances, and a quite variety of via cases can be modeled by rearranging them or changing the connection topology. Both the parallel plate impedances and the via-to-antipad capacitances are calculated by using well-known analytical formulations, found in the literature [3.17]-[3.21], and a quasi-analytical formulation by fitting a wide range of numerical values [3.1]. All the models have been presented by considering different via radii to show the effects of geometry variations on the simulation results, also, the dimensions can be known just within factory tolerances. Finally, the cavity model allows to obtain equivalent circuit representations for the self and transfer parallel-plate impedances to further simplify the models in narrower frequency ranges. Further work is though required at least along three different paths: expand the modeling approach to more than two vias, improve the modeling approach by introducing the physics that have been neglected and, finally, take into account a more realistic power plane environment than a simple ground via cage.

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4.   PHYSICS-BASED VIA MODELS WITH THE PARALLEL-PLATE IMPEDANCE INCLUDED: INCLUDING THE STRIPLINE TO VIA DISCONTINUITY

ABSTRACT

The physics-based via models described in [4.1] and [4.2] are further refined in this article by adding the stripline-to-via transition. Despite the importance of such feature, the incomplete models reviewed in [4.1] and [4.2] show good agreement between measured data and simulation results. Neglecting the transition is then a reasonable assumption for many geometries. Nonetheless, including the transition improves the one-to-one element-geometry relationship, no more topology changes are observed as a function of the stripline position with respect to the layer stack-up and the noise coupling between striplines and cavities can be accounted for, conversely to [4.1] and [4.2]. Not only, model-to-hardware comparisons of other via configurations shows a larger effect of this feature, and the behaviors cannot be captured, unless a complete model for the stripline-to-via transition is included. Measurements, in fact, provide the ultimate mean for validating the models and continuing in the effort of synthesizing physics-based representations to be run within SPICE or SPICE-like base tools.

4.1.   INTRODUCTION

A physics-based modeling approach has been reported in [4.1]-[4.6], based on circuit topology suggestions described in the literature, [4.7]-[4.8]. Its most distinctive feature has been the insertion of self and transfer parallel-plate impedances to model the return paths and the coupling paths of one or two vias in a multilayer environment. A controlled surrounding for the fields, i.e., a ground via cage, has been created for the

purpose of confining the physics of propagation and obtain concise circuit representations. The modeling approach for both single-ended, [4.1], and paired vias, [4.2], employs just transmission line models, capacitances and a one-port or a two-port matrix of parallel-plate impedances to account for via return paths and coupling paths between vias. The parallel-plate impedance elements are obtained in a closed format by using the Cavity Model approach [4.9]-[4.13], while the capacitance values are derived by curve-fitting a wide range of numerical values [4.1]. The most important feature neglected in all the models presented in [4.1] and [4.2] has been the via-to-stripline transition. This transition has been investigated in the literature and some modeling approaches have been reported [4.14]-[4.17]. In the current modeling approach, [4.1] and [4.2], the stripline is always symmetrical and the stripline-to-via transition is simply neglected by tightening together the top and bottom reference planes to create a single reference conductor. This assumption is correct if the geometry is perfectly symmetrical when looking upwards and downwards from the prospective of the stripline-to-via transition, since no voltage differential can develop between the two reference planes - unless intentionally excited. This type of symmetry, though, is not achievable in practice and connecting the two reference planes together precludes the modeling of any parallel-plate noise inside the planes hosting the stripline.

A model for this transition can be devised by looking at the physics of propagation and correspond circuit elements and geometrical features in the same fashion reported in [4.1] and [4.2] for single-ended and paired vias. Once the equivalent circuit representation is obtained and added to the current modeling approach, measured data are utilized to assess and quantify the improvements produced. Several test sites are laid out

for this purpose on a 16-layer printed circuit board. Each test site is enclosed into a cage of ground vias in order to achieve the desired field containment, [4.1]-[4.2], and the Recessed Probe Launch Technique [4.18] and a VNA are employed in the measurement set-up.

The article is organized as follows starting from the second section. The rationale for including the stripline-to-via transition is described in the second section. Then, an equivalent circuit model is reviewed is the third section. The improved modeling approach is utilized to build the via models and simulation results are compared with measured data in the fourth section and, finally, some considerations on the new models are discussed in the fifth section and final conclusions on the new models are drawn in the sixth and last section.

4.2.   NECESSITY OF INCLUDING THE STRIPLINE-TO-VIA TRANSITION

The physics-based via models presented in [4.1] and [4.2] were all obtained by neglecting the cavities hosting the striplines. A direct consequence of this assumption consists in topology changes as a function of the stripline position with respect to the vertical stack-up. For instance, the equivalent circuit model associated with the single-ended stub via neglects just the top-most cavity [4.1], since the striplines are both laid out between the top-most pair of planes On the other hand, the equivalent circuit model for the single-ended through via neglects the top-most and the bottom-most cavities [4.1], since the striplines are laid out between the corresponding planes. It would be preferable to have always the same model for the via and its return path, i.e., the same number of cavities, without any topology changes. and a better model for the stripline structure, since a two-node transmission line model do not enjoy a one-to-one relationship with the

corresponding geometry, i.e., top and bottom reference planes are shorted together. All the test sites investigated in [4.1] and [4.2] have been characterized by good model-to-hardware correlation, but by extreme topologies as well. The striplines are all laid out between the outer pair of planes and the signals do not jump any signal layer or jump the maximum number of signal layers. A topology where the signal jumps just one signal layer is investigated in this section, Fig. 4.1 (a) and (b). The equivalent circuit model is given in Fig. 4.2 and it is obtained by using the modeling procedure and circuit elements described in [4.1] and [4.2]. By reverse engineering the circuit representation of Fig. 4.2 to recover the via geometry of Fig. 4.1, it wouldn't be possible to understand whether the two striplines are laid out between the same pair of planes or adjacent pair of planes, hence the model is ambiguous. If the ambiguity of the topology wouldn't be enough, the comparison of measured data with simulation results for three different via radii [4.1] clearly indicates the incompleteness of the modeling approach, Fig. 4.3 and Fig. 4.4. The equivalent circuit model, as implemented in Fig. 4.2, cannot capture the physics of propagation.

Three different models for three different via radii are built to show the effect of geometry variations on the simulated S-parameter data. The comparison in Fig. 4.3 and Fig. 4.4 show some differences between the simulation results as a function of the via radius, hence, the via-to-antipad capacitance. This configuration, then, behaves like the stub via case, as the similarities with the S-parameter data in [4.1] also demonstrate. Contrarily to the stub via configuration though, a large discrepancy is shown around 12 GHz in the S_{21} plot of Fig. 4.4. A dip in the transmission parameter is observed for the measured data while a smooth behavior is observed for all the simulation results. On the

other hand, the different values assumed by the S_{11} parameter in Fig. 4.3 do not allow to appreciate the same discrepancies to the same extent. In fact, the values assumed by the reflection parameters in the frequency range, where the additional dip in the transmission parameter is observed, hide a possible discrepancy and the resulting curve do not indicate any unexpected behavior when compared to measured data.

(a)   (b)
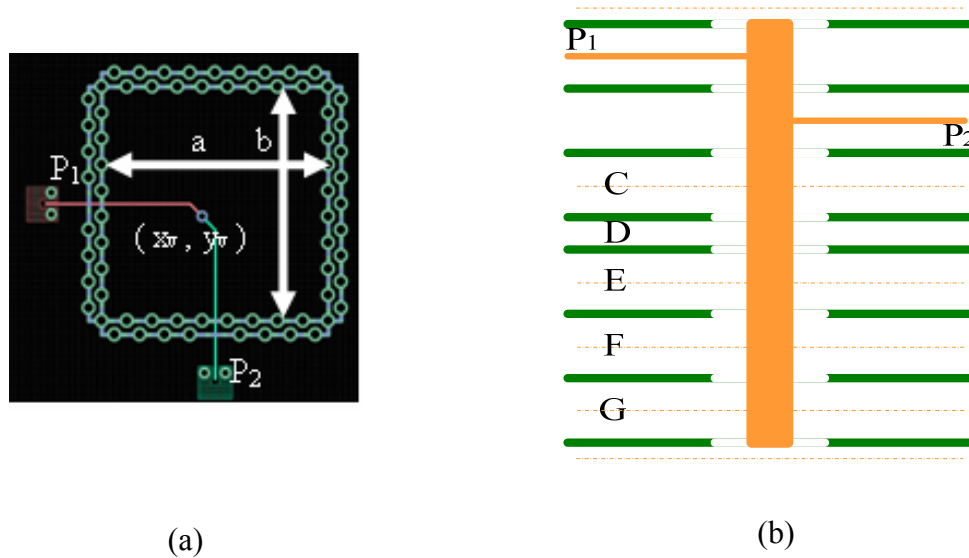
Fig. 4.1. (a) PCB layout excerpt of the via configuration with one signal layer jump. The coordinate set (x_{v1}, y_{v1}) corresponds to the one shown in Fig. 4.2 (b) of [4.1]. (b) Stack-up of the via configuration with one signal layer jump.
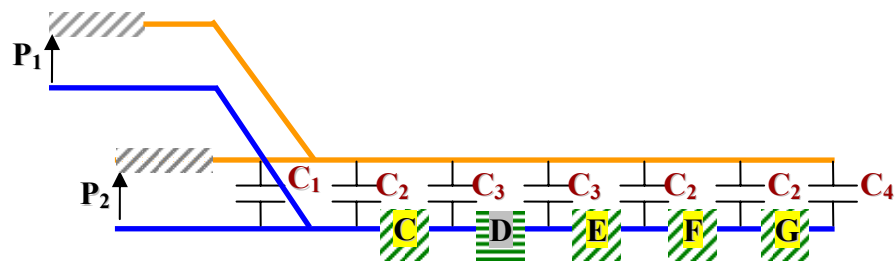
Fig. 4.2. Equivalent circuit model of the via geometry shown in Fig. 4.1 based on the approach and the values given in [4.1].
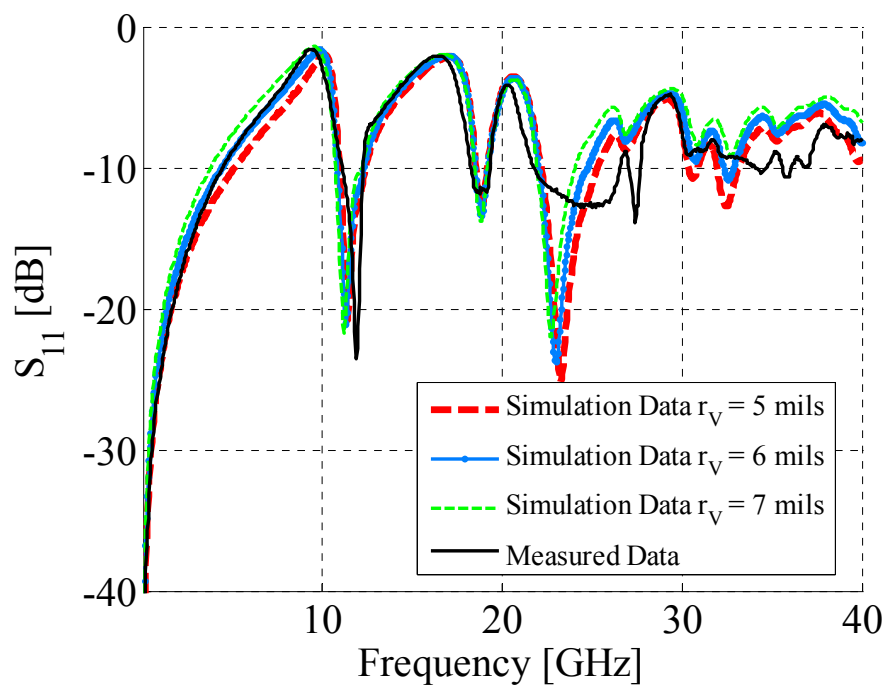
Fig. 4.3. Reflection parameter comparison between measured data and simulation results for the via geometry shown in Fig. 4.1.
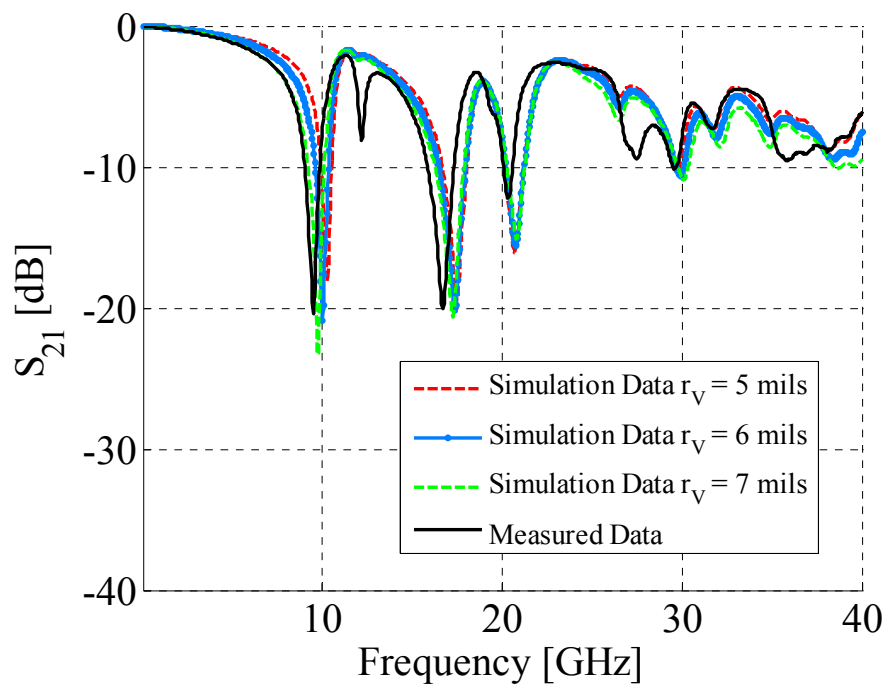
Fig. 4.4. Transmission parameter comparison between measured data and simulation results for the via geometry shown in Fig. 4.1.

4.3.   STRIPLINE-TO-VIA TRANSITION EQUIVALENT CIRCUIT MODEL

The next step for improving the current modeling approach consists in investigating the fields within stripline configurations. For the sake of simplicity, a symmetrical stripline configuration is considered throughout this article. The intentional mode usually launched on a stripline is the stripline mode, i.e., the electric field distribution is even with respect to the metal strip looking toward the upper reference plane and toward the lower reference plane. However, this mode is not supported by the parallel-plate geometry hosting the stripline, and noise coupling is not possible. The only possibility to observe noise coupling between the parallel-plate structure is to convert the stripline mode into an odd mode, i.e., the electric field is distributed in an odd fashion with respect to the center metal strip when looking toward the upper reference plane and the lower reference plane. This type of field distribution is also supported by the parallel plate geometry and noise can propagate from the stripline to anywhere within the planes. Now, the only location where mode conversion can occur is where the stripline meets the via barrel, because the stripline is symmetrical. However, no mode conversion can happen if also the signal paths are symmetrical from the transition prospective when looking upwards and downwards. In other words, parallel-plate noise cannot propagate, if the same exact geometry characterizes the two board sub-sections stacked on the top and the bottom of the planes hosting the stripline. This rationale is described and validated in Fig. 4.5. Two simple configurations are realized with a 3D full wave tool. The geometries consist of two and three pair of planes 360 mils by 360 mils lateral dimensions and 12 mil separation. In both cases, the second pair from the top hosts two sections of a 50Ω stripline, which are united at a point of x and y coordinates equal to 160 mils and 160

mils, where a 5 mils radius via is located. The via penetrates all the solid planes through a 15 mils antipad and the striplines are fed and/or terminated by using waveguide ports, so that the stripline mode is excited or terminated only. Finally, PEC boundary conditions are employed at the edge of the plane pair, to resemble the geometries presented in [4.1] and [4.2]. Both geometries are shown in Fig. 4.5 (a), (b), (c) and (d). The stripline is symmetrical and several field probes are located at different positions to monitor the amount of noise coupled into the planes due the mode conversion or lack thereof. The incident wave along the symmetrical stripline due to a symmetrical excitation can be rendered to be split in half along two propagating paths, one corresponding to the top surface of the strip and the top reference plane, the other between the bottom surface of the strip and the lower reference plane. In the configuration of Fig. 4.5 (a), each wave sees the same geometry when they hit the via barrel, hence, the same reflected wave is observed on both propagation paths. No voltage is developed between the bottom and top reference plane and no noise is coupled into the parallel-plate geometry. This argument is also supported by looking at the maximum value of the electric field over a cross section of the geometry, Fig. 4.5(c), and the field monitored along the z direction by two probes inside the middle pair, Fig. 4.5(e). The containment of the field in proximity of the stripline and the lack of electric field along the z direction indicates no parallel-plate noise. The only mode allowed to propagate within the middle planes is the stripline mode, while parallel plate modes are excited within the top and bottom pair of planes, due to the vertical component of the via current. If now the discontinuity is modified as shown in Fig. 4.5, the signal paths are no longer symmetrical from the transition prospective. The waves propagating along the two paths see different discontinuities and

(a) Symmetrical

(b) Asymmetrical

(c) Peak E-field observed at a given cross-section

(d) Peak E-field observed at a given cross-section

(e) E_z observed between the plane pair where the stripline sections are laid out

(f) E_z observed between the plane pair where the stripline sections are laid out
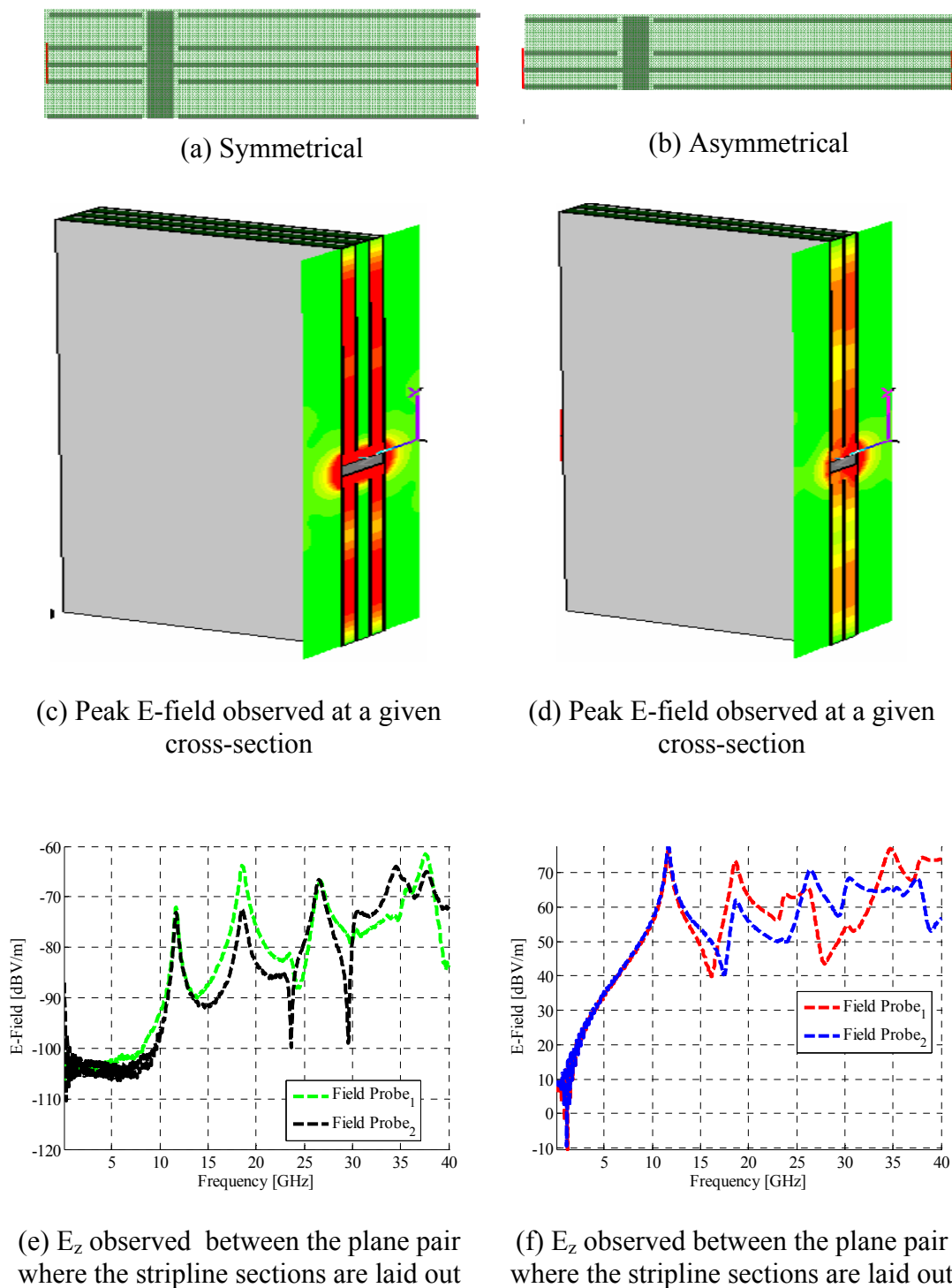
Fig. 4.5. (a) Symmetrical configuration under investigation. (b) Asymmetrical configuration under investigation. (c) Peak E-field observed over a cross-section of geometry (a). (d) Peak E-field observed over a cross-section of geometry (b). (e) E_z field observed at two given locations within geometry (a). (f) E_z field observed at two given locations within geometry (b).

a voltage differential is created between the two reference planes. This voltage can be supported by both the stripline and the parallel-plate geometry, and noise can couple into the planes now. The excitation of the parallel-plate mode can be observed by looking at the electric field distribution over the same cross section as before and the electric field along the z direction monitored at the same probe locations as before, respectively shown in Fig. 4.5(d) and (f).

The investigation of the fields has confirmed the necessity to build the transition model by establishing a complete relationship between circuit elements and geometry features. Treating the stripline configuration as a three-conductor structure has already been showed in the literature [4.14]-[4.17]. Moreover, separating the top reference conductor from the bottom reference conductor allows for the creation of a voltage difference in the case of an asymmetrical stripline-to-via transition. A three-conductor model for a 50Ω symmetrical stripline is then obtained by connecting in parallel two 100Ω transmission lines and joining the center conductor. Three-nodes then become available at both ends for connecting the stripline to the via models proposed in [4.1] and [4.2]. The one to one correspondence between geometry and circuit elements is finally shown in Fig. 4.6 (a), (b) and (c). In fact, it is possible to obtain a one-to-one correlation between the geometry features characterizing this discontinuity and all the circuit element utilized to model it. The investigation of the fields has confirmed the necessity to build the transition model by establishing a complete relationship between circuit elements and geometry features. Treating the stripline configuration as a three-conductor structure has already been showed in the literature, and the consistency with the via modeling proposed in the previous paragraph is shown in this section.
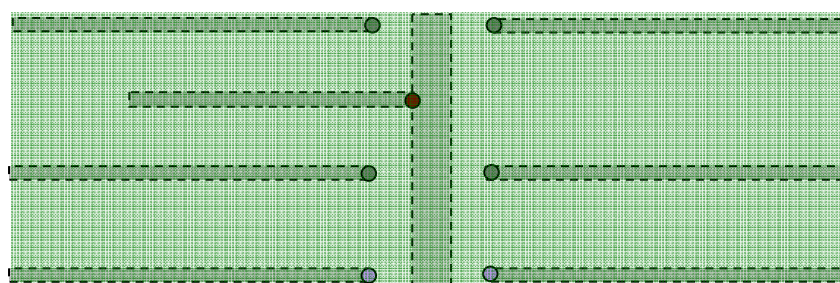
(a) Geometry
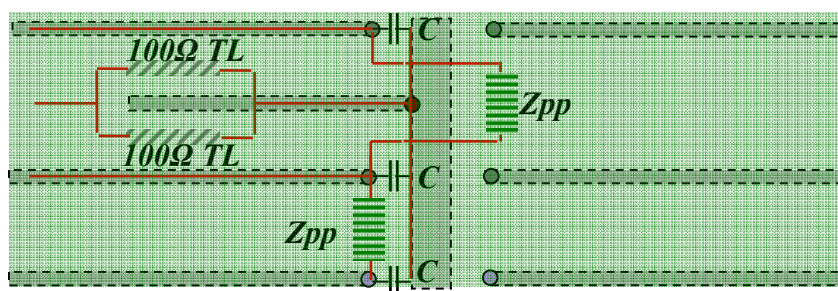
(b) Geometry and circuit
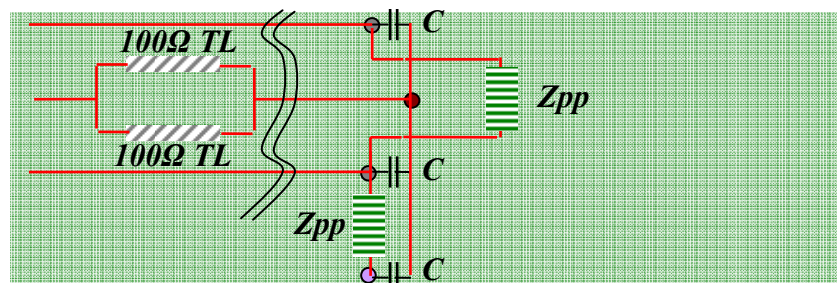
(c) Circuit only

Fig. 4.6. (a) Geometry under investigation. (b) Geometry plus circuit model. (c) Circuit model only.

4.4. BUILDING THE NEW VIA MODELS AND COMPARISON WITH OLD MODELS AND MEASURED DATA

The modeling approach allows now to treat independently the geometry corresponding to the transmission line model and the geometry corresponding to the via

plus its return path. For instance, the inconsistencies reported in the previous paragraphs regarding the stub via, the through via [4.1] and the via model of Fig. 4.2 can be all resolved. First, the via and its return path are modeled, then, the tri-conductor transmission line is attached where dictated by the actual via configuration under investigation. An example of this approach is shown in Fig. 4.7, where the via plus its
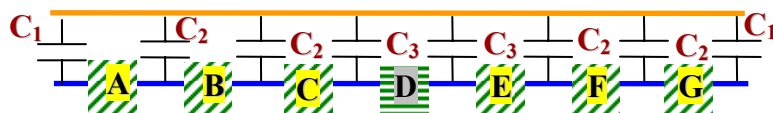

(a) Via plus its return path
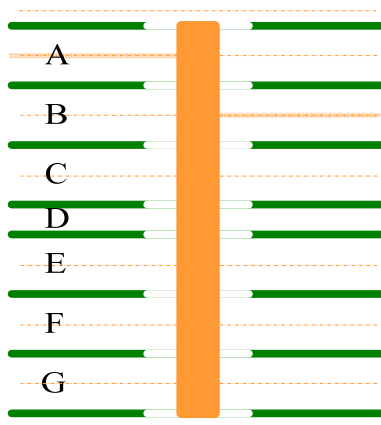
(b) Stack-up of interest
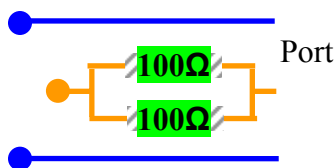
(c) 3-conductor TL

Fig. 4.7. (a) Circuit modeling of the via and its return path for the stack-up in (b). (b) Via stack-up of interest. (c) Three-conductor transmission line model.

return path model is shown in Fig. 4.7 (a) for the stuck-up in Fig. 4.7 (b). Depending

upon the position of the striplines with respect to the stack-up, the tri-conductor model

shown in Fig. 4.7(c) can be plugged across any plane pair. For instance, the via model

Fig. 4.1 can be built by plugging the transmission line model of Fig. 4.7(c) across cavity

A and cavity B. The final comparison between the old modeling approach and the new

modeling approach for the via geometry of Fig. 4.1 is reported in Fig. 4.8. Not only the

inconsistencies reported in the previous paragraph are overcame, the simulation results

reported in Fig. 4.9 and Fig. 4.10 show a better agreement, when compared with the

previous simulation results.
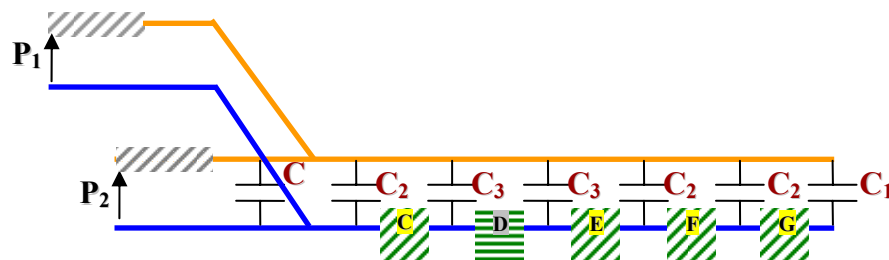
(a) Old model
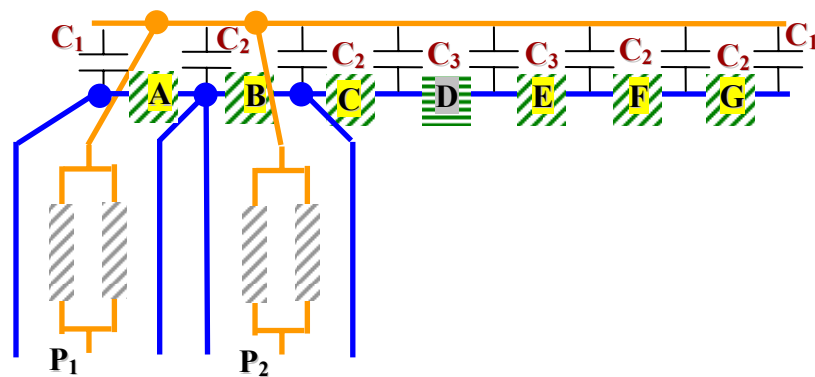
(b) New model

Fig. 4.8. Circuit topology comparison between the old modeling approach and the new
modeling approach for the via configuration given in Fig. 4.1.

Fig. 4.9. Reflection parameter comparison between measured data and simulation results for the via geometry shown in Fig. 4.1.

Fig. 4.10.Transmission parameter comparison between measured data and simulation results for the via geometry shown in Fig. 4.1.
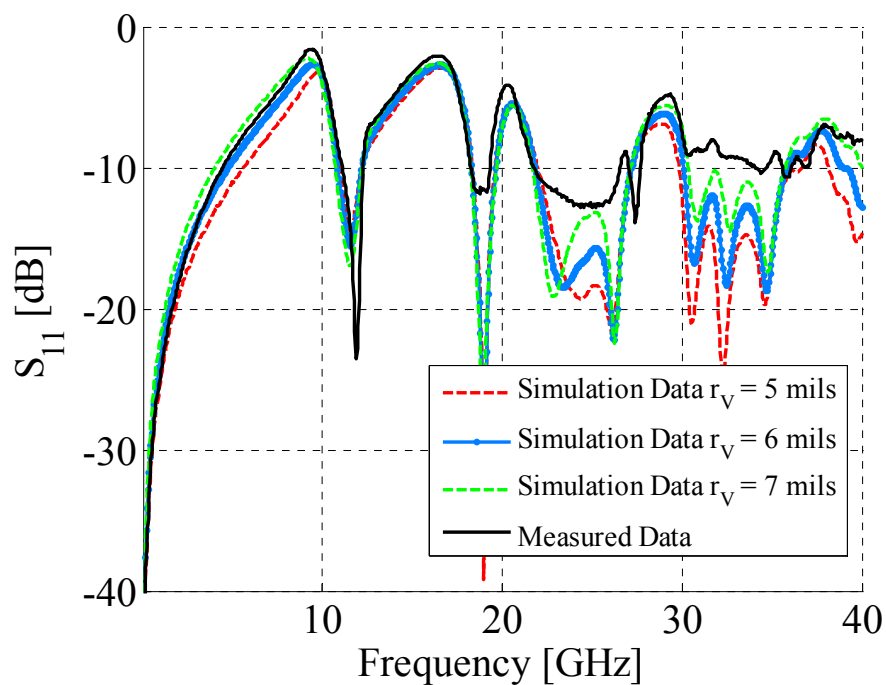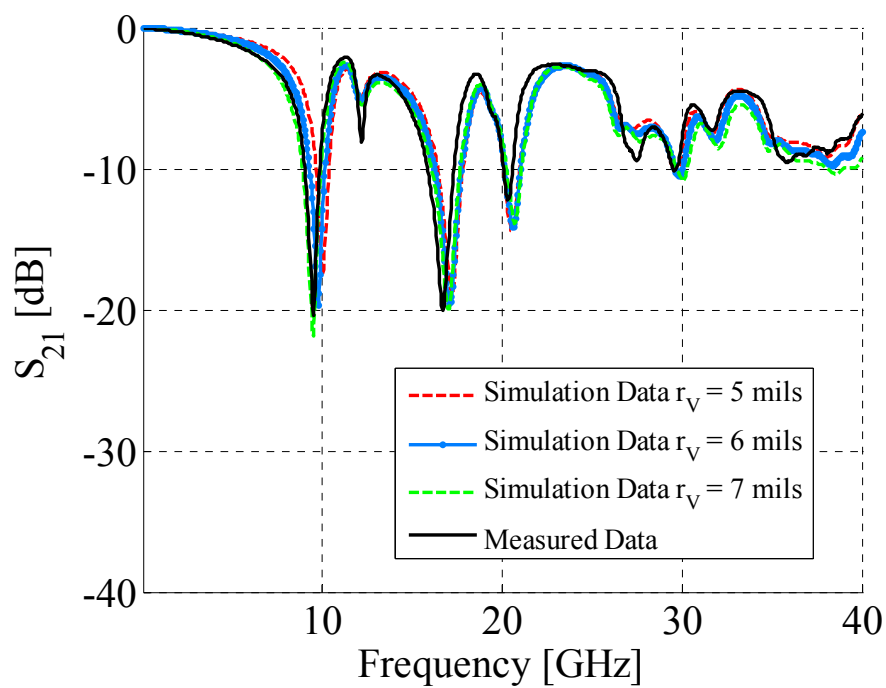
Both the S-parameter comparisons between measured data and simulation results in Fig. 4.9 and Fig. 4.10 show the improvement of the new modeling approach for the via of Fig. 4.1. The dip around 12 GHz is captured, also, the via reflection characteristics are represented by the new modeling approach. The variation as a function of the via radius confirms the resemblances between this and the single-ended stub case.

4.5.   CONSIDERATIONS ON THE MODELS

Although the new modeling approach reflects the physics of propagation and makes the topology independent from the location of the stripline, only the test site shown in Fig. 4.1 is effected by the accurate modeling of the stripline-to-via transition among all the test sites extensively analyzed in both [4.1] and [4.2]. The model-to-hardware correlation given in Fig. 4.11 and Fig. 4.12 for the stub and through via configurations shows the same model-to-hardware correlation as the one reported in [4.1]. Employing a two-conductor transmission line and neglecting the cavities hosting the striplines do not significantly affect the accuracy of the results. Nonetheless, the new modeling approach makes the circuit models more consistent from a topological prospective as the comparison between the stack-up and new equivalent circuit models, Fig. 4.13, demonstrates. Despite the improvement in the approach, other important factors haven't been considered so far. The assumptions have been discussed in [4.1] and [4.2] already. Nonetheless, some of those assumptions are noteworthy and are repeated in this paragraph. For instance, the effects of the stubs hanging from the top and the bottom of the via configurations. Also, no parasitics have been introduced yet to model with a higher degree of accuracy the recessed probe launching structures [4.18].
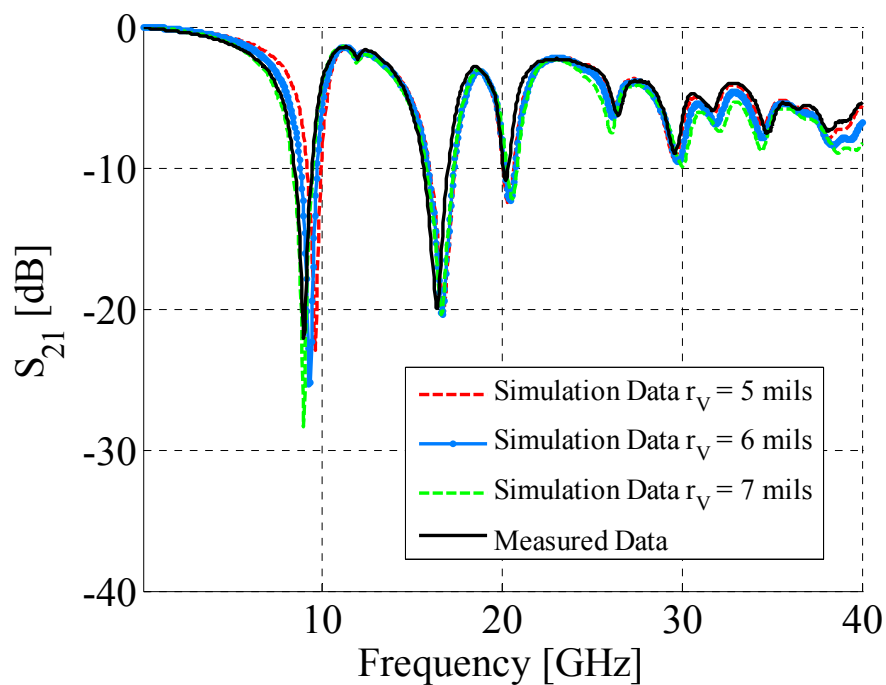
Fig. 4.11. Transmission parameter comparison between measured data and simulation results for the via geometry shown in Fig.4.13 (b).
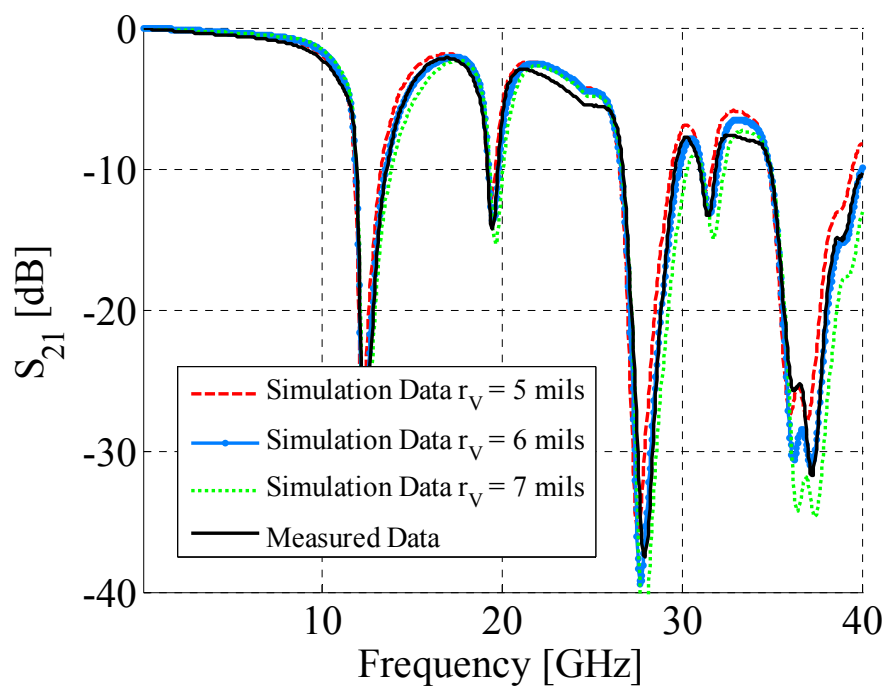
Fig. 4.12. Transmission parameter comparison between measured data and simulation results for the via geometry shown in Fig.4.13 (b).

(a) Stub via complete model

(b) Through via complete model
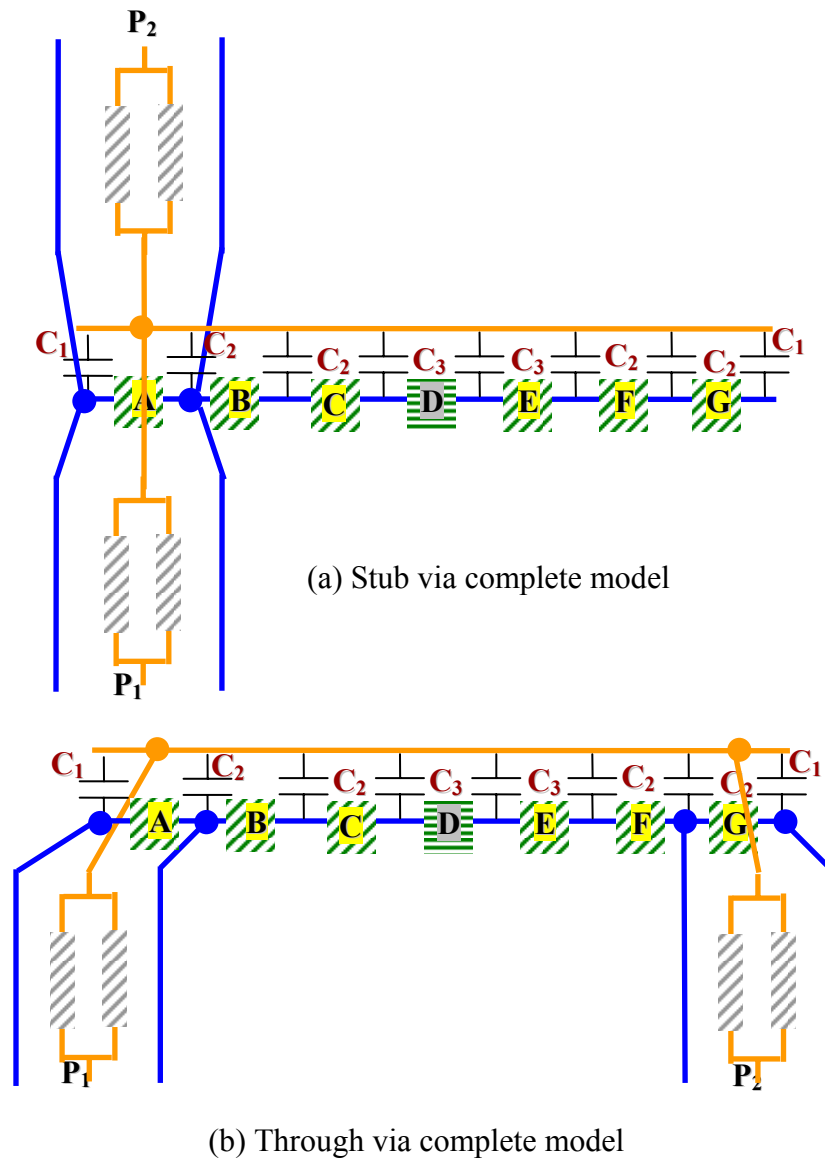
Fig. 4.13. Equivalent circuit representations for the stub via geometry (a) and through via geometry (b) obtained by adding the stripline- to-via transition model.

Moreover, the striplines have been assumed to be symmetrical and they have been modeled as a parallel combination of two 100Ω transmission lines with a frequency-independent relative permittivity and tangent delta.

4.6.   CONCLUSIONS

The physics based models already presented in [4.1] and [4.2] are improved in this article by including the stripline-to-via transition.. Although this assumption is shown not to be severe for many cases, it is very important to capture the physics of via transitions as the types of configurations investigated is increased and avoid topology changes as a function of the test site considered. The possibility to couple noise on the plane pair hosting the striplines has also been one of the interesting consequences of the new modeling approach. The converse phenomenon can be also captured now, i.e., noise coupling on the stripline due to other vias or stripline-to-via transitions. Another great advantage of the circuit model described in [4.1],[4.2] and here consists in employing few circuit elements, i.e., parallel-plate impedances, transmission lines and capacitances. More over, both the parallel plate impedances and the via-to-antipad capacitances are calculated by using analytical or semi-analytical close form expressions [4.1] and [4.10]-[4.13]. Finally, quite a variety of via topologies can be obtained by rearranging the constituting elements or changing the connection among them. Further work is though required at least along three different paths: expand the modeling approach to more than two vias, improve the modeling approach by introducing the physics neglected and, finally, take into account a more realistic power plane environment rather than a simple ground via cage.

4.7.   REFERENCES

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