A Review of Highly Efficient Class F Power Amplifier Design Technique in Gigahertz Frequencies

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***Abstract*—Highly efficient class F power amplifier (PA) in Gigahertz (GHz) frequencies for wireless application is reviewed in this paper. The study focused on the technique used in designing a class F PA especially at GHz frequencies. Several works on the class F PA with different semiconductor technologies from year 2001 to 2016 are discussed. Recent works on class F PA in wireless applications are examined and a comparison of the PA performances of various techniques is presented. Key performance indicators for high efficiency class F PA include power added efficiency (PAE) and output power (P_{out}).**

***Index Terms*—Class F; High Efficiency; Power Added Efficiency; Power Amplifier.**

I. Introduction

Power amplifier (PA) is a key element that boosts the electrical signal in a wireless system such as ultrawide band (UWB) [1]-[3], wireless local area network (WLAN) [4], and Worldwide Interoperability for Microwave Access (WiMAx). Class F PA is among the switching class of PAs that has widely gain interest for high efficiency and longer battery life. Class F PA delivers high efficiency at any GHz frequencies by harmonically tuned the drain voltage and current waveforms. Class F PA enables low switching driver compares to class E PA and only needs a low voltage at the output node to allow low stress on the device. An ideal class F PA is 100% efficient when the voltage and current waveforms are completely flat either as a short circuit for even harmonics or an open circuit for odd harmonics. As zero-power dissipation is present, no overlapping occurs across the active device [4].

Along with the advancement in semiconductor technology, different designs are proposed to match the optimum performance of class F PA. Technologies such as Gallium Nitride (GaN), Gallium Arsenide (GaAS), and Complementary Metal Oxide Semiconductors (CMOS) are in demand due to its compatibility with class F PA. Different approaches are presented by using an infinite number of odd- or even harmonics with lowest order being added first. Class F PA design with different techniques are analyzed in this paper. Common techniques for load input and output matching networks used in a class F PA design are such as lumped elements, transmission lines and load-pull/source-pull techniques.

This review is divided into sections as follows. Section II will analyze the problems and limitations in designing class F PA. Section III will explain in details on the proposed high efficiency PA design with perspective techniques. Section IV discussed the finding summary and the conclusion is given in Section V.

II. Problem and Limitation

A demanding PA is a PA with high efficiency, high output power, good gain and high linearity. Class F PA approach is first developed to increase the efficiency of linear PAs such as class A and AB. Among the switching (non-linear) PAs, class F PA is developed in frequency domain while class D and E are in time domain. This allow class F PA to boost the efficiency [5]. Basic component in any class F PA design is the matching input and output networks, which consist of an inductor and a capacitor. The designing and implementation of class F in radio frequency (RF) PAs remain challenging prior to the impedance adjustments for each harmonic network, which must be terminated per the number of order harmonic. The number of orders in a circuit can be up to fourth order. The number of harmonic determines the voltage and current waveforms as an overlapped waveform will reduce the efficiency. The number of harmonic presents in a class F design is a trade-off between linearity and efficiency while reducing power consumption in a transistor enables efficiency enhancement. Thus, the research is still being performed on the design of class F as termination of harmonics are impractical as well as the ability to compromise with other performance parameters such as gain, output power and stability.

III. Load Matching Network Techniques

Class F PA design is first recognized after it is being implemented and its general descriptions are presented in 1919. The problems in applying lumped element into the output networks of very high frequency (VHF) PA designs are noted in [6]. Thus, quarter-wavelength transmission lines are proposed to control the harmonics. Then, the first application of ultra-high frequency (UHF) class F PA is presented in [7]. Switching class D, E and F PAs are increasingly became a popular approach to improve the efficiency of UHF and microwave PAs although it is a difficult task to find transistors which capable to quickly switch the PAs at VHF. However, [8-9] proposed the idea of a class F PA with maximally flat waveform in 1997 before expanding his work to determine the relation of number of harmonics used in the design with the efficiency and upper

limits of output power.

A. Lumped Elements

The first paper that used load network with lumped elements (LC matching network) is proposed in [10]. Two microwave monolithic integrated circuit (MMIC) class F PAs with 2.0 and 2.8 GHz frequencies are fabricated in field-plated GaN technology for high power performance. The schematic circuit for 2.0 and 2.8 GHz PA are shown in Figure 1 and Figure 2. The overlapping between the current and voltage waveforms are minimized to improve the efficiency of the PA. For 2.0 GHz PA, resistor R_1 is added to improve the circuit stability while inductor L_2 and capacitor C_2 act as harmonic trap to tune the first harmonic while inductor L_3 and capacitor C_3 tune the second harmonic. The combination of L_3, L_4, C_3 and C_4 terminate the third harmonic to achieve 50Ω optimum impedance. The circuit achieves 50% of PAE and 38 dBm of P_{out}. Meanwhile, for 2.8 GHz PA, the transistor used to result in 46% of PAE, 7.0 W/mm of power density and 37 dBm of P_{out}. The proposed designs show the use of GaN class-F MMIC PA is possible to achieve high efficiency. However, both PAs achieve low gain which is only 10 dB.

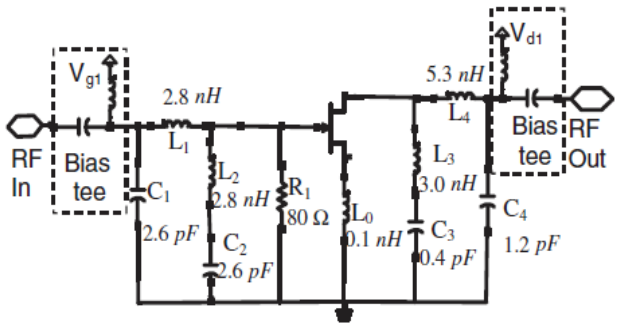

Figure 1: Proposed schematic circuit for 2.0 GHz PA [10]

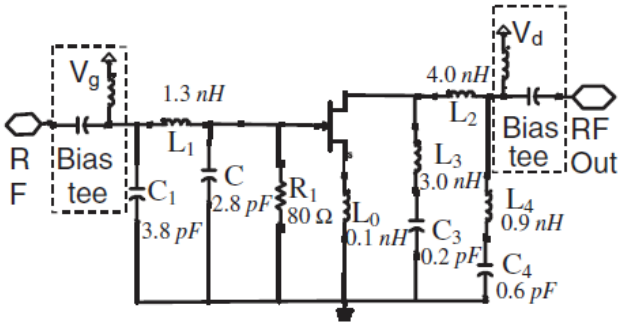

Figure 2: Proposed schematic circuit for 2.8 GHz PA [10]

Another design with different technology is presented in [11]. Two stages of the amplifier known as pre-amplifier stage and amplifier stage are implemented in CMOS class F PA to boost the gain and efficiency. The amplifier stages are shown in Figure 3. The PA achieved 21.8 dBm of P_{out} and 43.95% of efficiency at 2.4 GHz frequency.

Later, the same authors in [11] proposed a PA for 1.6 GHz frequency [12]. Third harmonic peaking of the suggested PA is shown in Figure 4 with two LC resonant circuits operated on the third harmonic where M_1 acted as a switch. The disadvantage of this design is it delivers a high PAE which is 42% yet it only achieves 18.98 dBm of P_{out}.

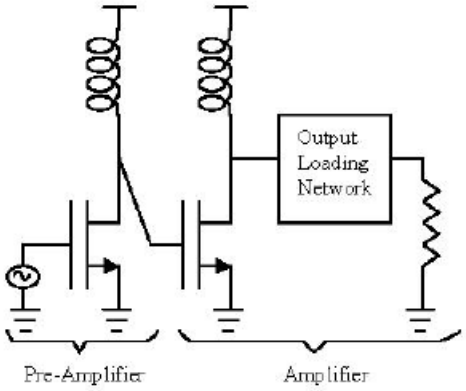

Figure 3: Schematic circuit of two stage 2.4 GHz PA [11]

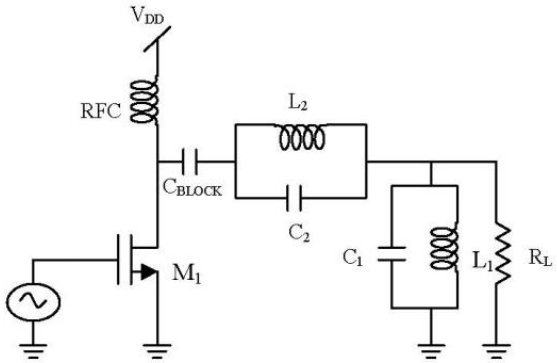

Figure 4: Third harmonic of proposed PA design [12]

Another MMIC with GaAs HEMT technology is proposed in [13]. As shown in Figure 5, the design is to test the dependency of PA on low supply voltages to compromise with output power and efficiency. An optimum conduction angle and load line selection is studied. A simple L matching network is used to maximize the power transfer. However, it leads to a more complex output network. Thus, three different LC circuits are used to obtain the required impedances. At a central frequency of 2.15 GHz, the design achieves 50% of PAE with low P_{out} which is 19.5 dBm only.

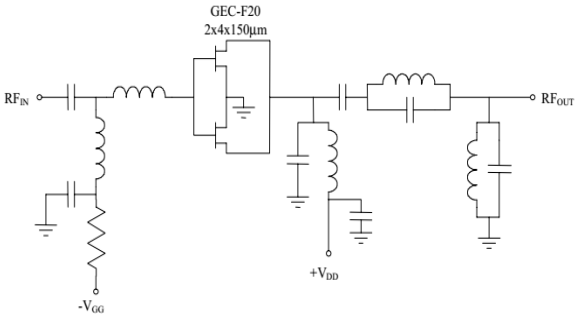

Figure 5: Schematic circuit of MMIC GaAs PA [13]

GaN HEMT technology is also used in [14,15,17,19]. Figure 6 shows a proposed high efficiency 2.45 GHz class F PA [14]. Two LC matching networks are applied to meet the impedances requirement of the circuit. The PAE obtained is 74.5% with 21.21 dBm of P_{out}. However, as a trade-off for its high efficiency, the gain achieved is quite low which only 9.21 dB.

In [15], a harmonic circuit (HCC) is implemented to provide short impedance for the control harmonic frequency to avoid any disturbances to occur. As shown in Figure 7, the proposed circuit delivers a P_{out} of 32.3 dBm. However, it achieves the minimum result of PAE which is only 35%.

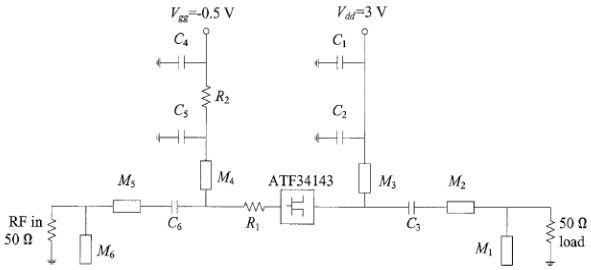

Figure 6: Schematic circuit of the 2.45 GHz PA [14]

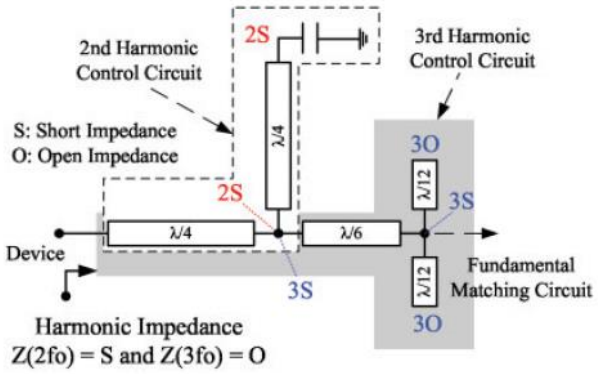

Figure 7: Proposed HCC of the class F PA [15]

Proposed PA design in [16,18] also implemented CMOS technology. The schematic circuit of [16] is shown in Figure 8. The number of harmonic network order is carefully studied. A tapered driver is implemented in the input stage while L_3 and C_3 used as LC resonant to make the third harmonic an open circuit. As the first CMOS PA presented, this PA design achieved 38% of PAE and 13.9 dB gain at 1.2 V supply voltage. The disadvantage of this PA is due to its low P_{out} which is only 12.4 dBm.

The use of capacitor in series and shunt inductor increase the complexity and efficiency of class F PA in [17], while in [18], two stage cascode class F PA is proposed to improve gain and linearity. Figure 9 shows the proposed PA that made up of three important stages to provide ample power gain and efficiency. The first stage (pre-amplifier stage) consist of four transistors in parallel with simple Cin and Lin used as input matching to reduce the resistance, thus produce high efficiency. Meanwhile, twelve parallel transistors are arranged in the second stage known as the amplifier stage to reduce the switch on-resistance. The final stage is the output stage. C1 and C2 act as DC blocking capacitors while two parallel LC networks, L3 and C3 act as a resonant. The fundamental frequency is resonated by L4 and C4. The simulation resulted in 60% of PAE, 12 dBm of P_{out} and 21.83 dB of maximum gain. As reference, the proposed PA design has the highest efficiency among CMOS class F PAs through simulation.

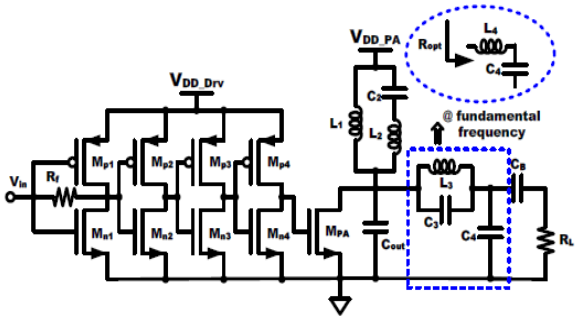

Figure 8: Schematic circuit of proposed Class F PA [16]

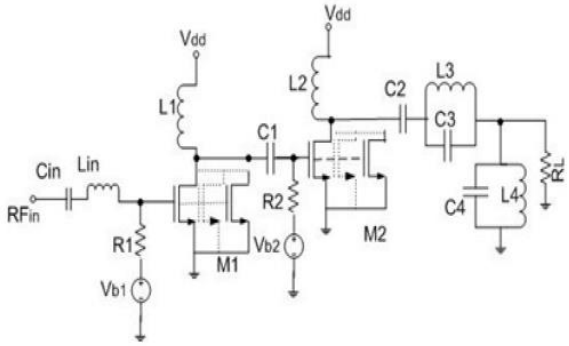

Figure 9: Schematic circuit of proposed CMOS two stage Class F PA [18]

B. Transmission Lines

The transmission line is another technique implemented in class F PA design. Transmission lines in the input/output networks allow the realization of the circuit to meet the essential impedance at the second harmonic of the circuit. [14]. Therefore, by using transmission line, an ideal class F PA with all even and odd harmonic terminations may achieve efficiency up to 88.4%. An earlier research of class F PA uses the transmission line for 900 MHz applications.

In 2001, the proposed PA implemented CMOS technology and transmission lines as the load matching network [20]. The output matching network is considered the most important block in the design as it must convert into 50 Ω of impedance. The schematic circuit of proposed PA is shown in Figure 10. This design used the bondwire inductor L_O with 0.7 nH/mm length to match the network. C_{D1} and C_{D2} capacitors provide an optimum termination for its second harmonic tuning while feedback resistor R_{G2} stabilized at lower frequencies. At 1.9 GHz frequency, 42% of PAE and 22.5 dBm of P_{out} are achieved. However, in this design, the supply voltage of 3 V used is considered large with only 10.5 dB of gain. Based on the performance, it shows the possibility to design a low voltage PA with CMOS technology for future work.

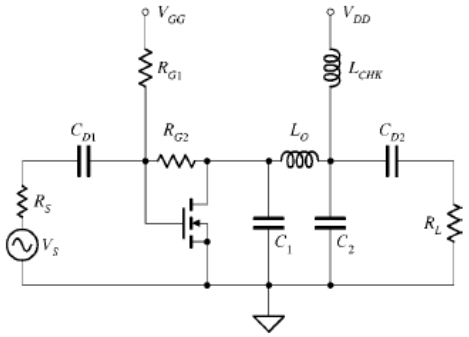

Figure 10: Schematic circuit of 1.9 GHz CMOS PA [20]

Proposed PA in [21] used two bondwires as the output matching network shown in Figure 11 to give minimum even harmonic impedances at the drain while maximum real impedance at the third harmonic is given at fundamental R_L. This further effectively eliminates the harmonics up to fourth order harmonic. In this design, the PA achieved 15.8 dB of gain, 81% of PAE and 40.8 dBm of P_{out} for 2.0 GHz frequency.

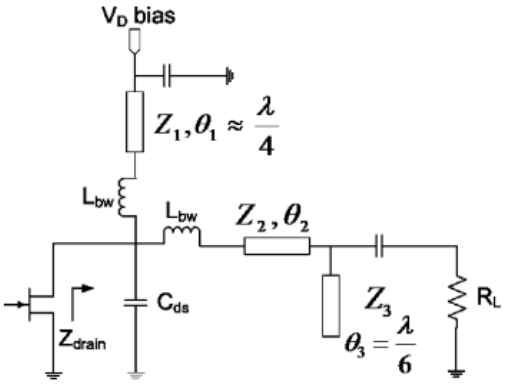

Figure 11: Output matching network of proposed PA [21]

Several PA designs has been proposed for 2.14 GHz application [22-24]. In [22], a technique known as Composite Right/Left Handed Transmission Line (CRLH-TL) is applied as harmonic trap. This technique is a combination of two capacitors (LC) in series and a shunt inductor (LL) valued 1pF and 2.7nH, respectively. Figure 12 shows the schematic circuit of the presented PA. The input of second harmonic termination comprises of the series TLs (λ/12) and shunt open stub (λ/8). The internal parasitic components are recompensed to obtain output power and efficiency. A maximum efficiency of 70.9% is obtained at a P_{out} of 40.2 dBm.

Meanwhile, the first concurrent dual band class F PA that implemented transmission lines are presented in [23]. Multiband load coupling using transmission lines able to tune the harmonics at two different frequencies. Figure 13 shows the final schematic of the proposed PA where an optimum dual-band matching networks are designed to keep pace with both frequencies. Four resonators are used where to adjust the length of stubs named TL_{1-7}. Thus, the PA achieves 32.8 dBm of P_{out} and 31.1 % of PAE at 1.7 GHz, while 34.4 dBm of P_{out} and 50% of PAE at 2.14 GHz, respectively.

In comparison with [21-23], the proposed 2.14 GHz class F PA in [24] implemented harmonic traps in the input/output matching networks. The blocking capacitance, the second and the third order harmonics tuning were applied in the output network to boost the efficiency and output power. The proposed class F PA achieved a high PAE of 75.8%. However, the PA design implemented an off-chip output matching and needs more harmonic traps which lead to decrement in overall PA performance. Besides, all proposed PAs in [21-23] achieved low gain.

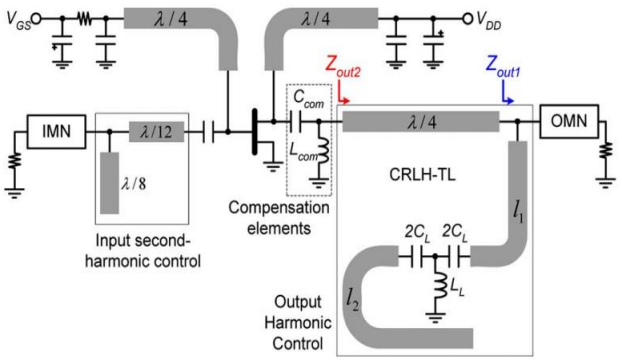

Figure 12: Schematic circuit of proposed class F PA [21]

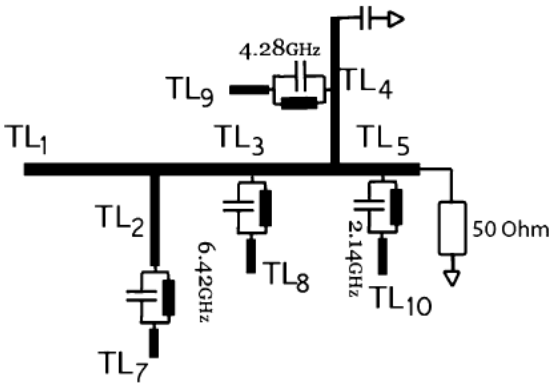

Figure 13: Schematic circuit of proposed dual band PA [23]

Figure 14 shows another proposed two stage cascode CMOS PA [25]. The proposed 2.4 GHz PA is composed of two cascade stages with input and output matching networks. transistors M_{1-4} are arranged in cascode to provide high gain and good isolation to the circuit. Multiple bondwires are used to eliminate noise, reduce power consumption, remove the parasitic capacitance of input stage and enlarge the operating bandwidth. Meanwhile, T_{L1-2} are quarter-wavelength transmission lines that used to ensure rectangular output voltages. A rectangular output voltages will lessen the overlap percentage between the voltage and current. Thus, power efficiency increases. The proposed class F PA obtained a PAE of 52.84 % and 20.7 dBm of P_{out}.

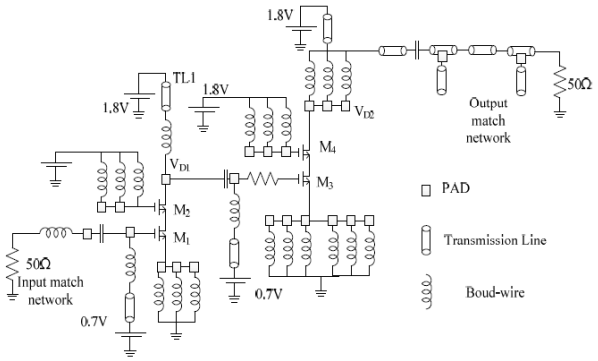

Figure 14: Full schematic of proposed PA [25]

Higher PAE is achieved for proposed PA that performed harmonic termination more than third order [26-28]. In

2014, concurrent dual band PAs are proposed in [29-31]. Figure 15 shows the proposed schematic design for 2.1 and 2.6 GHz frequencies [29]. The PA achieved 36.7 dBm of P_{out} and 72% of PAE at 2.1 GHz while at 2.6 GHz achieved 37.1 dBm of P_{out} and 62% of PAE. On-chip parasitic components, bonding wires and load-pull/source pull technique are performed for optimum efficiency. However, the PAE degraded as the frequency increases due to impedance loss.

In [30], a highly efficient class F PA is proposed with single band at 5.5 GHz and dual band at 5 and 12.0 GHz. Figure 16 shows the schematic circuit of 5.5 GHz PA while Figure 17 shows the schematic circuit for 5 and 12.0 GHz PAs. The number of harmonics is terminated using the harmonic termination network in the input and output of PA, resulting in 70% of PAE and 27.5 dBm of P_{out} are achieved in 5.5 GHz PA. Meanwhile, the 5 and 12.0 GHz PA 58% and 51% of PAE and 28.0 and 26.7 dBm of P_{out} respectively. The gain achieved for 5.5 GHz PA is only 13.7 dB while the dual band PA achieved 12.0 dB and 10.3 dB. However, the proposed PAs are not suitable for low frequency WiMAX application.

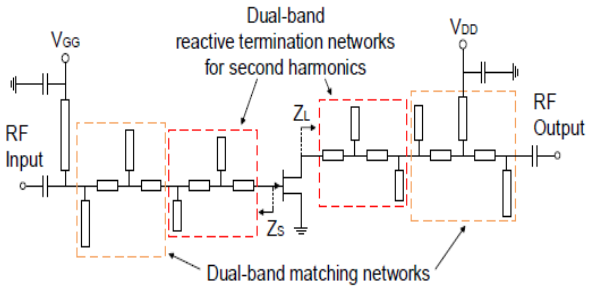

Figure 15: Concurrent dual band 2.1 and 2.6 GHz schematic circuit [29]

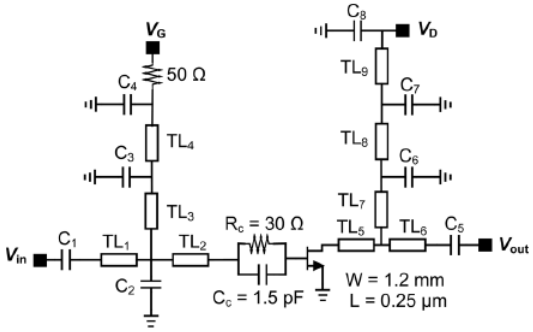

Figure 16: Schematic circuit of proposed 5.5 GHz PA [30]

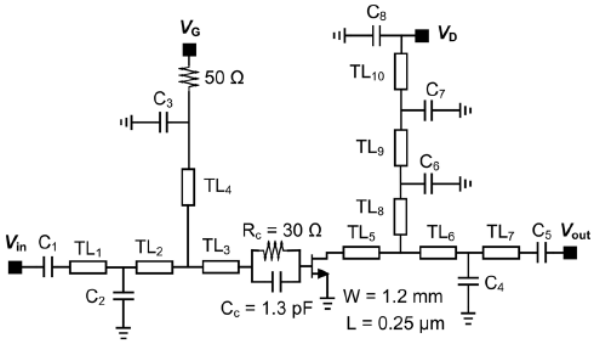

Figure 17: Schematic circuit of 5.0 and 12.0 GHz PA [27]

The implementation of transmission lines or bondwires are gaining interest for a highly efficient and high output power in a PA design. However, the length of transmission lines in matching networks of each harmonic is controlled by selecting reasonable values to ensure they are fit for an on-chip PA [32-34].

C. Load-pull/Source-pull

Load-pull/Source-pull technique is an emerging trend for high efficient and good performances in a PA design. A load-pull/source pull technique or system allows the active device to perform in various conditions to match the input/output network. This technique is implemented in [35] to determine the optimum harmonic loads at the first three harmonic frequencies.

Referring to Figure 18, the harmonic loads are set to 50 Ω except for the output of second and third harmonic load ZL_2 and ZL_3. Source impedance ZS_1 are altered at each simulation point to obtain a conjugate match of the input impedance. An essential load–pull simulation is done before performing load-pull simulation for ZS_2. Optimum values of other harmonic loads such are $ZL_{1\text{-}3}$, and ZS_3 are fixed. Short length open stub is available for the third harmonic load while ZS_3 is let to be open by both input configurations which leads to result in good input/output matches. The PA is designed using pHEMT technology and obtained 76% of PAE and 13 dB of gain.

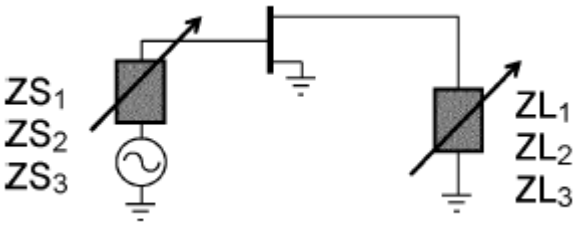

Figure 18: Load-pull/Source-pull circuit [35]

Another class F PA with load-pull/source pull technique is presented in [36]. The schematic circuit of proposed PA is shown in Figure 19. The proposed PA implemented cascode stages to generate distortion in the drain current of the transistor as an alternative to the usual sinusoidal waveforms. Instead, it is used to switch the transistor in the input driver while a push-pull configuration is added to the second stage of the input drive. The high knee voltage of CMOS technology resulting the transistor stress to decrease as the voltage of drain to gate is lower. Thus, the reliability of the RF PA increases. By using 3V voltage supply, the proposed PA is capable to deliver 49.59 % of PAE at 2.4 GHz frequency. However, only 19.3 dBm of output power is delivered.

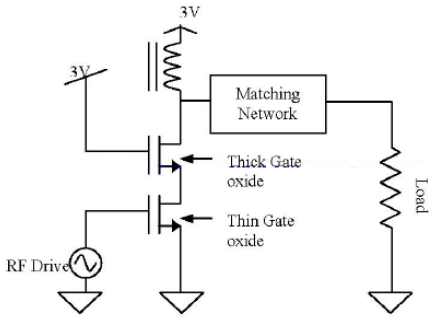

Figure 19: Schematic circuit of proposed PA with cascode stage [36]

In [38], only the fundamental and the first two harmonics were considered to improve efficiency and simplicity of the proposed PA design. Optimum impedance for the matching networks are verified through load-pull and source-pull simulations. Thus, the proposed PA which is shown in Figure 20 achieves a high efficiency. The matching input/output networks are made up of sub-matching networks and harmonic trap circuits for the harmonics present in the circuit. Optimum impedances are provided by five open circuit shunt stubs, S1 to S5 which are implemented to the input/output harmonic traps. A series RC circuits helps to stabilize the PA while T1 and T2 act as tuning transmission lines to compensate the parasitic effects from the GaN HEMT. This lead to an optimized source and load impedances. At 2.0 GHz, a PA with PAE of 80.1 % and P_{out} of 40.7 dBm are achieved.

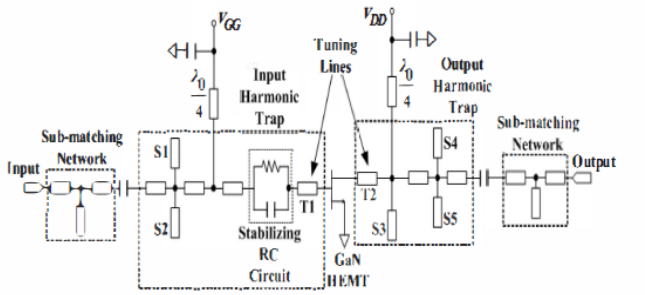

Figure 20: Schematic circuit of 2.0 GHz PA [38]

Class F PA design also implement load-pull/source-pull technique for high frequency application [37,39]. This technique helps to reduce the parasitic impact on the transistor. Therefore, it is suitable for microwave power transmission. Meanwhile, when it is presented in low frequency PA, the designs are too complex and large, making only the final combination of the schematic circuits are shown [40-42].

IV. Summary of Findings

In general, class F PA design is about achieving as flat as possible the voltage and current waveforms through open or short circuits in the matching networks. These waveforms can be achieved by modifying the values of each harmonics present in the PA to its optimum to increase overall efficiency and reduce power dissipation in the transistor. The order of harmonics must be selected properly as they consume more power and increase the complexity of the design. However, by eliminating the harmonics, it improves the efficiency. Class F PA with lumped LC load network easily switches the input/output matching networks to boost the gain and efficiency [10-19]. However, transmission line load network enhances the efficiency up to 80%, which is closer to the ideal class F operation [20-34]. Meanwhile, load-pull/source-pull technique is preferable for a single-chip PA [35-42]. The difference in technology used for fabrication process does not really affecting the efficiency. Therefore, selecting a suitable technique, best possible PAE, high output power and optimum gain are challenging in designing a highly efficient class F PA. Table 1 summarizes the comparison of current class F PA performances presented in this paper.

V. Conclusion

A review of highly efficient Class F PA design technique in Gigahertz frequencies has been discussed. Class F is suitable for any frequency of wireless application PA that demands for high efficiency, sufficient gain and high output power. The number of harmonic terminations with design techniques such as load network with lumped LC elements, transmission lines and load-pull/source-pull have been considered in class F PA design. However, the highest PAE achieved in current published data is 82.9% only. Thus, a theoretical 100% ideal efficient class F PA is still not achieved. Selection of technology does not affect the efficiency of a PA at any frequencies. This is shown from the previous works on available technologies; class F PA is still drawing attention for a low-cost and efficient system-on-chip PA. The authors believe new approach in designing a high efficiency class F PA can be implemented and class F PA design is relevant for future wireless RF application.

Acknowledgment

This work was supported by University Malaysia Sarawak and Ministry of Higher Education Malaysia via Fundamental Research Grant Scheme (FRGS).

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Table 1
Comparison of class F PA performances

Bil	Year	PAE (%)	Gain (dB)	Pout (dBm)	Frequency (GHz)	Technology
Lumped elements						
[10]	2006	50.00	10.0	38.0	2.0	GaN
		46.00	10.0	37.0	2.8	
[11]	2006	43.95	-	21.8	2.4	CMOS
[12]	2007	42.00	19.0	18.9	1.65	
[13]	2007	50.00	-	19.5	2.15	GaAs
[14]	2007	74.50	9.21	20.75	2.45	GaN
[15]	2009	35.00	-	32.30	2.14	
[16]	2011	38.00	13.9	12.4	2.4	CMOS
[17]	2013	18.38	19.57	39.57	1.7	GaN
[18]	2015	60.00	21.83	12.0	2.4	CMOS
[19]	2016	50.00	14.0	40.0	2.5	GaN
Transmission Lines						
[20]	2001	42.00	10.5	22.5	1.9	CMOS
[21]	2007	81.00	15.8	40.8	2.0	GaN
[22]	2008	70.90	11.1	41.1	2.14	
[23]	2008	31.10	-	32.8	1.7	
		50.00	-	34.4	2.14	
[24]	2011	75.80	18.0	37.6	2.14	
[25]	2012	52.84	-	20.7	2.4	CMOS
[26]	2012	79.00	-	33.3	5.65	GaN
[27]	2013	82.00	15.0	40.0	3.1	
[28]	2013	76.00	10.0	40.0	2.8	
[29]	2014	72.00	-	36.7	2.1	
		61.00	-	37.1	2.6	
[30]	2014	70.00	13.7	27.5	5.5	
		58.00	12.0	28.0	5.0	
		51.00	10.3	26.7	12.0	
[31]	2015	78.00	-	40.5	1.7	
		77.10	-	39.8	2.14	
[32]	2015	34.40	28.6	28.0	2.5	
[33]	2015	64.00	-	50.4	2.45	
[34]	2015	75.00	12.5	31.77	2.1	
Load-pull/Source-pull						
[35]	2006	76.00	13.0	21.0	2.0	GaN
[36]	2006	49.59	-	19.3	2.4	CMOS
[37]	2010	71.40	-	33.4	5.8	GaN
[38]	2013	80.10	12.7	40.7	2.0	
[39]	2014	60.00	47.07	14.0	5.8	
[40]	2015	82.90	12.0	39.0	1.89	
[41]	2015	-	44.8	-	1.0	
[42]	2016	56.00	36.0	34.00	1.9	