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Bi-directional of a Built-in Test Circuit for Interconnect Defects in Assembled PCBs

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***Abstract*—Bi-directional of a built-in test circuit is proposed to detect open defects at inputs and output interconnects between ICs and a PCB. The test circuit is based on an electrical characteristic of an inverter gate. A test method is related to supply current which flows to the inverter by providing a test signal to the test circuit. The test signal is generated by an AC voltage signal with a DC offset voltage. The open defects which occur at the interconnects will be detected by the large supply current flows to the inverter. On the other hand, if the defects don't occur, the supply current of the inverter is almost zero. Testability of the test circuit is examined using a Spice simulation. The results show that the open defects at the interconnects can be detected and located.**

***Index Terms*—Bi-directional; PCB; Spice Simulator; IC.**

I. Introduction

Open defects may occur at inputs and output interconnects between ICs (integrated circuits) and a PCB (printed circuit board) [1-2]. It is a challenge to detect the defects, since many kinds of IC package types are assembled on the PCB.

Boundary scan test methods have been proposed to detect the open defects by modeled it with stuck-at-faults [3-5]. The defects may not be always caused by the stuck-at-faults. Thus, it is difficult to estimate correctly which logic values will be generated by the defects which caused by the open defects fully at the interconnects.

Resistance measurements have been proposed to detect the open defects [6-7]. Resistance values will increase significantly caused by the open defect. However, the small open defects are not appropriate by the measurements.

The open defects may be detected by RF impedance analyses [8-9]. The impedance values increase in response to the open defects. However, it takes a long test time to detect the defects at high frequency operations.

We have proposed a built-in test circuit to detect the open defects [10]. Only the open defects at the input interconnects can be detected by the test circuit. Since the open defects may occur at the output interconnects, the test circuit should be revised. Thus, we propose a new built-in test circuit in which the open defects at the inputs and the output interconnects can be detected and located.

II. Bi-directional of a Built-in Test Circuit

An electrical characteristic of a CMOS inverter gate is shown in Figure 1. As shown in Figure 1(b), supply current iDD of almost zero will flow to the inverter, since an input voltage of the gate Vi is either H or L level signal. If Vi is specified in Equation (1), a pMOS P1 and an nMOS N1 in

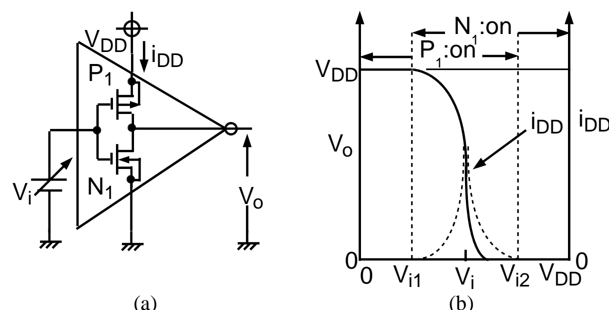

Figure 1: (a) measurement circuit; (b) DC characteristics

the gate turn on, large supply current iDD will flow to the inverter.

$$V_{i1} \leq V_i \leq V_{i2} \quad (1)$$

where V_{i1} and V_{i2} are defined in Figure 1(b). V_{i1} and V_{i2} are the minimum voltage of N_1 to be on and the maximum voltage of P_1 to be on, respectively.

A built-in test circuit *TC* is shown in Figure 2. A *TC* for an IC whose number of targeted input interconnects is *Ni* and targeted output interconnects is *Mi,* consists of (*Ni*+1) input buffers *IB*, (*Mi*+1) output buffers *OB*, a shift register *SR*, and *Ni* cells.

Each of *IB* and *OB* is made of two tristate buffers. Each *IB* is connected to an input of *SR* and to each the cell. Each *OB* is connected to an output of *SR* and to each output of a logic *core*.

The shift register *SR* is made of *Ni* D-FFs, an AND gate of two inputs, a RS-FF. *SR* is synchronized with a test clock signal *TCK* and is reset by a reset signal *RST*. An input and an output of *SR* are controlled by *IB* and *OB*, respectively.

Each of the cells consists of two multiplexers, two analog switches AS_1 and AS_2, an nMOS switch NM_1, and an inverter gate. AS_1 and AS_2, and NM_1 are made of transmission gates and a pass transistor, respectively. All switches of each the cell are controlled by each the output D-FF of *SR*. Moreover, AS_2 of each the cell is connected to a test signal T_{sig}.

T_{sig} is generated of an AC voltage signal V_{AC}, a DC offset voltage V_{DC}, a resistor R_S. Tsig is specified by Equation (2).

$$T_{sig} = V_{DC} + V_{AC} \sin(2.\pi.f_{AC}.t) \quad (2)$$

where $V_{DC} + V_{AC}$ should be in a range specified in the Equation (1) and is about half of V_{DD}. V_{AC} and f_{AC} are an amplitude and a frequency, respectively.

A test process of *TC* is shown in Figure 3. *TC* has two directions for testing all of the targeted interconnects. The directions are controlled by a test interconnect selector *TIS*. If a L level signal is provided to *TIS*, either H or L level signals are inputted to the targeted input interconnects from Di_1 to Di_{Ni} and outputted to the targeted output interconnects from Do_1 to Do_{Mi}, thus Di_1 to Di_{Ni} will be selected to be tested. On the other hand, Do_1 to Do_{Mi} will change to be tested by providing a H level signal to *TIS,* since either H or L level signals are inputted to the targeted output interconnects from Do_1 to Do_{Mi} and outputted to the targeted input interconnects from Di_1 to Di_{Ni}.

TC may select the IC works in a normal and a test mode. When a H and a L level signal are provided to test mode select *TMS*, the IC is in the normal mode and the test mode, respectively.

In the normal mode, supply current i_{DDS} of almost zero flows, since H or L level signals are outputted to each the cell from $cell_1$ to $cell_{Ni}$ to be propagated to the *core*.

In the test mode, the IC is in an initialization and to test each of the targeted interconnects. In the initialization, a L level signal is provided to *RST* and a test mode input *TMi*. To test each of the targeted interconnects, a H level signal is provided to *RST* and *TMi*.

Moreover, in the initialization, all the D-FFs of *TC* are initialized and generate L level signals from Q_1 to Q_{Ni}. AS_1 and AS_2, and NM_1 of each the cell are turned off and turned on, respectively. Supply current i_{DDS} of almost zero flows, since L level signals are generated from $cell_1$ to $cell_{Ni}$.

Further, to test each of the targeted open interconnects, a H pulse signal is generated of D-FFs from Q_1 to Q_{Ni}. AS_1 and AS_2, and NM_1 of each the cell are turned on and turned off, respectively. It is examined whether an open defect occurs at each of the targeted open interconnects.

In a defect-free IC, large supply current i_{DDS} of almost zero flows, since either H or L level signals are outputted from $cell_1$ to $cell_{Ni}$. When the open defect occurs at one of the targeted interconnects, an output cell of the targeted one is based on T_{sig}, thus, large supply current i_{DDS} flows and Equation (3) is satisfied.

$$i_{DDS} \geq i_{TH} \tag{3}$$

where i_{TH} is a threshold value and is determined by unit-to-unit variations in the defect-free IC.

An assembled PCB circuit made of one more testable designed ICs may be tested using a daisy chain style shown in Figure 4. One of two directions of the test circuit is selected by a test interconnect selector *TIS*. If a L level signal is provided to *TIS*, targeted input interconnects of the ICs will be selected to be tested. Targeted output interconnects will be selected to be tested by providing a H level signal to *TIS*. An open defect which occurs at one of the targeted interconnects can be detected by means large supply current i_{DDS} flows and the Equation (3) is satisfied.

III. Math And Equation Experimental Evaluation Using A Spice Simulation

An experimental circuit is proposed to examine testability of our built-in test circuit and is made of two ICs, *IC#1* and *IC#2*, shown in Figure 5. The ICs are designed using an SSI Spice net list library distributed by NXP Co. Ltd. Testability of the circuit is examined using a Spice simulation.

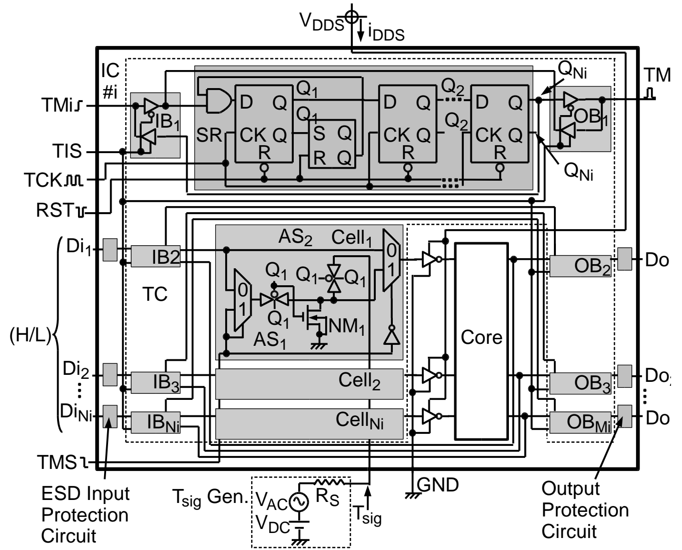

Figure 2: Bi-directional of built-in test circuit

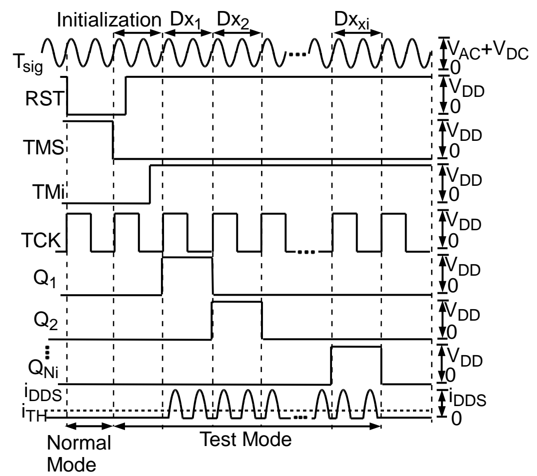

Figure 3: Test process of the test circuit

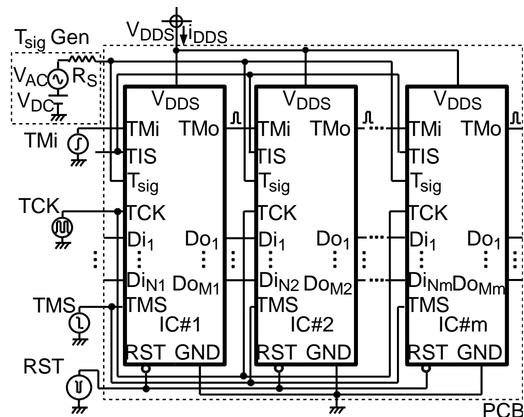

Figure 4: Daisy chain of testable designed ICs

An input interconnects of *IC#2* denoted as “*y*” is a targeted open defect. The open defect is inserted by replacing the interconnect between *x* and *y*. Supply voltage 3.3 V is provided to V_{DDS}. A parasitic *P* is inserted to each the input interconnect of *IC#2*. *P* is a parasitic resistor R_P, 0.1 Ω, and a parasitic capacitor C_P, 10 pF.

Voltages of V_{DC} and V_{AC} are 0.8 V. A resistor of R_S is 2.5 kΩ. Frequencies of *TCK* , f_{TCK}, and Di_1, f_{Di1}, are 500 kHz. Di_2 and *TMS* are provided by a H level signal and a L

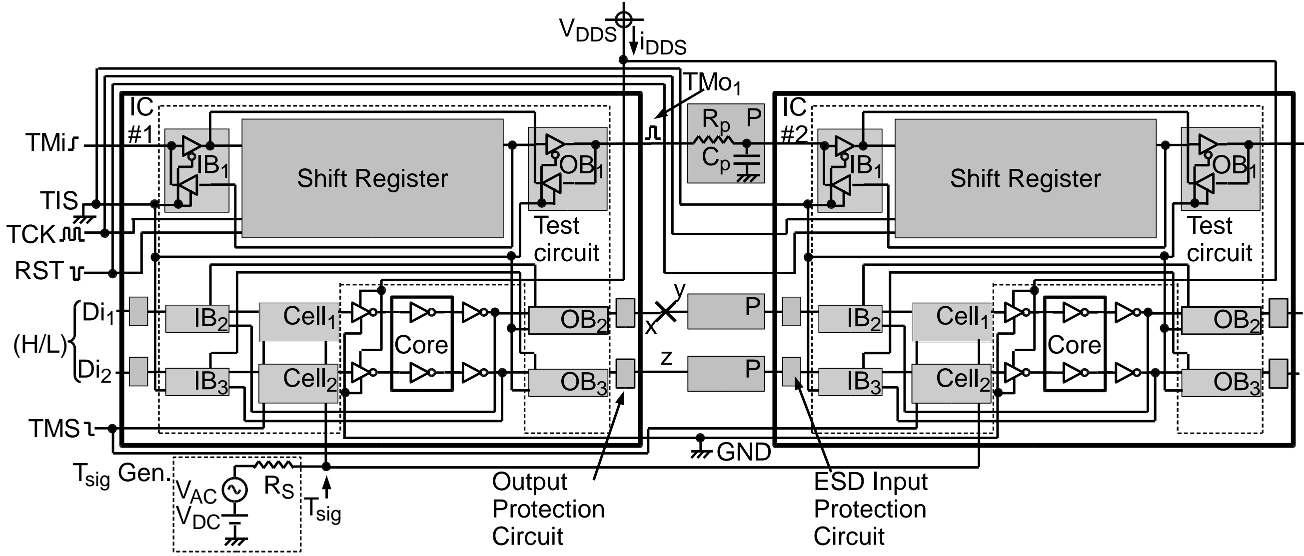

Figure 5: Experimental circuit

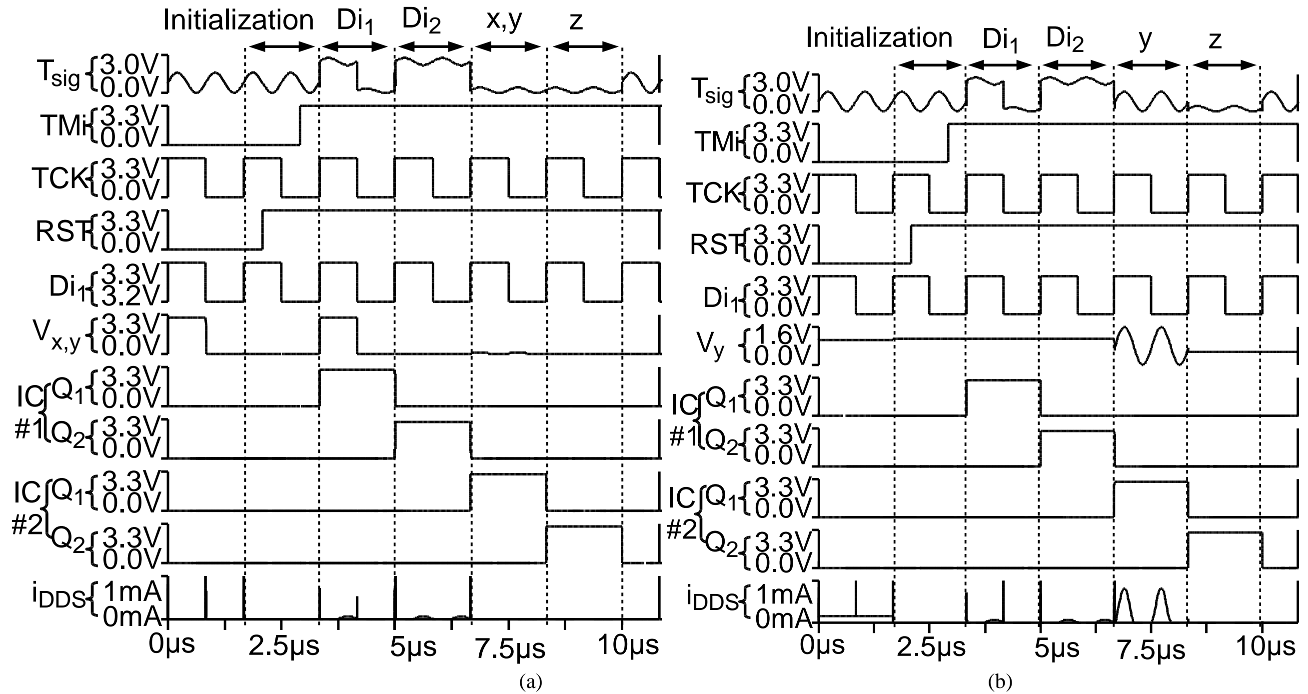

Figure 5: (a) Defect-free ICs; (b) Defective at *y* interconnect

level signal, respectively. A L level signal is provided to *TS* for selecting a direction that the input interconnects of the ICs will be selected to be tested.

Testability results are shown in Figure 6. The results show that the input interconnects of ICs can be selected to be tested by the direction. In Figure. 6(a) of defect-free ICs, large supply current i_{DDS} doesn't flow. The open defect at the targeted input interconnect can be detected and located by means large supply current i_{DDS} flows as shown in Figure. 6(b).

IV. Conclusion

A conclusion to review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions. Bi-directional of a built-in test circuit was proposed to detect open defects at inputs and output interconnects between ICs and a PCB. Directions of the test circuit is used to select which the interconnects will be tested. Testability of the test circuit is examined using a circuit simulation of a Spice simulator. The results show that the interconnects will be selected to be tested by the directions. Furthermore, the open defects can be detected and located by the test circuit.

It remains as a future work to examine testability of resistive open defects and test speed by the test circuit.

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