Implementation of Taguchi Modeling for Higher Drive Current (I_{ON}) in Vertical DG-MOSFET Device

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***Abstract*—Vertical Double-Gate (DG) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is capable to minimize various short channel effect (SCEs) problems. Vertical DG-MOSFET is constructed by having two gates that are able to control the channel from both sides and has better electrostatic control over the channel. Meanwhile, the drive current (I_{ON}) should be maintained above 0.2mA in order to decide the driving capability of the device. The drive current (I_{ON}) must be set at high value so that the transistor acquires superb driving characteristics that are capable to switch the device into on-state condition. This paper describes the design of a vertical DG-MOSFET, while keeping the drive current (I_{ON}) as maximum as possible, by utilizing both SILVACO TCAD software and statistical methods. Based on the ANOVA method, factor E (Halo Implant Energy – 45%), factor F (Halo Implant Tilt – 22%) and factor L (Compensation Implant Energy – 15.78%) were recognized as the most significant factors. The maximum value of drive current (I_{ON}) was observed to be at 0.3291 mA/µm with signal-to-noise ratio of -10.00dB.**

***Index Terms*— Analysis of Variance, ATHENA, ATLAS, MOSFET, Taguchi.**

I. INTRODUCTION

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is always regarded as the key component in RF, high frequency and high efficiency switching mechanism in electronic industry. The FET technology was invented in 1930, about 20 years before the introduction of the bipolar transistor. MOSFETs had been invented in the mid 70's and until now, research about MOSFET devices has been conducted globally. Nowadays, millions of MOSFET transistors are integrated in the advanced electronic devices, ranging from the microprocessor to random access memory (RAM).

Double-gate (DG) Metal Oxide Semiconductor Field Effect transistor (MOSFET) has been extensively studied since the last couple of years. One of the popular types of double-gate MOSFET was known as the Vertical DG-MOSFET. The basic architecture of Vertical DG-MOSFET consists of a silicon ridge of a few tenth of nanometer in thickness, and it was regarded as the active area of the MOSFET [1]. The channel length of the Vertical DG-MOSFET was normally adjusted by ion implantation and diffusion techniques. The advantage of the vertical DG-MOSFET is that the channel length is not dependent on the use of lithography. It can also be easily fabricated with both the front and back gates aligned together [2]. The main advantage of this architecture is its high possibility in reducing short channel effect (SCEs).

The main focus of this research is to optimize the drive current (I_{ON}) of vertical DG-MOSFET as the requirement for various switching mode application. A higher drive or on-state current (I_{ON}) could be gained by constructing the silicon pillar that separates the two gate electrodes. A silicon pillar of the vertical double-gate structure might be one approach, but the fabrication of the source/drain contact requires complicated processing. Moreover, the MOSFET performance might deteriorate from the depletion isolation effect., To overcome this problem, nitride barriers are developed near the source/drain junction edge

The main approach to obtain a higher value of drive current (I_{ON}) is by investigating various input process parameters of the device. MOSFET process invariability, such as the dopant concentration, temperature, rotation and etc. may contribute a significant impact on the output response of the device. By altering the dose, energy and tilt angle of this implant may change the profile and characteristic of the MOSFET device. In the design of devices with deep sub-micron technologies, the analysis of variability has become a very important tool to predict the response variation very early in the design cycle due to process parameter spreads [3].

Statistical modeling is one of the important tools to identify the input process parameters that contribute to the most impact on the MOSFET device characteristics. The optimization of manufacturing operations and products is one of the vital industrial functions to improve the product performance as well as to save manufacturing cost. Many researchers have proposed methods to adjust the threshold voltage (VTH), sheet resistance (Rs) and other response characteristics. Statistical methods are often carried out to optimize the process parameter variation. For example, Monte Carlo analysis is widely used to analyze parameter variability to generate response distributions. Although this method would produce very accurate analysis, it is still not efficient when dealing with a large number of variables.

One of the systematic and efficient ways to achieve an effecient analysis is to use an optimization method of

designing experiments based on Taguchi Methods. Taguchi Method provides one of the most efficient and reliable solutions in such cases with minimal experimental trials. Taguchi suggests a method of analyzing signal-to-noise ratios (S/N) using conceptual approach that involves graphing the effects and visually identifying factors that lead to the significant factors.

In this paper, Taguchi method was realized to be an important tool for identifying input process parameters, whose variability would impact most on the device characteristic. Taguchi method has become a powerful tool for improving productivity during research and development [4]. This is because the Taguchi method is a systematic application of design and analysis of experiments for the purpose of designing and improving product quality at the early or simulation design stage. A large number of experiments have to be carried out when the number of the input process parameters increases. To solve this task, the Taguchi method uses a special design of orthogonal arrays to study the entire process parameter space with only a small number of experiments [5, 6].

II. Material and Methods

A. N-channel Vertical DG-MOSFET Design

P-type silicon with <100> orientation was used as the main substrate for this experiment. Initial silicon was then being injected by boron with concentration of 1 x 10^{15}atom/cm^3. The silicon was etched in order to form a pillar or ridge that separated the two gates. The simulation process was followed by the gate oxidation process. The thickness of gate oxide was a parameter in vertical dimension that can determine the gate control. The next step was to dope a substrate ion which was injected with a boron into the silicon with a concentration of 9.55 x 10^{12}atom/cm^3. This was important in order to adjust the threshold voltage of the Vertical DG-MOSFET.

The next simulation process was to deposit polysilicon on top of the gate oxide. A layer of oxide was oxided on top of polysilicon deposition. Then, the polysilicon and polysilicon oxide were etched away to form a gate polysilicon. The gate was made of polysilicon due to its ability to prevent source/drain ions from penetrating into the channel region. Phosphor dosage of 1 x 10^{18} atom/cm3 was then doped into the polysilicon gate. This was done in order to increase the conductivity of polysilicon since polysilicon is a low conductivity metal. The conductivity of gate would affect the switching frequency of the transistor.

In order to get an optimum performance for the Vertical DG-MOSFET device, indium was doped. Halo implantation was conducted, followed by the depositing of sidewall spacers. Sidewall spacers were used as a mask for source/drain implantation. They were used to separate the gate with a source/drain metal to prevent them from being short-circuited due to the frequent occurance of the process variation in the fabrication process. Arsenic atom with a concentration of 1.25 x 10^{18} was implanted to ensure smooth current flow in the Vertical DG-MOSFET device.

Compensation implantation was utilized later by implanting phosphor dosage of 2.51 x 10^{12} atom/cm3. This step was taken in order to reduce parasitic effects that could lower the current. This transistor was then connected to the aluminum metal. The aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD), and unwanted aluminum was etched to develop the contacts [7, 8]. The procedure was completed after the metallization and etching were performed for the electrode formation, and the bonding pads were opened.

Once the devices were built with ATHENA, the complete devices can be simulated in ATLAS to provide specific characteristics, such as the sub-threshold drain current (I_D) versus gate voltage (V_G). The drive current (I_{ON}) can be extracted from that curve.

B. Taguchi Modeling using L_{12} Array Method

The electrical characteristic for Vertical DG-MOSFET device was experimented by obtaining and controlling the value of drive current (I_{ON}). The value of drive current (I_{ON}) was recorded in order to observe the dependability of the I_{ON} on various input process parameters. The value of response, I_{ON} was used to determine the driving characteristic of the device.

Table 1 shows the process parameters and their appropriate levels for the experiment. The selected process parameters were the substrate implant dose, V_{TH} implant energy, pocket-halo implant dose, compensation implant energy and etc. For Taguchi design method, two noise factors, gate oxide temperature and polysilicon oxidation temperature were used. These noise factors were differentiated in two levels in order to obtain four readings of V_{TH} for every row of experiment. The values of noise factors at different levels were listed in Table 2. Using the Taguchi method, the L_{12} (2^{11}) orthogonal array has eight experiments. The experimental layout for the process parameters using the L_{12} (2^{11}) orthogonal array is shown in Table 3.

Table 1
Input Process Parameters of Vertical DG-MOSFET device [9]

Sym.	Process Parameter	Units	Level 1	Level 2
A	Substrate Implant Dose	atom/cm^3	1x10^{15}	1.03x10^{15}
B	V_{TH} Implant Dose	atom/cm^3	9.55x10^{11}	9.58x10^{11}
C	V_{TH} Implant Energy	kev	10	12
D	Halo Implant Dose	atom/cm^3	1.17x10^{13}	1.20x10^{13}
E	Halo Implant Energy	kev	170	172
F	Halo Implant Tilt	degree	24	27
G	S/D Implant Dose	atom/cm^3	1.25x10^{18}	1.28x10^{18}
H	S/D Implant Energy	kev	45	47
J	S/D Implant Tilt	degree	80	83
K	Compensation Implant Dose	atom/cm^3	2.51x10^{12}	2.54x10^{12}
L	Compensation Implant Energy	kev	63	65

Table 2
Noise factors of Vertical DG-MOSFET device [9]

Sym.	Noise factor	Units	Level 1	Level 2
U	Gate Oxidation Temp	C°	930	933
V	Poly Oxidation Temp	C°	830	833

Table 3
Experimental Layout using L_{12} Orthogonal Array [10]

Exp. No.	Process Parameter Level										
	A	B	C	D	E	F	G	H	I	J	K
1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	2	2	2	2	2	2
3	1	1	2	2	2	1	1	1	2	2	2
4	1	2	1	2	2	1	2	2	1	1	2
5	1	2	2	1	2	2	1	2	1	2	1
6	1	2	2	2	1	2	2	1	2	1	1
7	2	1	2	2	1	1	2	2	1	2	1
8	2	1	2	1	2	2	2	1	1	1	2
9	2	1	1	2	2	2	1	2	2	1	1
10	2	2	2	1	1	1	1	2	2	1	2
11	2	2	1	2	1	2	1	1	1	2	2
12	2	2	1	1	2	1	2	1	2	2	1

III. Analysis of Vertical N-channel DG-MOSFET Device

The electrical characteristics result derived from the first set of experiment was done by using **ATHENA** and **ATLAS** module. The optimization result of the device utilized using Taguchi method approach will be shown in this section.

Fig. 1 depicts the doping concentration across the N-channel vertical MOSFET transistor. The figure also shows the doping level of silicon, silicon dioxide, polysilicon, silicon nitride and aluminum. Doping concentration is used to determine the electrical characterization of the transistor [10]. A good doping concentration will ensure the transistor to work well with excellent drive current control and fewer leakages current [11].

Fig. 2 shows the graph of sub-threshold drain current (I_D) versus gate voltage (V_G) at drain voltage V_D = 0.05V and V_D = 1.0V for Vertical DG-MOSFET device. The value of off-leakage current (I_{OFF}) and drive current (I_{ON}) can be extracted from the graph.

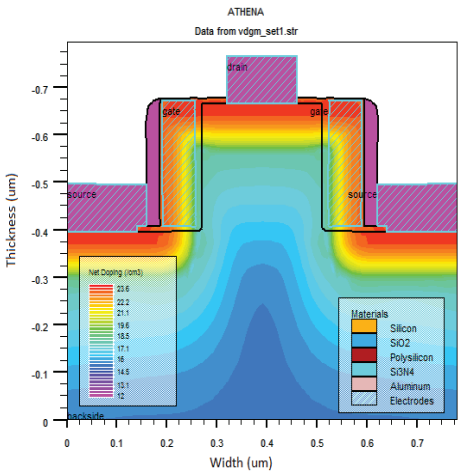

Figure 1: Contour Mode of Vertical DG-MOSFET device

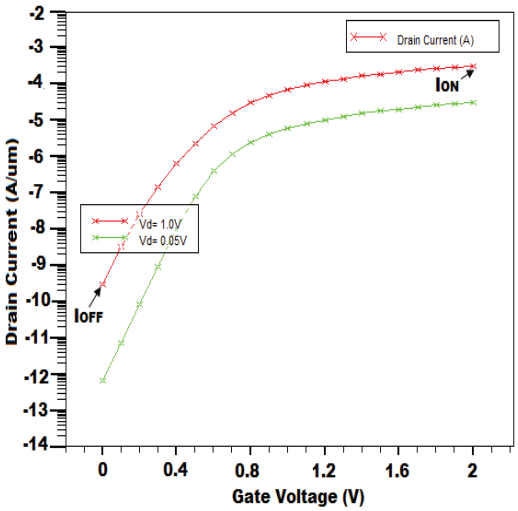

Figure 2: Graph of sub-threshold drain current (I_D) versus gate voltage (V_G)

From the graph of Fig. 2, it was observed that the value of drive current (I_{ON}) was at 0.3159mA. Although the result was above the minimum drive current (I_{ON}) = 0.2mA, it was still recommended to achieve I_{ON} as high as possible. To realize that particular objective, variations of several input process parameters need to be set in order to obtain the maximum value of drive current (I_{ON}). It is important to note that all the input process parameters cannot be varied randomly because it will eventually affect the structure of the device. Therefore, statistical modeling is required to identify the specific process parameter variation that could result in the most significant impact on the device characteristics.

IV. Analysis of Taguchi Method

Twelve different experiments in the vertical DG-MOSFET device were performed using the design parameter in the specified orthogonal array as shown in Table 3. Several experiments were run to determine which control factor or variable contributes to the most significant effect on the output response, I_{ON}. The outcome of the experiment also provides the most recommended value or optimum value for each individual factor. There were 11 input process parameters of vertical DG-MOSFET device involved in this experiment, which were the substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, halo implant dose, halo implant energy, halo implant tilt, S/D implant dose, S/D implant energy, S/D implant tilt, compensation implant dose, compensation implant energy and each of them were represented by A, B, C, D, E, F, G, H, J, K and L.

A. Drive Current (I_{ON}) Value Acquisitions

By utilizing the TCAD Simulator, ATHENA and ATLAS, the drive-on current (I_{ON}) for each individual experiment has been acquired. The variation of the process parameter level is shown in Table 3. The final results of the experiments are as presented in Table 4.

Table 4 shows the value of drive current (I_{ON}) for each set of experiment. The desired value of I_{ON} for MOSFET device must be above 0.2mA. It was observed that all the experiment sets produced I_{ON} values between 0.2654 and 0.3220 V. Therefore, all the experiment sets were suitable for the test of drive current (I_{ON}). For each set of experiment, there were four different readings of I_{ON}. It was because of the presence of combination levels of the noise factors represented by U_1V_1, U_1V_2, U_2V_1 and U_2V_2. Drive current (I_{ON}) is also known as drain saturation current (I_{Dsat}). The high value of I_{ON} is desired in order to gain superb driving capabilities of a MOSFET device. Normally, a high value of I_{ON} will lead to a higher leakage current (I_{OFF}). Such situation can be avoided through channel engineering method, where the leakage current (I_{OFF}) is controlled by the amount of channel doping concentration.

Table 4: I_{ON} Values for N-channel Vertical DG-MOSFET Device

Exp no.	Drive-on Current, I_{ON} (mA)			
	I_{ON1} (U_1V_1)	I_{ON2} (U_1V_2)	I_{ON3} (U_2V_1)	I_{ON4} (U_2V_2)
1	0.3159	0.3139	0.2939	0.2938
2	0.3120	0.3098	0.2912	0.2910
3	0.2933	0.2913	0.2725	0.2720
4	0.2976	0.2956	0.2757	0.2758
5	0.2758	0.2737	0.2561	0.2554
6	0.2836	0.2816	0.2640	0.2635
7	0.3009	0.2989	0.2796	0.2795
8	0.2861	0.2839	0.2665	0.2657
9	0.2810	0.2789	0.2606	0.2604
10	0.3220	0.3199	0.3007	0.3004
11	0.3093	0.3072	0.2873	0.2872
12	0.2970	0.2950	0.2754	0.2750

B. Analysis of Input Process Parameters Effects on Drive Current (I_{ON})

After twelve experiments of the L_{12} (2^{11}) array had been done, the next step was to determine which control factor would give the most significant impact on the output response, I_{ON}. Signal-to-noise (S/N) ratio was utilized in order to determine the optimal input process parameters and analyze the experimental data. There are three categories of the performance characteristics in the analysis of the S/N ratio, which are known as the lower-the-better, higher-the-better and nominal-the-better [12]. The S/N ratio for each level of process parameters is computed based on the S/N analysis. Regardless of the type of the performance characteristic, the larger S/N ratio is always to be recognized as the better performance characteristic [13, 8].

In this research, the drive current (I_{ON}) of the vertical DG-MOSFET device is categorized to the larger-the-best quality characteristics. The larger-the-best quality characteristic is continuous and nonnegative. The purpose of this category is to maximize the output response. The S/N ratio analyses are implemented in order to maximize the drive current (I_{ON}) value as large as possible.

The S/N ratio (larger-the-best), η can be expressed as [4]:

$$\eta = -10\log_{10}\left[\frac{1}{\eta}\sum_{i=1}^{\eta}\frac{1}{y_i^2}\right] \quad (1)$$

While n is the number of tests and Y_i is the experimental value of the drive current. The S/N ratios (larger-the-best) for the device were computed and recorded in Table 5 [4]. The effect of each input process parameter on the S/N ratio at the different level was separated because the experimental design is orthogonal. The S/N ratio (SNR) for each of the process parameters is summarized in Table 6.

Basically, the larger the S/N ratio, the quality characteristic for drive current (I_{ON}) is better [5]. The higher the quality characteristic value to the target, the better the device quality will be [14].

Table 5: Mean sum of SQ and S/N ratios for I_{ON}

Exp no.	Mean Sum of SQ	S/N Ratio (larger-the-Better) (dB)
1	1.08E1	-10.35
2	1.11E1	-10.44
3	1.26E1	-11.00
4	1.23E1	-10.88
5	1.43E1	-11.54
6	1.34E1	-11.29
7	1.20E1	-10.78
8	1.32E1	-11.21
9	1.37E1	-11.38
10	1.04E1	-10.17
11	1.13E1	-10.54
12	1.23E1	-10.90

C. Analysis of Variance (ANOVA)

The analysis of variance (ANOVA) is a common statistical method used to investigate which of the input process parameters significantly affect the performance characteristic [15]. Technically, ANOVA is defined as the decomposition of variance which acts as a tool to obtain a better feel for relative effect of the different factors. ANOVA is also required for estimating the error of variance for the factor effects and the variance of prediction error.

Table 6: S/N Responses for Drive Current (I_{ON})

Sym.	Process Parameter	S/N ratio (larger-the-best)		Max - Min
		Level 1	Level 2	
A	Substrate Implant Dose	-10.92	-10.83	-0.09
B	V_{TH} Implant Dose	-10.86	-10.89	-0.03
C	V_{TH} Implant Energy	-10.75	-11.00	-0.25
D	Halo Implant Dose	-10.77	-10.98	-0.21
E	Halo Implant Energy	-10.59	-11.15	-0.56
F	Halo Implant Tilt	-10.68	-11.07	-0.39
G	S/D Implant Dose	-10.83	-10.92	-0.09
H	S/D Implant Energy	-10.88	-10.87	-0.01
J	S/D Implant Tilt	-10.88	-10.86	-0.02
K	Compensation Implant Dose	-10.88	-10.87	-0.01
L	Compensation Implant Energy	-11.04	-10.71	-0.33

Basically, ANOVA utilizes parameter called as the sum of squares (SS), degree of freedom (DF), variance, F-value and percentage of each factor [16]. The variance (mean square) of the tested process parameter is defined as [4];

$$MS = \frac{SS}{DF} \quad (2)$$

In order to determine the significant level of process parameters with respect to the variance of all process parameters, F-value is computed. Basically, F-value is defined as the ratio between variance of factors effects and variance of error term. When the variance of error is zero, the F-value of all factors cannot be determined. Then, the variance of the error can be merged with another smaller factor variance to calculate a new error variance which can be used to achieve more accurate results. The process of disregarding an individual factor's contribution, and then subsequently adjusting the contribution of the other factor is known as pooling. The results of **ANOVA** for the vertical DG-MOSFET device are shown in Table 7.

Table 7
Results of ANOVA for Vertical DG-MOSFET Device

Sym.	Process Parameter	DF	SS (10^{-3})	MS (10^{-3})	F-value	Factor effect on SNR (%)
A	Substrate Implant Dose	1	8.2	8.2	-	1
B	V_{TH} Implant Dose	1	1	1	-	0
C	V_{TH} Implant Energy	1	62.6	62.6	22	9
D	Halo Implant Dose	1	44.2	44.2	16	6
E	Halo Implant Energy	1	313.6	313.6	112	45
F	Halo Implant Tilt	1	152.2	152.2	53	22
G	S/D Implant Dose	1	8.3	8.3	-	1
H	S/D Implant Energy	1	0.2	0.2	-	0
J	S/D Implant Tilt	1	0.4	0.4	-	0
K	Compensation Implant Dose	1	0.2	0.2	-	0
L	Compensation Implant Energy	1	109	109	39	15.78

According to these analyses, the most dominant factors for S/N ratio were factor E (Halo Implant Energy=45%), factor F (Halo Implant Tilt=22%) and factor L (Compensation Implant Energy =15.78%). Therefore, these factors should be set at 'best setting'. Factor C (V_{TH} Implant Energy=9%) and D (Halo Implant Dose=6%) were considered to be the significant factor, and they were not recommended to be changed. Meanwhile factor A, B, G, H, J and K were considered as the neutral or negligible factors. Therefore, they do not contribute any significant effect on the output response. In contrast with the nominal-the-best analysis, there is no calculation on factor effect on means. The percentage factor effect on S/N ratio indicates the priority of a factor (process parameter) to reduce variation.

The chart factor effect of I_{ON} for vertical DG-MOSFET device is shown in Fig. 3. The chart shows the type of control factor versus their corresponding signal-to-noise ratio in dB. The chart factor effect determines which level of individual input process parameters possess the highest signal-to-noise ratio. Only the highest level S/N ratio of each individual process parameter has been selected for the best setting of the design.

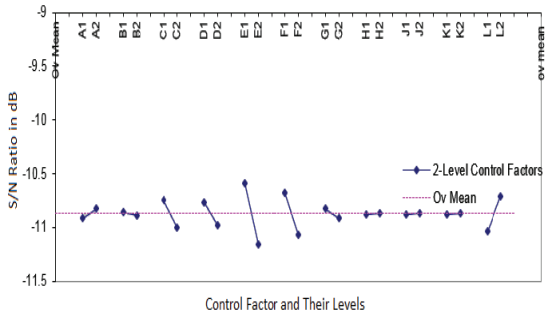

Figure 3: Chart Factor Effects

From Table 7, it was observed that factors E, F, and L were dominant while factors C and D were significant. This indicates that the level of factors E, F, K, C and D were not be changed. Factor A, B, G, H, J and K were recognized to be neutral or negligible, so any level of factor will not give any significant change on the response, I_{ON}.

In this case, all the levels of neutral factors were selected based on their highest S/N ratio. Therefore, the best level setting of process parameters is selected as A2, B1, C1, D1, E1, F1, G1, H2, J2, K2 and L2. Factor A, B, C, D, E, F, G, H, J, K and L each represented for substrate implant dose, V_{TH} implant dose, V_{TH} implant energy, halo implant dose, halo implant energy, halo implant tilt, S/D implant dose, S/D implant energy, S/D implant tilt, compensation implant dose and compensation implant energy.

D. Confirmation Test for Response, I_{ON}

The confirmation test is used to verify the estimated result with the experimental results. The best setting of the process

parameters for Vertical DG-MOSFET suggested by Taguchi Method is shown in Table 8.

Table 8
Best Setting of the Process Parameters for I_{ON}

Symbol	Process Parameter	Units	Best Value
A	Substrate Implant Dose	C^o	$1.03x10^{15}$
B	V_{TH} Implant Dose	atom cm^{-3}	$9.55x10^{11}$
C	V_{TH} Implant Energy	kev	10
D	Halo Implant Dose	atom cm^{-3}	$1.17x10^{13}$
E	Halo Implant Energy	kev	170
F	Halo Implant Tilt	degree	24
G	S/D Implant Dose	atom cm^{-3}	$1.25x10^{18}$
H	S/D Implant Energy	kev	47
J	S/D Implant Tilt	Degree	83
K	Compensate Implant Dose	atom cm^{-3}	$2.54x10^{12}$
L	Compensate Implant Energy	kev	65

The confirmation test was required in the Vertical DG-MOSFET design because the optimal combination of parameters and their levels, i.e. as A2, B1, C1, D1, E1, F1, G1, H2, J2, K2 and L2 respectively did not correspond to any experiment of the orthogonal array. The result of the final simulation for the device is shown in Table 9.

Before the optimization approaches, the best S/N ratio (larger-the-best) was -10.17 dB at the row of experiment no. 10 as shown in Table 9. The mean sum of SQ was at 1.04E1 which was the smallest value among the others. After the optimization approaches, the S/N ratio (larger-the-best) of drive current for vertical DG-MOSFET device was -10.00 dB as shown in Table 9. These values were within the predicted range. For the S/N ratio (larger-the-best), -10.00 dB was within the predicted range S/N ratio of -9.81 to -10.20 (-10.00 ± 0.19 dB).

These results indicate that Taguchi method is able to predict the optimum solution in obtaining the vertical DG-MOSFET fabrication recipe with the largest possible drive current (I_{ON}) value. The drive current (I_{ON}) value for the device after optimization approaches was observed to be at 0.3291mA/µm as shown in Table 9. This drive current (I_{ON}) value was observed to be the highest value among all the experiments done before. Drive current (I_{ON}) is one of the important characteristics to be optimized in order to produce high quality of MOSFET device [17].

Table 9
Results of the Confirmation Experiment for I_{ON}

Drive Current, I_{ON} (mA/µm)				SNR (larger-the-best)
I_{ON1} (U_1V_1)	I_{ON2} (U_1V_2)	I_{ON3} (U_2V_1)	I_{ON4} (U_2V_2)	
0.3291	0.3270	0.3067	0.3070	-10.00 dB

V. Conclusion

In conclusion, the largest possible value of drive or on-state current (I_{ON}) in the Vertical DG-MOSFET device was successfully predicted and designed by using SILVACO TCAD's simulation software and statistical modeling. The device was initially designed by utilizing ATHENA module in SILVACO TCAD. The electrical characteristics of the device were then extracted by using ATLAS MODULE. After discovering the suitable recipe for this device, statistical modeling was implemented. Taguchi method was selected to be an optimization tool for the vertical DG-MOSFET device. Taguchi method is capable of predicting which input process parameters contribute to the most significant impact on drive current (I_{ON}). The level of significance of each input process parameter on drive current (I_{ON}) was determined by using ANOVA. Based on the ANOVA method, factor E (Halo Implant Energy=45%), factor F (Halo Implant Tilt=22%) and factor L (Compensation Implant Energy=15.78%) had been recognized as the most significant factors. The final value of drive current (I_{ON}) was observed to be at 0.3291mA/µm with signal-to-noise ratio of -10.00dB. Therefore, L_{12} Taguchi method was observed to be an effective tool to maximize electrical response, I_{ON} in the vertical DG-MOSFET device.

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