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A Modified Source Impact Ionisation MOSFET (MS I-MOS) for Low Power and Fast Switching Digital Applications

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***Abstract*—This paper presents a two-dimensional (2D) modified source n-p-n impact ionisation MOSFET, called MS I-MOS, to suppress the short channel effects and increase the on-current (I_{ON}) to off-current (I_{OFF}) ratio. The proposed device is an n-p-n I-MOS on silicon on insulator (SOI), upon which a source engineering is performed. The proposed device inherits the characteristics of bipolar I-MOS, with the advantage of reduced floating body effect and the increased I_{ON} to I_{OFF} ratio, it exhibits a lower operating voltage than that of earlier I-MOS structures. The reliability issues related to hot carrier injection in the gate oxide has also been addressed effectively in the proposed structure due to lower operating voltage.**

***Index Terms*— Avalanche; Bipolar Junction Transistor (BJT); DIBL; Impact Ionization; Modified Source; Operating Voltage; Short Channel Effects.**

I. INTRODUCTION

The restive growth in the area of metal oxide semiconductor technology has only been possible by continuous scaling of device dimension with the purpose to develop a smaller, faster and cheaper device. Consequently, the performance of the device and its functionality improves with some restraints such as effects of short channel, drain induced barrier lowering (DIBL), induced hot carriers, etc. [1]. In the presence of these shortcomings, the performance of the device is gradually vitiated.

In the recent past, many researchers concocted silicon on insulator (SOI) as a standout technology to solve the above-expressed constraints emerged due to scaling. In SOI, there is a buried oxide (BOX) layer sandwiched between two silicon substrates and act as an insulator which isolates the operational part of the device from the substrate. Thus, it upsurges the electrical performance of the device by diminishing parasitic capacitance and junction capacitance, which further lessens the power consumption of the device and extends the device efficiency [2-4]. SOI technology has amazing capacities to tackle the SCEs issue and adapt to the hawkish scaling of the device without plunging with the device performance. With the urge to enhance the device performance, the researchers thought of different structures and advancements such as TFETs, I-MOS transistors, FinFETs, etc., embedded on SOI to additionally enhance the qualities of the devices, for example, low subthreshold slope, high drive current, low leakage current and high I_{ON} to I_{OFF} ratio [5-8].

Among the structures mentioned above, I-MOS became a potential candidate to replace conventional MOSFET because of its steep subthreshold switching property [7-8]. Various modifications and improvement have also been performed on I-MOS transistors to overcome its reliability problem such as large threshold shifts, high operating voltage and damage induced by hot carrier injections (HCIs) [9-16].

In the continuation to the study on I-MOS a Bipolar I-MOS transistor was introduced by M. J. Kumar *et al.* [15], which utilizes the internal amplification process of the BJT in a MOSFET to initiate the avalanche effect and reported a breakdown voltage around 2.85 V, subthreshold slope ~ 6.25 mV/decade and I_{ON} to I_{OFF} ratio close around 10^6. Due to its internal gain mechanism, bipolar I-MOS still stands as a potential candidate among several I-MOS devices on the basis of its overall performance. Still, like every device, there is a need for some reforms in its structure to improve its performance.

With the purpose to improve the characteristics of bipolar I-MOS, we have attempted to propose an n-p-n I-MOS with a modified source (MS I-MOS). The working principle of the proposed device and mechanism to initiate avalanche effect is similar to that of conventional bipolar I-MOS. An employed modified source in the proposed device offers better performance when compared to bipolar I-MOS that exhibits a lower breakdown voltage which is the operating voltage of the proposed device with certain characteristics such as higher drive current and I_{ON} to I_{OFF} ratio. The designing and characteristics of the proposed device are discussed in the following sections of the paper.

II. DEVICE STRUCTURE

The structural view of n-p-n modified source I-MOS (MS-IMOS) transistor and the conventional bipolar I-MOS transistor that is used for comparison that is shown in Figure 1(a) and (b). The MS-IMOS is a transistor in which a lightly doped n- region (1 x 10^{17} cm^{-3}) is created below the profoundly doped n+ source region (1 x 10^{20} cm^{-3}), and the gate covered a constrained part of the p-type silicon body region toward the source. This type of source engineering lowers the overall doping concentration and reduce the parasitic capacitance at the source side. Silicon dioxide is used as a gate oxide in MS-IMOS.

All the parameters and specifications which are used to simulate the proposed device along with the bipolar I-MOS is described in Table 1, which compares the parameters of both devices.

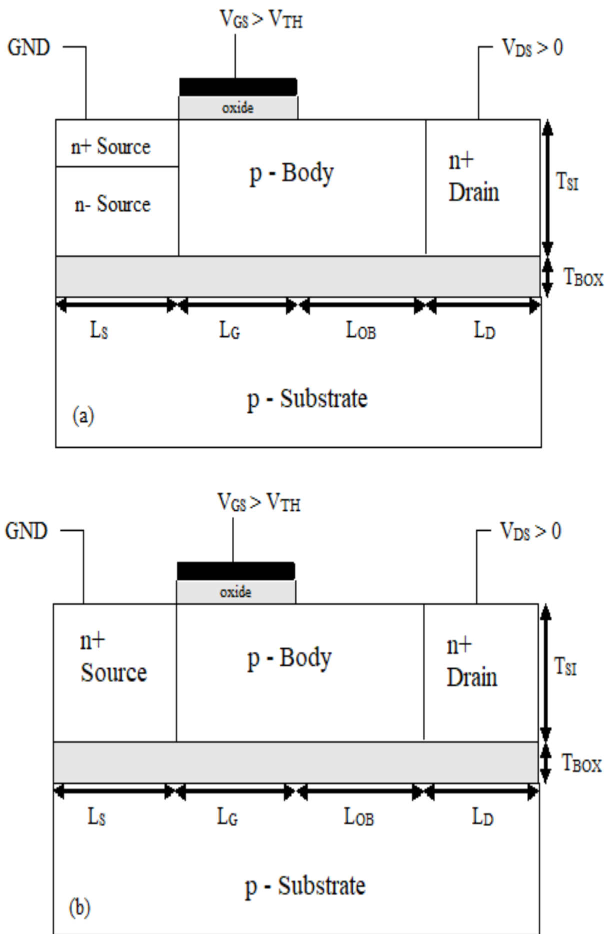


Figure 1: Diagrammatic representation of (a) MS I-MOS, and (b) Bipolar I-MOS

Table 1
Device Specifications for Bipolar I-MOS and the Proposed MS I-MOS

Parameter	Bipolar I-MOS [15]	MS I-MOS
Gate length, L_G	75 nm	75 nm
Oxide thickness, T_{OX}	1 nm	1 nm
Substrate doping	$5x10^{17}$ cm^{-3}	$5x10^{17}$ cm^{-3}
Source region doping	$1x10^{20}$ cm^{-3}	n+ $1x10^{20}$ cm^{-3} n- $1x10^{17}$ cm^{-3}
Drain region doping	$1x10^{20}$ cm^{-3}	$1x10^{20}$ cm^{-3}
BOX thickness, T_{BOX}	100 nm	100 nm
Silicon body thickness, T_{SI}	50 nm	50 nm
Open body length, L_{OB}	75 nm	75 nm
Source length, L_S	100 nm	100 nm
Drain length, L_D	100 nm	100 nm
Gate work function	4.6 eV	4.6 eV

The effect of two distinctive profile doping areas taken in the source region has already been studied on SOI MOSFET by Mishra *et al.* [17]. In the proposed device, a similar type of modification in the source region has been made keeping in mind the end goal to get low parasitic capacitances. This modification guarantees a more uniform electric field response in the area covered by the gate and to empower the device to build its drive current as per lessened off-state current, for getting the steep subthreshold slope. In this way, it helps to reduce hot carrier induced damage and hence, improves the reliability of the device. The use of fully depleted SOI (FDSOI) film in the proposed device is essential to evade floating body effects.

A device simulation tool ATLAS Silvaco [18] is utilised to confirm the conduct of the proposed device. Some specific models which are used for simulation incorporate concentration-dependent Shockley-Read-Hall (SRH) model, standard band-to-band tunnelling model, parallel electric field dependent mobility model, bandgap narrowing model, Fermi Dirac carrier statistics, Toyabe impact ionisation model [15].

III. RESULTS AND DISCUSSION

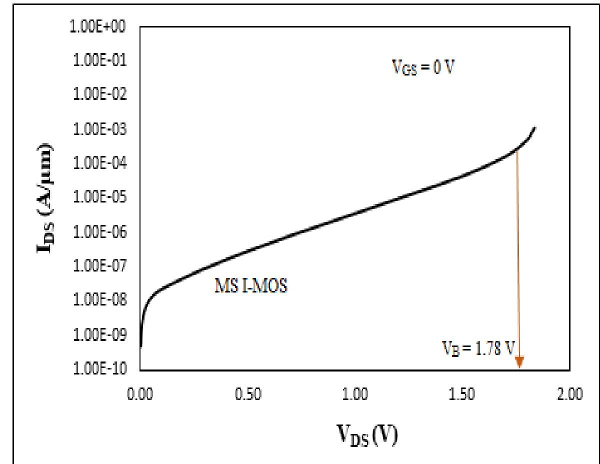


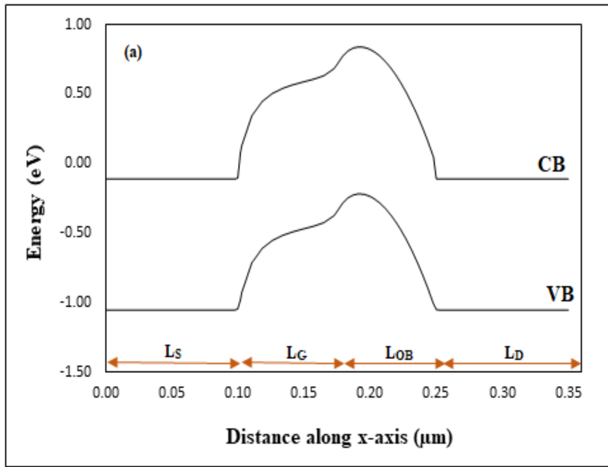
Figure 2: I_{DS}-V_{DS} characteristic of the proposed MS I-MOS transistor.

The I_{DS} versus V_{DS} graph for the proposed MS I-MOS is presented in Figure 2. The avalanche breakdown in the MS I-MOS occurs at the voltage (V_B) ~ 1.78 V, and then an abrupt rise of drain current is observed. The proposed device exhibits much lower breakdown voltage than that of aforementioned I-MOS transistors. In this way, we can state that the proposed device can work at a very low operating voltage, i.e. less than 1.78 V. Table 2 shows the Breakdown voltage comparison of proposed MS I-MOS with some of the I-MOS transistors.

Table 2
Breakdown Voltage Comparison of Proposed MS I-MOS with Previously Proposed I-MOS Transistors.

Reference no.	I-MOS transistors	V_B
[8]	p-i-n I-MOS	7.20 V
[15]	Bipolar I-MOS	2.85 V
[16]	Charge plasma n-p-n I-MOS	2.123 V
Proposed device	MS I-MOS	1.78 V

In thermal equilibrium (V_{DS}=0 V and V_{GS}=0 V) condition, the energy band diagram of I-MOS transistor examined at 2 nm beneath Silicon-insulator (SiO2) interface is shown in Figure 3(a). In this condition, the movement of electrons from source to drain region is prevented due to the presence of a high potential barrier and accordingly impact ionisation does not occur. Though, as the V_{DS} is increased from 0 to 1.75 V, decrement in the height of the potential barrier can be observed in Figure 3(b), it enables movement of electrons from source to drain region and thus, the ascent of electrons in the drain side results in reverse biasing of the drain-body junction which prompts the impact ionisation. The sudden rise of drain current as shown in Figure 2, is the aftereffect of a breakdown condition activated by impact ionisation. Hence, for the proposed MS IMOS, the whole internal mechanism to initiate the avalanche effect is similar to that of the bipolar I-MOS.



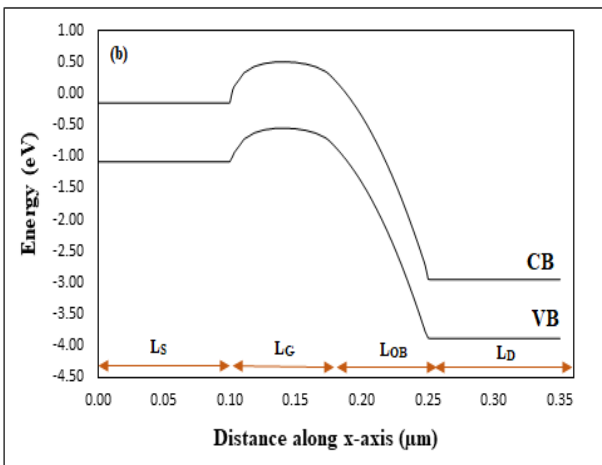


Figure 3: MS I-MOS energy band diagram in the thermal equilibrium condition (a) at V_{DS}=0 V and V_{GS} =0 V, and (b) at V_{DS}=1.75 V and V_{GS} =0 V.

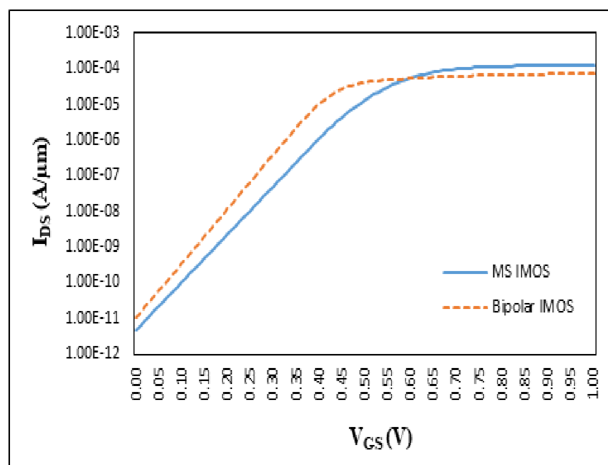
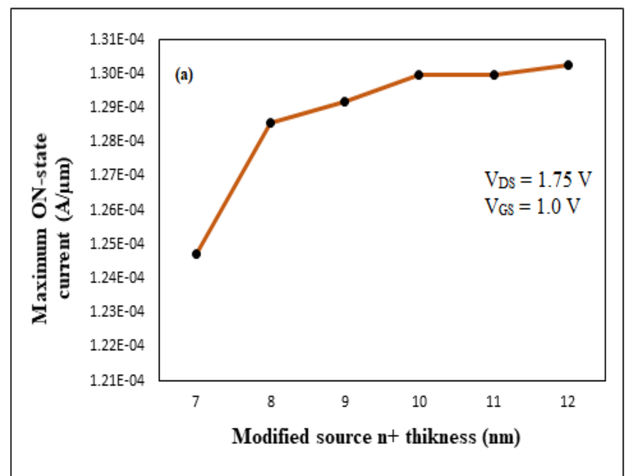
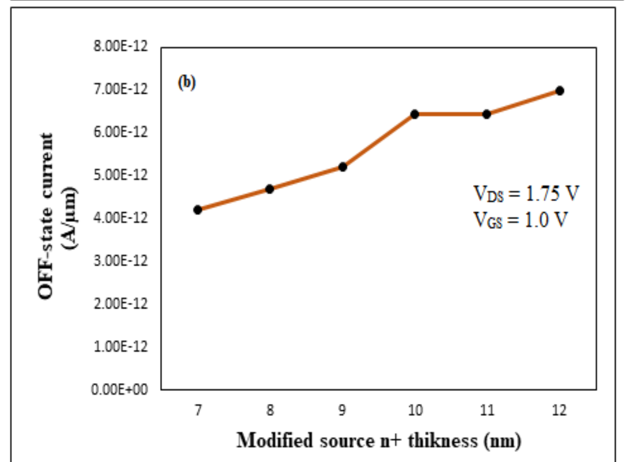


Figure 4: I_{DS} versus V_{GS} characteristics of the MS I-MOS (at V_{DS} =1.75 V) and bipolar I-MOS (at V_{DS} =2.5 V).

For I-MOS transistors, transconductance increases and the threshold voltage decreases with the increase in V_{DS}, but once it reaches to the breakdown voltage or above, transconductance of the I-MOS degrades abruptly [7][15], and therefore the maximum voltage applied to operate the device should be slightly lower than the breakdown voltage of that device. For our proposed device the operating voltage is 1.75 V, whereas 2.5 V is operating voltage for conventional Bipolar I-MOS. Therefore, to study the I_{DS}-V_{GS} attributes of the proposed device and bipolar I-MOS, the plotting is done by biasing drain-to-source voltage equal to the operating voltage of the respective devices. The comparison of I_{DS} versus V_{GS} characteristics of the MS I-MOS (at V_{DS} =1.75 V) with the bipolar I-MOS (at V_{DS} = 2.5 V) is illustrated in Figure 4. At V_{DS} = 1.75, ON-state and OFF-state current of the MS I-MOS are 1.29 x 10^{-4} A/μm and 4.70 x 10^{-12} A/μm, respectively. At V_{DS} = 2.5 V, bipolar I-MOS offered ON-state current and OFF-state current as 7.36 x 10^{-5} A/μm and 1.07 x 10^{-11} A/μm, respectively. Thus, we can say that the MS IMOS provides a higher drive current even at a lower operating voltage in comparison to bipolar I-MOS. The improvement of the drain current in MS IMOS is the direct result of low parasitic capacitance in the source region. I_{ON} to I_{OFF} ratio of the proposed MS IMOS is approximately equal to 2 x 10^7, which is 3.33 times greater than that of bipolar I-MOS (6 x 10^6).





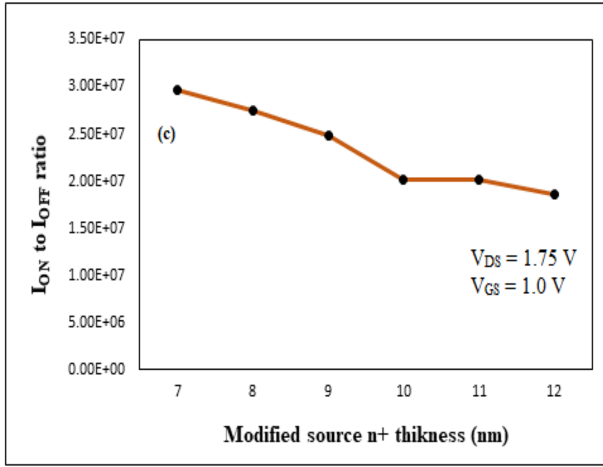


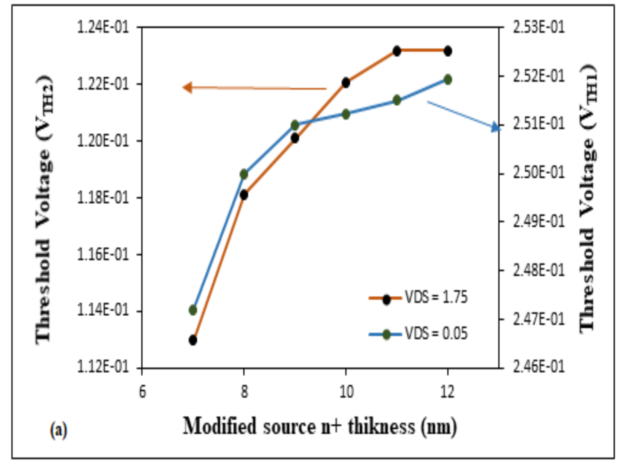
Figure 5: Behavior of (a) maximum ON-state current, (b) OFF-state current, and (c) I_{ON} to I_{OFF} ratio for different thicknesses of n+ region of the modified source of MS I-MOS at V_{DS} = 1.75 V and V_{GS} = 1.0 V.

Figure 5(a), (b) and (c), respectively demonstrate the impact of the thickness of the n+ region of modified source on the maximum ON-state (I_{ON}) current, OFF-state (I_{OFF}) current and I_{ON} to I_{OFF} ratio of the proposed device. We have varied the thickness of the n+ region of the modified source from 7 nm to 12 nm and analysed that I_{ON}, as well as IOFF increases as the thickness of n+ region, is increased. Thus, with the lower thickness of the n+ region, it is possible to achieve higher I_{ON}/I_{OFF}. Hence, without going beyond 8 nm thickness, a tradeoff between 7 nm and 8 nm has been made, and 8 nm thickness for the n+ region is selected over 7 nm for the only reason to achieve higher drive current without making any compromise with high I_{ON}/I_{OFF}.

DIBL is a vital parameter to check the effects of the short channel on a MOSFET. At higher drain voltages, the reduction in threshold voltage (Vth) of the transistor is an effect of DIBL. No DIBL effect might return to 0, but it must be in its minimum value so that the transistor performs efficiently and possess high reliability. It is expressed by [19]:

$$DIBL = \frac{V_{TH_1}\big|_{V_{DS(low)}} - V_{TH_2}\big|_{V_{DS(supply)}}}{V_{DS(supply)} - V_{DS(low)}} \qquad (1)$$

where, V_{TH_1} and V_{TH_2} are threshold voltages of the transistor at $V_{DS_{(low)}}$ = 0.05 V and $V_{DS_{(supply)}}$ = 1.75 V, respectively. The variations in threshold voltages, V_{TH_1} and V_{TH_2} of MS I-MOS and behavior of DIBL as a function of n+ region thickness is demonstrated, in Figure 6(a) and (b), respectively. From the results, it is observed that the change in V_{TH_1} and the change in V_{TH_2} is very minute and both increases with the increase in the thickness of n+ region (from 7nm to 12 nm) of modified source and as a result, the DIBL decreases with the increase in the thickness of highly doped n+ source region which concludes that with the increase in the thickness of the modified source region, the short channel effect (DIBL) decreases. The values of V_{TH_1} and V_{TH_2} at 8 nm thickness of n+ region are 0.249999 V and 0.118127 V, respectively. The value for DIBL which is obtained at 8 nm thickness of n+ region is 79.92242 mV/V.



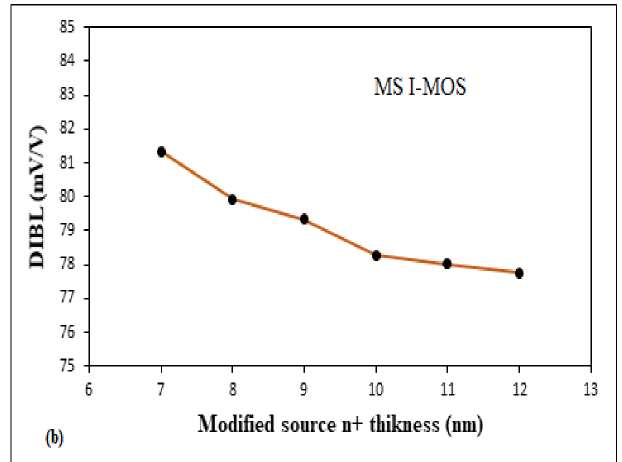


Figure 6: Behavior of (a) threshold voltages, V_{TH1} and V_{TH2}, and (b) DIBL as a function of n+ region thickness of modified source of the proposed MS I-MOS. Where, V_{TH1} and V_{TH2} are threshold voltages of the transistor at drain to source voltage of 0.05 V and 1.75 V, respectively.

IV. CONCLUSION

In this paper, an n-p-n I-MOS with a modified source is proposed. The high drive current and I_{ON}/I_{OFF}, with the decreased OFF-state current, clearly demonstrates that there is a significant improvement in the performance of the proposed MS I-MOS in comparison to corresponding bipolar I-MOS. The proposed device offers I_{ON} current of 1.29 x 10^{-4} A/μm and I_{OFF} current of 4.69 x 10^{-12} A/μm at an operating voltage of 1.78 V, which is 37% less than the bipolar I-MOS, and 75% smaller than the traditional p-i-n I-MOS. Hence, the circuit based on this device is suitable for low power digital applications. The I_{ON} to I_{OFF} ratio for MS I-MOS is 3.33 times greater than that of bipolar IMOS and 28 times of I_{ON} to I_{OFF} ratio of p-i-n I-MOS. Consequently, it is also suitable for fast switching applications.

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