Analyze of Process Parameter Variance In 19nm Wsi_2/Tio_2 NMOS Device Using 2k-Factorial Design

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***Abstract*— This paper investigates and analyzes the impact of process parameter variance on the drive current (I_{ON}) and leakage current (I_{OFF}) for 19nm WSi_2/TiO_2 NMOS device using 2k-factorial design. The four process parameter, namely halo implant dose, halo implant energy, source/drain (S/D) implant dose and S/D implant energy will be investigated and adjusted to improve the results. The simulated of the device was performed by using ATHENA module. Meanwhile the electrical characterization of the device was implemented by using ATLAS module. These two modules will be combined with 2k-factorial to aid design and optimize the process parameters. The most effective process parameter with respect I_{ON} and I_{OFF} were chosen depending on the percentage of the factor effect on S/N ratio that indicates the relative power of factor to reduce variation. The most dominant or significant factors in S/N Ratio are pocket halo implant dose and S/D implant energy. Meanwhile, the values of I_{ON} and I_{OFF} values for 19nm WSi_2/SiO_2 NMOS device after optimization approaches are 591.38 µA/µm and 2.217 pA/µm respectively. The results obtained are meet the requirement of International Technology Roadmap Semiconductor (ITRS) 2013 prediction.**

***Index Terms*— 2k-factorial Design; Ion implantation; NMOS Device.**

I. INTRODUCTION

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology has become popular in the microelectronic industry for almost a fifth decade. Because of that, the size of the MOSFET transistor has been decreasing continuously through the process of scaling validating based on Moore's Law [1]. Scaling down used to ensure the robust performance of transistor due to the high demand for smaller, faster and cheaper technology. However, there is some problem to further technology scaling due to the increasing of wafer fabrication process parameter variation [2]. The problem such as short-channel effect (SCE), and drain induced barrier (DIBL) lead in the introducing of a high-k material such as Titanium Oxide (TiO_2) [3]. Silicon oxide (SiO_2) has been used as the gate dielectric material for over a decade. Nowadays, replacing SiO_2 with high-k material as one of the new research initiatives to overcome those problems. A metal gate such as Tungsten Silicide (WSi_2) is used to eliminate Poly-Si depletion, which makes the leakage current are too high. This helps in producing better physical and electrical properties of a transistor [4,5].

In this project, it is necessary to understand and model manufacturing process variations for the prediction of device and circuit performance and to provide enough information for circuit designers to minimize the impact of parameter variation on the circuit performance and maximize the yield [6,7]. One of the statistical methods for identifying semiconductor process parameters, whose variability would impact on the device characteristics, is realized using 2k-factorial design [8].

II. METHODOLOGY

Based on an ITRS 2013 prediction, the threshold voltage (V_{TH}) of the 19nm NMOS device is 0.533V [9]. The research is based on simulation and program development and physical modelling of nano device performance. All the simulations used in this research are performed using a Silvaco TCAD tool. Initially, the main substrate which is P-type silicon with <100> orientation has been used. Then, the 200Å oxide layer was grown on top of silicon bulk. This oxide layer is important as it has been used as a mask during the P-well implantation process [10]. After the doping process was completed, the oxide layer has been etched, and it was followed by an annealing process. The function of annealing process was to strengthen the device's structure. Photo resistor layer was then deposited on the wafer layer, and any unwanted parts were etched away using the Reactive Ion Etching (RIE) process. The main purpose of an oxide layer grown on the trench sides was to eliminate impurity from entering the silicon substrate. After that, to eliminate extra oxide on the wafer, the Chemical Mechanical Polishing (CMP) was applied. A sacrificial oxide layer was then grown and etched to eliminate any defects on the surface. The high-k material, titanium oxide (TiO_2) was deposited to a thickness of 2nm. The next step was to implant boron difluoride (BF_2) into the N well active area in order to adjust the V_{TH} value.

Tungsten Silicide (WSi_2) was then deposited on the top of the bulk and etched accordingly to produce the gate contact point as desired. Sidewall spacer was then deposited to a mask for source/drain implantation. Arsenic was implanted with an appropriate value of concentration to get smooth current flow in NMOS device [11]. The next stage is to deposit Boron Phospor Silicate Glass (BPPG) layer. This layer was a Premetal dielectric (PMD) which is the first layer deposited on the wafer surface when the transistor produced. The transistor was then connected to aluminium metal. After that, the second aluminum layer was deposited on top of the

Intel-Metal Dielectric (IMD), and unwanted aluminium was etched to create the contacts [12]. The step was completed when etching and metallization were performed for electrode formation and bonding pads were opened. Figure 2 shows the Buried oxide layer formation in the 10nm SOI MOSFET device.

III. Result and Analysis

A. Design of Experiment

In the design of experiment (DoE), the 2k-factorial design suggested two options for four process parameters which are full factorial and half fraction design [8]. Full factorial design requires 16 experiment runs while half fraction design requires eight experiment runs. The L_8 half fraction design was selected for this study due to its minimum experiment runs. Table 1 shows the experimental layout for four process parameters using the L_8 2k-factorial design. Meanwhile, Table 2 shows the investigated ion implantation process of the device.

Table 1
L_8 2k-factorial Design

Experiment Number	Process Parameter Level			
	A	B	C	D
1	1	1	1	1
2	1	1	–1	–1
3	–1	1	–1	1
4	–1	–1	1	1
5	1	–1	–1	1
6	1	–1	1	–1
7	–1	–1	–1	–1
8	–1	1	1	–1

Table 2
Ion implantation process of the 19nm NMOS Device

Symbol	Control Factors	Units	(-1)	(+)
A	Halo Implant Dose	atom/cm^3	2.18	2.22
B	Halo Implant Energy	keV	170	172
C	S/D Implant Dose	atom/cm^3	9.67	9.73
D	S/D Implant Energy	keV	12	12.4

B. Multiple properties of 19nm WSi_2/TiO_2 NMOS device

This section describes the process of recording the data for multiple properties in the 19nm WSi_2/TiO_2 NMOS device. The involved electrical properties were known as ON-current (I_{ON}) and OFF-current (I_{OFF}) in which they were intended to be simultaneously optimized via 2k-factorial design. The 2k-factorial design provides a thorough investigation of the effect of multiple control factors on multiple electrical properties. Eight experiment runs were conducted in order to attain multiple values of I_{ON} and I_{OFF} according to the L_8 2k-factorial design as depicted in Table 3.

Table 3
I_{ON} and I_{OFF} of 19nm WSi_2/TiO_2 NMOS device

Experiment	I_{ON} (µA/µm)	I_{OFF} (pA/µm)
1	595.9	2.228
2	565.6	8.827
3	612.8	4.216
4	611.8	3.992
5	583.3	1.482
6	564.3	0.825
7	580.7	1.529
8	593.2	2.301

C. Estimation of Factor Effects towards I_{ON} and I_{OFF}

The analysis of multiple properties of the device imitated with the estimation of the influences of control factors A, B, C and D towards the variation of I_{ON} and I_{OFF} as tabulated in Tables 4 and 5 respectively.

Table 4
Estimation of factor Effect and Coefficients for I_{ON}

Term	Effect	Coef	SE Coef	T	P
A	-22.35	-11.18	0.1061	-105.36	0.000
B	6.85	3.43	0.1061	32.29	0.000
C	5.7	2.85	0.1061	26.87	0.000
D	25	12.50	0.1061	117.85	0.000

Table 5
Estimation of factor Effect and Coefficients for I_{OFF}

Term	Effect	Coef	SE Coef	T	P
A	-1.655	-0.827	0.172	-4.80	0.017
B	0.45	0.225	0.172	1.31	0.283
C	0.309	0.155	0.172	0.90	0.436
D	1.595	0.798	0.172	4.63	0.019

Based on Table 4 indicated that all the tested factors were significant towards I_{ON} values as their p-values were equal to zero. Meanwhile, Table 5 shows the most significant factor for I_{OFF} characteristic was factor A (Halo Implant Dose) which demonstrated the lowest p-value at 0.017. Based on the information attained from the estimation effect analysis, the normal plot of standardized effects was visualized. Figure 1 displays the normal plot of standardized effects for I_{ON}, indicating all the factors are significant towards I_{ON} characteristic since all the points are distributed away from the straight line.

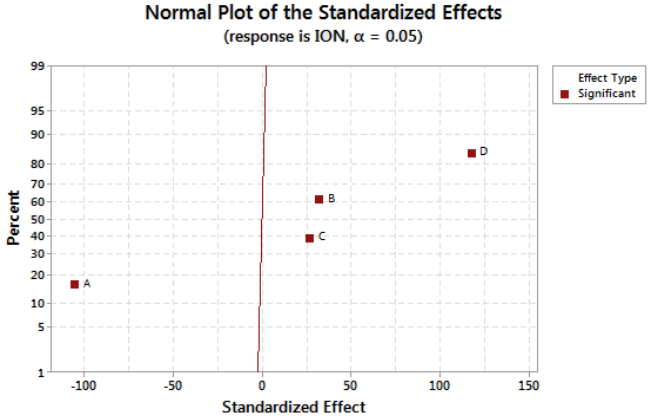

Figure 1: Normal plot of the Standardized Effects for I_{ON}

Figure 2 indicates both factors A (Halo Implant Dose) and D (S/D Implant Energy) are recognized as significant factors towards I_{OFF} characteristic where the points are spread away from the straight line.

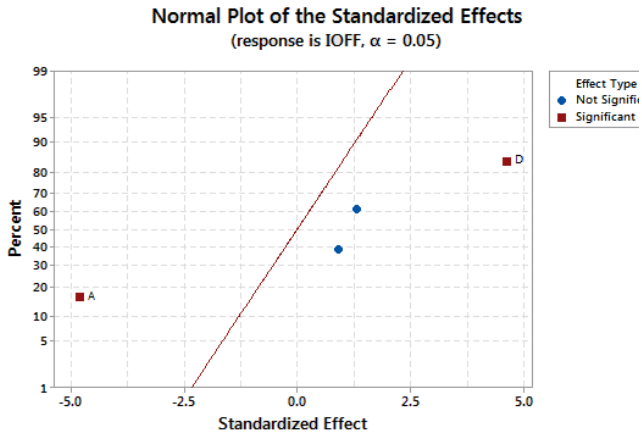

Figure 2: Normal plot of the Standardized Effects for I_{OFF}

Meanwhile factor B (Halo Implant Energy) and Factor C (S/D Implant Dose) are considered non-significant factors as the points are located near to the straight line. All the points along the line can be ignored. Only the significant effects which are located far from the line will be considered as significant factors. The guideline that was employed for the 2k-factorial analysis was based on 95% confidence level. Figures 3 and 4 show the Pareto charts of standardized effects for I_{ON} and I_{OFF} accordingly. Any factor effects that exceed the confident line will be regarded as significant.

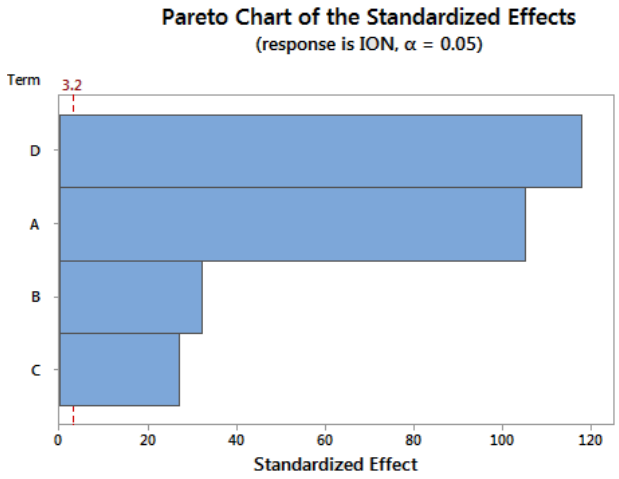

Figure 3: Pareto Chart of the Standardized Effects for I_{ON}

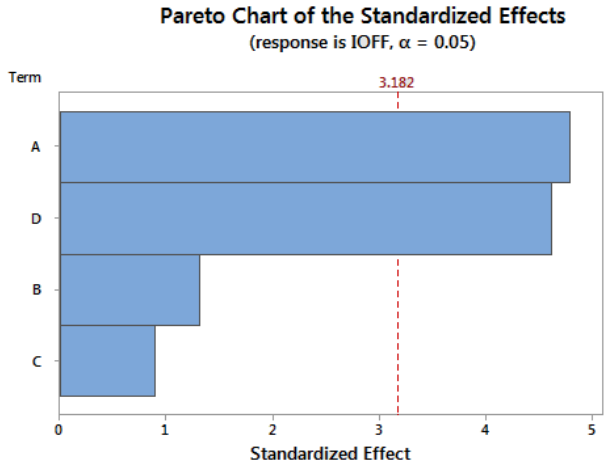

Figure 4: Pareto Chart of the Standardized Effects for I_{OFF}

Figure 3 indicates the main effect of the factors exceeded the confident line, justifying that all the factors can be considered significant upon I_{ON} variation. Meanwhile, Figure 4 shows that the main effect of factor A and D exceeded the confident line, proving that both factors were significant towards I_{OFF} variation. In contrast, the main effect of factor B and C were observed to be below the confident line, indicating that both factors were non-significant towards I_{OFF} variation.

The main effects plot for I_{ON} and I_{OFF} were depicted in Figures 5 and 6 respectively. Figure 5 shows that the slope of factor A was negative, implying that any increase in factor A will result in lower I_{ON} value. Meanwhile, the slope of the other factors was observed to be positive, indicating the I_{ON} of the device can be increased when factor B, C and D are increased.

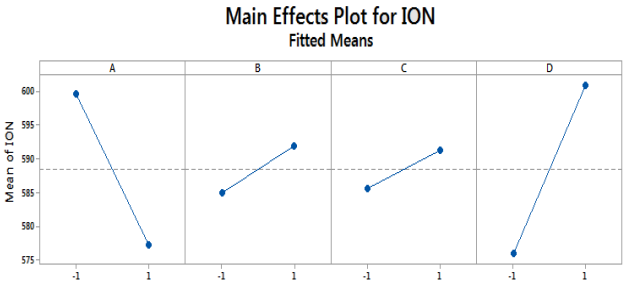

Figure 5: Main Effects Plot for I_{ON}

Figure 6 depicts the slope of the main effects of factor A was negative, indicating that the higher value of factor A will decrease the I_{OFF} of the device. The slope of the main effects of factor B, C and D were observed to be positive, implying that the increase in the value of these factors will contribute to the larger I_{OFF} characteristic.

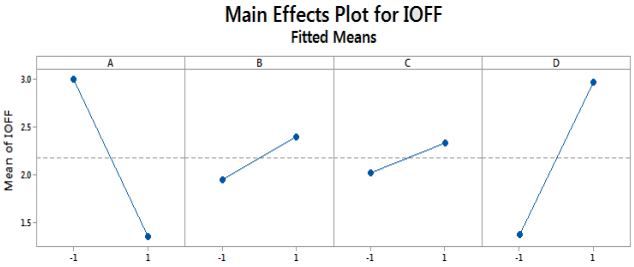

Figure 6: Main Effects Plot for I_{OFF}

D. Analysis of Variance (ANOVA)

Since the ANOVA involved multiple properties, the non-significant were not removed from the full model. The ANOVA for V_{TH}, I_{ON} and I_{OFF} were built to investigate the residual error in the full model. The P-value is defined as the probability of the residual error which is important to measure the significance of certain factor. Basically, a factor must have factor effects below than 0.05 to be considered significant where it reaches 95% of confident level [8]. Tables 6 and 7 show the ANOVA for I_{ON} and I_{OFF} characteristic respectively.

Table 6
ANOVA for I_{ON}

Source	DF	Adj SS	Adj MS	F-value	P-Value
A	1	999.05	999.05	11100.5	0
B	1	93.85	93.85	1042.72	0
C	1	64.98	64.98	722	0
D	1	1250	1250	13888.89	0
Error	3	0.27	0.09		
Total	7	2408.14			

Table 7
ANOVA for I_{OFF}

Source	DF	Adj SS	Adj MS	F-value	P-Value
A	1	5.4781	5.4781	26.06	0.017
B	1	0.4050	0.4050	1.70	0.283
C	1	0.1910	0.1910	0.80	0.436
D	1	5.0880	5.0880	21.42	0.019
Error	3	0.2376	0.2376		
Total	7	11.8748			

E. Optimization Analysis via Desirability Function

Desirability function was carried out using the Minitab Response Optimizer tool to optimize I_{ON} and I_{OFF} simultaneously. The optimal solution can be obtained through multiple level setting which can be pre-determined by the designer. Table 8 shows the preset condition for multi-response optimization in which both weight and importance were set to one.

Table 8
The preset condition for multi-response optimization

Response	Goal	Lower	Target	Upper	Weight	Importance
V_{TH} (V)	Target	0.525	0.533	0.544	1	1
I_{ON} (µA/µm)	Max	564.3	612.8		1	1
I_{OFF} (pA/µm)	Min		0.825	4.216	1	1

Figure 7 depicts the optimization plot for I_{OFF} and I_{ON} of the device. It was observed that the current value (red color) were more optimal levels of all the factors that satisfy multiple properties of the device. For factor A C and D, the optimal coded levels were predicted to be high (1.0) where the actual value was 2.22 atom/cm^3, 9.73 atoms/cm^3 and 12.4 keV. For factor C, the optimal coded level was predicted to be (-0.4) in which the actual value was 169.6 keV. The optimal level after optimization plot for I_{ON} and I_{OFF} are recorded in Table 9.

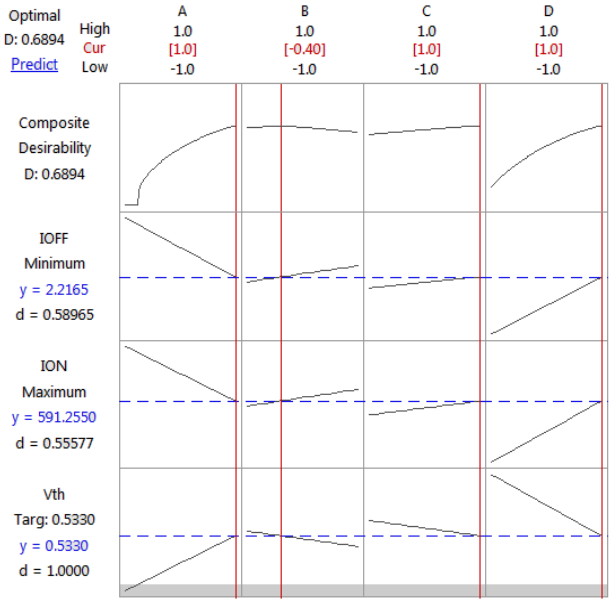

Figure 7: Optimization Plot for I_{OFF} and I_{ON} of the device

Table 9
Optimum Level after optimization plot for multiple responses

Symbol	Control Factors	Coded Value	Actual Value
A	Halo Implant Dose	1	2.22
B	Halo Implant Energy	-0.4	169.6
C	S/D Implant Dose	1	9.73
D	S/D Implant Energy	1	12.4

IV. CONFIRMATION TEST

The confirmation test is required to be conducted in order to verify whether the predicted optimal level of the control factors valid or not upon the actual experimental values [13]. The optimal setting of the control factors for 19nm WSi_2/TiO_2 channel NMOS device suggested by L8 2k-factorial design is shown in Table 10.

Table 10
Best Setting of Control Factors

Symbol	Control Factors	Units	Best Value
A	Halo Implant Dose	atom/cm^3	2.22
B	Halo Implant Energy	keV	169.6
C	S/D Implant Dose	atom/cm^3	9.73
D	S/D Implant Energy	keV	12.4

Finally, the improvement in I_{ON} and I_{OFF} characteristic was verified by simulating the device again using the best level setting. Table 11 shows the comparison of the final results with predicted results via 2k-factorial design and ITRS 2013 [9]. Based on Table 11, it can be observed that the results of the confirmation test indicated small percentage differences compared to the 2k-factorial prediction where I_{ON} and I_{OFF} characteristic was only varied for about 0.61% and 24%. These results justify that the 2k-factorial design is appropriate to be implemented in the device optimization. On top of that, the final results did meet the requirement I_{ON} and I_{OFF} characteristic according to ITRS 2013 prediction [9]. It can be concluded that the 2k-factorial design is capable of finding the robust process recipe while simultaneously optimized all the investigated electrical properties.

Table 11
The final result of Confirmation Test for Multiple Properties

Source	I_{ON} (µA/µm)	I_{OFF} (pA/µm)
Confirmation Test	587.7	1.685
2k-factorial Prediction	591.3	2.217
ITRS 2013 Prediction [9]	≥ 456	≤ 10

V. CONCLUSION

As a conclusion, the 2k-factorial is a reliable method in achieving the optimum solution in the nano scale NMOS device. In this research work, halo implant dose and S/D implant energy were identified as the most dominant process parameter that has the largest effect on the response characteristics of the WSi_2/SiO_2 NMOS device. Upon the optimization, the values of I_{ON} and I_{OFF} are 591.38 µA/µm and 2.217 pA/µm respectively. These values meet the requirement of the ITRS 2013. It was concluded that the ion implantation process variance contributes a large effect on the value of I_{ON} and I_{OFF} for the device. Thus, affecting the overall performance of a device.

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