A New Improvement of Reverse Voltage Single Phase Multilevel Inverter Topology

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Abstract **- The widely use of a multilevel inverter (MLI) in high power system applications proves that MLI is highly superior to the conventional inverter in reducing harmonic distortion. Basically there are three topologies of multilevel inverters that commonly used, which is cascaded H-Bridge, diode clamped and flying capacitor. Even though these inverters can produce low harmonic distortion, many switching devices are needed to perform high voltage level. However, the usage of a numerous number of switching devices can produce high switching losses. It also increases weight, space, cost and switching complexity of the hardware. Therefore, this study attempts to develop low harmonic distortion with less switching devices by improving the reverse voltage topology using MATLAB/Simulink software. The performance of proposed scheme was evaluated through an extensive test considering several scenarios such as amplitude modulation ratio (Ma), total harmonic distortion (THD) and switching scheme under various operating points. Moreover the effectiveness of the proposed scheme was verified by comparing its result with conventional MLI such as reverse voltage MLI topology and cascaded H-bridge topology.**

Index Terms **– Multilevel Inverter, Reverse Voltage, PWM Inverter, H-Bridge, Total Harmonic Distortion.**

I. INTRODUCTION

In the recent years, an enormous number of industries use an inverter in many applications. The inverter is recognized as the powerful electronic device to convert direct current (DC) to alternating current (AC). In industries, there are some components or appliances that need a high power source to be operated but it will damage the other load that is requiring a medium power source to operate.

Since 1975, an inverter is designed to overcome this situation. To give an outstanding performance to the inverter, the multilevel inverter (MLI) is introduced. MLI has more advantages than the conventional inverter [1]. It gives more power, operated using many switches instead of one, and it is applicable in many appliances. MLI consists of numerous power switches that are controlled to generate the power conversion into a small voltage step. There are three configurations of MLI namely Cascaded H-Bridge, Flying Capacitor and Diode Clamped [2]. Although this MLI has some benefits, several drawbacks are still observed, especially in high frequency switching components. It requires a lot of high frequency switching components that can cause switching power losses. The switching component depends on the level of voltages. The higher the level of voltage, the number of switches will increase. Another disadvantage of these topologies is that all switches should be selected from fast switches. The usage of high frequency switching component is expensive because more switching required and it prone to damage compared to low frequency switching component [3-4]. Moreover, it takes more space when executing the prototype. The conventional inverter also tends to have a complex controller, because the carrier has positive and negative parts. Thus, researchers introduce another topology named reversed voltage topology [5-6] that combined high switching frequency and low switching frequency in one circuit. It separates the circuit into two parts which are level generation part and polarity generation. The level generation part is responsible for generating a positive voltage. This part needs a high frequency switching to operate. For polarity generation part, it produces polarity of the output voltage. Only low frequency switching is required to generate half cycle of the output voltage. The advantage of reverse voltage topology is required less carrier signals and gate drives compare to the conventional multilevel inverter. Unfortunately, the number switches are not reduced by much.

The contribution of this paper consists of addressing the above discussed problem by improving the reverse voltage multilevel inverter (IRVMLI) topology. Compared with existing models, the novelty of this IRVMLI is the reduction of number switches and carrier signal at generation part. Nevertheless, the proposed technique would still produce low total harmonic distortion(THD) and fulfilled the IEEE 519. Furthermore, the proposed topology is more efficient as the inverter has a component that operates the switching power devices at line frequency. Thus, it leads to more simpler and reliable control of inverter as less switches working at high frequency levels.

II. REVERSE VOLTAGE MULTILEVEL INVERTER TOPOLOGY

This section describes the reversed voltage multilevel inverter (RVMLI) topology which includes a brief explanation of RVMLI and the development of IRVMLI.

A. Conventional Reverse Voltage Multilevel Inverter

Figure 1 illustrates the technology of reversed voltage MLI (RVMLI) topology introduced in (6), which consist of ten switches and three isolated dc sources. Generally, this topology can be divided into two part which is full bridge converter (right circuit) and output level without the polarity (left circuit) as depicted in Figure 1. It transfers the required output level to the output with the same direction based on the requirement of output polarity. Moreover, it reverses the voltage direction when the voltage polarity requires to changed for negative polarity.

The main advantages of RVMLI compared with conventional cascaded H-bridge topology is RVMLI

requires a less total number of switches and one-third of isolated power supplies to obtain the same level of output voltage. The number of switches in RVMLI topology can be obtained from the following equation:

$$S = ((N - 1) + 4) \quad (1)$$

where S is a number of swithes and N is a number of output voltage level.

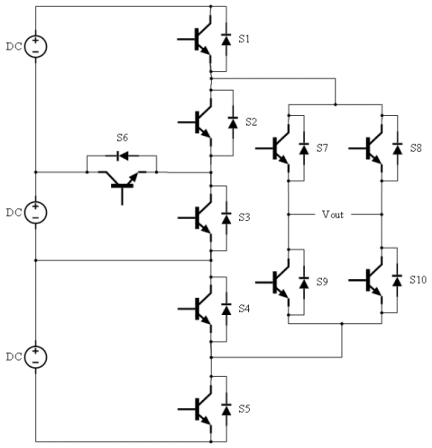

Figure 1: Conventional single phase 7-level of reverse voltage topology.

B Proposed Reverse Voltage Multilevel Inverter

Figure 2 represents the proposed IRVMLI topology scheme. The reduction number of switches are proposed in this study in order to improve the performance of RVMLI in term of power conversion efficiency and requires fewer gate drives. The proposed IRVMLI topology utilized only 8 switches rather than 10 switches in RVMLI topology. The number of switches at the generation part is reduced from six (conventional RVMLI) to four switching devices (see Figure 2). Besides, it required four diodes in order to replace that two switches devices. Therefore, the power conversion efficiency of proposed IRVMLI is increased.

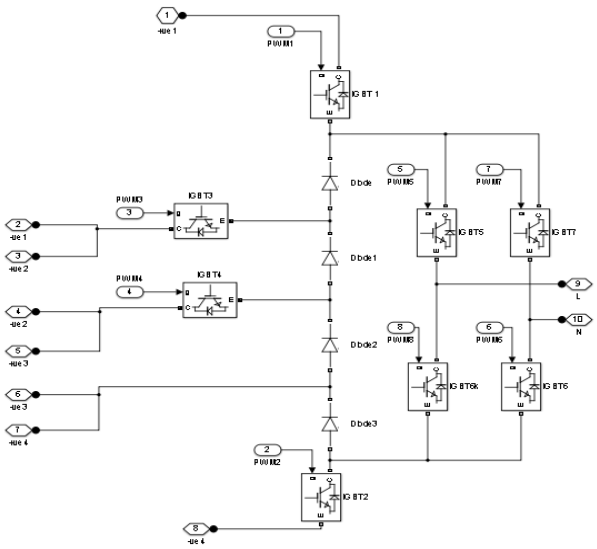

Figure 2: 7-level of -level of IRVMLI topology

Mathematically, the switches can be obtained as follows:

$$S = (N - 1) + 2 \quad (2)$$

where S is a number of swithes and N is a number of output voltage level.

C. Pulse Disposition Pulse Width Modulation (PD-PWM)

In the case of the level shifted pulse width modulation (PWM) method, it is similar to the phase shifted method in its number of carriers and the peak to peak voltage. The difference is the level of the carrier wave. The carrier wave is arranged according to the level of output. For instance, 7-level inverter needs 6 carrier waves, each carrier wave is arranged from the bottom of the reference waves up to the top level by level and compared to the reference waves. The output is distributed to the main switches to produce a sinusoidal output. One example for the type of multicarrier PWM for the level shifted method is phase disposition (PD) PWM. All carrier wave in this type is in the same phase [12].

Figure 3 shows the Simulink block diagram for PD-PWM. For reverse voltage topology, the sinusoidal waveform needs to be rectified first because in this topology the polarity can be changed by using H-Bridge circuit. Sine wave block is connected in series to absolute block to create a rectified wave. To create multilevel carrier, repeating sequence block is used to create a carrier waveform. Then, the carrier signal and constant block are sums to generate a multilevel carrier. This carrier and sinusoidal waveform are compared by using a relational operator to generate the switching scheme for IGBT in the inverter.

Figure 4 demonstrates the PD-PWM waveform for reverse voltage topology. The cascaded H-Bridge topology is using the same technique for PWM but the absolute block is not applied because it cannot change its polarity by its own. The carrier frequency for both topologies is set to 5 kHz and its fundamental frequency is 50 Hz. Figure 5 below shows the waveform of PD-PWM for cascaded H-Bridge.

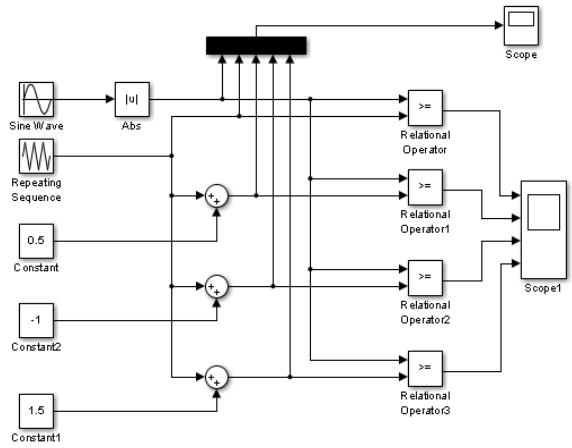

Figure 3: Simulink model for PD-PWM.

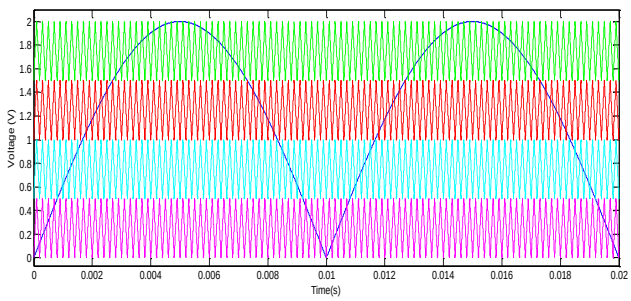

Figure 4: Waveform for PD-PWM reverse voltage

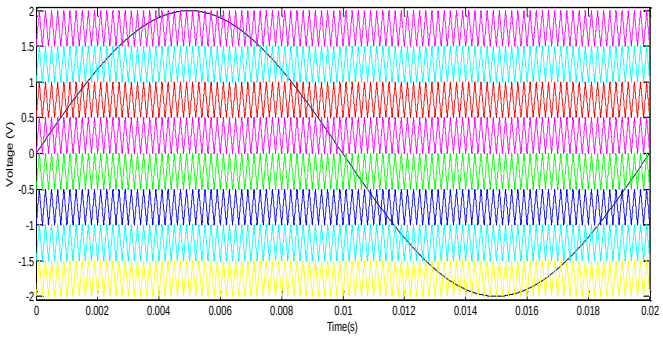

Figure 5: Waveform for PD-PWM cascaded H-Bridge.

III. PERFORMANCE ANALYSIS

The main concern in this MLI topology is the capability to fulfil the THD IEEE 591 standard. For this purpose, a number of switches, amplitude modulation index (Ma), total harmonic distortion current (THD_i) and total harmonic distortion voltaget (THD_V) are used as the index to evaluate the performance of MLI topology. These indices can be derived as follows:

(i) Number of switches is used to evaluate the number of switches used for MLI topology

(ii) Ma is amplitude modulation index. Mathematically, it can be expressed as follows:

$$M_a = \frac{V_m}{(\frac{n-1}{2})V_c} \quad (3)$$

where V_m represents the reference voltage, n represents the level output voltage and V_c represents the carrier signal.

(iii) THD_v is the total harmonic distortion voltage. It can be expressed as follows:

$$THD_v = \frac{\sqrt{\sum_{n=2}^{\infty}(V_{n,RMS})^2}}{V_{1,RMS}} \quad (4)$$

where n is a number of harmonics, V_{RMS} is root mean square (RMS) voltage and $V_{1,RMS}$ is fundamental voltage.

(iv) THD_i is the total harmonic distortion current and can be evaluated as follows:

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty}(I_{n,RMS})^2}}{I_{1,RMS}} \quad (5)$$

where n is a number of harmonics, I_{RMS} is the root mean square (RMS) current and $I_{1,RMS}$ is fundamental current.

IV. RESULT AND ANALYSIS

This section presents the test result of the proposed IRVMLI topology where all the initialization parameters and parameters settings various case studies scheme are tabulated in Table 1. The first part of this section describes the result obtained by applying the switching sequence for IRVMLI along with the conventional cascaded H-bridge MLI. Meanwhile, the second part of this section describes the result obtained by a number of the component for IRVMLI and conventional MLI such as RVMLI and cascaded H-bridge MLI. Lastly, the third part of this section described the result simulation for Ma THD index of IRVMLI and conventional MLI such as RVMLI and cascaded H-bridge.

A. Sequence Switching

The purposed of this study is to observe the sequence of switching devices for proposed IRVMLI and conventional MLI. Table 2,3 and 4 show the switching states for each level in IRVMLI, RVMLI and caccaded H-bridge inverter topologies respectively. From the table, IRVMLI only need 8 switching sequence to complete the switching sequence rather than conventional MLI that need 12 swi

Table 1
Parameter for cascaded H-bridge and IRVMLI

Parameter	
Voltage Source for Each Input	100V
Resistance Load	685.7143 Ω
Capacitive Load	13.92 μF
Inductive Load	0.8 H
Fundamental Frequency	50 Hz
Fundamental Amplitude	2 V
Carrier Amplitude	2 V
Carrier Frequency	5kHz

Table 2
Switching sequence for 9-level IRVMLI

O/p Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
4 Vdc	1	1	0	0	1	0	0	1
3 Vdc	0	1	1	0	1	0	0	1
2 Vdc	0	1	0	1	1	0	0	1
Vdc	0	1	0	0	1	0	0	1
0Vdc	0	0	0	0	1	0	1	0
-Vdc	0	1	0	0	0	1	1	0
-2 Vdc	0	1	0	1	0	1	1	0
-3 Vdc	0	1	1	0	0	1	1	0
-4 Vdc	1	1	0	0	0	1	1	0

Table 3
Switching sequence for 9-level RVMLI

O/p Voltage	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
4 Vdc	1	0	1	0	0	1	1	0	1	0	0	1
3 Vdc	0	1	1	0	1	0	1	0	1	0	0	1
2 Vdc	0	1	1	0	0	1	0	1	1	0	0	1
Vdc	0	1	1	0	0	1	1	0	1	0	0	1
0Vdc	0	1	0	1	0	1	1	0	1	0	1	0
-Vdc	0	1	1	0	0	1	1	0	0	1	1	0
-2 Vdc	0	1	1	0	0	1	0	1	0	1	1	0
-3 Vdc	0	1	1	0	1	0	1	0	0	1	1	0
-4 Vdc	1	0	1	0	0	1	1	0	0	1	1	0

Table 4
Switching sequence for 9-level cascaded H-Bridge

O/p Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}
4 Vdc	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
3 Vdc	1	0	0	1	1	0	0	1	1	0	0	1	0	0	1	1
2 Vdc	1	0	0	1	1	0	0	1	0	0	1	1	0	0	1	1
Vdc	1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1
0Vdc	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
-Vdc	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0
-2 Vdc	0	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0
-3 Vdc	0	1	1	0	0	1	1	0	0	1	1	0	1	1	0	0
-4 Vdc;	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0

Table 5
Number of the main component for single phase for different level output

NO	Cascaded 6(N-1)	NPC 6(N-1)	Flying Capacitor 6(N-1)	RV 3((N-1)+4)	IRV $\sum_{n>5} N-k$ $k=\frac{N-7}{2}; N=odd$
3	6	6	6	6	5
5	12	12	12	8	6
7	18	18	18	10	7
9	24	24	24	12	8
11	30	30	30	14	9
13	36	36	36	16	10
15	42	42	42	18	11
17	48	48	48	20	12
19	54	54	54	22	13
21	60	60	60	24	14
23	66	66	66	26	15
25	72	72	72	28	16
27	78	78	78	30	17
29	84	84	84	32	18
31	90	90	90	34	19

B. Number of components

Aforementioned, one of the main advantages of IRVMLI is less amount of high-switching-frequency components. Thus, this study is done in order to evaluate the amount of main switches based on level output voltage for IRVMLI and various conventional MLI topology such as RVMLI, flying capacitor and cascaded H-bridge. From the result in Table 5, it can be seen that as the output level increased, less amount of switches being utilized compared with others conventional MLI scheme. Thus, it can prove that the proposed IRVMLI required less number of switching component compared with the conventional MLI scheme as illustrated in Figure 6.

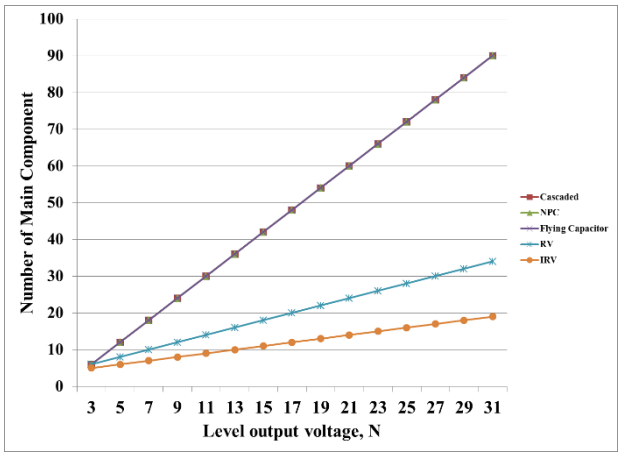

Figure 6: Required switches at various MLI

C. Performance of Total Harmonic Distortion (THD) based on Ma index

Table 6 illustrates the performance of proposed IRVMLI of THD current and voltage with various amount of Ma index for RL load. From the table, it shows that with a higher amount of Ma index, the amount of THD current and voltage would be low.

Table 6
THD performance of IRVMLI for RL load with various Ma index

Ma	THDi	THDv
0.2	1.87	76.95
0.6	0.68	24.44
1	0.42	13.68

The performance at Ma is 0.6 and 1 is analysed to evaluate further the performance of IRVMLI. Figures 7,8 and 9 show the performance of voltage and current waveform, THD_v and THD_i using 0.6 Ma index, respectively. THDv for RL load is 24.44%, meanwhile its THD_i is 0.68% as shown in Figure 9 and Figure 10, respectively. The output for voltage is 7 levels output waveform, while for the current is a sinusoidal output current. The voltage peak for this level is 299.2 V, while the current peak is 329.0 mA.

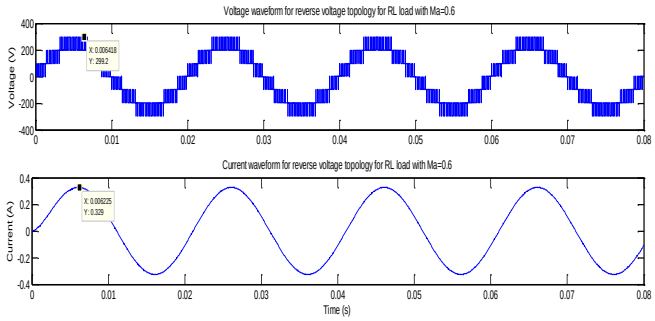

Figure 7: IRVMLI performance of current and voltage waveform for RL load with *Ma*=0.6.

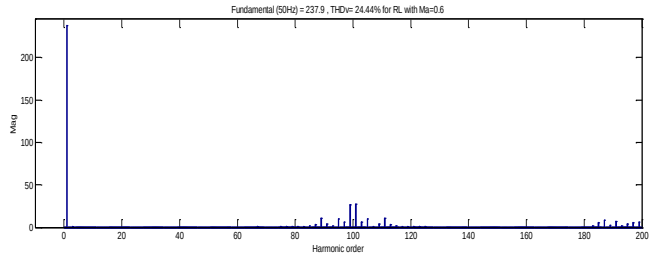

Figure 8: THD_v for IRVMLI with *Ma*=0.6.

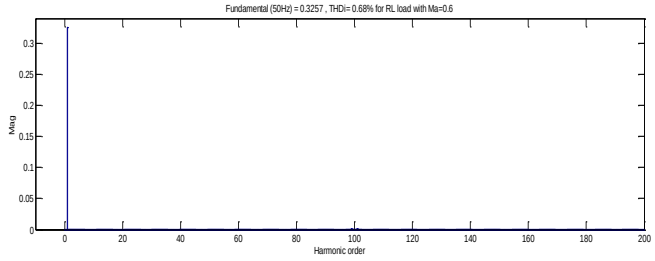

Figure 9: THD_i for IRVMLI with *Ma*=0.6.

Similarly, analysis at M_a is 1 for IRVMLI is performed. Figure 10 illustrates the voltage and current waveform performance for RL load. The THD_v for RL load is 13.68%, meanwhile the THD_i of RL load is 0.42% (see Figure 11 and 12, respectively). The output voltage has 9 levels output waveform and the current is sinusoidal output current. Voltage peak for this level is 400 V whereas current peak is 550.3 mA.

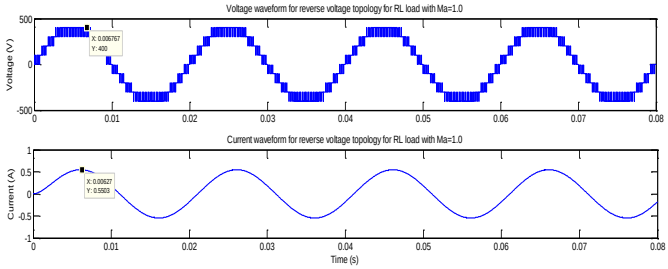

Figure 10: IRVMLI performance of current and voltage waveform for RL load with *Ma*=1.0

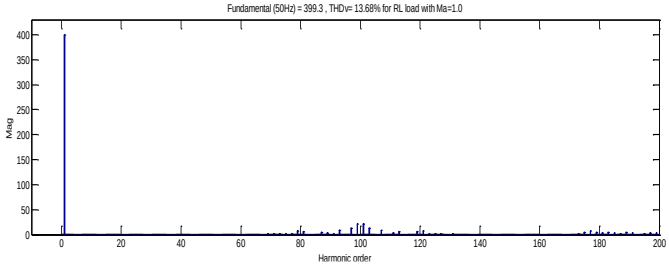

Figure 11: THD_v for IRVMLI with *Ma*==1.0.

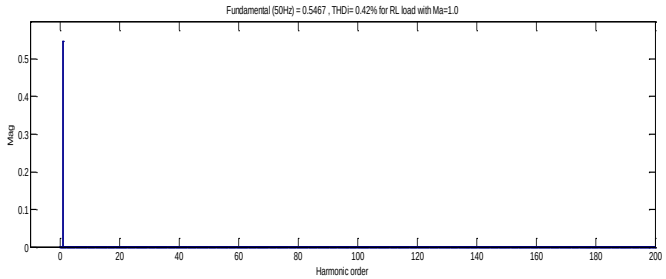

Figure 12: THD_i for IRVMLI with *Ma*=1.0.

D. Competitive comparison with conventional MLI

To demonstrate the good performance of the proposed IRVMLI, using the same parameter setting as tabulated in Table 1, both conventional MLI such as RVMLI and H-bridge scheme is simulated in Simulink/Matlab software. The performance of THD_i and THD_v based on various Ma index are summarized in Table 6 and Table 7, respectively. From the observation, it proves that IRVMLI complied with IEEE 519 as same as others conventional MLI such as RVMLI and cascaded H-Bridge.

Table 6
Performance of THD_i

Ma	IRVMLI	RVMLI	Cascade H-Bridge
0.2	1.87	1.84	1.84
0.6	0.68	0.58	0.58
1	0.42	0.33	0.34

Table 7
Performance of THD_v

Ma	IRVMLI	RVMLI	Cascade H-Bridge
0.2	76.95	76.71	76.99
0.6	24.44	24.32	24.35
1	13.68	13.69	13.73

V. CONCLUSION

From the simulation, it concludes that the reverse voltage topology for the multilevel inverter is slightly better in total harmonic distortion for voltage and current as compared with cascaded H-Bridge multilevel inverter. This topology is also produced the same output voltage and current as cascaded H-Bridge multilevel inverter. The main problem in the conventional multilevel inverter, it needs to use many high frequency switching components to generate the multilevel output. The increases of the level are directly proportional to the level of the output. The reverse voltage is hybrid topology that combines the low and high switching to get the output as same as the conventional inverter. It uses PD-SPWM control method. The proposed topology PWM has less complexity because of it generates only positive

carrier for PWM control. This hybrid inverter required less switching components compared to the conventional method. It also needs a half of the carrier frequency needed in the conventional inverter to generate the same level.

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