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Compact quadrature oscillator with voltage and current outputs using only single VDTA and grounded capacitors

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A possible design of the compact sinusoidal quadrature oscillator using single voltage differencing transconductance amplifier (VDTA) and only two grounded capacitors has been presented. The presented quadrature oscillator provides the following attractive properties: (i) canonic form and resistor less structure; (ii) availability of the explicit quadrature voltage outputs and current outputs; (iii) electronic controllability of the oscillation frequency (ω_0); and (iv) low active and passive sensitivities. To support the validity of the oscillator, PSPICE simulation results have also been provided.

Keywords: Voltage differencing transconductance amplifier, Quadrature oscillator, Dual-mode operation, Resistorless circuit, Electronically tunable

1 Introduction

The voltage differencing transconductance amplifier (VDTA) is the recently defined controllable active building block, and increasingly being used in numerous applications. In the more recent works, its applications and advantages especially in the synthesis of active filters[1-6] and sinusoidal oscillators[7-9] have increased considerably as they have been found to be able to provide the electronic tuning through the transconductance gain g_m of the VDTA, and reduce the number of the passive components used for their circuit realizations[10].

Sinusoidal quadrature oscillators, i.e., generators producing two identical sinusoidal output signals equally in amplitude and frequency but having 90° phase shifted, are very frequently used in wide scope of electronic engineering applications. For this reason, a number of voltage and current-mode sinusoidal quadrature oscillators have been already realized by utilizing the advantages of different types of versatile active building blocks[9,11-27]. However, the previously quadrature oscillators suffer from one or more of the following disadvantageous features:

(i) They employ more than one active circuit building block[9,11-21,25-26].

(ii) They use any external passive resistors, which is not canonic and resistorless structure[11-20,22-27].

(iii) They do not provide electronic controllability to their circuit parameters[11-15,18,24-25]

(iv) The passive components used in their realization are floating, which is not convenient for integrated circuit implementation[12-15,19-20,22-23,25].

(v) They cannot generate voltage-mode and current-mode quadrature signals simultaneously[9,11-23].

In this paper, a simple scheme for the realization of the sinusoidal quadrature oscillator with voltage and current outputs has been considered. To perform a compact and resistorless quadrature oscillator, the circuit is based on the use of a single VDTA and only two grounded capacitors. When compared to the already reported works[9,11-27], the proposed dual-mode quadrature oscillator exhibits the following salient characteristics: uses only one active element and two grounded capacitors, a resistorless design, dual-mode operation, i.e., voltage and current quadrature outputs, high-impedance current outputs, electronic adjustment of the frequency of oscillation, and low sensitivity performance. The characteristics of the circuit are studied in detail and demonstrated through the PSPICE simulation with acceptable results.

2 Circuit Descriptions

The electrical symbol of the VDTA is shown in Fig. 1. Its ideal characteristic can be described by the following matrix:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_{mF} & -g_{mF} & 0 & 0 \\ 0 & 0 & g_{mS} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_{zc} \\ v_z \end{bmatrix} \quad \ldots (1)$$

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where g_{mF} and g_{mS} are the first and second transconductance gains of the VDTA, respectively. In general, both transconductance gains are controllable electronically by the external DC bias currents. According to above describing-relations, the differential input voltage (v_p-v_n) is converted to currents at the terminals z (i_z) and zc (i_{zc}), respectively, by the transconductance g_{mF}, and the corresponding voltage drop at the terminal z is conveyed to currents at the terminals x (i_x) by the transconductance g_{mS}.

The possible CMOS realization of the VDTA is shown in Fig. 2, which actually consists of two interconnected Arbel-Goldminz transconductances[28]. Each of them realizes two independent electronically tunable transconductance gains g_{mF} and g_{mS}. Their values can be approximated as, respectively:

$$g_{mF} \cong \left(\frac{g_1 g_2}{g_1 + g_2}\right) + \left(\frac{g_3 g_4}{g_3 + g_4}\right) \quad \ldots (2)$$

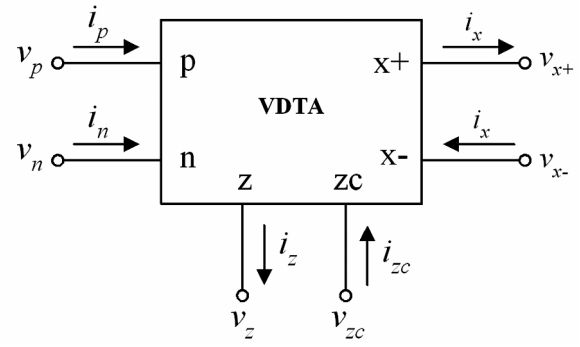

Fig. 1 — Circuit representation of the VDTA

and $g_{mS} \cong \left(\frac{g_5 g_6}{g_5 + g_6}\right) + \left(\frac{g_7 g_8}{g_7 + g_8}\right)$ … (3)

where $g_i = \sqrt{I_{Bi}\mu C_{ox}\frac{W_i}{L_i}}$ is the transconductance value of the i-th MOS transistor (i = 1, 2, …, 8), I_{Bi} is the bias current of the MOS M_i, μ is the free carrier mobility in the channel, C_{ox} is the gate-oxide capacitance per unit area, and W_i and L_i are the channel width and length of the transistor M_i, respectively.

A realization scheme for a compact sinusoidal quadrature oscillator with explicit voltage and current outputs is shown in Fig. 3. The configuration is canonic in component count, since it consists of merely one VDTA and two grounded capacitors. It should be noted that the two quadrature current outputs i_{o1} and i_{o2} exhibit high-input impedances that permit the ease of cascading, and both capacitors C_1 and C_2 are grounded that is particularly beneficial from the viewpoint of ease of monolithic integration. A routine circuit analysis of Fig. 3 yields the following results. The voltage transfer function of the first transconductance stage of the VDTA is given by:

$$T_F(s) = \frac{V_{o2}(s)}{V_{o1}(s)} = \frac{g_{mF}}{sC_2} \quad \ldots (4)$$

and that of the second transconductance stage is:

$$T_S(s) = \frac{V_{o1}(s)}{V_{o2}(s)} = -\frac{g_{mS}}{sC_1} \quad \ldots (5)$$

Hence, the loop gain of Fig. 3 can be expressed as:

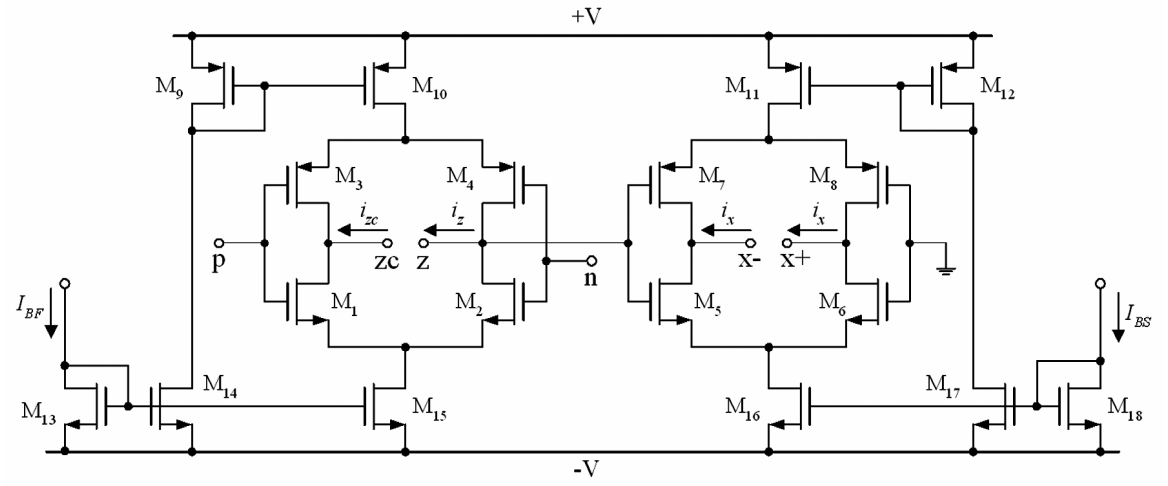

Fig. 2 — CMOS implementation of the VDTA

$$T_F(s)T_S(s) = -\frac{g_{mF}\,g_{mS}}{s^2 C_1 C_2} \quad \ldots (6)$$

For sinusoidal oscillations, the loop gain is set to unity at $s = j\omega$. This, along with Eq. (6), gives the following characteristic equation for Fig. 3:

$$s^2 C_1 C_2 + g_{mF}\,g_{mS} = 0 \quad \ldots (7)$$

From Eq. (7), the oscillation frequency can also be obtained as:

$$\omega_o = 2\pi f_o = \sqrt{\frac{g_{mF}\,g_{mS}}{C_1 C_2}} \quad \ldots (8)$$

For simplicity, if $g_m = g_{mF} = g_{mS}$ and C, $= C_1 = C_2$, then the parameter ω_o in Eq. (8) turns to:

$$f_o = \frac{g_m}{2\pi C} \quad \ldots (9)$$

This means that the frequency of oscillation f_o can be tuned electronically by means of g_m through adjusting the external bias currents $I_B = I_{BF} = I_{BS}$.

Also from Fig. 3, the two marked quadrature voltages (v_{o1} and v_{o2}) and currents (i_{o1} and i_{o2}) are related as, respectively:

$$v_{o2} = -\frac{j\omega C_1}{g_{mS}} v_{o1} \quad \ldots (10)$$

and $$i_{o2} = \frac{j\omega C_2}{g_{mS}} i_{o1} \quad \ldots (11)$$

which are ensured that the output voltages and the output currents are in quadrature signals.

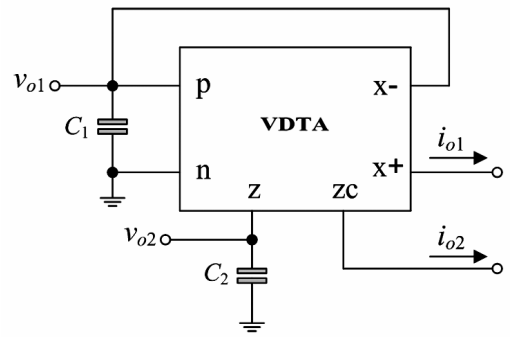

Fig. 3 — Proposed dual-mode quadrature oscillator

3 Tracking Error Analyses and Sensitivity Study

The practical characteristics of the VDTA taking into account the tracking errors of the device can be expressed as:

$$\begin{bmatrix} i_p \\ i_n \\ i_z \\ i_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \beta_F g_{mF} & -\beta_F g_{mF} & 0 & 0 \\ 0 & 0 & \beta_S g_{mS} & 0 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_{zc} \\ v_z \end{bmatrix} \quad \ldots (12)$$

where β_F and β_S are respectively the non-ideal transconductance gains of the VDTA, which deviate from their ideal values by tracking errors ε_F and ε_S, where $|\varepsilon_F|$, $|\varepsilon_S| << 1$. Therefore, considering the effects of the VDTA non-idealities defined in Eq. (12), the modified ω_o of the proposed quadrature oscillator in Fig. 3 can be written as:

$$\omega_o = \sqrt{\frac{\beta_F \beta_S g_{mF}\,g_{mS}}{C_1 C_2}} \quad \ldots (13)$$

It is clearly seen from Eq. (13) that the ω_o–value is slightly affected by the transconductance tracking errors of the VDTA. However, these deviations can be compensated by pre-distortion of the transconductance gains (g_{mF} and/or g_{mS}) of the VDTA.

The sensitivity of the ω_o for the oscillator in Fig. 3 with respect to its active and passive components can be derived as :

$$S_{g_{mF}}^{\omega_o} = S_{g_{mS}}^{\omega_o} = S_{\beta_F}^{\omega_o} = S_{\beta_S}^{\omega_o} = \frac{1}{2} \quad \ldots (14)$$

and $$S_{C_1}^{\omega_o} = S_{C_2}^{\omega_o} = -\frac{1}{2} \quad \ldots (15)$$

From Eqs (14) and (15), all the active and passive sensitivities are within 0.5 in absolute value, which is an advantageous feature of the proposed canonical oscillator.

4 Effects of Parasitic Impedances

In order to complete non-ideal analysis, it is useful to consider the parasitic elements of the VDTA device used in the quadrature oscillator of Fig. 3. Including the corresponding terminal parasitic elements, the practical model of the VDTA can be shown[5] in Fig. 4. It is seen that there are the parasitic resistances and capacitances $(R_p//C_p)$, $(R_n//C_n)$, $(R_z//C_z)$, $(R_x//C_x)$

appearing in parallel connection at the corresponding terminals of the VDTA. Typically, these parasitic resistances and capacitances are in the order of several MΩ and pF, respectively. Considering these parasitic, the oscillator given in Fig. 3 is then modified to Fig. 5, where $R'_1 = (R_p \,//R_x)$, $C'_1 = (C_1//C_p//C_x)$ and $C'_2 = (C_2//C_z)$. However, in practice, the values of the external capacitors C_1 and C_2 can be considered to be sufficiently larger than the parasitic capacitance values, i.e., $C_1 >> (C_p//C_x)$ and $C_2 >> C_z$. As a result, it becomes obvious that $C'_1 \cong C_1$ and $C'_2 \cong C_2$. Therefore, the total impedance at the terminal p (Z_1) is approximated to:

$$Z_1 \cong \frac{R'_1}{R'_1 C_1 s + 1} \quad \ldots (16)$$

The action of Z_1 at the terminal p of the actual VDTA limits the performance of the oscillator at the low-frequency range. According to Eq. (16), the operating frequency range can be easily defined as:

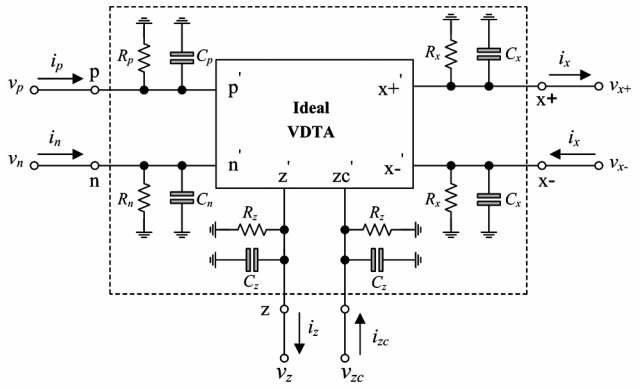

Fig. 4 — Practical model of the VDTA including its terminal parasitic impedances

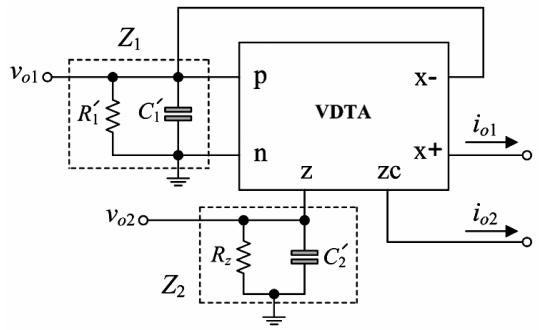

Fig. 5 — Proposed quadrature oscillator of Fig. 3 considering the terminal parasitic impedances of the VDTA

$$f >> \frac{1}{2\pi(R_p \,//\, R_x)C_1} \quad \ldots (17)$$

In a similar analysis, the frequency restriction stemmed from the z-terminal parasitic impedance (Z_2) can also be defined as:

$$f >> \frac{1}{2\pi R_z C_2} \quad \ldots (18)$$

5 Simulation Results and Discussion

The proposed quadrature oscillator with voltage and current outputs in Fig. 3 was simulated using PSPICE program. In simulations, the CMOS-based VDTA circuit given in Fig. 2 was used with the TSMC 0.25 μm CMOS process technology, and ±1.5 V voltage supply. The aspect ratios of the MOS transistors are indicated in Table 1.

As an example, the proposed quadrature oscillator in Fig. 3 was designed to obtain the oscillation frequency f_o = 95 kHz. By using Eq. (9), the designed component values were calculated as: $g_m = g_{mF} = g_{mS}$ = 0.6 mA/V ($I_B = I_{BF} = I_{BS}$ = 100 μA) and $C = C_1 = C_2$ = 1 nF. Figure 6 shows the simulated steady-state waveforms of quadrature outputs (v_{o1}, v_{o2}) and (i_{o1}, i_{o2}). The simulated f_o was measured as approximately 97 kHz, where the quadrature outputs different in phase by 86°. Figure 7 shows the simulated frequency spectrums of the quadrature output waveforms, where the values of the corresponding total harmonic distortion (THD) at all the outputs were around 2.46 %. Also from the simulation results, the total power consumption was found to be 2.09 mW. For the above designed values, the electronic control property of f_o with a variable I_B is displayed in Fig. 8. Obviously, the f_o is varied from approximately 30 kHz to 166 kHz for I_B, variation from 10 μA to 300 μA, respectively. A comparison results

Table 1 — Transistor aspect ratios used in the CMOS VDTA circuit of Fig. 2

Transistors	W/L (μm/μm)
M_1 - M_2	15.75/0.25
M_3 - M_4, M_9 – M_{10}	20.3/0.25
M_5 – M_6	14.55/0.25
M_7 – M_8	23.3/0.25
M_{11} - M_{12}	5.2/0.25
M_{13}	14.5/0.25
M_{14}	15.5/0.25
M_{15}	18/0.25
M_{16}	3.2/0.25
M_{17} - M_{18}	2.8/0.25

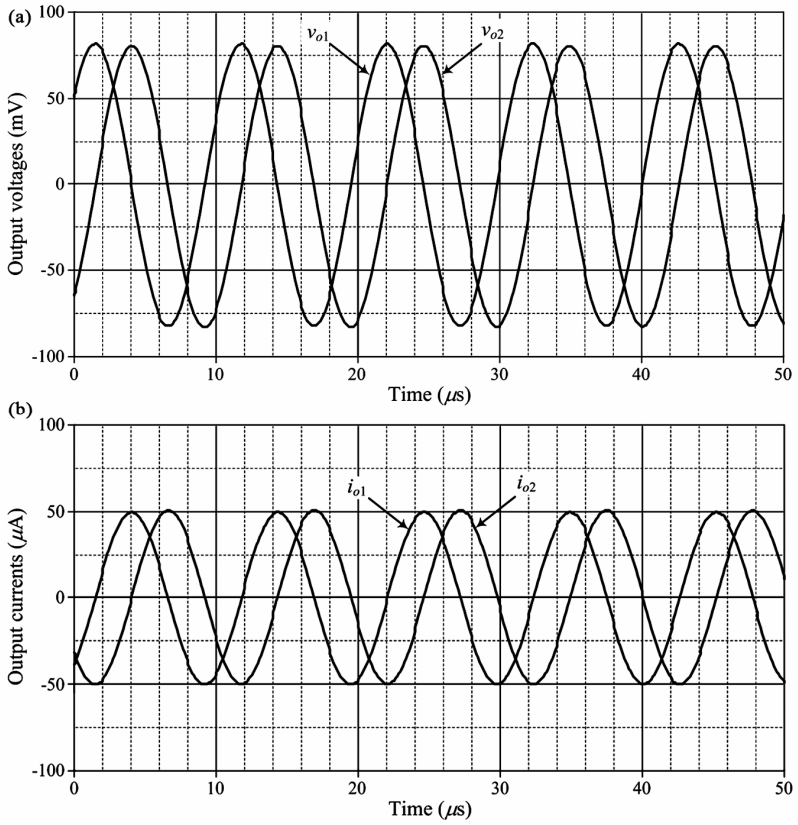

Fig. 6 — Simulated steady-state waveforms of quadrature outputs (a) output voltages v_{o1} and v_{o2} and (b) output currents i_{o1} and i_{o2}

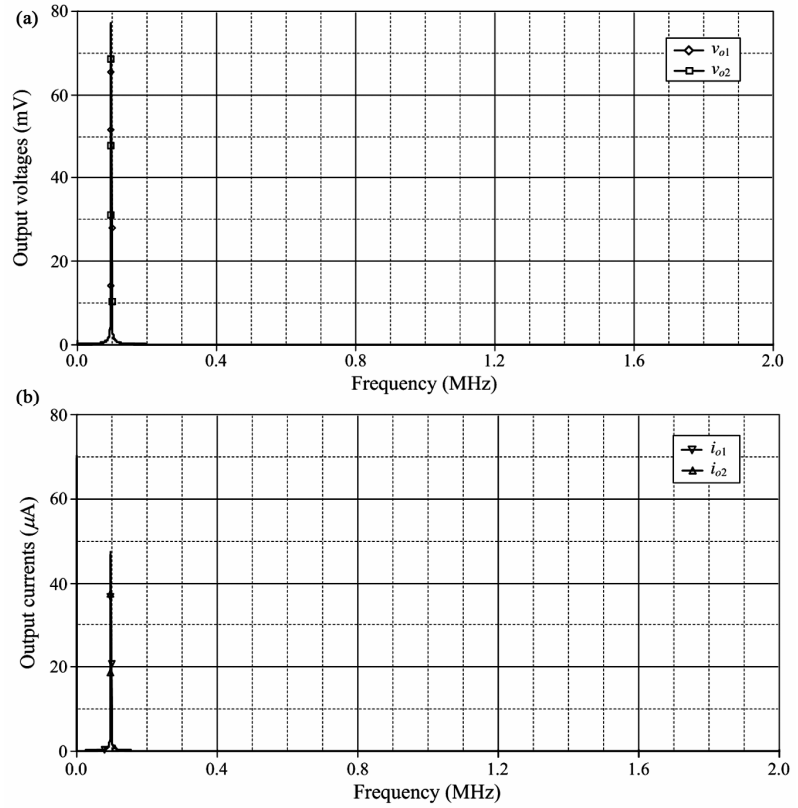

Fig. 7 — Simulated frequency spectrums of quadrature outputs (a) output voltages v_{o1} and v_{o2} and (b) output currents i_{o1} and i_{o2}

Table 2 — Comparative study of the proposed quadrature oscillator in Fig. 3 with the previous designs

Reference	Number of active element	Number of $R + C$	Grounded elements only	Electronic tuning	Dual-mode quadrature outputs	Technology	Supply voltages (V)	THD (%)	Total power consumption (mW)
[9]	VDTA = 2	0 + 2	yes	yes	no	TSMC 0.18-µm	±0.9	3.00	N/A
[11]	CCII = 3	4 + 2	yes	no	no	AD844	±12	N/A	N/A
[12]	DVCC = 3	3 + 2	no	no	no	TSMC 0.35-µm	±2	N/A	3.72
[13]	CDBA = 2	3 + 2	no	no	no	AD844	±12	1.58	N/A
[14]	CDBA = 2	4 + 2	no	no	no	AD844	±12	2.95	N/A
[15]	CDBA = 2	3 + 2	no	no	no	AD844	±12	1.94	N/A
[16]	CCCDBA = 2	1 + 2	yes	yes	no	TSMC 0.18-µm	±2	2.00	N/A
[17]	GCFTA = 1, VF = 1	1 + 2	yes	yes	no	PR100N, NP100N	±2	1.67	N/A
[18]	DVCC = 3	3 + 2	yes	no	no	0.5-µm CMOS	±2.5	2.00	N/A
[19]	CDTA = 2	4 + 2	no	yes	no	MIETEC 0.5-µm	±2.5	1.00	N/A
[20]	CFTA = 2	1 + 2	no	yes	no	MIETEC 0.5-µm	±2.5	N/A	N/A
[21]	CDTA = 3	0 + 2	yes	yes	no	PR100N, NP100N	±3.0	2.50	N/A
[22]	CDTA = 1	1 + 2	no	yes	no	0.7-µm CMOS	N/A	0.16	N/A
[23]	CDTA = 1	1 + 2	no	yes	no	MIETEC 0.5-µm	±2.5	3.00	N/A
[24]	FDCCII = 1	2 + 2	yes	no	no	TSMC 0.18-µm	±2.5	2.76	118.1
	FDCCII = 1,	3 + 2	yes	no	yes			2.86	129.4
[25]	CDBA = 2	3 + 2	no	no	yes	Macro-model	N/A	N/A	N/A
[26]	CDTA = 2	1 + 2	yes	yes	yes	MIETEC 0.5-µm	±2.5	N/A	N/A
[27]	CCTA = 1	2 + 2	yes	yes	yes	PR100N, NP100N	±3.0	3.00	N/A
This work	VDTA = 1	0 + 2	yes	yes	yes	TSMC 0.25-µm	±1.5	2.46	2.09

Notes:
N/A = Not Available, CCII = Second-Generation Current Conveyor, DVCC = Differential Voltage Current Conveyor,
CDBA = Current Differencing Buffered Amplifier, CCCDBA = Current Controlled Current Differencing Buffered Amplifier,
GCFTA = Generalized Current Follower Transconductance Amplifier, UGVF = Unity-Gain Voltage Follower,
CDTA = Current Differencing Transconductance Amplifier, CFTA = Current Follower Transconductance Amplifier,
FDCCII = Fully- Differential Second-Generation Current Conveyor.

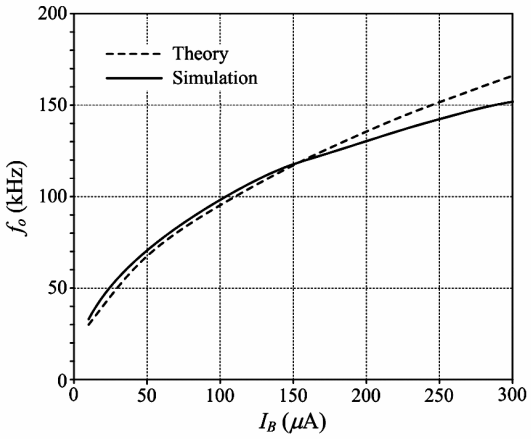

Fig. 8 — f_o variation with I_B

for the proposed compact quadrature oscillator designed in this work and the previously reported ones[9,11-27] is summarized in Table 2.

6 Conclusions

This paper proposes a circuit design for a compact resistorless sinusoidal quadrature oscillator. The proposed dual-mode quadrature oscillator features the following salient benefits simultaneously : (i) uses only one VDTA and two grounded capacitors, which is a canonical and resistorless configuration; (ii) produces voltage-mode as well as current-mode quadrature outputs explicitly; (iii) provides high-output impedance quadrature currents, thus permit the feature of cascadability; (iv) offers an electronic tuning of the oscillation frequency; and (v) has low active/passive sensitivity performance. It has been shown by PSPICE program that the simulation results agree well with the theoretical conclusions.

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