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Low voltage high bandwidth self-biased high swing cascode current mirror

Nikhil Raj[a]*, Ashutosh Kumar Singh[b] & Anil Kumar Gupta[c]

[a]Department of Computer and Communication Engineering, Manipal University, Jaipur 302 006, India

[b]Department of Computer Application, National Institute of Technology, Kurukshetra 136 119 India

[c]Department of Electronics and Communication Engineering, National Institute of Technology, Kurukshetra 136 119 India

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A low voltage self-biased high swing cascode current mirror (SHCCM) with improved bandwidth has been proposed. The recently reported SHCCM architecture use the bulk-driven quasi-floating gate (BDQFG) MOS transistors to enhance the effective transconductance which improves the current mirror input resistance and bandwidth range over the same architecture realized using bulk-driven MOS transistors. To further improve the bandwidth the proposed BDQFG based SHCCM uses two resistances which makes the current mirror frequency response free from input capacitors and also reduces the parasitic capacitance effect which results in increased bandwidth with an advantage of having no degradation in other performance parameters of current mirror. The proposed current mirror operates well for input current range from 0 to 200 μA with good linearity and shows the bandwidth of 298 MHz (i.e., 1.6 times over prior reported BDQFG based SHCCM). The observed input and output resistance is 306 Ω and 165 kΩ, respectively. Further, the THD analysis is carried to prove the robustness of proposed current mirror. The complete analysis is performed on UMC 0.18 μm technology using HSpice.

Keywords: Bulk-driven MOS, Quasi-floating-gate MOS, Low-voltage, Current Mirror, Bandwidth

1 Introduction

Prolonging the battery life time is the basic requirement of modern portable electronics and battery-powered implantable and wearable medical devices. In context to this, many efforts and techniques have been exerted for realizing circuits which can work at sub-volt supply[1]. The scaling of supply voltage strongly affects the performance of analog circuits and does not guarantee reliable performance since the threshold voltage does not scale down proportionally. The supply voltage must be at least equal to or greater than the threshold of MOS transistors used in circuit realization. So, using conventional technique for circuit design at sub-volt supply without sacrificing the desired performance has becomes a tedious task nowadays. Therefore, various techniques have been proposed in literature which reduces the threshold voltage effect or even remove it thereby facilitate the circuits to operate at low voltage (LV). Few techniques frequently adopted are categorized as subthreshold[2], level shifter[3], bulk driven (BD)[4], floating gate (FG)[5-7], quasi-floating gate (QFG)[8-10]. Among these the BD is found to be most suitable approach for realizing low voltage low power circuits as it do not require any special arrangement for threshold voltage removal form input signal path. The bulk-input demand maximum supply not more than a BJT junction turn-on potential to prevent latch-up and so the technique is found suitable for battery-operated portable devices. From literature survey it has been found that most of the recent publications are based on BD approach[11-13].

Though using BD, FG and QFG techniques offer high functionality at low voltage low power capability these techniques have drawback of poor transconductance and low transition frequency. As a result, the circuits suffer reduced bandwidth and low gain structures. Besides, the FG and QFG based circuits also require large chip area. However, a most promising technique has been revealed in literature which congregates the characteristic of BD and FG/QFG MOS transistor. The technique is named as BDFG/BDQFG[14], i.e., BD MOS transistor configured in FG/QFG mode. Using BDFG/BDQFG the structure results in enhanced transconductance over separate BD and FG/QFG MOSFET. Compared to QFG, the FG based circuits suffer few drawbacks such as charge trapping, poor transconductance, and poor bandwidth. In context to this BDQFG has gained considerable potential interest over BDFG. Few latest

*Corresponding author (E-mail: nikhilpub@gmail.com)

research articles published has used the BDQFG technique in realisation differential difference current conveyor[15], differential difference amplifier[16], rectifier[17], etc. Moreover, the recently published article has proved experimentally the advantage of using BDQFG technique for realizing low power circuits[18,19]. In this paper, a low voltage high bandwidth SHCCM based BDQFG MOSFET is presented.

Current mirror is the most important and fundamental block for analog circuits. Realizing current mirror with bulk as input requires very low supply voltage and best suits to low power devices. However, the BD based current mirrors have limited applications due to poor current matching, less operating range and smaller bandwidth due to low transconductance. The proposed current mirror increases the bandwidth of prior reported low voltage BDQFG SHCCM[20] without degrading any of other performance parameter and consuming the same level of power consumption.

2 Bulk Driven and Bulk Driven Quasi Floating Gate MOSFET

2.1 BD MOSFET

The conventional MOSFET is a four terminal device whose fourth terminal, the bulk is connected to negative/positive supply for N-channel/P-channel transistor, respectively, or to their source terminal. Using bulk as signal input removes the threshold voltage limitation from input path. The very first article used BD technique to design differential amplifier[21]. The schematic of N-channel BD MOSFET is shown in Fig. 1. The dc bias voltage V_{bias} at gate of transistor MN creates the channel whereas the input signal is applied at bulk which modulates the drain-to-source current even with very low amplitude of input signal.

The most significant drawback related to the bulk-driven is its small body transconductance (g_{mb}) which is 3 to 5 times smaller than gate transconductance and poor transition frequency[17] (f_T). The g_{mb} relation with gate transconductance (g_{mb}) is given as:

$$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f - V_{SB}}} g_m = \eta g_m \quad \text{... (1)}$$

where γ is the body effect coefficient, ϕ_f is the Fermi-potential, V_{SB} is the source-to-bulk potential. The normal range of η varies from 0.2 to 0.4. However, the bio-signals being small in amplitude and low frequency range suits the use of BD approach for signal processing which ranges in kHz.

2.2 BDQFG MOSFET

The schematic of N-channel BDQFG MOSFET MN is shown in Fig. 2. The input capacitor *C* along with P-channel MOS transistor MP forms QFG node for MN and its bulk acting as input tied to its respective gate forms the BDQFG structure. Under DC, the structure behaves as standard BD MOSFET whereas for AC analysis it combines the characteristics of BD and QFG MOSFET. This results in effective transconductance higher than separate BD or QFG transconductance and also increased transition frequency (f_T). The effective transconductance (g_{meff}) of BDQFG MOSFET is given as:

$$g_{meff} = kg_m + g_{mb} = (k + \eta)g_m \quad \text{... (2)}$$

where k is the effective capacitance ratio of input to the total capacitance seen at QFG of MN The comparative analysis on MOSFET parameters in saturation mode using BD and BDQFG technique is shown in Table 1.

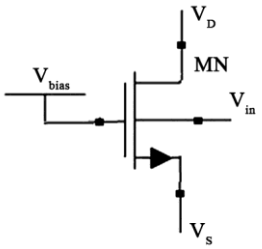

Fig. 1 – N-channel BD MOS transistor

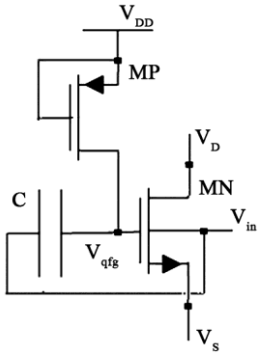

Fig. 2 – N-channel BD-QFG MOS transistor

Table 1 – Comparison of MOSFET parameters using BD and BDQFG technique

Parameter	BD	BDQFG
Threshold	removed	removed
Transconductance	$(0.2-0.4)\,g_m$	$(0.7-1)\,g_m$
Output conductance	λI_{DS}	$\left(C_{gd,MP}/C_{T,qfg}\right)g_m + \lambda I_{DS}$
Transition frequency	$(0.3-0.5)\,f_T$	$(0.7-0.9)\,f_T$

3 Proposed Current Mirror

In deep submicron technology, the conventional two transistor based current mirror does not fulfill the required performance of ideal current mirror. The short channel MOS device often results high output conductance and hence poor current matching. In this context, the cascode current mirror[22] (CCM) was proposed which provide high output impedance and suits high performance applications like in design of second generation current conveyors, op-amps, LNA etc. Though the CCM offers high output impedance but its reduced output signal swing due to overdrive voltage required by output MOSFET puts limitation on its uses for circuits requiring rail-to-rail operation. However, this overdrive voltage requirement got reduced by placing a series resistance *R* at the drain contact of input MOS transistor and the architecture was named as self-biased high swing cascode current mirror[23] (SHCCM). The detailed analysis of this current mirror and its modification in terms of output resistance can be found in[24]. However, for low voltage operation this gate driven SHCCM was realized using only BD MOS transistors and this BD based SHCCM[25] which when compared with its gate driven counterpart showed an improvement not only in terms of low voltage operation but also resulted in improved performance parameters. However, the BD SHCCM has disadvantage of high input resistance, low output resistance and poor bandwidth. To enhance the performance the BD SHCCM when modified using BDQFG MOS transistor showed a significant improvement in terms of input resistance and bandwidth response[20]. The schematic of SHCCM based on BD and BDQFG reported in literature is shown in Figs 3 and 4, respectively.

In Fig. 3, the four BD N-channel MOS transistors (M_1-M_4) are used to realize the SHCCM. The use of offset current $\left(I_{offset}\right)$ at output node is for minimizing the mismatch between input and output current due to non-linear behavior of BD MOSFET at low supply.

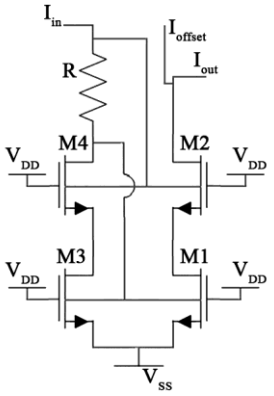

Fig. 3 – Low Voltage BD based SHCCM[25]

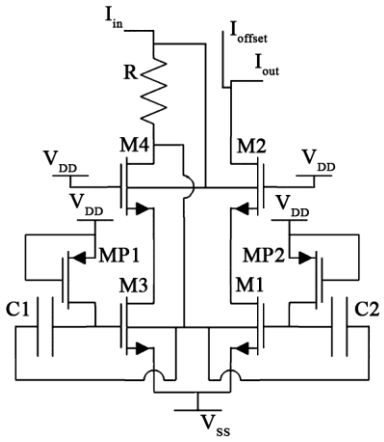

Fig. 4 – Low voltage BDQFG based SHCCM[20]

Due to poor transconductance (i.e., body transconductance) of M_1 and M_3 MOSFETs, such current mirror results in not only high input resistance but also low bandwidth. The improvement to these parameters of current mirror was replacing these BD MOSFETs by BDQFG MOSFETs as shown in Fig. 4 where the M_3 and M_1 MOS transistor are replaced by BDQFG MOS transistor whereas M_2 and M_4 are kept in normal BD mode. However, the increased capacitances of BDQFG especially due to input capacitors, the enhancement in bandwidth is achieved till certain limit.

In proposed current mirror, the range of bandwidth is further increased by reducing the effect of input capacitances on the bandwidth response without degrading any other performance parameters. The architecture of proposed high bandwidth SHCCM based on BDQFG MOSFET is shown in Fig. 5. The modification is carried out by using resistance R_1 and R_2 in series to input capacitors C_1 and C_2, respectively, of MOSFETs M_3 and M_1, respectively.

Through analysis, it has been observed that using these resistors causes the circuit's frequency response gets independent of the effect of input capacitors and also to parasitic gate-to-source capacitances of M_1 and M_3 which results in bandwidth enhancement over prior architectures. Moreover, these resistors does not have impact on effective transconductance of M_1 and M_3 MOS transistor and so high bandwidth is achieved without degrading other parameters.

In Fig. 6, the resistors R_1 and R_2 realization is done using N-channel MOS transistors MR_1 and MR_2, respectively. These MOS transistors MR_1 and MR_2 are made to operate in linear regime biased using N-channel MOS transistor (M_5, M_6) and (M_7, M_8), respectively.

3.1 Input resistance

The small signal model for calculating the input resistance ($R_{in,\text{Proposed}}$) of proposed current mirror is shown in Fig. 7 where:

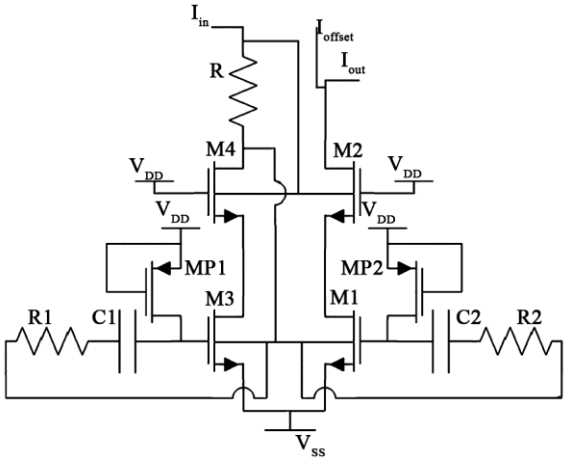

Fig. 5 – Proposed low voltage BDQFG SHCCM with enhanced bandwidth

At node 2:

$$i_{in} = g_{mb4}\left(V_1 - V_3\right) - g_{m4}V_3 + \frac{V_2 - V_3}{r_{o4}} \quad \text{... (3)}$$

At node 3:

$$i_{in} = \left(kg_{m3} + g_{mb3}\right)V_2 + \frac{V_3}{r_{o3}} \quad \text{... (4)}$$

$$V_2 = V_1 - i_{in}R \quad \text{... (5)}$$

Putting Eq. (5) in Eq. (4):

$$V_3 = \left(1 + \left(kg_{m3} + g_{mb3}\right)R\right)r_{o3}i_{in} - \left(kg_{m3} + g_{mb3}\right)r_{o3}V_1 \quad \text{... (6)}$$

From Eqs (3), (5) and (6):

$$R_{in} = \frac{V_1}{i_{in}} = \frac{\left(R(kg_{m3} + g_{mb3})(g_{m4} + g_{mb4})r_{o3}r_{o4} + (g_{m4} + g_{mb4})r_{o3}r_{o4}\right)}{(kg_{m3} + g_{mb3})(g_{m4} + g_{mb4})r_{o3}r_{o4}} \quad \text{... (7)}$$

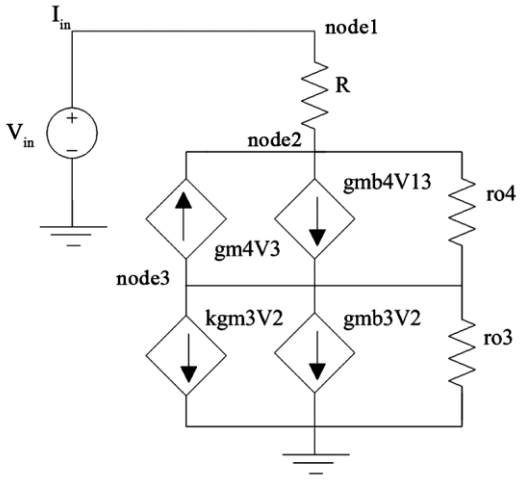

Fig. 7 – Small signal model for calculating input resistance

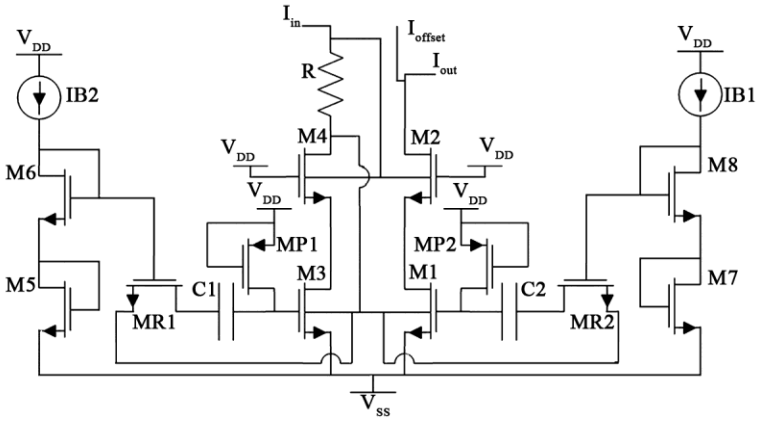

Fig. 6 – Final proposed low voltage BDQFG SHCCM with enhanced bandwidth

Hence:

$$R_{in,\text{Proposed}} \approx R + \frac{1}{kg_{m3} + g_{mb3}} \quad \text{... (8)}$$

Similar analysis when carried for BDQFG based SHCCM (Fig. 4) results in the input resistance as:

$$R_{in,BDQFG} \approx R + \frac{1}{kg_{m3} + g_{mb3}} \quad \text{... (9)}$$

And for the BD based SHCCM (Fig. 3), the input resistance is given by:

$$R_{in,BD} \approx R + \frac{1}{g_{mb3}} \quad \text{... (10)}$$

From Eqs (8) and (9), no difference is observed in terms of input resistance. However, the advantage of using BDQFG in lowering of input resistance can be observed by comparing Eqs (8) and (9) with Eq. (10).

3.2 Output resistance

The small signal model for calculating the output resistance ($R_{out,\text{Proposed}}$) of proposed current mirror is shown in Fig. 8 where:

At node 6:

$$i_{out} = -\left(g_{m2} + g_{mb2}\right)V_5 + \frac{V_6 - V_4}{r_{o2}} \quad \text{... (11)}$$

At node 4:

$$V_4 = r_{o1} i_{out} \quad \text{... (12)}$$

From Eqs (11) and (12):

$$i_{out} = -\left(g_{m2} + g_{mb2}\right) r_{o1} i_{out} + \frac{V_6 - r_{o1} i_{out}}{r_{o2}} \quad \text{... (13)}$$

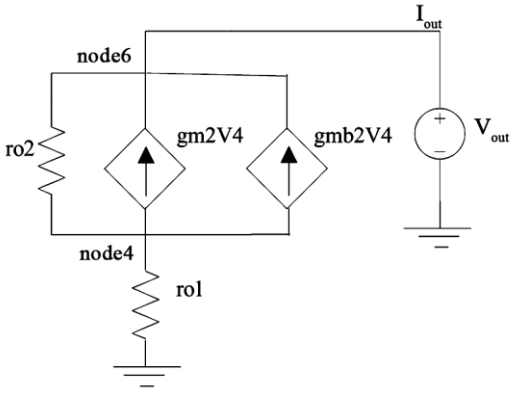

Fig. 8 – Small signal model for calculating output resistance

$$R_{out} = \frac{V_6}{i_{out}} \approx r_{o1} + r_{o2} + \left(g_{m2} + g_{mb2}\right) r_{o1} r_{o2} \quad \text{... (14)}$$

Since $g_m r_o >> 1$

$$R_{out,\text{Proposed}} \approx \left(g_{m2} + g_{mb2}\right) r_{o1,qfg} r_{o2} \quad \text{... (15)}$$

Similar analysis when carried for BDQFG based SHCCM (Fig. 4) results in the output resistance as:

$$R_{out,BDQFG} \approx \left(g_{m2} + g_{mb2}\right) r_{o1,qfg} r_{o2} \quad \text{... (16)}$$

And for the BD based SHCCM (Fig. 3), the output resistance is given by:

$$R_{out,BD} \approx \left(g_{m2} + g_{mb2}\right) r_{o1} r_{o2} \quad \text{... (17)}$$

From Eqs (15) and (16), no difference is observed in terms of output resistance whereas comparing with Eq. (17), due to increased output conductance of BDQFG MOS transistor M_1 the degraded output resistance is achieved. The improvement to such low output resistance has been achived in the architectures[26,27] at the cost of increased power dissipation.

3.3 Bandwidth

The small signal model for calculating the bandwidth ($\omega_{0,\text{Proposed}}$) of proposed current mirror is shown in Fig. 9. The output conductance and the C_{gd} effects are neglected in comparison to C_{gs} of saturation mode transistors. Here, C_{sb} and g_{mb} are neglected in comparison to C_{gs} and g_m of M_2 and M_4, respectively. In Fig. 9:

At node 3:

$$sC_{gs4}V_3 + \left(kg_{m3} + g_{mb3}\right)V_2 + g_{m4}V_3 = 0 \quad \text{... (18)}$$

$$V_3 = -\frac{\left(kg_{m3} + g_{mb3}\right)}{g_{m4} + sC_{gs4}} V_2 \quad \text{... (19)}$$

At node 2:

$$s\left(C_{sb1} + C_{sb3}\right)V_2 + \frac{V_2}{R_1 + \frac{1}{s\left(C_1 // C_{gs3}\right)}} - g_{m4}V_3 + \frac{V_2}{R_2 + \frac{1}{s\left(C_2 // C_{gs1}\right)}} + \frac{V_2 - V_1}{R} = 0 \quad \text{... (20)}$$

Assume $C_1 = C_2, C_{gs3} = C_{gs1}, R_1 = R_2$

$$s\left(C_{sb1} + C_{sb3}\right)V_2 + \frac{2s\left(C_1 // C_{gs3}\right)V_2}{1 + sR_1\left(C_1 // C_{gs3}\right)} - g_{m4}V_3 - i_{in} = 0 \quad \text{... (21)}$$

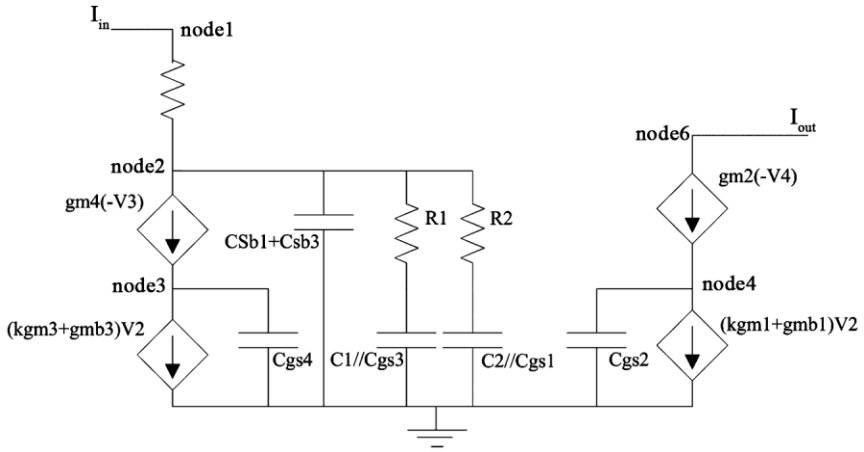

Fig. 9 – Small signal model for calculating bandwidth

From Eqs (19), (20) and (21):

$$i_{in}=\frac{2C_{gs4}C_{sb1}}{\left(g_{m4}+sC_{gs4}\right)}\times\left(s^2+\frac{g_{m4}}{C_{gs4}}s+\frac{g_{m4}\left(kg_{m3}+g_{mb3}\right)}{2C_{gs4}C_{sb1}}\right)V_2 \quad \text{... (22)}$$

At node 6:

$$i_{out}=-g_{m2}V_4 \quad \text{... (23)}$$

At node 4:

$$-g_{m2}V_4=\left(kg_{m1}+g_{mb1}\right)V_2+sC_{gs2}V_4 \quad \text{... (24)}$$

From Eqs (23) and (24):

$$i_{out}=\frac{g_{m2}}{g_{m2}+sC_{gs2}}\left(kg_{m1}+g_{mb1}\right)V_2 \quad \text{... (25)}$$

From Eqs (22) and (25):

$$A_I=\frac{i_{out}}{i_{in}}=\frac{g_{m2}\left(kg_{m1}+g_{mb1}\right)\left(g_{m4}+sC_{gs4}\right)}{2C_{gs4}C_{sb1}\left(g_{m2}+sC_{gs2}\right)}\times\frac{1}{\left(s^2+\frac{g_{m4}}{C_{gs4}}s+\frac{g_{m4}\left(kg_{m3}+g_{mb3}\right)}{2C_{gs4}C_{sb1}}\right)} \quad \text{... (26)}$$

Let $g_{m2}=g_{m4}$, $g_{mb2}=g_{mb4}$, $g_{m3}=g_{m1}$, $C_{gs2}=C_{gs4}$

$$A_I=\frac{i_{out}}{i_{in}}=\frac{g_{m2}\left(kg_{m1}+g_{mb1}\right)/2C_{gs4}C_{sb1}}{\left(s^2+\frac{g_{m4}}{C_{gs4}}s+\frac{g_{m4}\left(kg_{m3}+g_{mb3}\right)}{2C_{gs4}C_{sb1}}\right)} \quad \text{... (27)}$$

Hence:

$$\omega_{0,\text{Proposed}}=\sqrt{\frac{g_{m2}\left(kg_{m1}+g_{mb1}\right)}{2C_{gs2}C_{sb1,3}}} \quad \text{... (28)}$$

Similar analysis when carried for BDQFG based SHCCM (Fig. 4) results the bandwidth as:

$$\omega_{0,BDQFG}=\sqrt{\frac{g_{m2}\left(kg_{m1}+g_{mb1}\right)}{2C_{gs2}\left(C_{sb1,3}+\left(C_{1,2}\,//\,C_{gs3,1}\right)\right)}} \quad \text{... (29)}$$

And for the BD based SHCCM (Fig. 3), the bandwidth is given by:

$$\omega_{0,BD}=\sqrt{\frac{g_{m2}g_{mb1}}{2C_{gs2}C_{sb1,3}}} \quad \text{... (30)}$$

Comparing Eqs (29) and (30), the increased transconductance of M_1 results in high bandwidth for Fig. 4. However, the input capacitors and parasitic gate-to-source capacitances of M_3 and M_1 puts a limit on the bandwidth range. In this context, the proposed current mirror does not experience such effects and hence results in highest bandwidth as visible in Eq. (28).

4 Simulation Results

The current mirrors shown in Figs 3, 4 and 6 are simulated on UMC 0.18 μm mixed-mode twin-well technology at ± 0.2V supply with the help of HSpice simulator. The simulation results confirm the small signal analytical results. The MOS transistors width and length of referred current mirrors and proposed current mirror is listed in Table 2. The other assumed parameters for simulations are also listed in Table 2.

In Fig. 10, the output current is plotted in relation to output voltage for input current values till 200 μA in steps of 50 μA. As discussed, under DC conditions BDQFG behaves as BD MOS transistor so the overlapping for referred and proposed current mirror is observed. The overlapping of plots is also observed for current transfer characteristic shown in Fig. 11 for input current swept from 0 to 200 μA and the

corresponding percentage error in current transfer is shown in Fig. 12. The frequency response is shown in Fig. 13. It is observed that the proposed current mirror shows the highest bandwidth of 306 MHz over BD and BDQFG which provide 80 MHz and 180 MHz respectively. Further, the input and output impedance is shown in Figs 14 and 15, respectively where a negligible variation can be observed between BDQFG and proposed but better than BD based SHCCM.

The non-linearity analysis of BD, BDQFG and proposed current mirror is shown with the help of total harmonic distortion (THD) calculation for sinusoidal input current signal at frequency of 1 MHz, 10 MHz and 20 MHz at a quiescent current of 160 µA. The THD percentages at above stated frequencies are shown in Figs 16–18. It is observed that with increase in input signal amplitude and frequency there is corresponding increase in THD percentage. The THD is found to be much better than simple BD SHCCM and remains around 5% even for 20MHz input signal. Also a very slight variation in THD is observed between BDQFG and proposed current mirror.

The complete HSpice simulation results are summarized in Table 3 which concludes that the proposed current mirror results in high bandwidth over prior arts at the same level of power consumption.

Table 2 – *W* and *L* of MOS transistors used in BD, BDQFG and proposed current mirror

Transistors	*W* (µm)	*L* (µm)	Transistors	*W* (µm)	*L* (µm)
M_1	207	0.54	M_7	2.16	0.54
M_2	207	0.54	M_8	2.16	0.54
M_3	207	0.54	MR_1	10.08	0.54
M_4	207	0.54	MR_2	10.08	0.54
M_5	2.16	0.54	MP_1	0.36	0.36
M_6	2.16	0.54	MP_2	0.36	0.36

R=100 Ω ,*C1*=*C2*=1pf, supply= ± 0.2V

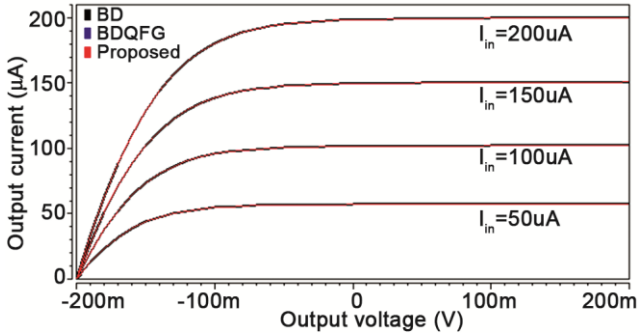

Fig. 10 – DC output characteristic of BD, BDQFG and proposed current mirror

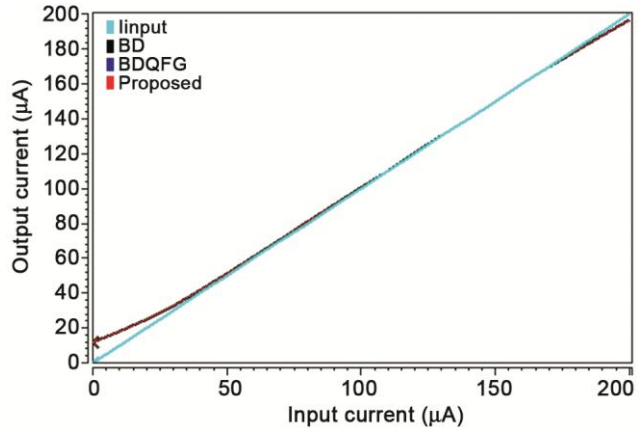

Fig. 11 – Current transfer characteristics of BD, BDQFG and proposed current mirror

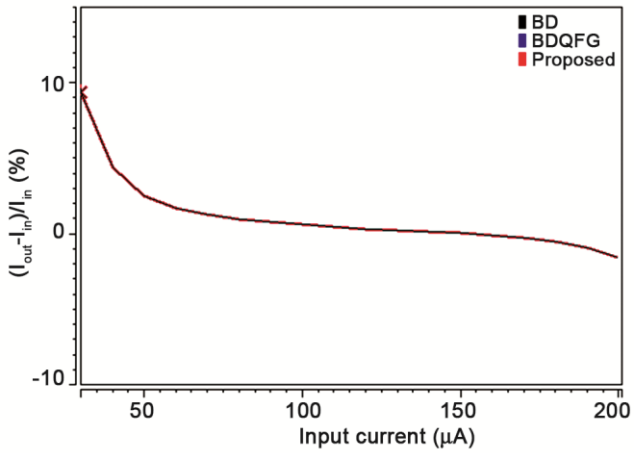

Fig. 12 – Percentage error in current transfer characteristics of BD, BDQFG and proposed current mirror

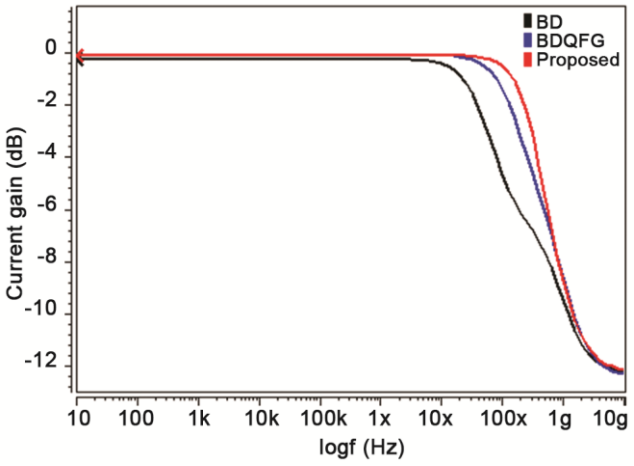

Fig. 13 – Frequency responses of BD, BDQFG and proposed current mirror

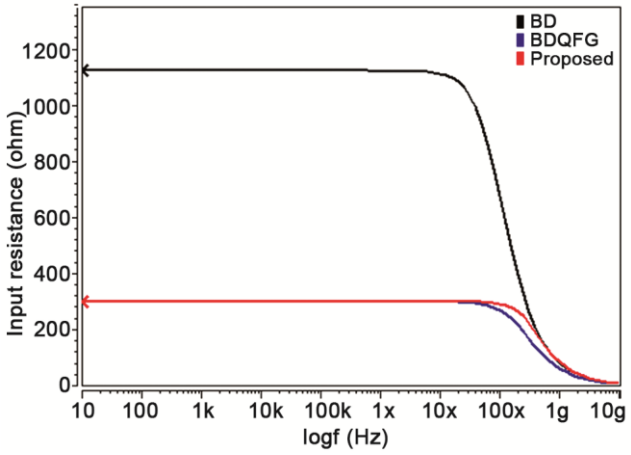

Fig. 14 – Input resistances of BD, BDQFG and proposed current mirror

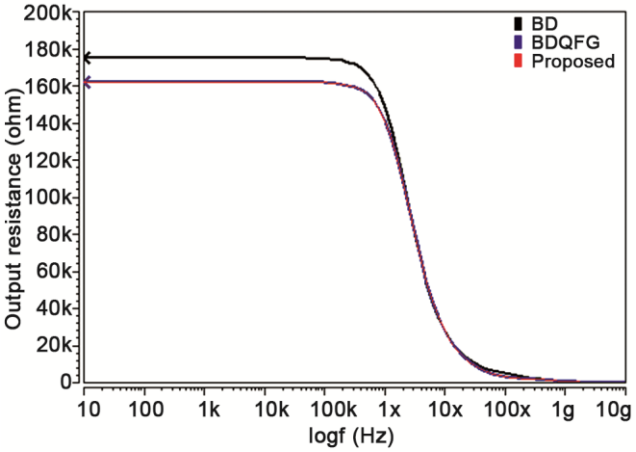

Fig. 15 – Output resistance of BD, BDQFG and proposed current mirror

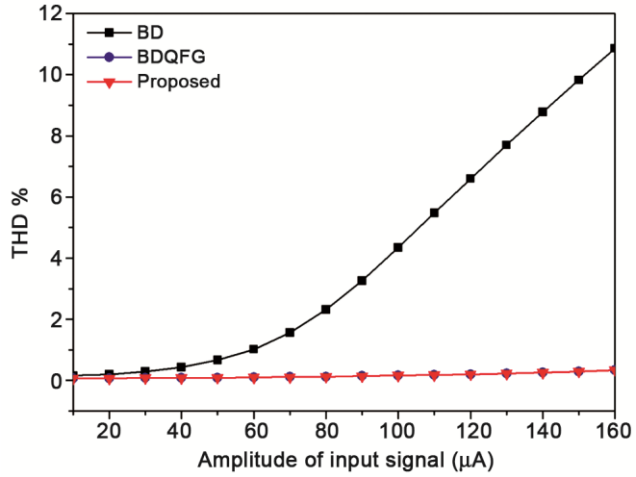

Fig. 16 – THD plot of BD, BDQFG and pProposed current mirror at 1MHz input sinusoidal signal

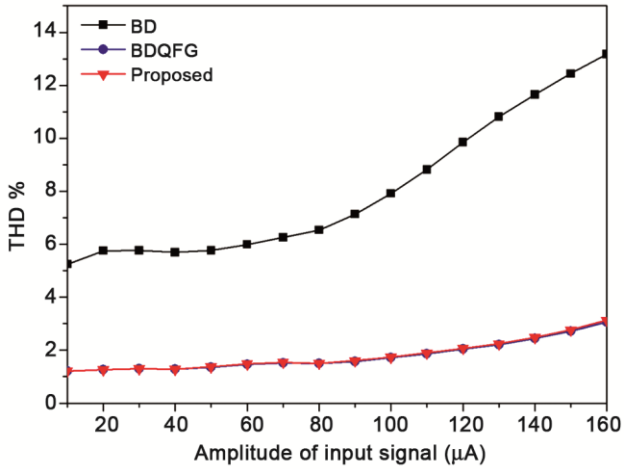

Fig. 17 – THD plot of BD, BDQFG and proposed current mirror at 10MHz input sinusoidal signal

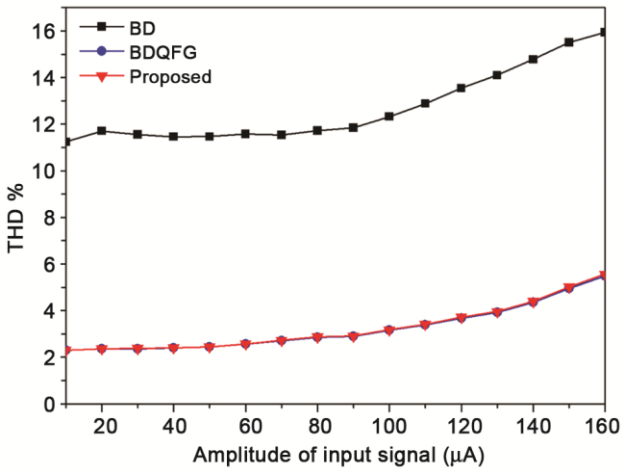

Fig. 18 – THD plot of BD, BDQFG and proposed current mirror at 20MHz input sinusoidal signal

Table 3 – Comparative analysis on Current Mirror performance

Parameters \ Reference	[25]	[20]	Proposed BDQFG SHCCM
Input current range (μA)	0-200	0-200	0-200
Input resistance (Ω)	1.16 k	306	306
Output resistance (Ω)	175 k	165 k	165 k
Bandwidth (MHz)	57	180	298
Supply (V)	± 0.2	± 0.2	± 0.2
Technology (μm)	UMC 0.18	UMC 0.18	UMC 0.18

5 Conclusions

In this paper, a high bandwidth BDQFG based SHCCM is presented. The achieved high bandwidth in without using any complex circuitry encourages its application for low power designs. The THD analysis carried proves the robustness of proposed current mirror. The complete analysis is carried out in

technology file of 0.18 μm provided by UMC with the help of HSpice.

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