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An Efficient Approach for Power Delivery Network Design With Closed-Form Expressions for Parasitic Interconnect Inductances

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Abstract—Investigation of a dc power delivery network, consisting of a multilayer PCB using area fills for power and return, involves the distributed behavior of the power/ground planes and the parasitics associated with the lumped components mounted on it. Full-wave methods are often employed to study the power integrity problem. While full-wave methods can be accurate, they are time and memory consuming. The cavity model of a rectangular structure has previously been employed to efficiently analyze the simultaneous switching noise (SSN) in the power distribution network. However, a large number of modes in the cavity model are needed to accurately simulate the impedance associated with the vias, leading to computational inefficiency. A fast approach is detailed herein to accelerate calculation of the summation associated with the higher-order modes. Closed-form expressions for the parasitics associated with the interconnects of the decoupling capacitors are also introduced. Combining the fast calculation of the cavity models of regularly shaped planar circuits, a segmentation method, and closed-form expressions for the parasitics, an efficient approach is proposed herein to analyze an arbitrary shaped power distribution network. While it may take many hours for a full-wave method to do a single simulation, the proposed method can generally perform the simulation with good accuracy in several minutes. Another advantage of the proposed method is that a SPICE equivalent circuit of the power distribution network can be derived. This allows both frequency and transient responses to be done with SPICE simulation.

Index Terms—Cavity resonators, circuit modeling, inductance, power distribution.

I. INTRODUCTION

MULTILAYER printed circuit boards (PCBs) employing entire layers or large area fills for power and ground planes are commonly used for dc power distribution for inte-

grated circuits (ICs) operating at a high speed. The power and ground planes essentially form a parallel plate wave guide. The parallel plate wave guide provides a good noise coupling path, which can lead to signal integrity (SI) problems, such as faulty switching of circuits or failure of systems. Noise coupled into the power distribution structure can also radiate through the fringing fields at the edges or can couple to nearby structures, resulting in electromagnetic interference (EMI) problems. Therefore, a good design of the power distribution network is essential to ensure signal integrity and to reduce the risk of EMI problems.

Full-wave numerical methods, such as the finite-difference time-domain (FDTD) method [1]–[3] and the partial-element equivalent circuit technique (PEEC) [4], [5], are often employed to investigate the power integrity problem. While full-wave methods are accurate, they are, in general, time and memory consuming. Methods to improve the efficiency of full-wave simulators, i.e., a parallel-distributed method [6], have been proposed in the literature. A power/ground structure with thickness much less than the smallest wavelength of interest can be considered as a two-dimensional (2-D) microwave planar circuit with n observable ports [7], and the associated Z-parameter matrix can be derived analytically using the cavity model for simple shapes. The cavity model of a rectangular power-bus structure developed for microstrip patch antennas [8] has been previously applied for power distribution networks in digital design as well [9]–[11]. For irregular shapes, a segmentation method can be employed [12], [13]. Therefore, the distributed behavior of an arbitrary shaped power distribution network can be characterized with the cavity model and the segmentation method. However, an infinite summation of modes appears in the Z-matrix of the cavity model. The infinite summation has to be truncated in a practical calculation. It is demonstrated in Section II that a large number of modes has to be included to model the impedance of vias with good accuracy. The calculation of a large number of modes leads to computational inefficiency, and it also increases the number of elements in the SPICE equivalent circuit. A Chebyshev expansion was applied to the high-order modes to accelerate the computation in microstrip antenna applications [14]. This algorithm is employed herein, and further approximations are made to speed up the calculation. Comparing the speed of the regular cavity model and that of the fast algorithm, a speed-up factor of seventy has

been achieved for the case demonstrated in Section II. The fast algorithm also significantly reduces the number of circuit elements for the SPICE simulation. In the case demonstrated in Section II, while 50 000 circuit elements were required for the regular cavity model to achieve good accuracy, only 180 elements were needed for the fast algorithm.

Considering only the distributed nature of the power distribution network, however, is not sufficient. Parasitics associated with the lumped component interconnects also play an important role in the response of the power distribution network. While there are many closed-form expressions of parasitic inductances [15]–[17], their applicability for calculating interconnect parasitics on PCBs is unknown. Full-wave methods are employed herein to verify closed-form expressions. This paper proposes an approach, which systematically combines the existing methods, namely, the cavity model with the fast algorithm, the segmentation method, and closed-form expressions for parasitic interconnect inductance, to effectively model a power distribution network. While it may take hours to do a single simulation with a full-wave approach, it only takes a few minutes for the proposed method. Moreover, with the equivalent circuit of the power distribution network, the appropriate port connections, and the interconnect parasitic inductances, a comprehensive circuit model can be derived for power integrity design of an irregularly shaped multilayer PCB, and it can be simulated with SPICE both in the time and frequency domains.

The modeling of the distributed nature of the power delivery network is presented in Section II. After a brief review of the cavity model, the effect of the high-order modes on the accuracy of the modeling is examined. Simulated results indicate that a large number of modes are needed to achieve good accuracy. A fast algorithm is then presented, and a factor of more than 70 in speed improvement is achieved for the fast algorithm as compared to the regular cavity model. The segmentation method is also summarized in Section II for completeness. The agreement between the measurements and the segmentation method in conjunction with the fast cavity model illustrate the applicability of the proposed method for the investigation of irregularly shaped power distribution networks. Closed-form expressions for the interconnect parasitics are given in Section III. The closed-form expressions were examined with a full-wave method for typical layout geometries of decoupling capacitors, and the errors relative to the full-wave method are explained based on the relevant physics. In Section IV, two examples are presented, one is a three-layer PCB with seven decoupling capacitors, and the other is a structure with three planes. Good agreement for both cases has been obtained. The conclusion is given in Section V.

II. FAST CALCULATION OF THE IMPEDANCE MATRIX OF A POWER AREA AND A SPICE EQUIVALENT CIRCUIT

A power delivery network having a thickness much less than the smallest wavelength of interest can be characterized by a 2-D Helmholtz equation in terms of the E-field normal to the planes, along with the open boundary conditions (perfect magnetic wall) around the periphery of the planes [7], [8]. Then, the power delivery network can be considered as a 2-D microwave

planar circuit with n external observation ports. For power and ground planes with simple shapes, such as a rectangle and an equilateral triangle, the impedance matrix can be obtained analytically [7], [9]–[11], as summarized in Table I.

The SPICE equivalent circuits for the rectangular and the equilateral triangular power distribution networks can be derived from (3) and (4) in Table I, respectively, as shown in Fig. 1. The effect of the interplane capacitance as well as each mode is represented in the equivalent circuit. Parameters C_0, L_{mn}, and G_{mn} can be calculated from the board dimensions and the dielectric properties, as given in Table I. The turns ratios of ideal transformers, N_{mni} $(i = 1, \ldots, n)$, contain information regarding the location and dimension associated with port i.

A. Fast Algorithm for the Cavity Model and the Corresponding Equivalent Circuit

The double infinite summations in (1) and (2) (see Table I) must be truncated in practice. An equilateral triangular power distribution network was constructed with a double-sided FR4 board to investigate the effect of the number of calculated modes on the response of the network. The thickness of the board was 1.27 mm (50 mils), and the edge length a was 20 cm, as shown in Table I. A surface-mount assembly (SMA) connector was soldered at (4.5 cm, 2.6 cm) as the feeding port, and S_{11} was measured with an HP8753D network analyzer. Port extensions were performed to extend the measurement reference plane to the ground plane of the board. So, only the center conductor of the SMA connector inside the board needs to be considered in the modeling. The measured S_{11} values were converted to the input impedance $|Z_{\text{in}}|$ as shown in Fig. 2. The input impedance $|Z_{\text{in}}|$ was also calculated using (2) with a relative dielectric constant of $\varepsilon_r = 4.3$, and a loss tangent of $\tan \delta = 0.02$. The inductive behavior of the SMA center conductor inside the plane pair is included in the cavity model, as explained in Section III. While the discrepancy between the measurement and the cavity result truncated at $n \times m = 20 \times 20$ modes is large, the agreement between the measurement and the cavity result truncated at 200×200 modes is good, indicating that the high-order modes affect the accuracy of the cavity model, especially for the nulls where the impedance is low. However, it is not computationally efficient to calculate the cavity model with a large number of modes, especially for the case of a large number of ports, which is common in a practical design, since each IC pin of interest and each decoupling capacitor introduces a port. An efficient algorithm for calculating the high-order modes is presented next.

The term $1/(k^2 - k_{mn}^2)$ in (1) and (2) in Table I can be expanded in Chebyshev polynomials for $k_{mn} \geq 2k$ as [18]

$$\frac{1}{k^2 - k_{mn}^2} = -\frac{1}{k_{mn}^2} \left[0.989 + 0.333 \frac{k^2}{k_{mn}^2} + e \left(\frac{k}{k_{mn}} \right) \right],$$
$$\left| e \left(\frac{k}{k_{mn}} \right) \right| < 0.013. \quad (5)$$

The approximation in (5) can be applied to both the rectangular and the equilateral triangular geometries. The rectangular geometry is used below to demonstrate the fast calculation algorithm.

TABLE I
IMPEDANCE MATRICES AND NETWORK PARAMETERS FOR RECTANGULAR AND EQUILATERAL TRIANGULAR POWER AREA FILLS

	Rectangle	Equilateral triangle
Geometry		
Impedance matrix	$$Z_{ij}(\omega) = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \frac{j\omega\mu d N_{mni}N_{mnj}}{ab\left(k_{mn}^2 - k^2\right)} \quad (1)$$ m and n: the mode indices $$k_{mn}^2 = \left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2$$ $$k = \omega\sqrt{\varepsilon\mu}\left(1 - j\frac{\tan\delta + r/d}{2}\right)$$ $$r = \sqrt{\frac{2}{\omega\mu\sigma}}$$ $$N_{mni} = c_m c_n \cos(\frac{m\pi x_i}{a})\cos(\frac{n\pi y_i}{b})$$ $$\sin c(\frac{m\pi W_{xi}}{2a})\sin c(\frac{n\pi W_{yi}}{2b})$$ $$c_m, c_m = \begin{cases} 1 & m,n = 0 \\ \sqrt{2}, & m,n \neq 0 \end{cases}$$	$$Z_{ij} = \frac{4j\omega\mu d}{\sqrt{3}a^2}\sum_{-\infty}^{+\infty}\sum_{-\infty}^{+\infty}\frac{\left(N_{1mni}N_{1mnj} + N_{2mni}N_{2mnj}\right)}{k_{mn}^2 - k^2} \quad (2)$$ m, n and l: $m + n + l = 0$, the mode indices $$k_{mn}^2 = \frac{16\pi^2}{9a^2}\left(m^2 + mn + n^2\right),$$ $$k = \omega\sqrt{\varepsilon\mu}\left(1 - j\frac{\tan\delta + r/d}{2}\right),$$ $$N_{1mni} = Pl(x_i, y_i, l, m, n)$$ $$+ Pl(x_i, y_i, m, n, l) + Pl(x_i, y_i, n, l, m)$$ $$N_{2mni} = P2(x_i, y_i, l, m, n)$$ $$+ P2(x_i, y_i, m, n, l) + P2(x_i, y_i, n, l, m)$$ $$Pl(x_i, y_i, l, m, n,) = \frac{(-1)^l}{3}\cos(\frac{2\pi l x_i}{\sqrt{3}a})\sin c(\frac{\pi l W_{xi}}{\sqrt{3}a}),$$ $$\cos(\frac{2\pi(m-n)y_i}{3a})\sin c(\frac{\pi(m-n)W_{yi}}{3a})$$ $$P2(x_i, y_i, l, m, n,) = \frac{(-1)^l}{3}\cos(\frac{2\pi l x_i}{\sqrt{3}a})\sin c(\frac{\pi l W_{xi}}{\sqrt{3}a})$$ $$\sin(\frac{2\pi(m-n)y_i}{3a})\sin c(\frac{\pi(m-n)W_{yi}}{3a})$$
Equivalent circuit representation	$$Z_{ij}(\omega) = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{N_{mni}N_{mnj}}{\frac{1}{j\omega L_{mn}} + j\omega C_0 + G_{mn}} \quad (3)$$ $$\omega_{mn} = \frac{1}{\sqrt{\varepsilon\mu}}k_{mn}, \; C_0 = \frac{ab\varepsilon}{d}, \; L_{mn} = \frac{1}{C_0\omega_{mn}^2},$$ $$G_{mn} = C_0\omega_{mn}(\tan\delta + \frac{r}{d})$$	$$Z_{ij}(\omega) = \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty}\frac{N_{1mni}N_{1mnj} + N_{2mni}N_{2mnj}}{\frac{1}{j\omega L_{mn}} + j\omega C_0 + G_{mn}} \quad (4)$$ $$\omega_{mn} = \frac{1}{\sqrt{\varepsilon\mu}}k_{mn}, \; C_0 = \frac{\sqrt{3}a^2\varepsilon}{4d},$$ $$L_{mn} = \frac{1}{C_0\omega_{mn}^2}, \; G_{mn} = C_0\omega_{mn}(\tan\delta + \frac{r}{d})$$

If k_0 corresponds to the highest frequency of interest, (1) can be approximated by

$$Z_{ij} \approx \frac{j\omega\mu d}{ab}\left(\sum_{k_{mn}<2k_0}\frac{N_{mni}N_{mnj}}{k_{mn}^2 - k^2} + X_0 + X_1 k^2\right) \quad (6)$$

where

$$X_0 = 0.989\left(\sum_{m=0}^{\infty}\sum_{n=0,(m,n)\neq(0,0)}^{\infty}\frac{N_{mni}N_{mnj}}{k_{mn}^2} - \sum_{k_{mn}<2k_0,(m,n)\neq(0,0)}\frac{N_{mni}N_{mnj}}{k_{mn}^2}\right)$$
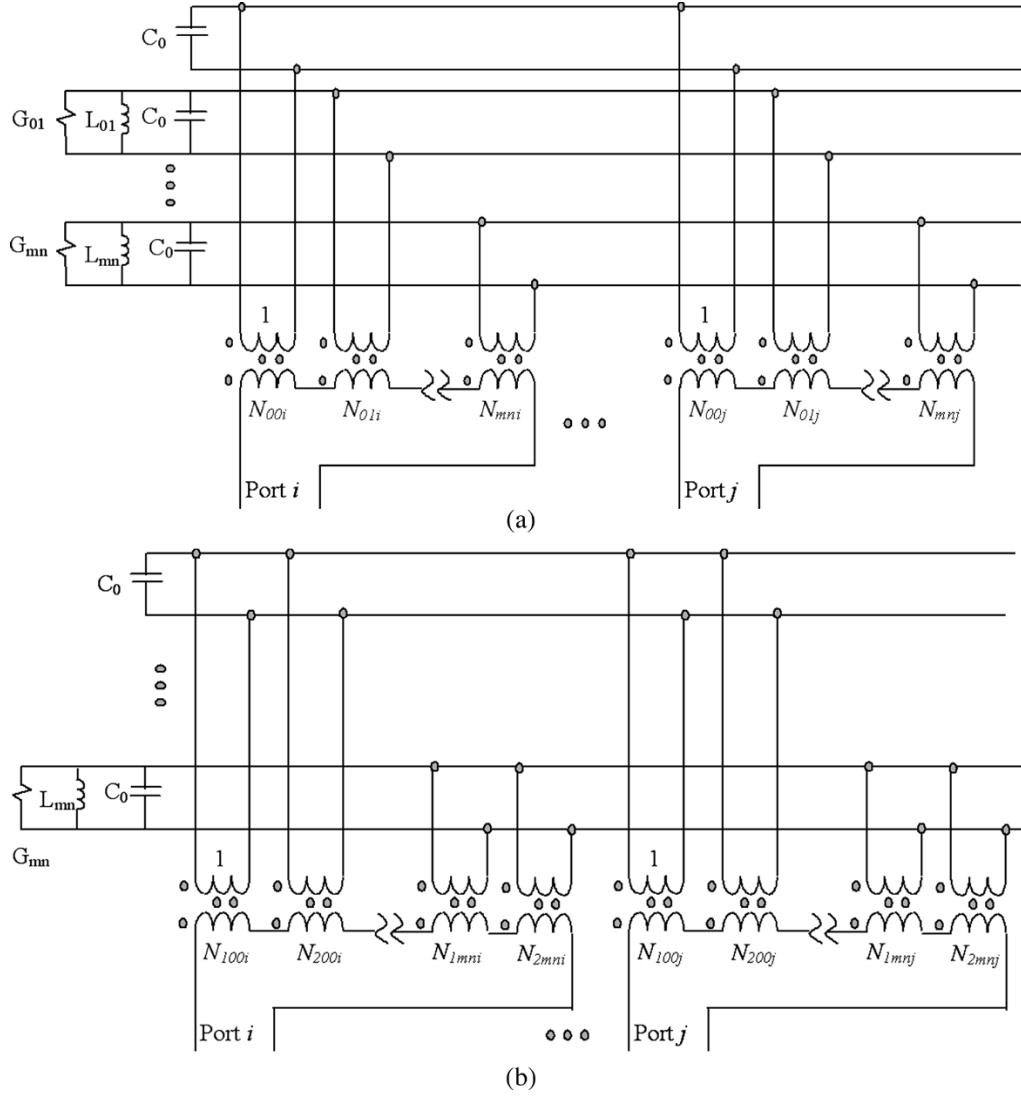
Fig. 1.   Eequivalent circuits of a rectangular and an equilateral triangular power distribution network. (a) Equivalent circuit of a rectangular power distribution network. (b) Equivalent circuit of an equilateral triangular power distribution network.
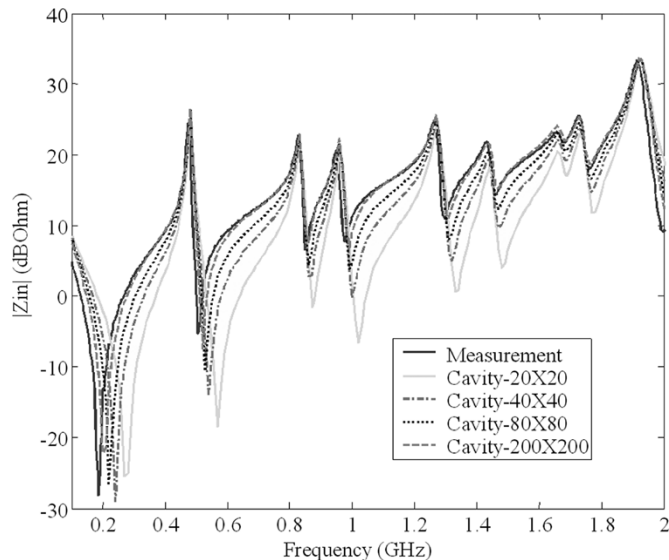

Fig. 2.   Accuracy of the cavity model as a function of the number of modes for an equilateral triangular structure with lateral length of $a = 20$ cm.

and

$$X_1 = 0.333 \left(\sum_{m=0}^{\infty} \sum_{n=0,(m,n)\neq(0,0)}^{\infty} \frac{N_{mni}N_{mnj}}{k_{mn}^4} \right.$$
$$\left. - \sum_{k_{mn}<2k_0,(m,n)\neq(0,0)} \frac{N_{mni}N_{mnj}}{k_{mn}^4} \right).$$

Since the terms X_0 and X_1 are independent of frequency, they need to be calculated only once for the entire frequency range of interest. Therefore, (6) represents a considerable improvement in the speed of the overall calculation time.

Since the second term in (5) varies as k^2/k_{mn}^2, it can be neglected in comparison to the first term when k_{mn} is large compared to k. The maximum error in neglecting the second term in (5) is less than 10% for $k_{mn} > 2k$. Consequently, the cavity model can be further approximated by

$$Z_{ij} \approx \frac{j\omega\mu d}{ab} \left(\sum_{k_{mn}<2k_0} \frac{N_{mni}N_{mnj}}{k_{mn}^2 - k^2} + X_0 \right). \tag{7}$$

Employing a Fourier series summation formula $\sum_{m=0}^{\infty}(C_m\cos mx/(m^2-\alpha^2))= -(\pi/\alpha)(\cos(x-\pi)\alpha/\sin\pi\alpha)$ [19], the double summation $\sum_{m=0}^{\infty}\sum_{n=0,(m,n)\neq(0,0)}^{\infty}(N_{mni}N_{mnj}/k_{mn}^2)$ in X_0 can be reduced to a single summation leading to [20]

$$\frac{j\omega\mu d}{ab}\sum_{m=0}^{\infty}\sum_{n=0,(m,n)\neq(0,0)}^{\infty}\frac{N_{mni}N_{mnj}}{k_{mn}^2}$$
$$\approx\sum_{n\neq0}^{\infty}\frac{\omega\mu da}{j2b}C_n\cos\left(\frac{n\pi y_i}{b}\right)\cos\left(\frac{n\pi y_j}{b}\right)$$
$$\times\operatorname{sinc}\left(\frac{n\pi W'_{yi}}{2b}\right)\operatorname{sinc}\left(\frac{n\pi W'_{yi}}{2b}\right)$$
$$\times\frac{[\cos(\alpha_n x_-)+\cos(\alpha_n x_+)]}{\alpha_n\sin\alpha_n}\qquad(8)$$

where $\alpha_n=ja(n\pi/b)$, $x_\pm=1-|x_i\pm x_j|/a$. The approximation $\sin c(m\pi W_{xi}/2a)\sin c(m\pi W_{xj}/2a)\approx1$ was made to obtain (8). This approximation models the rectangular port i as an equivalent flat strip of width W'_{yi}. The equivalent strip width can be found as [21]

$$W'_{yi}=\exp\left(\frac{3}{2}\right)r_i\qquad(9)$$

where r_i is the radius of a circular port with the same cross-sectional area of the rectangular port. Since α_n is imaginary, the series in (8) converges rapidly. Therefore, a fast single summation calculation for the impedance matrix can be achieved. The fast single summation is particularly useful when the number of ports is large.

The reactance term $(j\omega\mu d/ab)X_0$ in (7) represents the contributions of the high-order modes. Since it is linearly dependent on the frequency, the reactance term can be represented by an inductance as

$$L^{ij}=\frac{\mu d}{ab}X_0.\qquad(10)$$

An equivalent circuit representation for the fast calculation is then shown in Fig. 3. The L^{ii} represents a "self" inductance associated with port i, and L^{ij} represents a "mutual" inductance between ports i and j.

A test board was built to verify the fast algorithm. The test board was a 15.2 by 9-cm double-sided board with a feeding port at (12.2 cm, 6 cm) and a shorting pin at (3 cm, 3 cm), as shown in Fig. 4. The dielectric layer between the two solid planes was 50 mils thick with a relative permittivity of $\varepsilon_r=4.3$ and a loss tangent of $\tan\delta=0.02$. An SMA connector was mounted as the feeding port, and the width of the center conductor of the SMA connector was 1.27 mm (50 mils). The diameter of the shorting pin was also 1.27 mm (50 mils). The input impedance was measured from 100 MHz to 3 GHz using an HP8753C network analyzer. The input impedance was also simulated using the cavity model with the voltage at the shorting port set to zero. The results are shown in Fig. 4, and good agreement between the measurements and the cavity modeling results was obtained. A summation over 100×100 modes was required to achieve the accuracy shown. The CPU time for the regular cavity model as
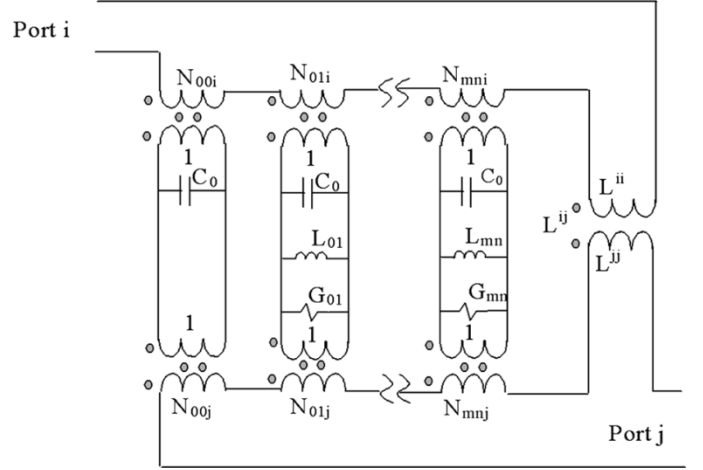

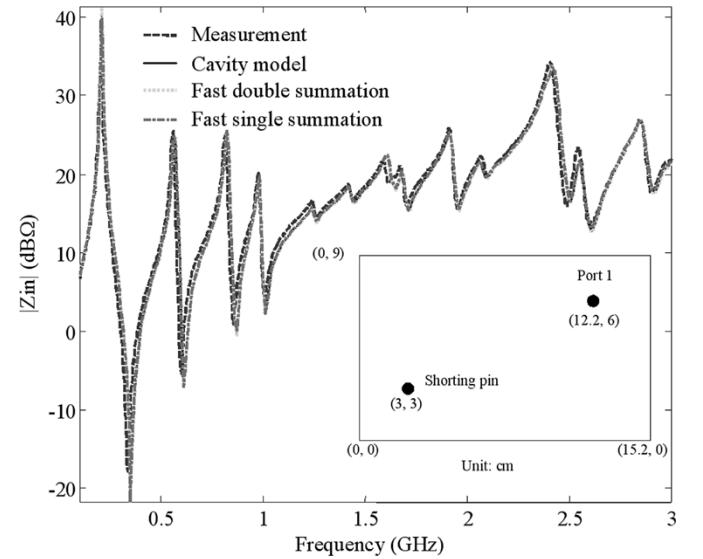Fig. 3. SPICE equivalent circuit for the fast algorithm.

Fig. 4. Comparison of the measurements, the regular cavity model, and the fast algorithm for the input impedance of the two-layer board with a shorting pin.

TABLE II
CALCULATION TIME USING DIFFERENT CALCULATION APPROACHES FOR THE TWO-LAYER BOARD WITH A SHORTING PIN

Approach	Regular cavity model	Fast double summation	Fast single summation
CPU time (s)	261.3	4.84	3.53

in (1), the fast double summation approach as in (7), and the fast single summation approach as in (8) are listed in Table II. An AMD 1.4-GHz computer was used to perform all the calculations. The truncated mode number for all the approaches was set to $m=n=100$. While it took 261 s for the regular cavity model to calculate 100×100 modes, it only took 4.8 s for the fast double summation algorithm, and the CPU time was further reduced to 3.5 s when the fast single summation was employed. From Fig. 4, it is seen that the results of measurements, the regular cavity model, the fast double summation and the single summation match closely over the entire frequency range, indicating the accuracy of the fast algorithm. Accuracy
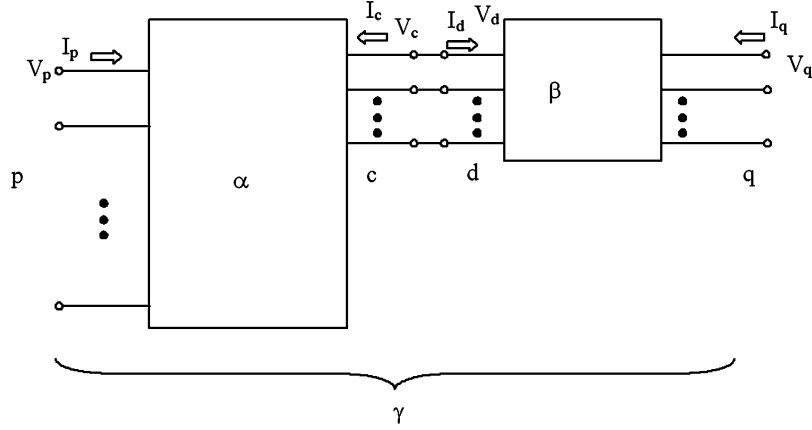
Fig. 5.   Illustration of the segmentation method for a power distribution network of an irregular shape.

of the proposed equivalent SPICE model in the time domain is demonstrated in [22].

B. Segmentation Method

For a power-bus with an irregular shape, a segmentation method can be used for analysis [12], [13], if the pattern can be divided into segments having regular shapes. Consider the planar circuit shown in Fig. 5. The continuous interconnection between the α- and β-segments is replaced by a discrete number of interconnected ports, denoted c-ports on the α-segments and d-ports on the β-segments. Ports p and q are the external (unconnected) ports of the α- and β-segments, respectively. The Z-matrices for α-, β-, and γ-segments, namely, $\widetilde{Z}_\alpha$, $\widetilde{Z}_\beta$, and $\hat{Z}_\gamma$, respectively, can be partitioned into submatrices corresponding to the external (unconnected) and connected ports as

$$\widetilde{Z}_\alpha = \begin{bmatrix} \widetilde{Z}_{pp\alpha} & \widetilde{Z}_{pc} \\ \widetilde{Z}_{cp} & \widetilde{Z}_{cc} \end{bmatrix} \tag{11}$$

$$\widetilde{Z}_\beta = \begin{bmatrix} \widetilde{Z}_{dd} & \widetilde{Z}_{dq} \\ \widetilde{Z}_{qd} & \widetilde{Z}_{qq\beta} \end{bmatrix} \tag{12}$$

$$\widetilde{Z}_\gamma = \begin{bmatrix} \widetilde{Z}_{pp\gamma} & \widetilde{Z}_{pq} \\ \widetilde{Z}_{qp} & \widetilde{Z}_{qq\gamma} \end{bmatrix}. \tag{13}$$

Enforcing the continuity of voltage and current on ports c and d, $\widetilde{Z}_\gamma$ can be calculated as [13]

$$\widetilde{Z}_\gamma = \begin{bmatrix} \widetilde{Z}_{pp\alpha} - \widetilde{Z}_{pc}\widetilde{Z}'_{dp} & \widetilde{Z}_{pc}\widetilde{Z}'_{dq} \\ \widetilde{Z}_{qd}\widetilde{Z}'_{dp} & \widetilde{Z}_{qq\beta} - \widetilde{Z}_{qd}\widetilde{Z}'_{dq} \end{bmatrix} \tag{14}$$

where $\widetilde{Z}'_{dp} = [\widetilde{Z}_{cc} + \widetilde{Z}_{dd}]^{-1}\widetilde{Z}_{cp}$ and $\widetilde{Z}'_{dq} = [\widetilde{Z}_{cc} + \widetilde{Z}_{dd}]^{-1}\widetilde{Z}_{dq}$. It is straightforward to apply the segmentation method to the equivalent circuit by simply connecting the c-ports of the α-circuit to the d-ports of the β-circuit.

Fig. 6 shows a test board with FR4 as the dielectric material. The board thickness was 1.02 mm (40 mil). Two SMA connectors were soldered on the board to measure the Z-parameters. In the cavity model, the pattern was divided into three smaller rectangles with each piece modeled using (1). In the calculations, four discrete interconnected ports were used to represent the continuous interconnection between two adjoining rectangles. Then, the impedance for the entire board was calculated
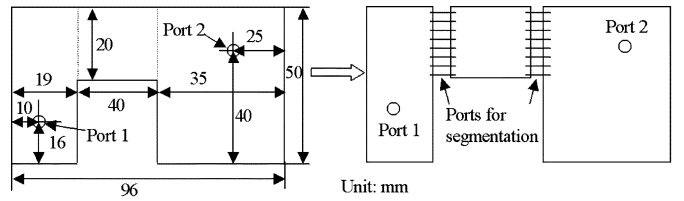

Fig. 6.   Irregular shaped power/ground structure for the demonstration of the segmentation method.

using the segmentation method. The relative dielectric constant was $\varepsilon_r = 4.3$, and the loss tangent was $\tan\delta = 0.02$ in the model. The modeled results agree well with the measured results for both $|Z_{11}|$ and $|Z_{21}|$, as shown in Fig. 7.

III. CALCULATION OF PARASITIC INDUCTANCES

Decoupling capacitors are widely used in power delivery networks to mitigate switching noise from ICs. Decoupling capacitors can provide a low-impedance path to shunt transient energy to ground at the IC source in relatively low frequency ranges. However, a real capacitor includes both parasitic inductance and parasitic resistance associated with the interconnects and the package of the capacitors. The global decoupling capacitors are generally not effective in the high-frequency range when it acts as a high-impedance element due to the series parasitic inductance [23], [24]. While local decoupling capacitors can be effective up to the gigahertz range due to the mutual coupling between the two vias associated with the capacitors and its adjacent IC device, its benefit cannot be effectively achieved when the ratio of L_2/L_1, as shown in Fig. 8, is approximately greater than one [5]. Therefore, closed-form expressions of the parasitic inductances are desired for quantifying the layout of the decoupling capacitors on a power delivery network for both global and local decoupling. The parasitic inductance calculated with closed-form expressions can also be incorporated in the equivalent circuit of the power delivery network for SPICE simulations.

The current path of the decoupling capacitor can be decomposed into two loops, as shown in Fig. 8. One is the loop formed by the current flowing through the capacitor and the current flowing on the upper surface of the return plane, denoted by
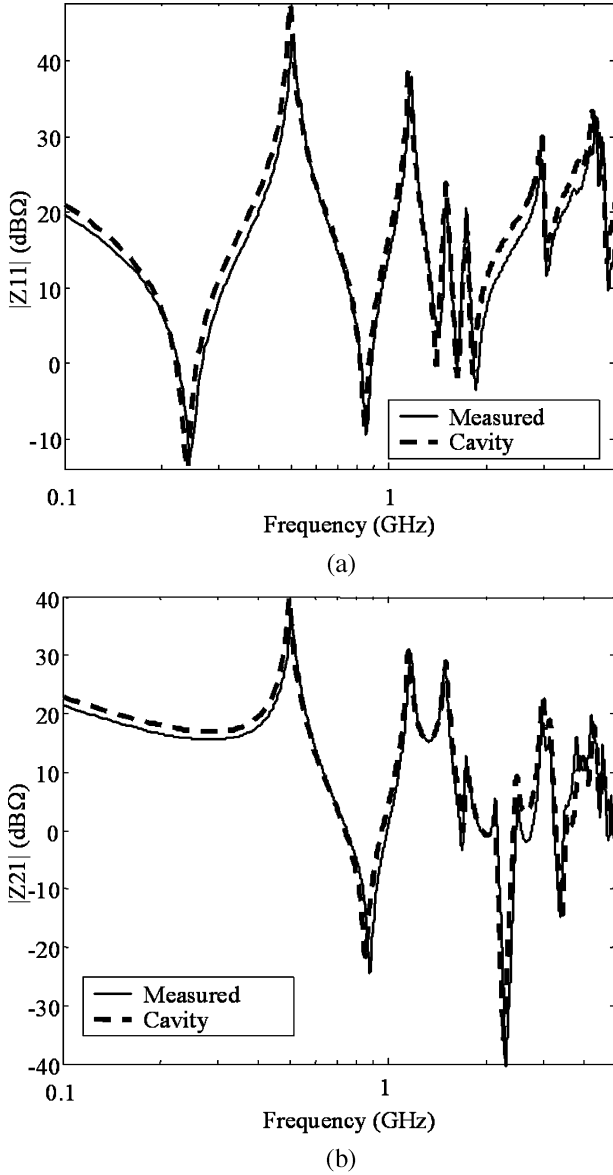
Fig. 7. Self and transfer impedances of the power/ground structure with an irregular shape.
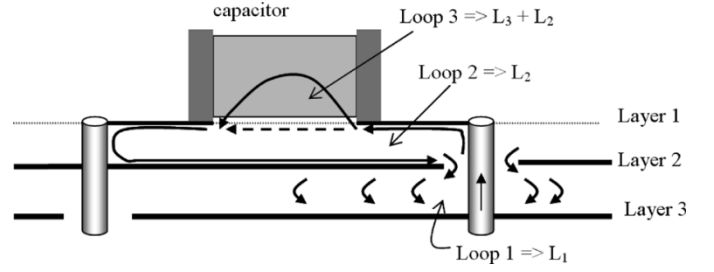

Fig. 8. Illustration of parasitic inductances associated with a decoupling capacitor.

to use an approximated value for engineering estimations. The approximated value can be obtained by well-designed methods [25], and the method using an impedance analyzer with open and short compensation is employed herein. The focus of this paper is on the calculations of L_1 and L_2.

The inductance L_1 is associated with the current flowing through the via. Since the input impedance of the cavity model was derived from the Green's function for a spatial delta current density injected perpendicularly into the planes [7], L_1 is included in the cavity model in the infinite summation expressions (1) and (2). It should be noted that since the boundary condition at the feed port is replaced with an impressed source, that while the feed port inductance is included for L_1 in the cavity model, the mutual inductance associated with a changing current distribution on the two vias while bringing two-ports in proximity [23], is not. It was demonstrated that L_1 was associated with the high-order modes in the cavity model, and was dependent on the position of the via [26]. A closed-form expression of L_1 was given in [27]. For multilayer applications, the parasitic inductance associated with the interconnect segment inside the planes can also be taken into account by connecting ports of multiple cavity models, as illustrated in Section IV-B. This section focuses on the closed-form expression of the loop inductance above the planes, L_2.

The flux wrapping Loop 2 in Fig. 8 can be decomposed approximately into two orthogonal contributions: the flux due to the vertical geometry defined by the vias, as shown in Fig. 9(b), and the flux due to the horizontal geometry encompassed by the trace and the upper plane, as shown in Fig. 9(c) [16]. For $(l/d) > 2.5$, the current distribution can be assumed uniform both along the periphery of the via, and along the length of the via [16]. Then, the inductance associated with the first contribution, i.e., from the vias, can be calculated as [16]

$$M_{ps} = \frac{\mu_0}{2\pi} h_s \left\{ \ln \left[\frac{h_s}{l} + \sqrt{1 + \left(\frac{h_s}{l} \right)^2} \right] \right.$$
$$\left. + \frac{l}{h_s} - \sqrt{1 + \left(\frac{l}{h_s} \right)^2} \right\} \qquad (15a)$$

$$L_{ps} = \frac{\mu_0}{2\pi} h_s \left\{ \ln \left[\frac{h_s}{r_w} + \sqrt{1 + \left(\frac{h_s}{r_w} \right)^2} \right] \right.$$
$$\left. + \frac{r_w}{h_s} - \sqrt{1 + \left(\frac{r_w}{h_s} \right)^2} \right\} \qquad (15b)$$

$$L_{\text{via}} = 2(L_{ps} - M_{ps}) \qquad (15c)$$

Loop 3 in Fig. 8. Another portion of the interconnect inductance results from the current flowing along the via connected to the lower plane denoted by L_1. The coupling between these two loops can be neglected if the plane structure is sufficiently large, and the flux penetrating through the via antipad is negligible. The parasitic inductance associated with Loop 3 can be approximated by a summation of L_2 and L_3. The inductance L_2 corresponds to the current loop Loop 2 when the capacitor is shorted by a trace that is directly on top of the PCB, as indicated by the dashed arrow and the current path on the return plane. The inductance L_3 is defined as the difference between the inductance associated with Loop 3 and the inductance associated with Loop 2, and it is caused by the current path deviation in the capacitor. The inductance L_3 denotes the increament in inductance between an ideal current path and the real current path through the capacitor. While L_3 is dependent on the capacitor mounting structure, i.e., it is dependent on the distance between the capacitor and the return plane, it is reasonable
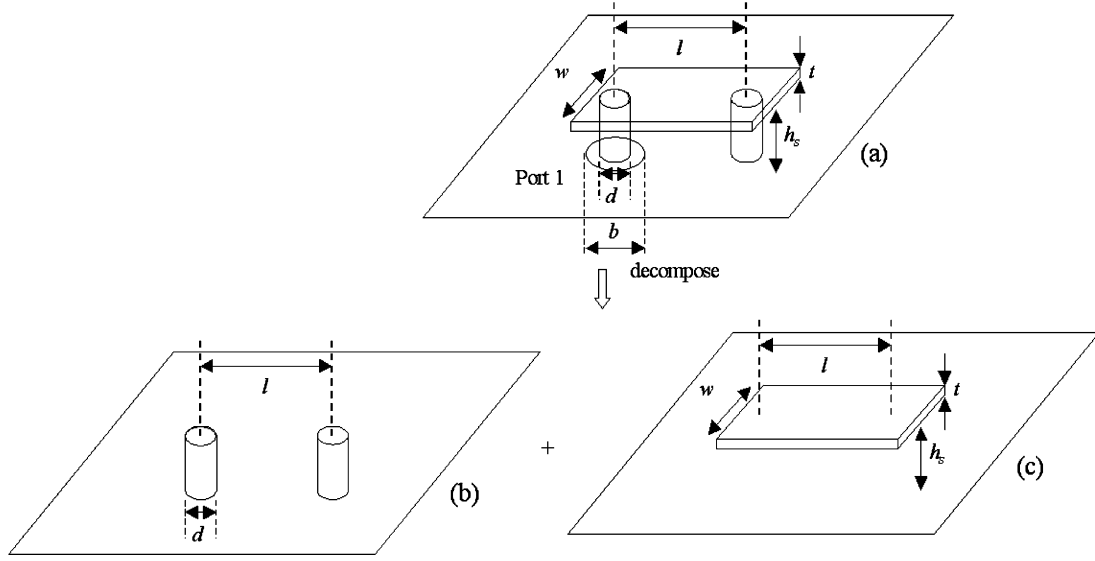
Fig. 9. Decomposing Loop 2 into two contributions to calculate the inductance.

where r_w is the radius of the via, $r_w = d/2$. Definitions of other parameters in these equations are shown in Fig. 9.

The inductance associated with the contribution from the microstrip can be calculated using image theory to remove the plane. The resulting closed-form expression has been derived in [17]. The mutual inductance between the microstrip and its image M_t and the self-inductance of the microstrip L_t are

$$
\begin{aligned}
M_t = \frac{0.001}{w^2} \Bigg(& -\frac{2}{3}(w^2 - 2p^2 + l^2)\sqrt{w^2 + p^2 + l^2} \\
& + l(w^2 - p^2)\ln\left(\frac{l + \sqrt{w^2 + p^2 + l^2}}{-l + \sqrt{w^2 + p^2 + l^2}}\right) \\
& + \frac{2}{3}(w^2 - 2p^2)\sqrt{w^2 + p^2} \\
& + l^2 w \ln\left(\frac{w + \sqrt{w^2 + p^2 + l^2}}{-w + \sqrt{w^2 + p^2 + l^2}}\right) \\
& - 4wpl \cdot \tan^{-1}\left(\frac{wl}{p\sqrt{w^2 + p^2 + l^2}}\right) \\
& + \frac{2}{3}(-2p^2 + l^2)\sqrt{p^2 + l^2} \\
& + p^2 l \ln\left(\frac{l + \sqrt{p^2 + l^2}}{-l + \sqrt{p^2 + l^2}}\right) + \frac{4p^3}{3} \Bigg)
\end{aligned}
\tag{16a}
$$

$$
\begin{aligned}
L_t = \frac{0.002}{3w^2} \Bigg(& 3w^2 l \ln\left(\frac{l + \sqrt{w^2 + l^2}}{w}\right) \\
& \times 3l^2 w \ln\left(\frac{w + \sqrt{w^2 + l^2}}{l}\right) \\
& - (w^2 + l^2)^{\frac{3}{2}} + l^3 + w^3 \Bigg)
\end{aligned}
\tag{16b}
$$

where $p = 2h_s$. Then the total inductance associated with the horizontal geometry L_{trace} is

$$
L_{\text{trace}} = L_t - M_t.
\tag{16c}
$$

The derivation in [17] assumed a uniform current distribution along the length and width of the trace. The total inductance L_2 associated with Loop 2 in Fig. 8 is then

$$
L_2 = L_{\text{via}} + L_{\text{trace}}.
\tag{17}
$$

The inductance L_2 is meaningful only at low frequencies when the input impedance associated with Loop 2 can be viewed as linearly dependent on the frequency. However, at high frequencies, Loop 2 behaves like a transmission line. Assuming the transmission line is lossless, the input impedance can be written as $Z_{in} = jZ_0 \tan(2\pi(l/\lambda))$, where l is the length of the transmission line, and λ is the wavelength. If l is much less than λ, Z_{in} can be approximated as $Z_{in} \approx jZ_0(2\pi(l/\lambda))$, exhibiting inductive behavior. The error of this approximation is within 10% for $l/\lambda < 0.08$, and within 20% for $l/\lambda < 0.11$.

A full-wave method, CEMPIE, was employed to evaluate (17) and the underlying approximation, for calculating the parasitic interconnect inductance associated with SMT capacitors. CEMPIE is a circuit extraction approach based on a mixed-potential integral equation formulation [28], and is a type of partial element equivalent circuit (PEEC) formulation [29]–[31]. It employs an integral equation formulation with a quasistatic layered media dyadic Green's function, and enforces the boundary condition on metal surfaces. If a perfect electric conductor (PEC) boundary condition is used for the metal surfaces, the electric field integral equation can be written as

$$
\hat{n} \times \left[j\omega \int_{S1+S2} \overline{\overline{G}}^A(\vec{r}, \vec{r}') \bullet \vec{J}(\vec{r}')ds' + \nabla\phi(\vec{r}) \right] = 0,
$$
$$
\vec{r} \in S1 \cup S2 \tag{18}
$$

where $S1$ represents the horizontal metal surfaces, corresponding to PCB planes and traces; S2 represents the vertical metal surfaces, corresponding to the vias; $\vec{J}$, $\overline{\overline{G}}^A$, and ϕ are the current density, the quasistatic dyadic Green's function, and the scalar electric potential, respectively. Applying the method of moments to (18), with Rao, Wilton, and Glisson (RWG)
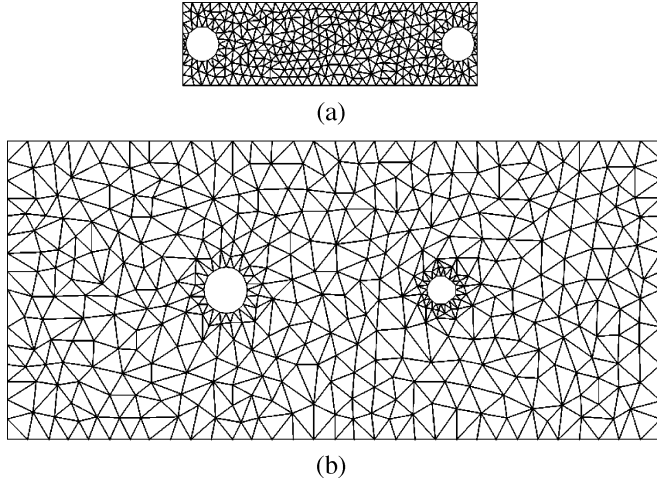
(a)

(b)

Fig. 10.   Discretization in CEMPIE for modeling the parasitics associated with a decoupling capacitor. (a) Mesh of the microstrip. (b) Mesh of the return plane.

basis functions for the planar surfaces [32], and roof-top basis functions for the vertical (via) surfaces, and assuming ϕ is constant within a cell, the edge current i can be related to ϕ as

$$j\omega[L][i] - [\Lambda][\phi] = 0 \tag{19}$$

where $[L]$ is the branch-wise inductance due to its coefficient $j\omega$, and $[\Lambda]$ is the connectivity matrix that relates cell quantities to edge quantities. Defining a nodal current I as the total current flowing out of a mesh cell, and applying the continuity of current, the surface charge Q on each cell can be related to I as

$$-j\omega[Q] = [I] + [I^e] \tag{20}$$

where I^e is the external impressed current on the cells. The nodal current I can be related to the edge current i with the connectivity matrix as $[I] = [\Lambda^T][i]$. The surface charge Q can be related to ϕ by the scalar electric potential Green's functions as $[\phi] = [K][Q]$. A mixed-potential integral equation can then be derived as

$$\begin{bmatrix} j\omega C & \Lambda^T \\ -\Lambda & j\omega L \end{bmatrix} \begin{bmatrix} \phi \\ i \end{bmatrix} = \begin{bmatrix} -I^e \\ 0 \end{bmatrix}, \quad \text{where } [C] = [K]^{-1}. \tag{21}$$

A relationship between the node potential ϕ and the impressed current I^e can be written as

$$[Y][\phi] = [-I^e] \tag{22}$$

where $[Y]$ is the nodal admittance matrix, and $[Y] = [\Lambda^T L^{-1} \Lambda]/(j\omega) + j\omega[C]$. Then, the network parameters can be extracted from the Y-matrix for ports of interest.

In the CEMPIE simulations below, an external port, Port 1, is defined between the antipad on the return plane and the via, as shown in Fig. 9(a). The round via was discretized into 20 edges with each edge as a current branch. The current branches were connected to a pseudonode and an external impressed current was injected into the node. The injected current spreads on the vertical surfaces of the via where all interactions are included; therefore, the impedance can be correctly modeled by the CEMPIE method. The impedance associated with Port 1 is extracted from the Y-matrix. The impedance varies linearly with frequency at low frequencies, exhibiting an inductive behavior.
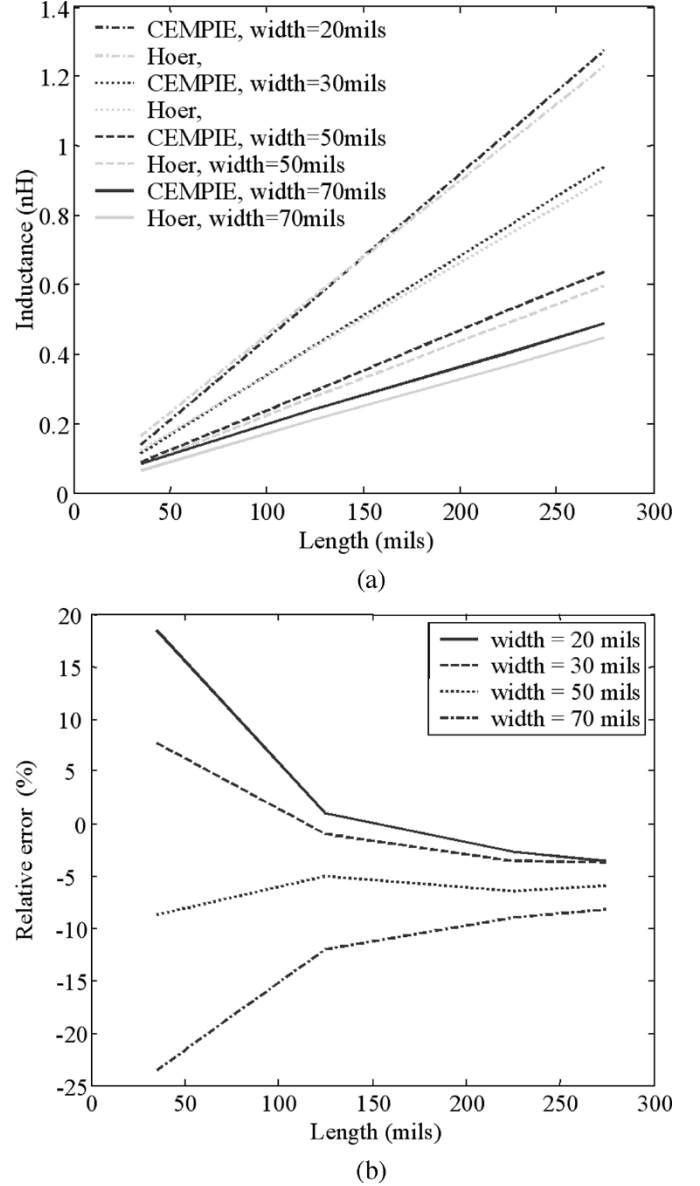

(a)

(b)

Fig. 11.   Parasitic inductance varying with trace length and trace width. (a) Parasitic inductance. (b) Relative error.

The slope of the impedance magnitude is calculated as the parasitic interconnect inductance L_2. The metal planes in CEMPIE, including the trace and the return plane are meshed with triangular cells, and the via wall is meshed into rectangular cells. Typical meshes for the trace and the return plane are shown in Fig. 10. A parametric study was considered based on the trace length l, trace width w, height h_s, and via diameter d, as shown in Fig. 9.

Fig. 11 shows the parasitic inductance varying with the trace length l and width w, while the height h_s is 0.10 mm (4 mils), and the via diameter remains at 0.33 mm (13 mils). These parameters were chosen according to dimensions that are commonly used in current engineering design. In the CEMPIE simulations, the antipad has a diameter of 0.89 mm (35 mils). The relative error of (17) is in general within 10% for lengths longer than 2.54 mm (100 mils). When the length is short and the width
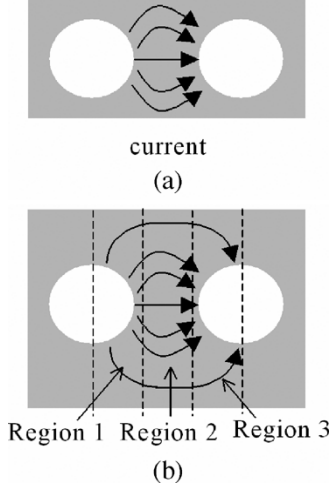
Fig. 12.   Illustration of current distribution on the trace when the length is short. (a) The trace is short and narrow. (b) The trace is short and wide.

is narrow, the assumption of a uniform current distribution on the via wall fails. More current concentrates on the via wall which is the inner side of Loop 2, as shown in Fig. 12(a). Consequently, the current path is shorter than the length from via center to center, which is used in (16). As a result, expression (17) overestimates the parasitic inductance. When the width of the trace increases, the current spreads itself along the width of the trace, as shown in Fig. 12(b). While it may be sufficient to assume that the current is uniformly distributed in Region 2, as shown in Fig. 12, the assumption is not valid in Regions 1 and 3. In Regions 1 and 3, the current concentrates at the vias, whose diameter is much smaller than the width of the trace, leading to larger parasitic inductance. Therefore, expression (17) underestimates the parasitic inductance, since it assumes a uniform current distribution along the entire length (via center to center). As the length of the trace increases, the contribution of the inductive current transition from the via to the trace is smaller, and the parasitic inductance is better predicted with (17). Simulations show the current distributions of the two cases shown in Fig. 12.

Next, the via diameter and height were varied to evaluate the accuracy of (17) for different package sizes of decoupling capacitors. The length and width associated with different dimensions were chosen as shown in Table III. The via diameter varies from 0.33 mm (13 mils) to 1.02 mm (40 mils), and the height h_s changes from 0.10 mm (4 mils) to 2.29 mm (90 mils). The results from expression (17) compared to that from the CEMPIE simulations are shown in Table IV.

The current distribution on the trace is shown in Fig. 12(b) when the ratio of the via diameter to the trace width is small. With an increase in the ratio of the via diameter to the trace width, the current distribution changes, as shown in Fig. 12(a). Consequently, the error of expression (17) increases in the over-estimation direction for each capacitor size, as the via diameter varies from 13 mils to 40 mils, as shown in Table IV. Expression (17) overestimates the parasitic inductance for $h_s \geq 0.25$ mm, and the maximum discrepancy occurs when the h_s is in the range from 0.25 to 0.5 mm. The reason is currently unknown.

Capacitor size	Length from via center to via center l (mm)	Width w (mm)
0402	2.92	0.64
0603	3.38	0.76
0805	5.21	1.27
1206	5.87	1.78

The maximum error of (17) in Table IV is 18%, which may still be acceptable for engineering purposes.

IV. CORRELATION WITH THE MEASUREMENTS

Measurements and full-wave modeling have been employed to verify the results from the approach proposed herein. The first test case includes a single pair of power and ground planes. The second test case considers a power plane with two ground planes.

A. Power Bus With Global Decoupling Capacitors

An FR4 three-layer rectangular power delivery network with seven decoupling capacitors was built to verify the proposed complete approach for power integrity design. The dimensions of the test board were 3.0 cm in width and 12.4 cm in length. The spacing between the top layer to the ground plane was 0.030 cm (12 mils), and the dielectric thickness between the ground and power layers was 0.083 cm (33 mils), as shown in Fig. 13. The widths of the PCB traces associated with the decoupling capacitors were all 0.1 cm (40 mils), and the lengths were varied from 0.6 cm (236 mils) to 0.25 cm (98 mils). The capacitors mounted on the board had the same nominal capacitance of 10 nF and the same package size of 0603. Two SMA connectors were soldered at Port 1 and Port 2, and the S-parameters were measured with an HP8753C network analyzer.

The structure can be characterized with a network of nine ports. The Z matrix of the network can be written as

$$\begin{bmatrix} \overline{V}_e \\ \overline{V}_c \end{bmatrix} = \begin{bmatrix} \overline{\overline{Z}}_{ee} & \overline{\overline{Z}}_{ec} \\ \overline{\overline{Z}}_{ce} & \overline{\overline{Z}}_{cc} \end{bmatrix} \begin{bmatrix} \overline{I}_e \\ \overline{I}_c \end{bmatrix} \tag{23}$$

where $\overline{V}_c = [V_3 \ldots V_9]^T$ corresponds to the seven decoupling capacitor ports, $\overline{V}_e = [V_1 \, V_2]^T$ corresponds to the two observation ports. For the ports connecting to the decoupling capacitors, the currents are related to the voltages as

$$\overline{V}_c = -\overline{\overline{Z}}_L \overline{I}_c \tag{24}$$

where $\overline{\overline{Z}}_L$ is a diagonal matrix with the diagonal element, $Z_{Lii} = R_i + j\omega L_i + 1/j\omega C_i$, $i = 1, \ldots, 7$, where $C_i = 10$ nF is the nominal capacitance, R_i is the equivalent series resistance (ESR), and L_i is the equivalent series inductance (ESL). The ESR R_i is dominated by the ESR of the capacitor package since the trace on the board is short and the ESR associated with the trace due to the skin effect is small. The ESL L_i has two contributions, one is the ESL of the capacitor package L_c, and the other is the parasitic inductance L_t of the loop bounded by the PCB trace and the ground plane. The ESR R_i and the ESL L_c were measured as 0.13 Ω and 0.4 nH using an impedance analyzer HP4291B with 16193A test fixture, respectively, for a

TABLE IV
PARASITIC INDUCTANCE VERSUS. VIA DIAMETER d, HEIGHT h_s, AND CAPACITOR SIZE

Parasitic inductance (nH)		0402			0603			0805			1206		
		CEM-PIE	(17)	Err* (%)	CEM-PIE	(17)	Err (%)	CEM-PIE	(17)	Err (%)	CEM-PIE	(17)	Err (%)
$h_s = 0.1$ mm	d=0.33mm	0.44	0.44	0.6	0.46	0.44	-3.5	0.47	0.45	-4.7	0.41	0.38	-7.8
	d=0.51mm				0.42	0.44	5.7	0.45	0.44	-2.1	0.39	0.37	-5.2
	d=0.76mm							0.43	0.44	2.6	0.37	0.37	2.9
	d=1.02mm							0.40	0.44	9.9	0.35	0.37	5.6
$h_s = 0.25$ mm	d=0.33mm	0.80	0.87	9.0	0.84	0.90	7.1	0.94	0.97	3.7	0.86	0.86	-0.2
	d=0.51mm				0.78	0.88	12.7	0.90	0.95	6.5	0.82	0.84	2.2
	d=0.76mm							0.84	0.94	11.7	0.77	0.82	7.6
	d=1.02mm							0.79	0.93	17.8	0.72	0.82	13.2
$h_s = 0.51$ mm	d=0.33mm	1.20	1.35	12.8	1.30	1.43	10.1	1.56	1.65	6.0	1.48	1.53	3.2
	d=0.51mm				1.20	1.37	14.4	1.47	1.59	8.5	1.40	1.47	4.9
	d=0.76mm							1.37	1.55	13.0	1.30	1.42	9.4
	d=1.02mm							1.30	1.52	17.1	1.20	1.40	16.3
$h_s = 0.76$ mm	d=0.33mm	1.60	1.72	7.5	1.71	1.84	7.5	2.07	2.20	6.1	2.00	2.09	4.5
	d=0.51mm				1.58	1.74	10.0	1.94	2.10	8.0	1.88	1.99	5.8
	d=0.76mm							1.80	2.01	11.8	1.75	1.91	8.9
	d=1.02mm							1.69	1.96	16.1	1.63	1.86	13.8
$h_s = 1.52$ mm	d=0.33mm	2.52	2.61	3.6	2.71	2.81	3.7	3.33	3.47	4.2	3.34	3.45	3.2
	d=0.51mm				2.46	2.58	5.0	3.10	3.24	4.6	3.11	3.22	3.5
	d=0.76mm							2.84	3.04	8.6	2.85	3.02	6.0
	d=1.02mm							2.65	2.91	9.8	2.65	2.88	8.9
$h_s = 2.29$ mm	d=0.33mm	3.30	3.44	4.2	3.57	3.69	3.3	4.40	4.54	3.3	4.50	4.59	2.0
	d=0.51mm				3.24	3.33	2.7	4.09	4.18	2.3	4.16	4.23	1.7
	d=0.76mm							3.73	3.86	3.5	3.81	3.91	2.5
	d=1.02mm							3.46	3.64	5.3	3.53	3.69	4.5

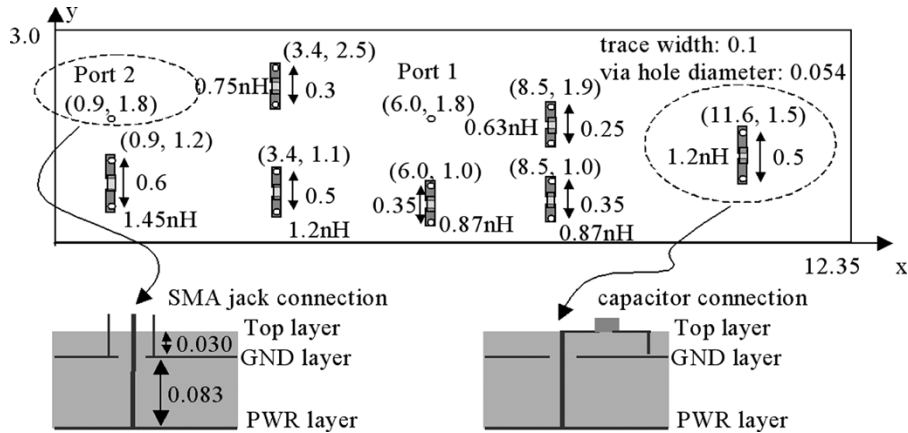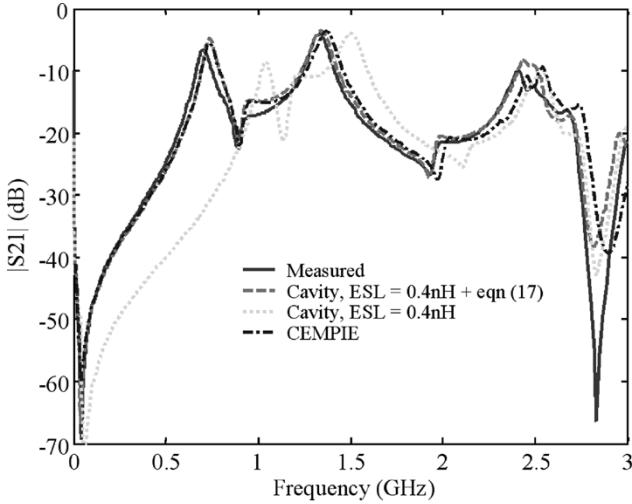* Error is calculated as $(L_{(17)} - L_{CEMPIE}) / L_{CEMPIE}$.

Fig. 13. Three-layer rectangular power delivery network with seven decoupling capacitors. Units: centimeters.
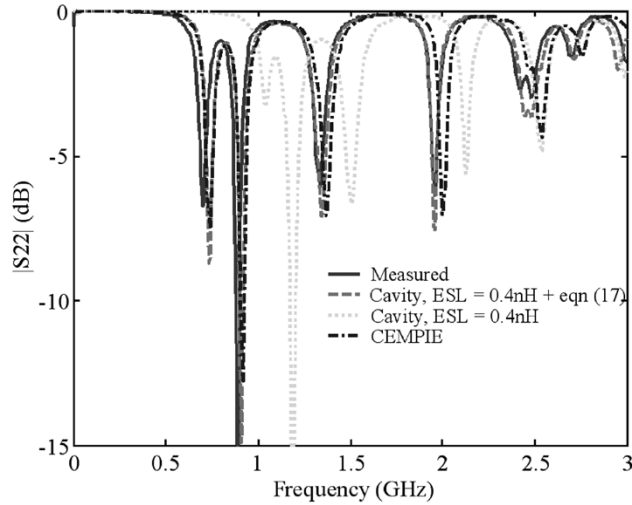
package size of 0603. The parasitic inductance L_t can be calculated with (17). The total parasitic inductance associated with each capacitor is shown in Fig. 13. The longest trace length on the test board is 0.6 cm, corresponding to 0.11λ at 3 GHz when the effective dielectric constant is 3.5 [33], which may cause the impedance at 3 GHz to be 20% off if the inductance valid at low frequency is used. However, this may still be acceptable for engineering purposes. Therefore, the parasitic inductances in Fig. 13 were used throughout the entire frequency range up to 3 GHz. Substituting (24) into (23) and solving for $\overline{V}_e$

$$\overline{V}_e = \left[\overline{\overline{Z}}_{ee} - \overline{\overline{Z}}_{ec}(\overline{\overline{Z}}_L + \overline{\overline{Z}}_{cc})^{-1}\overline{\overline{Z}}_{ce} \right] \overline{I}_e = \overline{\overline{Z}}_{ee}^{total}\overline{I}_e \quad (25)$$

Fig. 14. S-parameters of the power distribution network with seven decoupling capacitors.

Fig. 15. Geometry of a three-layer power-bus structure. Units are in centimeters.

where $\overline{\overline{Z}}_{ee}^{\text{total}}$ is the impedance matrix of the two observation ports when the decoupling capacitors are taken into account. The S-parameters can then be calculated as
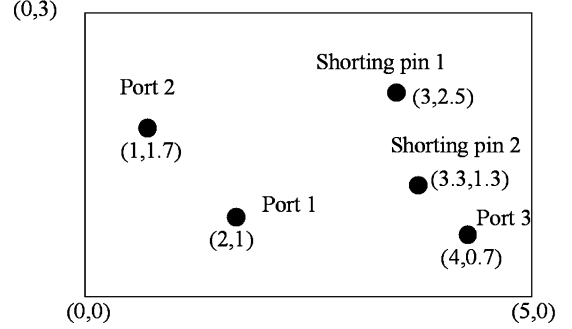
$$\overline{\overline{S}} = \left(\frac{\overline{\overline{Z}}_{ee}^{\text{total}}}{50} + I\right)^{-1} \left(\frac{\overline{\overline{Z}}_{ee}^{\text{total}}}{50} - I\right) \qquad (26)$$

where I is an identity matrix. The relative dielectric constant was $\varepsilon_r = 4.3$ and the loss tangent was $\tan\delta = 0.02$ in the cavity model, corresponding to typical values of the FR4 material.

The measured and cavity-modeled S-parameters are shown in Fig. 14. While the results from the cavity model do not agree with the measurements when only the ESLs of the capacitor package are considered, the results agree well with the measurements when the parasitic inductances calculated with (17) are included. The first null in $|S21|$ is due to the series resonance of the decoupling capacitors with the parasitic inductance. The first bare board resonance is approximately 580 MHz, which is not seen in either $|S21|$ or $|S22|$. The resonances in $|S21|$ and $|S22|$

are due to the interaction between the parasitic inductances and the board resonant structure. The agreement between the measurement and the cavity results when the parasitic inductances associated with the PCB layout are included indicates that the cavity model in combination with the closed-form expression (17) is applicable to power integrity designs. The results from the CEMPIE simulation are also shown in Fig. 14. The agreement between the measurements and the results from CEMPIE are good below 2 GHz, the discrepancy at high frequency may be due to the coarse mesh on the planes. The mesh size is limited by the memory that was required for solving for the inverse of the Y-matrix extracted from CEMPIE. It may also be possibly due to the quasistatic Green's function approximation in CEMPIE.

B. Multilayer Board

A three-layer power distribution network was designed to verify whether the cavity model could be employed to model multilayer boards. The board geometry is shown in Fig. 15. The three planes G1, P, and G2 form two power delivery structures, namely, A and B. Plane G1 is connected to plane G2 through shorting pin 1, and plane P is connected to plane G2 through shorting pin 2. Port 1 is the feeding port, exciting both power-bus structures A and B. Ports 2 and 3 are the observation ports. At high frequencies, where the skin depth is much less than the thickness of the planes, the current flowing on the upper surface of plane P is decoupled from the current flowing on the bottom surface of plane P. At the antipads of plane P, the current on the upper surface and the current on the bottom surface must be continuous. Therefore, an equivalent network representation can be derived with the cavity model for the three-layer power-bus structure, as shown in Fig. 16. Then, $|Z_{11}|$, $|Z_{21}|$ and $|Z_{31}|$ can be calculated from the network representation.
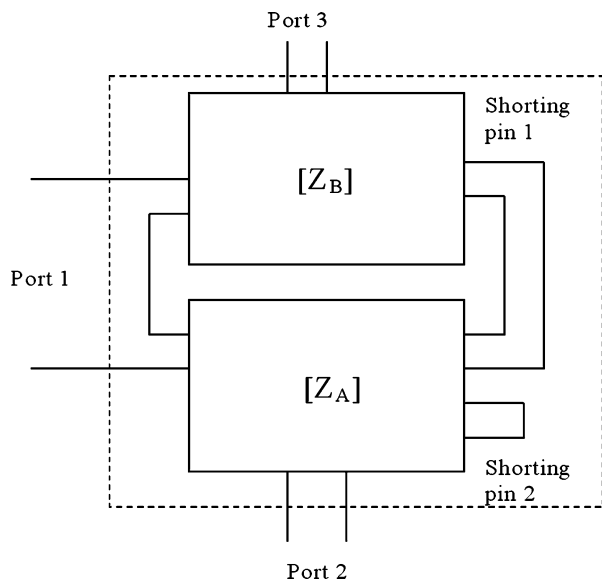
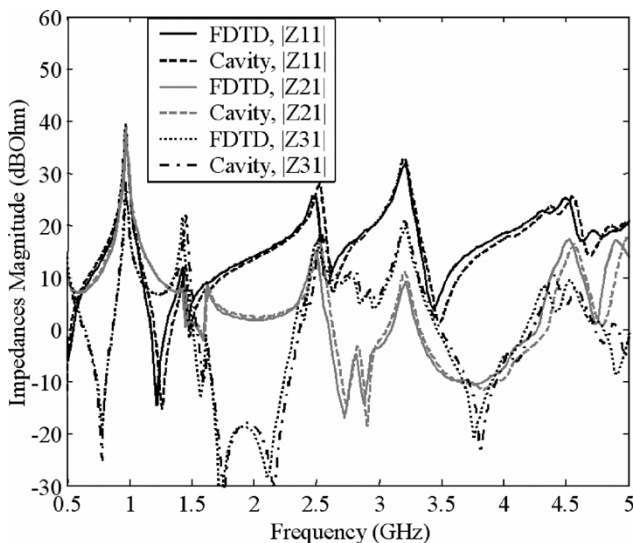Fig. 16. Network representation of the three-layer power-bus structure.

Fig. 17. Comparison of impedances from the cavity model and that from the FDTD approach for the three-layer power delivery structure.

The FDTD method was employed to model the three-layer structure as well. In the FDTD modeling, the shorting pins and the center conductor of port 1 are modeled as 1×1 mm square PEC (perfect electrical conducting) blocks. The antipads in plane P are square cutouts with dimensions of 2×2 mm. The dielectric material between the planes is modeled as a Debye material with the same parameters as used in [2]. The planes were simulated as PECs for simplicity, though it is also possible to simulate them as copper. The results from the cavity model are compared to that from the full-wave FDTD method in Fig. 17. Good agreement between the cavity model and the full-wave FDTD method was achieved. The discrepancy in the magnitudes is within 3 dB for $|Z_{11}|$, $|Z_{21}|$, and $|Z_{31}|$, and the discrepancy in the resonant frequencies is within 5% in general. The good agreement indicates that the cavity model is applicable to a multilayer power delivery networks.
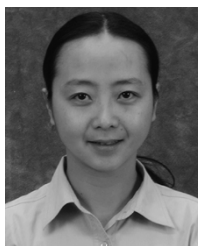
V. DISCUSSION AND CONCLUSION

The cavity model, its equivalent circuit, and the segmentation method were used herein to study irregular-shaped power delivery networks on layered substrates that use large area fills for power and ground. Vias that penetrate the planes were modeled as ports in the cavity model. The vias can be associated with the decoupling capacitors, the IC pins of interest, and the layer transitions of the signals. The ports associated with a single via penetrating multiple planes can then be connected, i.e., the shorting pin 1 in Fig. 16, to model the power delivery network with multiple layers. The ports associated with the decoupling capacitors can be connected to the decoupling capacitors with an ESR and ESL. The ESL of the decoupling capacitor includes the parasitics of the capacitor package as well as the interconnect parasitics of the PCB layout. Closed-form expressions of the interconnect parasitic inductance associated with decoupling capacitors is verified with a full-wave method. An application of the proposed method to a complex power distribution network is demonstrated in [34].

Measurements and full-wave simulations have been performed to validate the approach shown herein. Good agreement has been achieved between the results from the method, the measurements and/or the full-wave methods, indicating the suitability of applying the proposed method to power integrity design.

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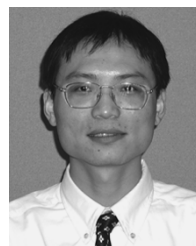
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