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Power Bus Decoupling on Multilayer Printed Circuit Boards

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***Abstract*—Guidelines for the selection and placement of decoupling capacitors that work well for one-sided or two-sided printed circuit boards are not appropriate for multilayer boards with power and ground planes. Boards without internal planes take advantage of the power bus inductance to help decouple components at the higher frequencies. An effective decoupling strategy for multilayer boards must account for the low inductance and relatively high capacitance of the power bus.**

I. Introduction

A SUDDEN change in the amount of current drawn by a component on a printed circuit board can cause a momentary drop (or surge) in the voltage on the power distribution bus. This voltage transient can be sufficiently large to interfere with the normal operation of other components on the board. Ground bounce or delta-I noise, as this phenomenon is called, is a common problem in high-speed printed circuit board and integrated circuit designs. Decoupling capacitors connected to the power and ground leads are typically added to mitigate this problem. Decoupling capacitors help to stabilize the power distribution bus by supplying current that opposes any change in the bus voltage. However, decoupling capacitors use space and add cost to printed circuit board designs. Therefore, considerable effort has been devoted to modeling and understanding the ground bounce phenomenon in order to better understand how to most effectively use decoupling capacitors. Several researchers (e.g., [1]–[4]) have employed lumped element circuit models to study the delta-I noise problem. Time and frequency domain circuit simulations have demonstrated excellent agreement with measured results. Djordjevic and Sarkar recently applied a three-dimensional numerical modeling technique to the analysis of delta-I noise on integrated circuits and multilayer boards [5]. Their results confirm the validity of the lumped element circuit models used by other researchers at frequencies below board resonances.

While there are many well-established guidelines for the selection and placement of decoupling capacitors, not all of these apply to multilayer printed circuit boards. This paper develops and analyzes basic models of a multilayer printed circuit board power distribution bus. The results presented indicate that multilayer board decoupling strategies must place an increased emphasis on minimizing interconnect inductance. They also show that the location of decoupling capacitors on a multilayer board is not nearly as critical as the method used to connect them to the power and ground planes.

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II. Modeling Boards without a Power Plane

Consider the simple model of an electronic system illustrated in Fig. 1(a). This model can be applied at frequencies where the impedance of the printed circuit board traces is low enough to ensure that the voltage difference between any two points on the power traces is negligible. If the current demands of each component on the printed circuit board are constant, the voltage at each component is equal to the power supply voltage. However, a change in the current drawn by the components on the board results in a voltage drop across the inductance of the power distribution wires. The voltage at the input of the printed circuit board is reduced by the amount of this voltage drop,

$$V_{\text{board}}(t) = V_{\text{supply}} - (L_P + L_G)\frac{di(t)}{dt}.$$

Printed circuit boards cannot always be located near the power supply, so power distribution inductances on the order of 10 μH or greater are not uncommon. A printed circuit board drawing as little as 300 mA in 1 μsec through a 10 μH inductance will experience a 3-volt drop in the supply voltage, which can be sufficient to cause components on the board to malfunction. A bulk decoupling capacitor on the board near the power input can help alleviate this problem. In the time domain, the capacitor can be viewed as a local source of charge. As the voltage of the board begins to drop, the current supplied by the bulk decoupling capacitor is,

$$i = C_b\frac{dV}{dt}. \tag{1}$$

This current helps to meet the needs of the components on the board and reduces the delta-I voltage drop across the power lead inductance. After the momentary need for current has been met, the capacitor is recharged by the power supply.

In the frequency domain, the bulk decoupling capacitor can be viewed as a low-impedance power source. In the absence of the bulk decoupling capacitor, the impedance of the power supply as viewed from the board is,

$$Z_{\text{supply}} = j\omega(L_P + L_G). \tag{2}$$

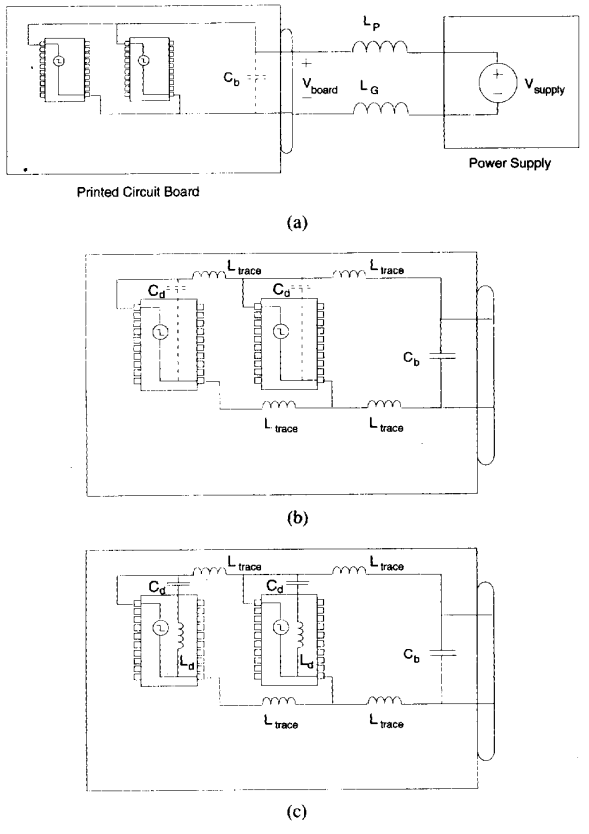

Fig. 1. (a) Low-, (b) middle-, and (c) high-frequency models of the power distribution on a simple printed circuit board.

The voltage at the power input of the printed circuit board is,

$$V_{\text{board}} = V_{\text{supply}} - I(\omega)Z_{\text{supply}}(\omega). \tag{3}$$

For a given amount of current drawn by the board, a larger Z_{supply} results in a greater deviation from V_{supply}. A bulk decoupling capacitor at the power input reduces the power supply impedance as viewed from the board.

$$Z_{\text{supply}} = \frac{j\omega(L_P + L_G)}{1 - \omega^2(L_p + L_G)C} \tag{4}$$

A smaller supply impedance stabilizes the voltage at the board input by providing more current for a given change in the voltage.

Fig. 1(b) illustrates a power distribution model that is valid at higher frequencies where the inductance of the power distribution traces on the board is no longer negligible. The inductance of these traces is typically on the order of 100 nH or greater on a board without internal power and ground planes. A device drawing as little as 30 mA in 1 nsec through 100 nH can produce a 3-volt transient at its own power pins and at the pins of every component connected to the power traces beyond the switching device.

A decoupling capacitor between the power and ground pins of each switching component helps to mitigate this problem. In the time domain, this capacitor is a local source of current that is specified to meet the needs of a single component. In the frequency domain, the decoupling capacitor lowers the impedance of the power bus as viewed from the nearby component. The capacitor has relatively little effect on the power bus impedance of components located farther away due to the high impedance of the connecting traces. Therefore, at these frequencies, components located away from the decoupling capacitor do not draw significant charge from it.

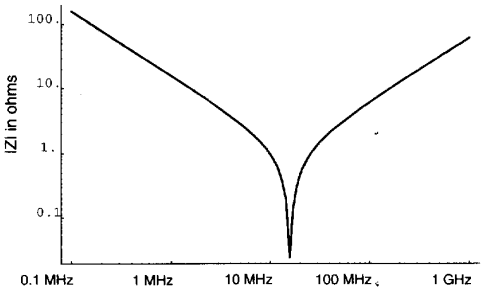

Fig. 2. Impedance of a 0.01-μF capacitor connected through a 10-nH trace inductance.

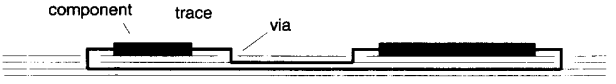

Fig. 3. Surface-mount capacitors on a multilayer board.

At higher frequencies, the inductance associated with the current path formed by the traces connecting the decoupling capacitor to the component being decoupled can no longer be neglected. The circuit model of the power distribution traces on the board must be modified to include these inductances as shown in Fig. 1(c). In the time domain, this inductance can be viewed as limiting the maximum rate of change of current supplied by the decoupling capacitor. In the frequency domain, this inductance prevents the impedance provided by the decoupling capacitor from decreasing with frequency indefinitely. Fig. 2 shows a plot of the impedance of a 0.01-μF capacitor connected through a 10 nH trace inductance. At frequencies less than 16 MHz the impedance is approximately that of an ideal capacitor and the inductance can be neglected. At frequencies near 16 MHz, the LC combination is resonant and the impedance is a minimum. At frequencies greater than 16 MHz, the impedance is approximately that of the inductance alone.

The frequency at which the impedance reaches a minimum is called the *self-resonance* frequency of the capacitor [6]. At any frequency where the impedance of the decoupling capacitor is lower than that of the power distribution bus, the capacitor is supplying most of the current and serving to stabilize the power bus voltage. For printed circuit boards without power and ground planes, the lead inductance of the capacitor is generally much less than the power distribution bus inductance. Therefore, even beyond self resonance, the impedance of the decoupling capacitor remains well below that of the power distribution bus. For this reason, on boards

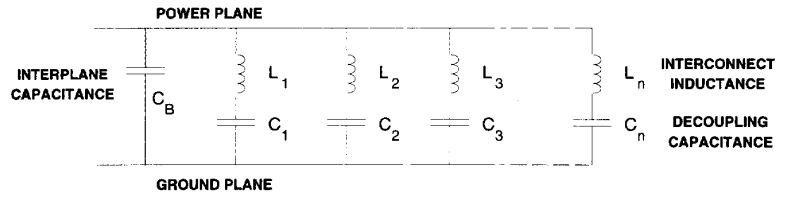

Fig. 4. Model of the power distribution bus on a multilayer board.

without power and ground planes, decoupling capacitors are usually effective even at frequencies significantly greater than the self-resonance frequency.

III. Modeling Multilayer Printed Circuit Boards

Trace routing on printed circuit boards populated with large numbers of tightly packed components is difficult to accomplish with one-sided or two-sided boards. Boards with internal power and signal layers are commonly employed for high-speed, high-density designs. Typically, a multilayer board will devote entire layers to power distribution. These layers are normally solid planes, often on adjacent layers. As a result, the impedance of the power distribution bus on a multilayer board tends to be much lower than the power distribution bus impedance of boards without power and ground planes.

At low frequencies, the lumped circuit model for a multilayer board is identical to the model of a nonmultilayer board shown in Fig. 1(a). Bulk decoupling at the power inputs to the printed circuit board serves to stabilize the voltage between the power and ground planes whenever a change in the current demand causes a delta-I voltage drop across the power leads.

The feature that causes multilayer board decoupling to be different from single-sided or double-sided board decoupling is that the component-to-component power distribution impedance is very small in boards with power and ground planes. A cross-sectional view of surface-mount components connected to the power and ground planes of a multilayer board is illustrated in Fig. 3. The inductance associated with currents flowing in the power distribution bus of a multilayer board is typically on the order of 0.05 nH/cm. On most multilayer boards, the maximum inductance of the planes between any two components is significantly less than 1 nH. Conversely, the interconnect inductance (i.e., the inductance associated with the traces connecting a component to vias and the vias themselves) is typically 2.5–10 nH or greater [7].

A lumped element circuit model of the power distribution bus on a multilayer printed circuit board is shown in Fig. 4. This model accounts for the interconnect inductance of the decoupling capacitors and is valid at frequencies where the board dimensions are small relative to a wavelength. C_B is the capacitance between the power and ground planes, which is typically on the order of 2–15 nF for 6–10 inch square boards with an 8–10 mil power plane spacing. C_1–C_n model the decoupling capacitors connected between the power and ground planes of the printed circuit board. L_1–L_n represent the inductance of the loop formed by the capacitor and the vias and traces connecting the capacitor to the planes.

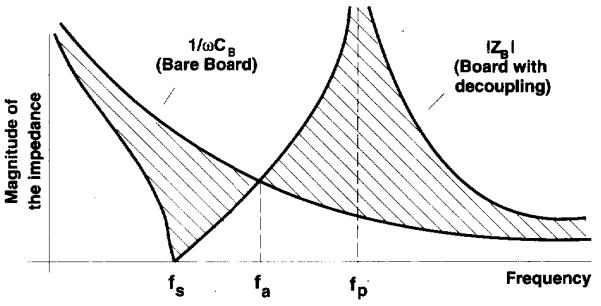

Fig. 5. Board impedance of a multilayer board with n identical decoupling capacitors.

As this model indicates, the power distribution trace inductance no longer serves to isolate different components. When a switching device draws additional current from the power bus causing a fluctuation in the voltage between the planes, all components that are connected to the power and ground planes experience the same fluctuation. Current is supplied not only by the nearest decoupling capacitor, but all capacitors connected between power and ground.

The effectiveness of a particular decoupling capacitor at a given frequency depends on its impedance relative to the impedance of the other decoupling capacitors and the board capacitance. At the frequencies at which the model in Fig. 4 is valid (typically below 200–300 MHz), it is apparent that the position of a decoupling capacitor is not nearly as important as its interconnect inductance.

IV. Analytical Results

A. Frequency Domain

A typical printed circuit design will employ decoupling capacitors with several different values, and the inductances associated with the traces connecting these decoupling capacitors to the power bus will vary. The elements of the lumped circuit model will then, in general, be different for each branch of the model in Fig. 4. This general lumped element circuit model is easily analyzed with computer circuit analysis packages. However, simple analytical expressions result, from which insight can be gained, if the capacitance and interconnect inductance values of each parallel branch are assumed equal, (i.e. $C_1 = C_2 \cdots C_n, L_1 = L_2 = \cdots L_n$). The impedance between the power and ground planes is then

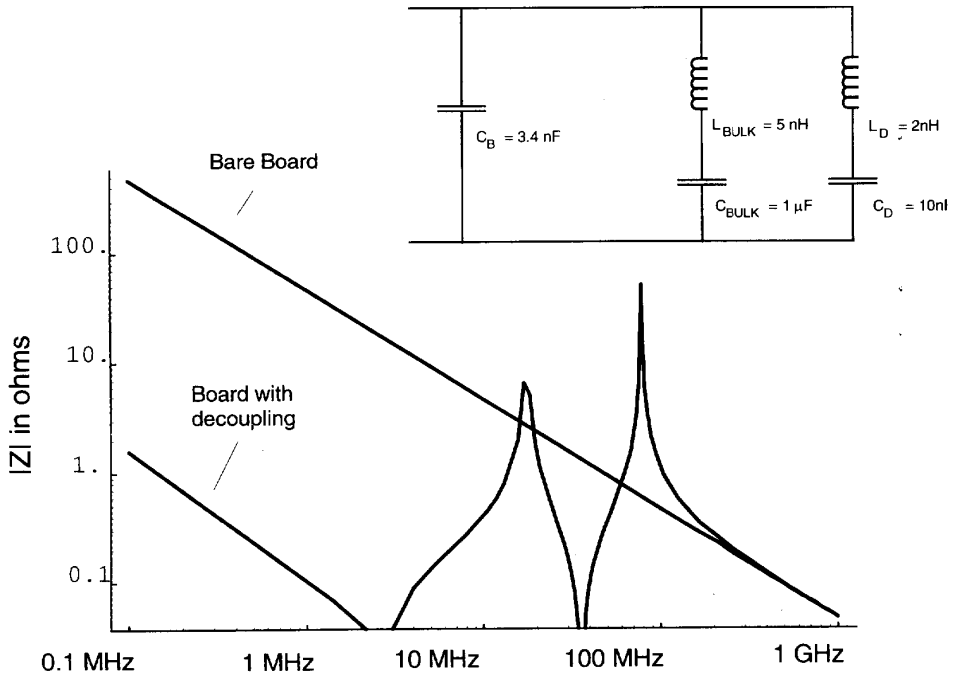

Fig. 6. Baord impedance of a two-decoupling-capacitor circuit.

given by

$$Z_B = \frac{j\left(\frac{\omega L_1}{n} - \frac{1}{n\omega C_1}\right)}{1 - \omega C_B\left(\frac{\omega L_1}{n} - \frac{1}{n\omega C_1}\right)}. \tag{5}$$

The board impedance is zero at the series-resonance frequency

$$f_s = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{6}$$

and infinite at the parallel-resonance frequency,

$$f_p = f_s\sqrt{1 + \frac{nC_1}{C_B}}. \tag{7}$$

The series resonance is the frequency at which the decoupling capacitors resonate with their own interconnect inductances. The parallel resonance is the frequency at which the board capacitance resonates with the interconnect inductances of the decoupling capacitors.

The board impedance is plotted as a function of frequency in Fig. 5. At frequencies less than the series-resonance frequency, the impedance is approximately that of an ideal capacitor,

$$Z_B \approx \frac{1}{j\omega(nC_1 + C_B)}. \tag{8}$$

For frequencies near the series-resonance frequency f_s, the impedance given by (5) is less than the impedance due to the parallel combination of the decoupling and board capacitance. However, at frequencies higher than f_s, the decoupling capacitor branches begin to behave inductively due to the interconnect inductances. The frequency at which the magnitude of the board impedance is the same with or without the decoupling capacitors is given by

$$f_a = f_s\sqrt{1 + \frac{(nC_1)}{(2C_B)}}. \tag{9}$$

For frequencies above f_a, the board impedance is higher than it would be with no added decoupling capacitors and the added capacitors provide no benefit. At these frequencies, the voltage is less stable and the board is less able to respond to demands for additional current.

This simple analysis suggests that minimizing the series inductance of the decoupling capacitor connection is paramount to achieving the ideal capacitor behavior over the widest possible frequency range. Lowering the interconnect inductance increases the series and parallel-resonance frequencies, thereby extending the range of ideal capacitor behavior. For a given interconnect inductance, the frequency range of the decoupling capacitors can also be extended by increasing n, the total number of decoupling capacitors. Increasing n does not affect the series resonance, but it increases the parallel-resonance frequency.

Fig. 6 shows the modeled response of a two-decoupling-capacitor circuit on a multilayer board. In this case the two decoupling capacitors have different values. Note that there are now two series resonances and two parallel resonances. The series-resonance frequencies (corresponding to the zeroes in the expression for the power distribution impedance) can be calculated in a straight-forward manner using,

$$f_{s_1} = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{10}$$

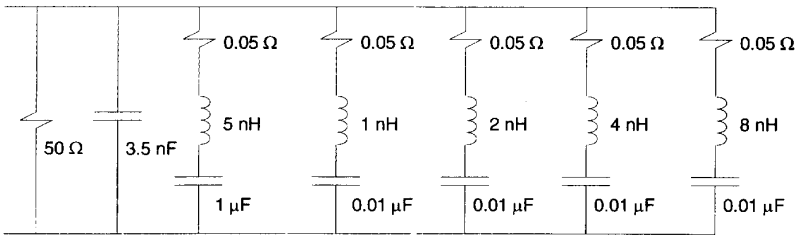

Fig. 7. Model of a multilayer board power distribution bus.

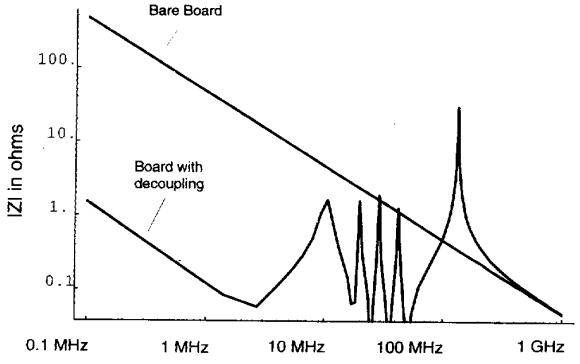

Fig. 8. Impedance of a board with 5 decoupling capacitors.

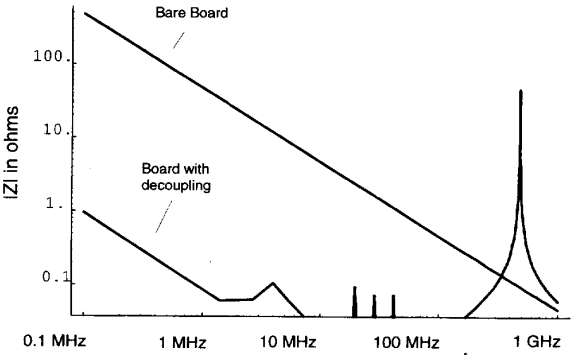

Fig. 9. Impedance of a board with 65 decoupling capacitors.

$$f_{s_2} = \frac{1}{2\pi\sqrt{L_2 C_2}} \tag{11}$$

where C_1 and C_2 are the values of the two decoupling capacitors, and L_1 and L_2 are the corresponding interconnect inductances. In this example, the larger "bulk" decoupling capacitor causes a zero in the response to occur at 2.25 MHz. The smaller "local" decoupling capacitor is series resonant at 35.6 MHz.

Parallel resonances correspond to poles in the board impedance expression. An exact expression for the parallel-resonance frequencies is difficult to obtain for an arbitrary number of decoupling capacitors, however the poles and zeroes must alternate, so there is exactly one parallel resonance between each pair of series resonances. For the circuit in Fig. 6, parallel resonances occur at approximately 25 MHz and 80 MHz. At frequencies above approximately 100 MHz, the effect of the decoupling is negligible and the impedance is approximately that of the board capacitance, C_B.

Fig. 7 shows a circuit model that more closely represents an actual multilayer printed circuit board design. The interplane capacitance of the board is 3.4 nF. A 50 ohm resistor represents the dc load due to the active components on the board, although its presence has little effect on the overall board response. Five decoupling capacitors are used in this model. One bulk decoupling capacitor, $C_b = 1\,\mu$F, and four local decoupling capacitors, $C_d = 10$ nF. Each decoupling capacitor has a different interconnect inductance (1–8 nH) associated with it. A series resistance of 0.05 ohms was added to each decoupling capacitor. This resistance was chosen as a nominal value based on measurements of the interconnect trace resistance for actual surface mount decoupling capacitors mounted on a multilayer printed circuit board.

The magnitude of the power distribution bus impedance of this model is plotted as a function of frequency in Fig. 8. The series-resonance frequencies can be calculated using (6), while each parallel resonance occurs between two series resonances. The decoupling capacitors significantly reduce the power distribution impedance below about 7 MHz due primarily to the large bulk decoupling capacitor. Between 7 and 70 MHz, the "local" 10 nF capacitors provide most of the decoupling and the impedance fluctuates due to the closely spaced series and parallel-resonances. The average impedance in this band is still below that of the bare board. Between 70 and 200 MHz, the last parallel resonance causes the decoupled board impedance to be higher than the bare board impedance. Above 200 MHz, the decoupling capacitors have little effect on the board impedance.

Fig. 9 shows the response of a board model similar to the one in Fig. 7 with 64 10 nF decoupling capacitors instead of 4. In this case, 16 capacitors are connected through each of the 4 trace inductances (1, 2, 4, and 8 nH). The additional capacitors have little effect on the impedance at low frequencies, where the bulk decoupling capacitor is effective. This is because the 60 additional capacitors only raise the total available capacitance from 1043.4–1643.4 nF.

At frequencies beyond the first resonance however, the impedance of the bulk decoupling capacitor is relatively high. The charge stored in the 1000 nF capacitance is essentially unavailable to the circuit. In the 10–100 MHz range, the added decoupling capacitors decrease the overall board impedance by approximately a factor of 16. In addition, although the series-

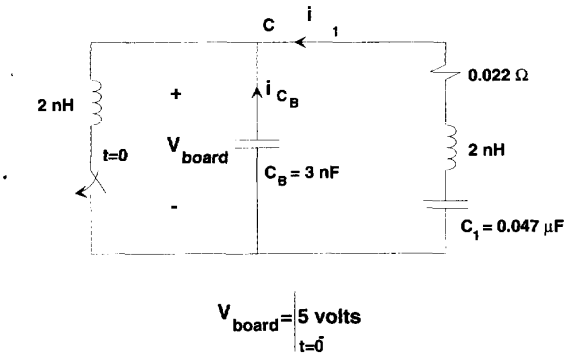

Fig. 10. Time-domain model of a multilayer board power distribution bus.

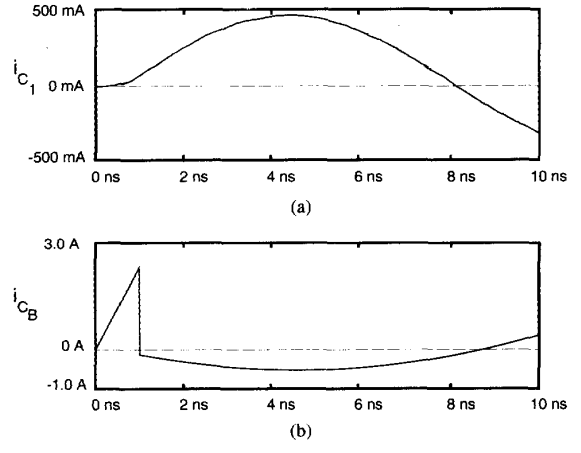

Fig. 11. Current supplied by (a) board and (b) decoupling capacitances.

resonance frequencies are unchanged, the highest parallel resonance is shifted upward in frequency by approximately a factor of 4 ($\sqrt{n}$). Therefore, the range of frequencies at which the added decoupling is effective is extended by approximately a factor of 4 (i.e., from 90 to about 360 MHz). Above this frequency range however, even with 64 added decoupling capacitors, the impedance is greater than or equal to the impedance due to the board capacitance alone.

B. Time Domain

Since the response of a decoupling capacitor to a sudden change in the demand for current is often of interest, it is helpful to interpret the frequency domain impedance response in terms of a capacitor's ability to supply current in the time domain. The low frequency impedance between the power and ground planes is an indication of how much the voltage on a board will change when experiencing a relatively slow transient. It is also an indication of the time-average voltage swing experienced during a faster transient. The lower the impedance, the more current the board can supply when it experiences a sudden change in the voltage. The high-frequency impedance is an indication of how much current the board can initially supply in response to a fast transient. Boards with the lowest impedance above 100 MHz can supply

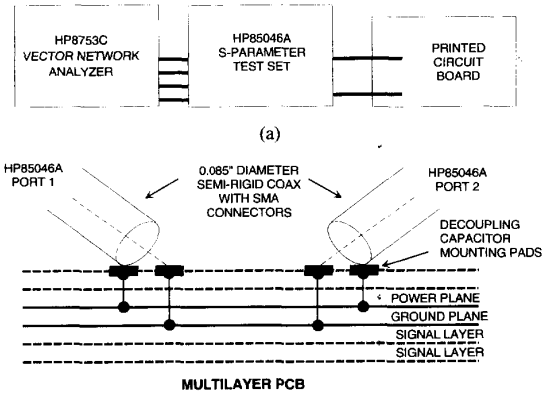

Fig. 12. Test configuration for measuring power distribution bus impedance.

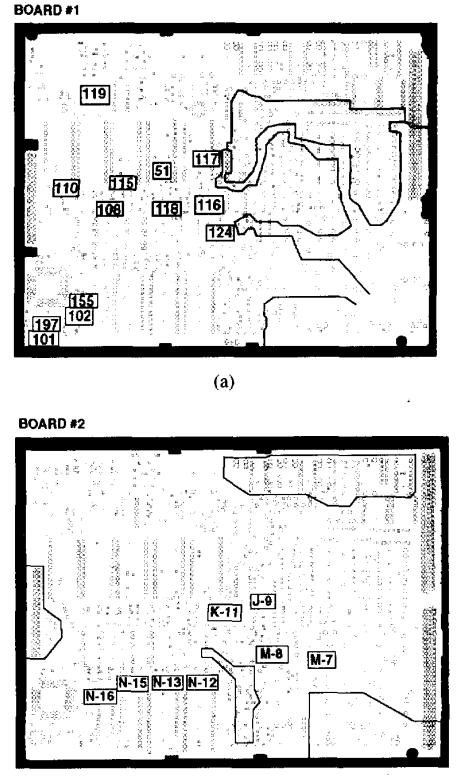

Fig. 13. Locations of decoupling capacitor mounting pads. (a) Board #1. (b) Board #2.

the greatest amount of current (for a given voltage change) during the first few nanoseconds of a sudden transient.

As an example of how this applies to multilayer printed circuit board decoupling, consider the simple circuit in Fig. 10. The upper and lower nodes again correspond to the power and ground planes of a multilayer board. The switch represents a device on the printed circuit board that suddenly demands additional current at time $t = 0$. The 2 nH inductor in series with the switch is typical of an interconnect inductance that

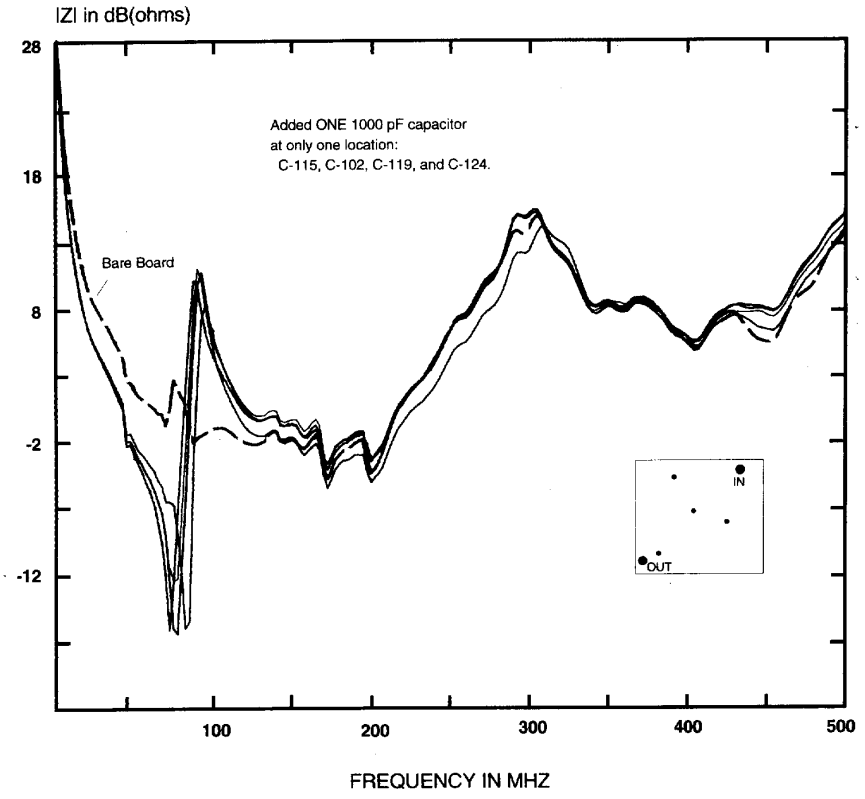

Fig. 14. Board #1 impedance for 4 different capacitor locations.

might connect a switching device to power and ground. C_B is the interplane capacitance of the board and C_1 is a 47 nF decoupling capacitor connected to the board through a 2 nH interconnect inductance. Prior to $t = 0$ the potential across these capacitors is 5 volts. In the frequency domain, this circuit has a series resonance at 16.4 MHz and a parallel resonance at 65 MHz. The time domain response of the circuit in Fig. 10 was obtained using SPICE. Because switches in a SPICE model must be voltage or current controlled, a fourth branch was added to the circuit in Fig. 10 containing a $10\,\mu$V source in series with a $10\,\mathrm{M}\Omega$ resistance. The source/resistor combination was used to control the switch without significantly affecting the circuit response. Fig. 11 shows the current drawn from the power plane and the current drawn from the decoupling capacitor when the switch is closed for 1 nanosecond and then opened. Note that virtually all of the current supplied to the switching device is provided by the interplane capacitance of the board, C_B. The decoupling capacitor cannot respond sufficiently fast to provide significant amounts of current.

V. Measured Results

In order to accurately measure the magnitude of the impedance of a printed circuit board, the test set-up illustrated in Fig. 12(a) was employed. A vector network analyzer with an S-parameter test set was connected to the printed circuit board power plane through semi-rigid, 0.085″, coaxial-cable probes. These probes were soldered directly to decoupling capacitor bonding pads. The center conductor of the coaxial cable was connected to the ground plane and the outer shield was connected to the power plane as shown in Fig. 12(b).

The printed circuit board impedance can be directly related to the measured S_{21} between the attached coaxial cable probes as

$$S_{21} = \frac{Z_B}{Z_B + \frac{1}{2}Z_o} \tag{12}$$

where Z_B is the printed circuit board impedance, and $Z_o = 50$ ohms is the characteristic impedance of the measurement system. For $Z_B \ll Z_o$, which is generally the case, except possibly at the parallel-resonance frequencies,

$$|S_{21}| \approx \frac{|Z_B|}{25} = (|Z_B| - 28)\ \mathrm{dB}. \tag{13}$$

Although in theory the board impedance could be derived from a one-port measurement as

$$Z_B = Z_o \frac{1 + S_{11}}{1 - S_{11}}, \tag{14}$$

this procedure is not very accurate. Since the board impedance is primarily reactive, the magnitude of S_{11} is nearly unity and an accurate determination of the phase of S_{11} is critical. Using (13), the magnitude of Z_B can be easily extracted from a measurement of the magnitude of S_{21} without requiring phase information.

TABLE I
INTERCONNECT INDUCTANCE VALUES FOR BOARD #1 AND BOARD #2

Board #1		Board #2	
Capacitor Location	Inductance (nH)	Capacitor Location	Inductance (nH)
C-51	2.6	J-9	4.2
C-101	4.7	K-11	3.8
C-102	3.2	M-7	4.0
C-108	2.7	M-8	4.0
C-110	6.8	N-12	5.4
C-115	3.6	N-13	4.4
C-116	6.4	N-15	7.7
C-117	5.3	N-16	3.4
C-118	4.2		
C-119	3.4		
C-124	3.4		
C-155	4.5		
C-197	5.4		

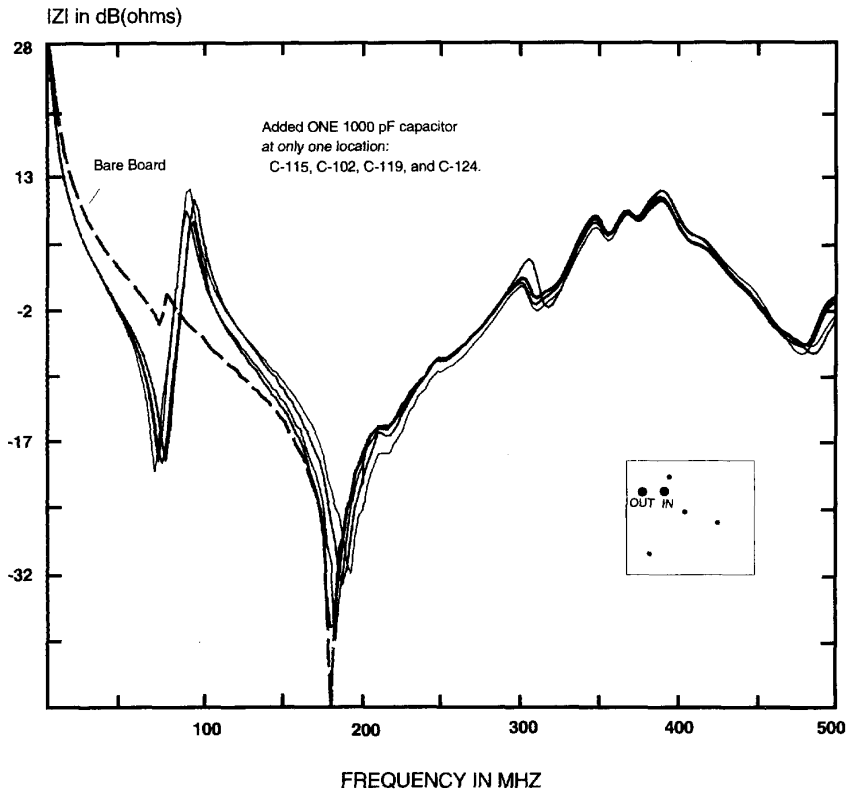

Fig. 15. Board #1 impedance for 4 different capacitor locations with different input and output locations.

It should be noted here that the inductance associated with the connection of the test ports was not accounted for in the derivation of (12). An analysis including this inductance for the configurations tested shows that it contributes less than 1% error to the resonance frequency. Up to 60 MHz, (12) was found to agree to within less than 1 dB with the measured S_{21}.

The test system in Fig. 12 was employed to measure the inductance and resistance of typical interconnects, and the magnitude of the printed circuit board impedance. The tests were performed primarily on two functional printed circuit board designs and a third board that was designed and manufactured specifically for this study. The board designations used in the remainder of this paper are the following.

- Board #1: 10 layer, $8'' \times 9''$, C_B measured = 2.6 nF.
- Board #2: 6 layer, $8'' \times 9''$, C_B measured = 3.4 nF.
- Board #3: 4 layer: $7'' \times 8''$, C_B measured = 15.3 nF.

The power and ground planes of the first two boards do not make maximum use of the board area available, hence

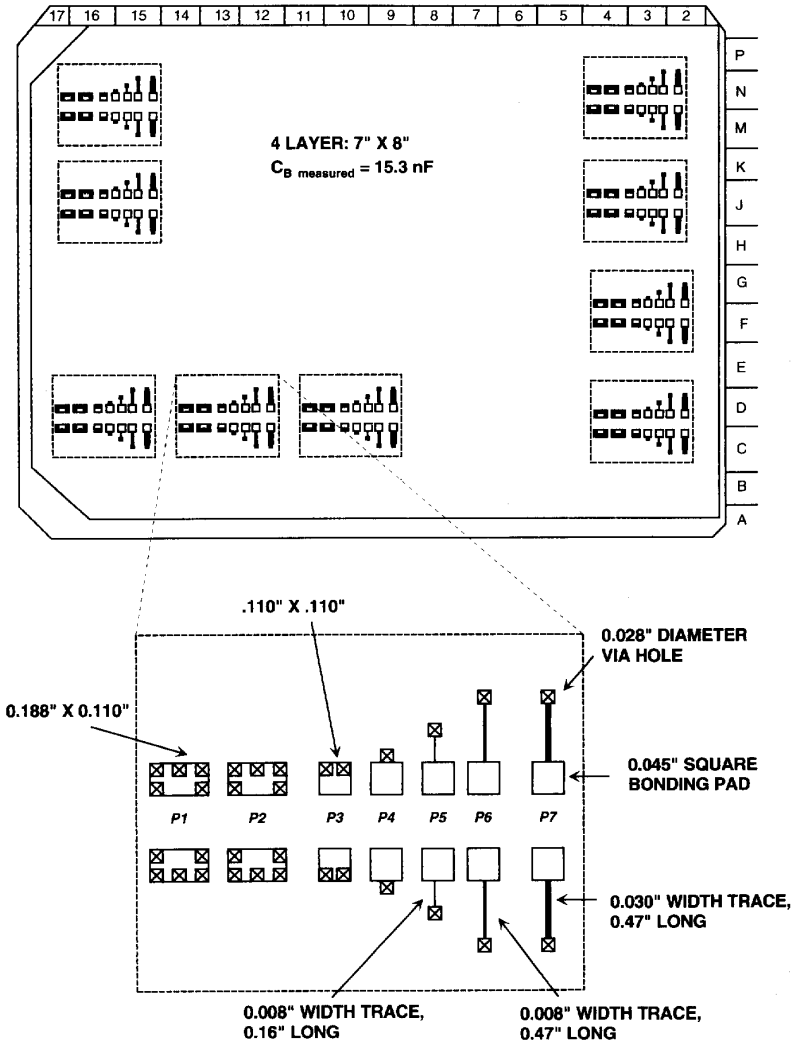

Fig. 16. Board #3 layout and dimensions of capacitor interconnects.

the smaller value of interplane capacitance. Representative decoupling capacitor locations were identified on each of the first two boards. Their approximate positions on the board are shown in Fig. 13.

The interconnect inductance associated with each capacitor position was determined by shorting the capacitor mounting pads and measuring the frequency at which the interconnect inductance resonated with the plane capacitance. The short was implemented using a wide strap soldered across the narrow gap of the interconnect. The strap was the full width of the bonding pad (or approximately the width of a capacitor body). Thus the inductance contributed by this connection was small relative to the via and trace inductance. The measured inductance for each capacitor position is given in Table I. The minimum inductance measured for these circuit designs was 2.6 nH and the maximum value was 7.7 nH. For other printed circuit boards investigated during the course of this study, values of measured inductance ranged from 2.5–10 nH.

Fig. 14 shows the measured board impedance as a function of frequency when a single 1 nF capacitor is located at four different positions on Board #1. A measurement of the impedance of the bare board (no capacitors) is also plotted for comparison. There is a small glitch in the measured response at approximately 70 MHz, which is due to the non-zero inductance of the probe connections. Since this was a production board, the only access to the power and ground planes was through existing decoupling capacitor mounting pads. The interconnect inductance of the probes does not significantly affect the other board impedance measurements. The series and parallel resonances in Fig. 14 are readily identified and it is apparent that above the parallel-resonance frequency, the presence or absence of the decoupling capacitor has little effect in any position. The series-resonance frequencies shift depending on the value of the interconnect inductance. However, the relative position of a particular decoupling capacitor on the board has very little effect on the response.

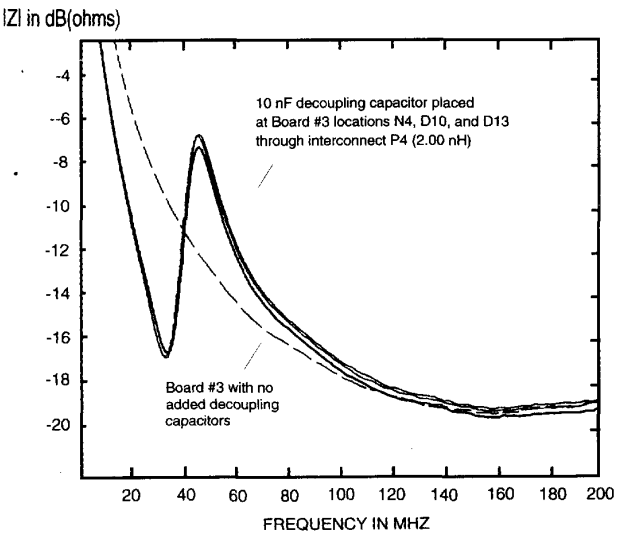

Fig. 17. Board #3 impedance with a 10-nF capacitor at 3 different locations.

Fig. 15 is similar to Fig. 14 with the exception that the input and output test ports are in close proximity rather than on opposite sides of the board. Again it is observed that below approximately 200 MHz it is the inductance of the capacitor mounting location that affects the response, and the location of the capacitor on the board is relatively unimportant. Above 200 MHz, the distributed inductance of the power bus begins to have a significant effect on the board impedance and the shape of the response is dependent on the location of the probes. However even above 200 MHz, the board impedance remains independent of the capacitor location, because the decoupling capacitor does not supply significant current.

Board #3 was designed and manufactured specifically for this study. This multilayer board contained 63 bonding pads for surface-mount capacitors connected to the power bus through six different geometric configurations of varying inductance and resistance. The bonding pads were made larger (more surface area) than typically used so that low inductance bonding configurations using multiple via holes could be studied. The board layout and dimensions of the capacitor interconnects are shown in Fig. 16.

The series inductance and resistance of each decoupling capacitor interconnect was measured using the network analyzer as described in the previous section. The series resistance was obtained from measurements of S_{11} at the parallel-resonance frequency. Values for the six different geometries shown in Fig. 16 are provided in Table II. As expected, the inductance and resistance are highest for the longest and narrowest traces.

Fig. 17 shows the power distribution bus impedance of Board #3 when a 10 nF capacitor is positioned at 3 different locations. Each location uses the P4 interconnect (2.00 nH). As the figure indicates, the position of the capacitor has very little effect on the board impedance at any frequency. Beyond the parallel resonance, the impedance is virtually the same with or without the capacitor.

The effect of multiple decoupling capacitors on the measured board impedance is illustrated in Fig. 18. The curve

TABLE II
INTERCONNECT INDUCTANCE VALUES FOR BOARD #3

Capacitor Interconnect	Resistance (mΩ)	Inductance (nH)
P_2	12	0.61
P_3	17	1.32
P_4	22	2.00
P_5	54	7.11
P_6	95	15.7
P_7	53	10.3

labeled "2 capacitors" shows the measured impedance of Board #3 with a 106 nF and a 10.5 nF capacitor, each connected to 1.32 nH mounting pads. Using a model similar to the one in Fig. 4, the calculated series-resonance frequencies are 13 and 47 MHz. The calculated parallel-resonance frequencies are 27 and 50 MHz. These correspond reasonably well to the measured nulls and peaks in the board response. The curve labeled "5 capacitors" shows the measured impedance of the same board with one 106 nF capacitor and four 10 nF capacitors. All of the capacitors are connected to 1.32 nH mounting pads. Since the four 10 nF capacitors are all connected through identical mounting pads, their series-resonance frequencies are the same. Therefore, the 5-capacitor board response is expected to have nulls in the same positions as the 2-capacitor response. The parallel-resonance frequencies are shifted however. The model predicts that parallel resonance should occur at 18 and 78 MHz on the 5-capacitor board. These frequencies are close (within 10 and 4% respectively) to the measured peaks in the board response.

VI. CONCLUSION

Unlike boards without internal power and ground planes, multilayer boards have a built-in capacitance that is a more effective source of current than surface decoupling capacitors at high frequencies. In the time-domain, this means that most of the initial current supplied to a fast switching device is provided by the interplane capacitance.

On printed circuit boards that do not have internal power and ground planes, it is important to locate decoupling capacitors near to the active devices that they are intended to decouple. The capacitors nearest the active device are the primary source of high frequency current even at frequencies well above the capacitor's self-resonance frequency. However, on printed circuit boards that do have internal power and ground planes, all decoupling capacitors are shared in the frequency range in which they are effective (typically below 200–300 MHz), and the location of a decoupling capacitor on the board is relatively unimportant.

At frequencies above series resonance, the inductive reactance of decoupling capacitors on a multilayer board resonates with capacitance within and on the board resulting in undesirable peaks in the board impedance. Beyond the highest parallel-resonance frequency, added decoupling capacitors on a multilayer board supply relatively little current to the active devices and are therefore ineffective.

Reducing the inductance of the interconnects is perhaps the best way to get added decoupling capacitors to be effective at higher frequencies. Large vias or multiple vias within the capacitor bonding pads can be used to achieve interconnect

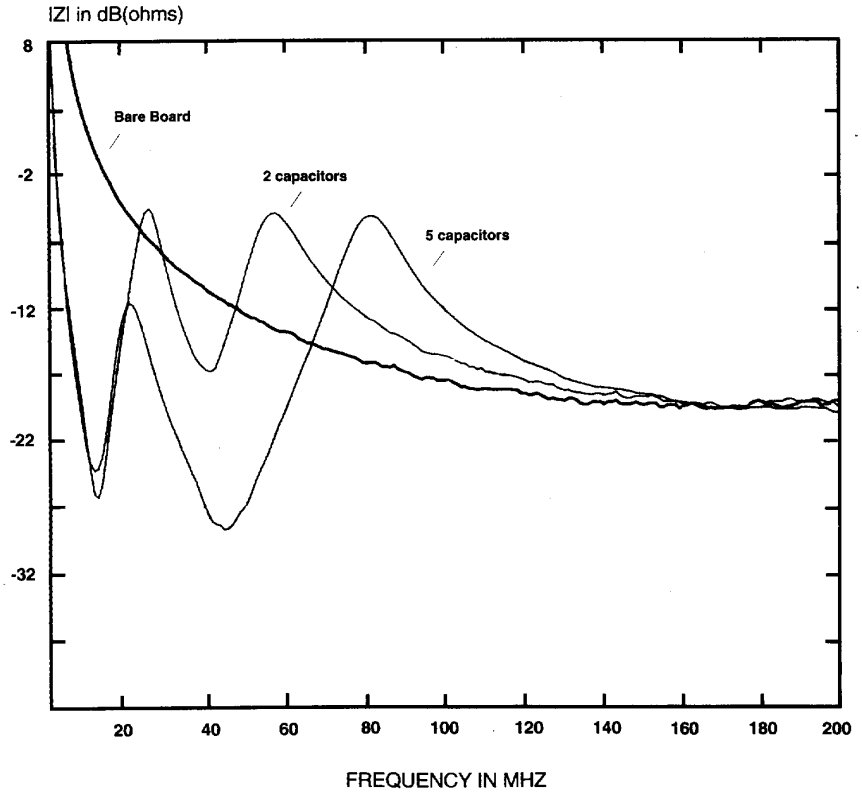

Fig. 18. Board #3 impedance with 0, 2, and 5 capacitors.

inductances less than 1 nH. Using many decoupling capacitors with the same value and same interconnect inductance also increases the effective frequency range as indicated by (5) and (9).

Different circuits and different board layouts may require different decoupling and power distribution strategies. However, the results presented here indicate that existing multilayer board designs with typical interconnect inductances of 2–10 nH do not make effective use of all the added decoupling capacitors. Multilayer boards with a few nanofarads of interplane capacitance that have decoupling capacitors connected through a few nanohenries of inductance derive very little benefit from any of the added decoupling capacitors above approximately 100–200 MHz.

ACKNOWLEDGMENT

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REFERENCES

[1] B. Rubin and W. D. Becker, "The modeling of delta-I noise in high performance computer modules," in *Conf. Rec. 17th Asilomar Conf. Circ., Syst., and Comput.*, IEEE Cat. #83CH1939-8, Oct. 31/Nov. 2, 1983.

[2] N. Raver *et al.*, "Circuit noise study," in *Proc. Tech. Prog. NEPCON WEST 92*, Anaheim Convention Center, Anaheim, CA, Feb. 23–27, 1992, pp. 77–86.

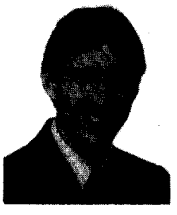
[3] R. Downing, P. Gebler, and G. Katopis, "Decoupling capacitor effects on switching noise," in *Conf. Rec. IEEE Topical Meet. Elect. Perform. Electron. Packaging*, IEEE Cat. #92TH0452-5, Apr. 22–24, 1992.

[4] C. R. Paul, "Effectiveness of multiple decoupling capacitors," *IEEE Trans. Electromagn. Compat.*, vol. 34, pp. 130–133, May 1992.

[5] A. R. Djordjevic and T. K. Sarkar, "An investigation of delta-I noise on integrated circuits," *IEEE Trans. Electromagnetic Compat.*, vol. 35, no. 2, pp. 134–147, May 1993.

[6] H. W. Ott, *Noise Reduction Techniques in Electronic Systems*, 2nd ed. New York: John Wiley Interscience, 1988.

[7] T. Van Doren, J. Drewniak, and T. Hubing, "Printed circuit board response to the addition of decoupling capacitors," Tech. Rep. #TR92-4-007, UMR EMC Lab., Sept. 30, 1992.



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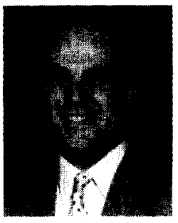

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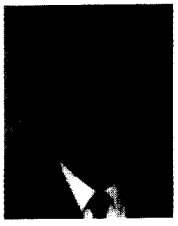

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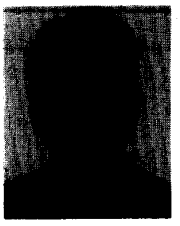

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