01 Mar 2000

Behavioral IGBT Modeling for Predicting High Frequency Effects in Motor Drives

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***Abstract*—A first-order behavioral IGBT/gate drive model is proposed together with a procedure for deriving all model parameters. Despite the simplicity of the proposed model, comparison of model predictions with hardware measurements demonstrate the model to be accurate in predicting turn-on and turn-off transients.**

***Index Terms*—Behavioral modeling, IGBT.**

I. Introduction

DETAILED simulations of motor drives and other power electronics equipment meant for use in full component or systems studies generally treat semiconductor devices as ideal or nearly ideal switches in which the semiconductors are either completely on or completely off [1]. This idealization is made for the sake of computational efficiency, and is generally appropriate for the types of studies for which the simulations are meant—low frequency (kHz range and less) harmonic analysis, transient stability, etc.

However, there are a host of problems also at the system level, which are related to switching devices acting as noise sources, and thereby exciting parasitics in power-electronic circuits. These problems include; semiconductor device stresses due to switching transients [2], electromagnetic compatibly problems (particularly in regard to common-mode currents [3]), over-voltages at the machine terminals due to resonance and transmission-line effects [4], and capacitive effects in the electric machinery such as bearing currents that leads to fluting [5], [6].

Time-domain simulation of undesirable high-frequency effects requires nonideal semiconductor device models, detailed representations of circuit parasitics, and finally, detailed high-frequency models of the electric machines. The focus of this paper is the development of a suitable semiconductor device model for the insulated gate bipolar transistor (IGBT). There are two basic approaches to deriving such a model. First, a physics-based approach may be used [7], [8]. However, such models are complicated and are not computationally conducive to system simulation. For example, a 5th order IGBT model has been reported [8], which, while very useful for some analysis is not conducive to a total system analysis due to the fact that the total system order becomes very high when every semiconductor in the system is represented in this fashion. A second approach is the use of behavioral models [9]–[11]. For example, a 4th-order behavioral IGBT model is proposed in [9], and is shown to compare well to a physics-based model. Nevertheless, existing behavioral models are still more complex than is desirable in a system simulation environment.

A new behavioral IGBT model especially well suited to system analysis is proposed herein. This model has several benefits for system simulations in that; it is dynamically first-order, and therefore, not computationally intensive, all parameters are readily measurable, and it provides the noise source for excitation of system parasitics so that the EMC/EMI problems noted above can be further studied. Although there are disadvantages of this approach such as the model is not as conducive to the design of base drive circuitry as other models [7]–[12], and spurious turn-on of the IGBT due to dv/dt effects cannot be predicted; the model is excellent for assessing the impact of the IGBT performance on the rest of the circuit or system. Comparison of simulation results based on the proposed model with measurements in a test circuit demonstrates that the proposed model yields accurate predictions of device performance.

II. Model Structure

The proposed behavioral IGBT model is shown in Fig. 1. The model consists of two parallel branches. The first branch is a series connected ideal diode, time-varying conductance $G(t)$, and a constant voltage source v_{ss}. In the steady-state, with the device on, $G(t)$ will take on a positive constant value such that this part of the circuit will approximate the static I-V characteristic of the IGBT. Conversely, in the steady state with the device off, $G(t)$ will go to zero. After the device is turned on or off, $G(t)$ will vary between steady-state on and off values in such a way as to represent the effects of a changing carrier distribution within the semiconductor. The second branch in the model, a voltage dependent capacitance and series resistance, represent the effects of the junction capacitance of the back-to-back diodes in the BJT portion of the device.

Neither the gate-to-emitter voltage nor the gate current is an input to the behavioral model. At first glance, a two-terminal model seems inappropriate, since a terminal for turning the device on or off is not provided. In this model, however, the effect of the gate-drive circuit is captured in $G(t)$, including rise and fall times, and propagation delays. This greatly facilitates system simulation, since it provides a means for including the effects of the gate-drive circuit without simulating it in detail.

Manuscript received November 5, 1997; revised September 25, 1999. This work was supported by the University of South Carolina under Grant N00014-96-1-0926 with the Office of Naval Research. Recommended by Associate Editor, G. Dubey.

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Publisher Item Identifier S 0885-8993(00)02347-4.

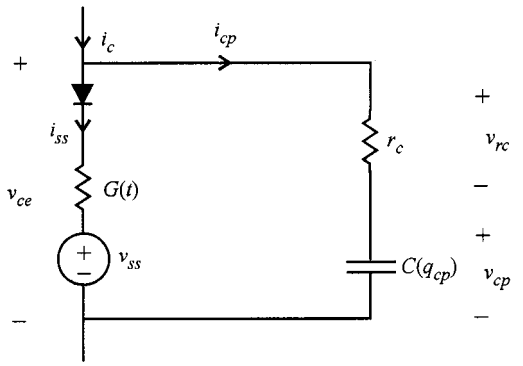

Fig. 1. Behavioral IGBT model.

The computational advantages and savings from a system simulation perspective are significant. However, there are disadvantages in that the model may not be readily used to design base-drive circuitry, and spurious turn-on of the IGBT cannot be predicted.

The proposed model is formulated such that the collector current i_c, and the logic switching signal are inputs, and the collector-emitter voltage v_{ce} is an output as seen from Fig. 1. Although the switching signal is not indicated in Fig. 1, its effect is upon $G(t)$ and will be described in a later section. As with any dynamic model, the functional form must be such that the model outputs and time derivatives of the state variables can be calculated in terms of the input and state variables. The first step in doing this is the calculation of the conductance $G(t)$. In order to specify the conductance, it is convenient to define the turn-on time t_{on}, and turn-off time t_{off} as the amount of time it takes for the IGBT carrier populations to reach steady state after the logic signal to the gate drive circuit has made an on- or off-transition, respectively. It is also convenient to define the turn-on and turn-off switch times, t_{sw_on} and t_{sw_off}, as the instant in time of the last off-to-on and on-to-off transitions of the logic input to the gate drive circuitry. With these definitions, the conductance is

$$G(t) = \begin{cases} 0 & \begin{cases} t \geq t_{sw\_off} + t_{off} \\ \text{and } t_{sw\_off} > t_{sw\_on} \end{cases} \\ G_{turn\_on}(t - t_{sw\_on}) & t_{sw\_on} + t_{on} \\ & \geq t > t_{sw\_on} \\ G_{on} & \begin{cases} t \geq t_{sw\_on} + t_{on} \\ \text{and } t_{sw\_on} > t_{sw\_off} \end{cases} \\ G_{turn\_off}(t - t_{sw\_off} & t_{sw\_off} + t_{off} \\ & \geq t > t_{sw\_off} \end{cases} \tag{1}$$

where $G_{turn\_on}(t)$ and $G_{turn\_off}(t)$ are the transient conductance after turn-on and turn-off relative to the time at which the logic input to the gate drive module has undergone an off-to-on or on-to-off transition, and G_{on} is the on-state conductance after the switching transient is over.

The next step is calculation of the capacitor voltage

$$v_{cp} = f_C(q_{cp}). \tag{2}$$

where q_{cp}, the capacitor charge, is the state variable. The collector-emitter voltage is determined from the conductance and capacitor voltage by

$$v_{ce} = \begin{cases} \dfrac{i_c r_c + v_{ss} G(t) r_c + v_{cp}}{G(t) r_c + 1}, & i_c r_c + v_{cp} > v_{ss} \\ r_c i_c + v_{cp}, & i_c r_c + v_{cp} \leq v_{ss}. \end{cases} \tag{3}$$

The two expressions in (3) correspond to the ideal diode being forward and reverse biased, respectively. The two branch currents are then

$$i_{co} = \frac{v_{ce} - v_{cp}}{r_c}. \tag{4}$$

and

$$i_{ss} = \begin{cases} G(t)(v_{ce} - v_{ss}), & i_c r_c + v_{cp} > v_{ss} \\ 0, & i_c r_c + v_{cp} \leq v_{ss}. \end{cases} \tag{5}$$

The only state variable in this model is the capacitor charge, which is related to the branch current i_{cp} by

$$\frac{dq_{cp}}{dt} = i_{cp}. \tag{6}$$

Although this model is quite simple, it can nevertheless be used to accurately portray the switching behavior of the power semiconductor. It is now appropriate to discuss the measurement procedure by which the parameters $t_{on}, t_{off}, G_{turn\_on}(t)$, $G_{turn\_off}(t)$, G_{on} and $f_C(q_{cp})$ are determined.

III. Parameter Measurement

The model shown in Fig. 1 is of a form such that the parameters may be readily measured or extracted from experimental data based on a series of four tests—a static I-V characteristic, an off-state capacitance test, a turn-on characterization test, and a turn-off characterization test. The procedure for each of these tests follows, and example results are provided for a 600 V, 50 A Fuji Electric 1MBI50L-060 IGBT driven by a Fuji Electric EXB840 gate drive circuit. The test circuit in which the model is applied used two of these devices with the model parameters determined for only one particular device.

A. Static I-V Characterization

The static I-V characteristic of the IGBT is determined first. It is important to conduct the test quickly, and at an appropriate temperature if the model is being used to determine conduction losses. For the sample device, the I-V curve is shown in Fig. 2. For large values of V, the characteristic becomes approximately linear and can be represented by

$$i_c = G_{on}(v_{ce} - v_{ss}). \tag{7}$$

where G_{on} is the slope, and v_{ss} is the v_{ce}-axis intercept. For the sample Fuji IGBT, $v_{ss} = 1.91$ V and $G_{on} = 55.8\ \Omega^{-1}$.

B. Capacitance Characterization

In the on state, the current is predominantly through $G(t)$. Therefore, the capacitive branch of the equivalent circuit is characterized with the IGBT in the off-state. A test circuit for this characterization is depicted in Fig. 3. The device Q1 acts as a

switch in order to conduct the test, and Q2 is the device under test. The resistor R_1 limits the current to the operating range of the semiconductors. The resistor R_2 is chosen small enough so as to pull the collector-emitter voltage of the device under test to zero when Q1 is off but large enough that the final Q2 collector-emitter voltage after Q1 is turned on is reasonably close to v_{dc}. The test itself consists of running a number of trials in which the Q2 collector current and collector-emitter voltage are measured as Q1 is turned on with various values of v_{dc}.

The procedure for each trial is as follows. First, a small negative voltage v_{ge} consistent with the turn-off voltage of the base drive circuit is applied to the gate of the device under test. Initially, Q1 is also turned off so that the collector-emitter voltage and collector current of the device under test is zero. Next Q1 is turned on and the Q2 collector-emitter voltage and collector current are measured through the turn on transient of Q1 for each test value of dc source voltage. In these tests a Tektronix A6302 current probe was used. The capacitor charge q_{cp} is determined by integrating the collector current. When performing this integration, any dc offset from the collector current measurement must be removed prior to the integration. Next, the Q2 collector-emitter voltage v_{ce} is plotted versus the capacitor charge q_{cp} during the turn-on transient of Q1. In the steady-state, the collector-emitter voltage is equal to the nonlinear capacitor voltage. Therefore, the endpoint of the transient charge-voltage trajectory represents one point of the capacitor voltage versus charge characteristic.

This process is repeated for several values of the dc source voltage in order to construct a family of collector-emitter voltage versus charge characteristics as illustrated in Fig. 4. Measurements were conducted on the sample device for v_{dc} equal to 25, 50, 100, 200, 300, 400, 500, and 550 V. For this test, R_1 and R_2 were 180 Ω and 470 Ω, respectively. Using curve-fitting techniques, the end-points were used to construct an approximation to the nonlinear capacitor voltage versus charge characteristic (which is also superimposed on Fig. 4). A functional form approximating this relationship that is nearly linear for small and large values of its argument, and having a tailorable transition in between was chosen. In particular, the voltage-charge characteristic was approximated by

$$f(q_{cp}) = \frac{2\alpha_d}{\pi}((q_{cp}-q_T)\tan^{-1}(T(q_{cp}-q_T)) - q_T\tan^{-1}(Tq_T)) + \alpha_a q_{cp} + \frac{\alpha_d}{\pi T}[\ln(1+T^2q_T^2) - \ln(1+T^2(q_{cp}-q_T)^2)] \quad (8)$$

where α_d and α_a are the difference and sum of the initial and final slopes of the voltage charge characteristic divided by two, respectively, q_T is the charge about which the change in slope is centered, and T is related to the tightness of the transition between the region with the initial slope and the region with the final slope. For the sample device, α_d, α_a, q_T, and T have values of 1.86e9 F^{-1}, 2.73e9 F^{-1}, 31.7 nC, and 2.07e8 nC^{-1}, respectively.

The series resistance r_c, is determined next with the same test data that was used to generate the capacitor voltage relationship, although only data for one trial, typically the one with the highest dc voltage is used. Since the charge may be determined

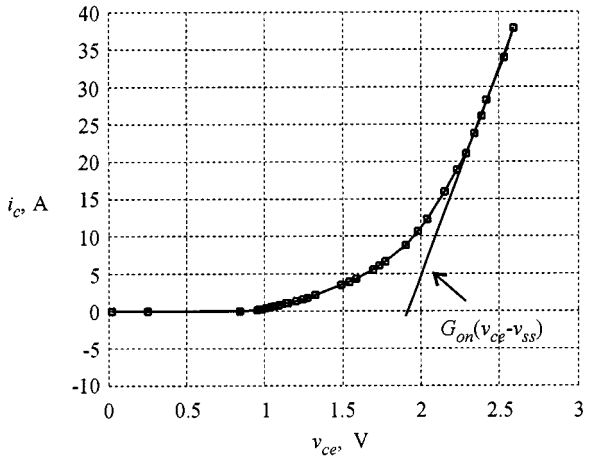

Fig. 2. Static I-V characteristic.

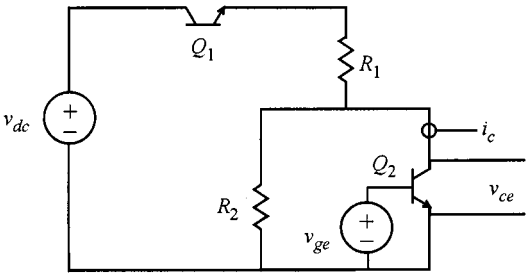

Fig. 3. Test circuit to determine $f_c(q_{cp})$ and r_c.

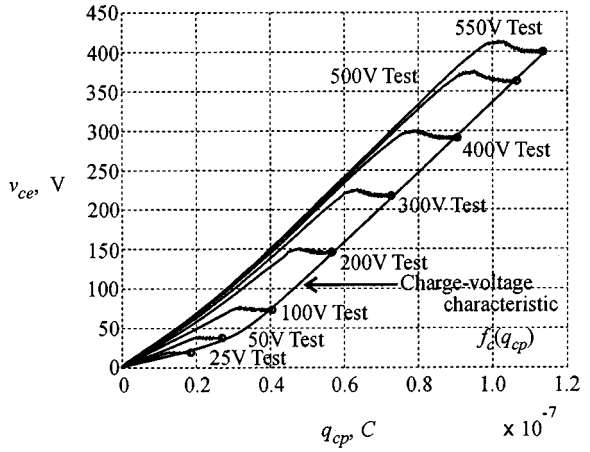

Fig. 4. Voltage-charge characteristic.

at any point in time, and the relationship between the capacitor voltage and charge has been obtained, it is possible to determine the capacitor voltage $f_C(q_{cp})$ (as shown in Fig. 4) at any point in time during the trial, from which the voltage across the resistor r_c may be found as

$$v_r = v_{ce} - f_c(q_{cp}). \quad (9)$$

The resistor voltage is plotted as a function of the current i_{cp} throughout the transient of the trial in Fig. 5. Since the model is only approximate, the characteristic is not a straight line. However, it may be numerically fitted to a straight line with zero

intercept as an approximation. Performing such a fit in the case of the sample device yields $r_c = 77.8\ \Omega$.

C. Turn-On and Turn-Off Characterization Test

The test circuit for the turn-on characterization test used to determine t_{on} and $G_{turn\_on}(t)$ during the turn-on transient of the IGBT is shown in Fig. 6. The IGBT is used to switch on and off a resistive load r_l with parasitic inductance L_l. The load value is selected so as to exercise the full operating range of the device. An RC snubber of resistance r_s, capacitance C_s, and parasitic inductance L_s is used to prevent an overly large voltage spike when the IGBT is turned off. The voltage source represented by v_{ge} should be the entire gate drive circuit that will be used in conjunction with the IGBT. The IGBT is turned on using the gate-drive circuit, and the logic signal into the base-drive circuit, denoted by S. The collector current and the collector-emitter voltage are recorded. These measured collector current and collector-emitter voltage waveforms will be denoted i_{c_meas} and v_{ce_meas}, respectively.

The first step in processing this data is to remove any dc offsets from the waveforms resulting from the voltage and current probes. In order to remove the dc offset from the current waveform, the current waveform during a brief period before the device is turned on is averaged in order to determine the offset value. This offset is then subtracted from the measured current waveform. The voltage offset is removed by subtracting the average voltage after the turn on transient is over from the voltage waveform, and adding the on-state voltage determined from the static I-V characteristic.

Once the dc offsets in the voltage and current measurements have been determined, the measured waveforms i_{c_meas} and v_{ce_meas} are injected into the proposed model in order to determine $G_{turn\_on}(t)$, where t is relative to the logic input command signal off-to-on transition. The first step in doing this is to determine the current into the capacitive branch, which is determined using (4) with v_{ce_meas} and v_{cp} as calculated from (4), (6), and (8). From the behavioral model, $G_{turn\_on}(t)$ can be expressed in terms of the calculated capacitive branch current i_{cp}, the measured collector emitter voltage v_{ce_meas}, and measured collector current i_{c_meas} as

$$G_{turn\_on}(t) = \frac{i_{c\_meas} - i_{cp}}{v_{ce\_meas} - v_{ss}}. \tag{10}$$

The turn on time t_{on} is determined as the amount of time necessary for $G_{turn\_on}(t)$ to reach G_{on}.

Fig. 7 illustrates $G_{turn\_on}(t)$ for the sample device using the test circuit depicted in Fig. 4 with $r_l = 24.4\ \Omega$, $L_l = 2.22\ \mu$H, $r_s = 24.9\ \Omega$, $C_s = 0.81$ nF, $L_s = 2.63\ \mu$H and $v_{dc} \approx 300$ V (the approximation is due to the voltage distortion arising from the source impedance). In this figure, t is referenced from the point where the logic signal swings from LO to HI. Once $G_{turn\_on}(t)$ is determined, it is stored in a table and calculated as an interpolated function when using the model. The turn-on time of 3.3 μs can be determined by looking for the point where $G_{turn\_on}(t)$ becomes sufficiently close to G_{on} to be approximated by that value.

The turn-off test is essentially identical to the turn-on test with the exception that the device is turned off rather than on.

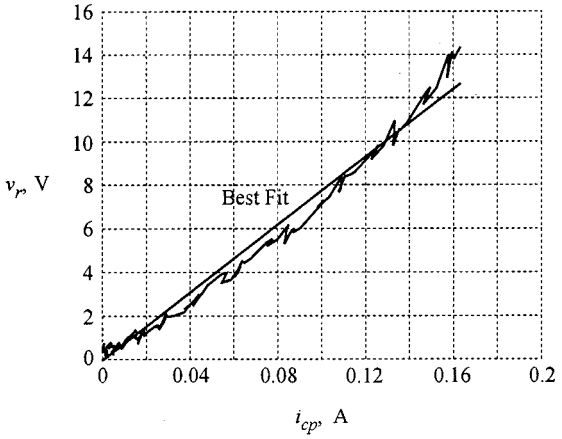

Fig. 5. Determination of r_c.

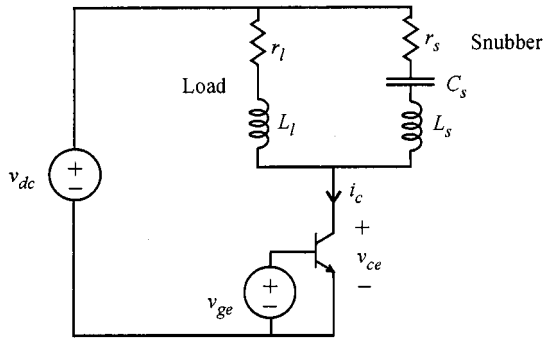

Fig. 6. Test circuit to determine $G(t)$.

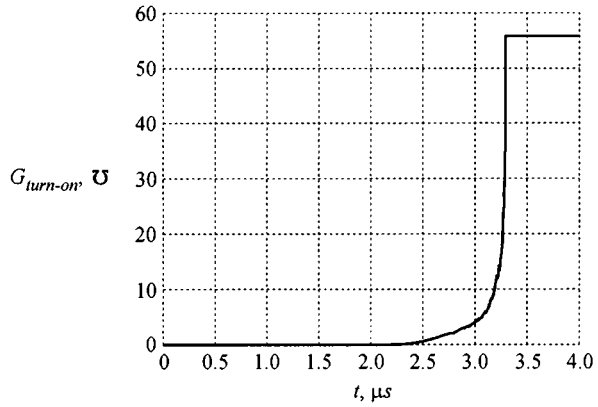

Fig. 7. $G(t)$ during turn-on.

As in the case of the turn-on test, it is important to remove dc offsets from the voltage and current measurements. In this case, however, the voltage offset is calculated prior to turn-off and the current offset after turn-off. In addition, in performing this test, time is referenced relative to the point where the device is turned off. The same procedure applies to the calculation of $G_{turn\_off}(t)$ as in the case of the turn-on test, and the same test circuit and source voltage were used. The resulting conductance profile for the sample device is shown in Fig. 8, from which t_{off} is determined to be 2.8 μs. It is interesting to observe that the rate of decay of $G_{turn\_off}(t)$ decreases considerably as the device

turns off—this is a direct result of the current-tail phenomenon which is in this way incorporated into the model.

IV. Model Validation

The circuit shown in Fig. 9 was used to validate the proposed model. This circuit was chosen because it contains two devices, only one of which is characterized. Further, the circuit allows an alternating current to be drawn, as is the case with motor drives. The upper IGBT is the same device used to illustrate the characterization procedure given above, while the parameters of the lower device were assumed to be the same as that of the device under test in order to demonstrate that part-to-part variations do not critically change the parameters. Parameter values for the load, snubbers, and parasitics were measured to 10 MHz with an HP4193A Vector Impedance Meter and are given in Table I.

Based on (1)–(6) and the circuit elements of Fig. 9 a state space system model for the test circuit was developed and implemented in advanced continuous simulation language (ACSL) [13]. In this model the collector current and TTL level switching signal were inputs, and the collector-emitter voltage was the output. The time varying conductance, $G(t)$ was implemented using a table in which the independent variable, t can be defined. This is a useful feature in that after each switching transition, a 'dummy' time variable can be reset to zero so that the model will be ready for the next switching event, and the correct $G(t)$, ($G_{turn\_on}(t)$ or $G_{turn-off}(t)$) can be invoked.

Due to distortion of the source voltages arising from the source impedance, the measured source voltages were inputs to the simulation. In this way, the critical comparison can be made without characterizing the source. Care must be taken in that the timing of the source voltages, v_{dcl} and v_{dcu} must coincide with the switching signals, collector-emitter voltages, and collector currents of the IGBT's. For this comparison, two four-channel Tektronix 420A oscilloscopes were both triggered with the same signal (upper transistor switching signal) through the external trigger port, and all scope settings were identical. These waveforms were then brought into the simulation where the source voltages were utilized for excitation, the switching signals for turning the devices on and off, and the other waveforms for comparison. Since the ripple on the source voltage decayed rapidly, and was not more than 12% of the mean value, simulations for constant source voltages were also performed. The level of the constant source voltages applied was determined from the mean of the measured source voltages during circuit steady-state conditions, with both devices off and all transients settled out. The applied voltages were determined to be $v_{dcl} = 152.0$ V, and $v_{dcu} = 143.0$ V. Fig. 10 depicts the turn-on transient for the upper transistor. The traces depicted are the upper and lower measured source voltages v_{dcl} and v_{dcu}, upper transistor collector-emitter voltage v_{ceu}, and upper transistor collector current i_{cu}. The agreement between the measured and simulated collector-emitter voltage and collector current is good. The constant source voltage simulation is in good agreement as well.

The upper transistor turn-off transient is shown in Fig. 11. Again, the measured source voltages, upper transistor collector-emitter voltage, and upper transistor collector current

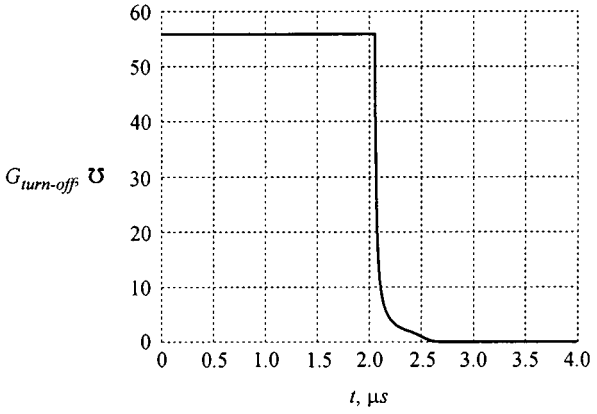

Fig. 8. $G(t)$ during turn-off.

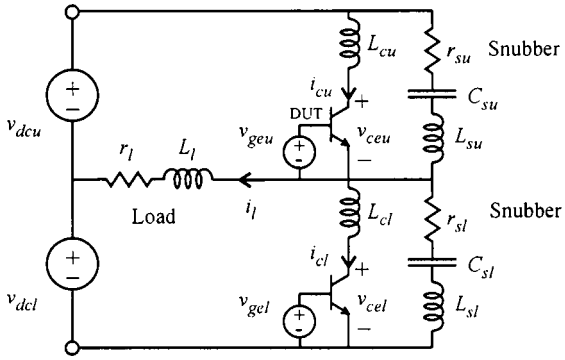

Fig. 9. Model validation circuit.

TABLE I
Validation Circuit Parameters

r_l=9.50 W	C_{su}=0.955 nF
L_l=2.62 mH	L_{su}=2.30 mH
L_{cu}=95.4 nH	r_{sl}=25.5 W
L_{cl}=95.4 nH	C_{sl}=0.967 nF
r_{su}=25.4 W	L_{sl}=2.36 mH

waveforms are shown. The simple first-order model predicts the over-voltage in collector-emitter voltage well. In particular, the model predicts the over-voltage to less than 1% with measured source voltages as inputs, and 1.8% for constant source voltages.

Figs. 12 and 13 depict the turn-on and turn-off transients for the lower transistor, respectively. Although, the agreement is not as good as in Figs. 10 and 11 since the lower device was not characterized, the simple model again predicts the dynamics well. During turn-off the model predicts the over-voltage of the lower transistor collector-emitter voltage to 8.5% with measured source voltages as inputs, and to 13.2% for constant source voltages.

Although not shown for brevity, this study was repeated with a total DC rail voltage ($v_{dcu} + v_{cdl}$, approximately even split) of

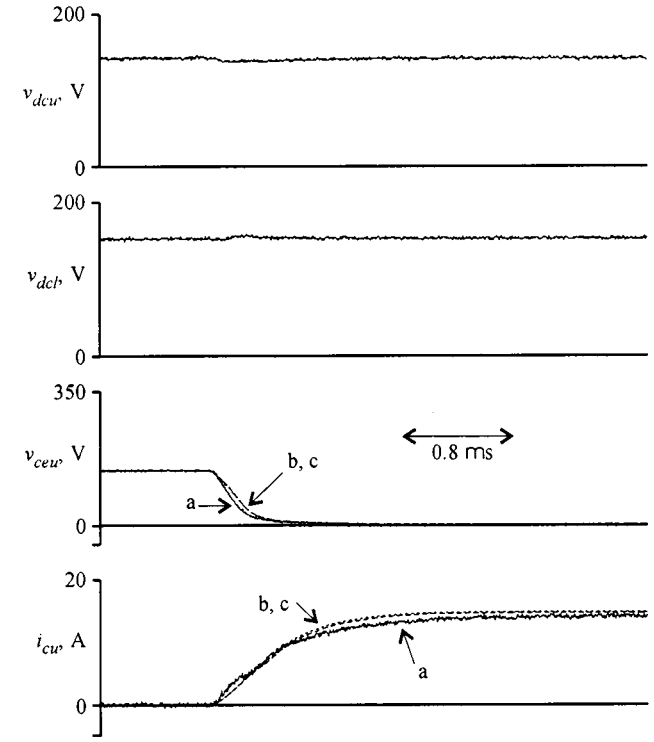

Fig. 10. Upper transistor turn-on transient; (a) measured, (b) simulated with measured source input, (c) simulated with constant source input.

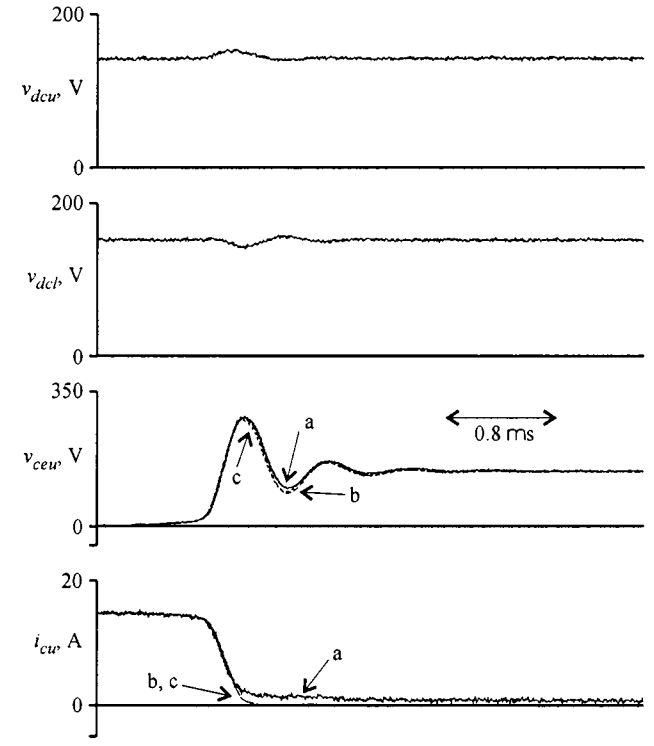

Fig. 11. Upper transistor turn-off transient; (a) measured, (b) simulated with measured source input, (c) simulated with constant source input.

75 V, 150 V, and 225 V, thereby varying the on state current over a considerable range. In each case, the agreement between the simulated and measured results were consistent with the study shown herein.

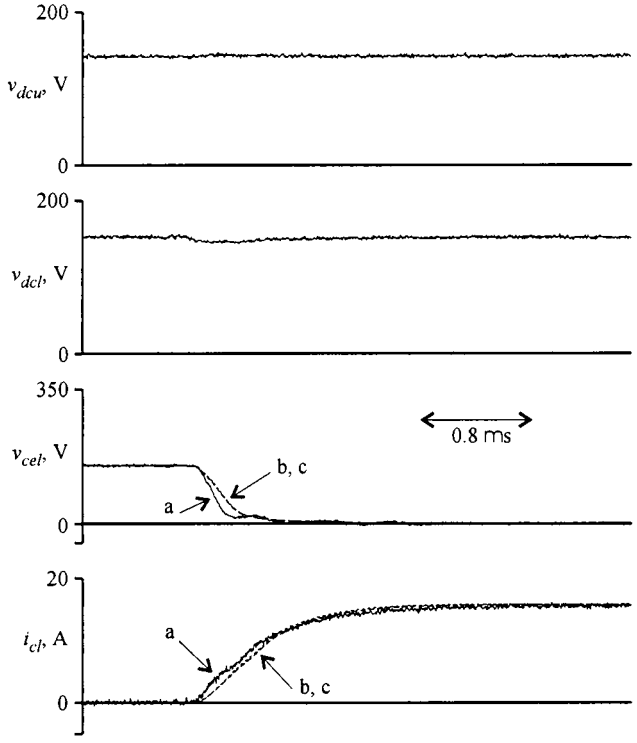

Fig. 12. Lower transistor turn-on transient; (a) measured, (b) simulated with measured source input, (c) simulated with constant source input.

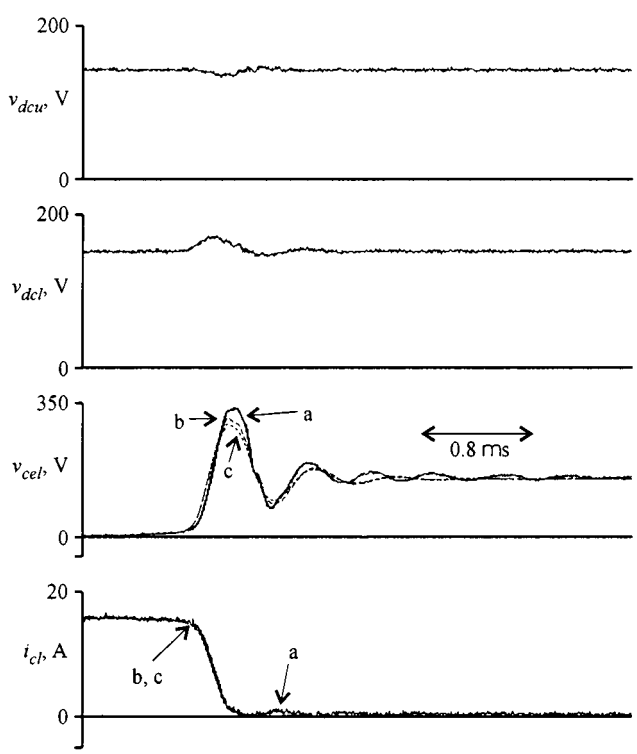

Fig. 13. Lower transistor turn-off transient; (a) measured, (b) simulated with measured source input, (c) simulated with constant source input.

V. Conclusion

A simple behavioral model of an IGBT with its associated gate drive circuitry was proposed and experimentally verified.

The model is considerably simpler than previous behavioral models, and all parameters are readily derived experimentally. The simplicity of the proposed model makes it particularly appropriate for system simulation of high frequency effects in power electronic circuits and motor drives. One aspect of the model which has not been explored is the ability to accurately predict the device performance under soft-switched conditions. However, in this case it is likely that the dynamics will be dominated by the resonant circuitry rather than the IGBT. Additional future work which is needed is to combine this model with a suitable diode and machine models [14] in order to represent complete motor drives.

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