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Control Technique for Series Input-Parallel Output Converter Topologies

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***Abstract* – A series input-parallel output dc-dc converter topology inherently provides output current sharing among the phases, provided the input voltages are forced to share. With conventional output voltage feedback controls, input voltage sharing is unstable. Recent literature work proposes complicated feedback loops to provide stable voltage sharing, at the expense of dynamic performance. In the current work, a simple controller based on the sensorless current mode approach (SCM) stabilizes voltage sharing without compromising system performance. The SCM controllers reject source disturbances, and allow the output voltage to be tightly regulated by additional feedback control. With SCM control in place, a "super-matched" current sharing control emerges. Sharing occurs through transients, evolving naturally according to the power circuit parameters. The control approach has considerable promise for high-performance voltage regulator modules, and for other applications requiring high conversion ratios. Experimental results confirm the control operation. A sample four-phase converter has demonstrated good disturbance rejection, static sharing, and dynamic sharing.**

I. Introduction

A series input-parallel output (SIPO) topology shows promise in systems requiring high performance and high conversion ratio. For example, a 36 V-to-0.7 V four-phase converter, shown in Fig. 1, has been constructed with an effective ripple frequency of 600 kHz. If voltage sharing among the phases is forced at the input, then current sharing at the output follows. Conventional methods of output control (current mode or voltage mode) do not generate stable input voltage sharing, so recent work in the literature has constructed complex feedback loops that stabilize sharing [1]-[3]. A simple control scheme is presented here that stabilizes sharing with no compromise in system response.

A number of topologies provide high step-down conversion ratios. At the most basic level, a buck converter can be used for an arbitrary conversion ratio. Losses become significant and efficiency drops quickly at extreme input-to-output ratios. Other topologies have been suggested which require a greater number of components and complex control.

There are two common solutions to balance high conversion ratio with system complexity. Multiple stages may be cascaded [4]-[5], each with a much lower conversion ratio than the overall system ratio. In this case, several stages that are each rated for the total output power are required—for m stages, mP_{out} must be processed. Another option is to use an isolated converter, with a turns ratio in the transformer to increase the conversion ratio at a given duty cycle. The common push-pull topology requires switching devices rated for twice the input voltage, in some cases crossing boundaries into different device technologies.

A less typical third option is to configure converter input ports in series, then interconnect their outputs in parallel to build a SIPO converter. Relatively low conversion ratios and voltage ratings for each converter (referred to here as a phase) can support a high overall system conversion ratio and input voltage rating. A SIPO converter is composed of n isolated phases, each processing a fraction P_{out}/n of the power and operating at a fraction V_{in}/n of the input voltage. Device selection may be optimized; for example, n may be varied to enable the use of a particular MOSFET. A 36 V-to-0.7 V converter can be built using four phases and 30 V MOSFETs or six phases and 20 V MOSFETs, for example. There is no practical limit to the number of phases that can be used in the SIPO arrangement. The total power being handled remains the same regardless of n, so the same total magnetic volume and the same total semiconductor area would be required. The duty ratio can be adjusted by the turns ratio a of the transformers to always be near unity for maximum efficiency and minimum ripple. In contrast, single-stage non-isolated converters would each need to use an extremely small duty ratio, while multi-stage converters need to handle more total power.

The SIPO control technique presented below is based on

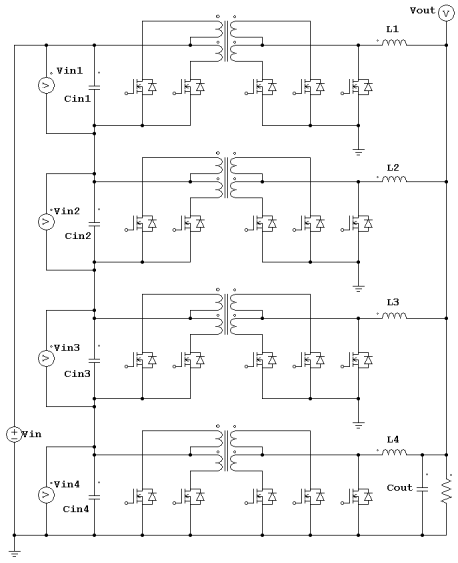

Fig. 1. Four-phase SIPO converter.

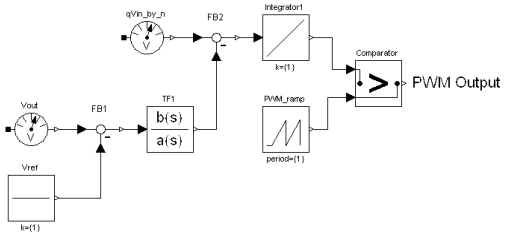

Fig. 2. Conceptual SCM closed-loop controller.

the sensorless current mode method [6], or SCM. SCM provides excellent source rejection with a simple controller and no current sensing. Perfect load regulation can be achieved with a modest outer feedback loop.

II. Sensorless Current Mode Technique

SCM can be considered as a modified flux estimator [6]. The voltage applied to a magnetic structure is integrated, yielding a quantity proportional to the flux in the core. There is an approximately linear relationship between current and flux in an inductor, so the volt-second result is proportional to current.

Two concepts are used to convert the estimator to a controller. First, desired reference voltage values are used in place of measured voltages. Next, the result of the integral is compared to a ramp to generate switching commands. SCM is used to control a buck converter in [6], where actual output voltage is replaced by a reference. Tracking is limited only by parasitic output impedances, and a closed-loop controller can be used to generate the SCM reference from the difference between desired and actual output voltage to make tracking ideal.

In the SIPO controller, the SCM control signal could be computed differently for each phase, taking into account the individual phase input voltages $\left(V_{in,i}\right)$ for phase *i*, as

$$\int \left(q_1(t) V_{in,i} - V_{ref}^* \right) dt. \tag{1}$$

However, a modest modification of SCM is useful with the series input structure. Not only is measured output voltage replaced by a reference, V_{ref}^*, but the input voltage is also replaced by the desired value, V_{in}/n. When this ratio is used in the control law in place of the actual phase input voltage, the controller in fact supports ideal matching of the *n* input voltages. The SCM control law for the SIPO circuit can be represented as a signal to be compared to a PWM ramp,

$$\int \left(q_1(t) \frac{V_{in}}{n} - V_{ref}^* \right) dt \tag{2}$$

where V_{ref}^* is generated from the desired output voltage reference, V_{ref}, and actual output voltage, V_{out}, to create a closed-loop system and $q_1(t)$ is a logic '1' when either primary side switch is on (see Fig. 1). The conceptual loop is shown in Fig. 2.

III. System Dynamics

Balanced dynamic load current and input voltage sharing are crucial for effective operation of the converter. Suppose there is a disturbance such that one of the phase output currents, I_{out1}, changes by some small amount while the output voltage remains constant. The duty ratio will not change under SCM because there is no current feedback in (2), so the corresponding input current, I_{in1}, will change by the same fraction as I_{out1}. The input phase voltage, V_{in1}, will begin changing as the integral of the difference between I_{in1} and nominal input current, I_{in}, as governed by the input capacitance C_{in1}. The change in V_{in1} will affect the output current, determined by the phase's output impedance, Z_{out1},

$$I_{out1} = \frac{DV_{in1}/a - V_{out}}{Z_{out1}} \tag{3}$$

Z_{out1} is generally small at the frequencies of interest, so a small change in V_{in1} will give a large change in I_{out1}. This results in a rapid dynamic current balancing that can be termed "super-matching." In most topologies, $Z_{out1} = sL_{out1} + R_{out1}$, representing the output inductance and all of the parasitic resistances. Combining (3) with the input capacitor action determines how I_{out1} evolves with respect to the nominal output current, I_{out},

$$I_{out1} = I_{out} \frac{1}{1 + sC_{in1}Z_{out1}} = I_{out} \frac{1}{1 + sC_{in1}R_{out1} + s^2 L_{out1}C_{in1}} \tag{4}$$

A second order system emerges with poles determined by input capacitance and output inductance, damped by the sum of all lossy elements in the converter. The transformer turns ratio cancels out, as does the duty cycle. The designer should minimize input capacitance while maintaining system stability and meeting ripple current ratings to obtain the best possible dynamic voltage and current sharing. Smaller capacitors yield a faster change in input voltage in response to a disturbance, pushing the corner of the second order output current response to higher frequencies. The matching occurs without feedback and is determined solely by the construction of the converter.

The above analysis holds so long as the output voltage remains constant through a transient, which is typically not the case. Instead, one might ask whether the sharing is stable while the input voltage remains constant and the rest of the circuit is operating. Assume the load is an ideal current sink having infinite incremental impedance, a worst-case scenario. The duty cycle for all *n* phases is the same, *D*, so the equivalent circuit is shown in Fig. 3. The transformers are identical and ideal, representing the averaged PWM process. Each phase can be collapsed into an equivalent impedance, $Z_{in,i}$, defined looking out of the secondary of the transformer.

Suppose phases 2 through n are identical, but phase 1 is not. Instead, the phase 1 inductance is $Z_{L1} = (1+\varepsilon) Z_L$. Also,

$$\sum_{i=1}^{n} dv_i = 0 \tag{5}$$

which follows from constant input voltage. That is, if one phase voltage increases, the rest need to decrease so that the total change is zero. With these definitions, circuit analysis is straightforward. The admittance of phase 1 is

$$Y_{in1} = \frac{di_1}{dv_1} = \frac{\partial i_1}{\partial v_1} + \sum_{i=2}^{n} \left(\frac{\partial i_1}{\partial v_i} \frac{dv_i}{dv_1} \right) \tag{6}$$

The admittance of the other phases can be defined in a similar fashion. The resulting impedance of phase 1 is:

$$Z_{in1} = \frac{Z_L^2 (1+\varepsilon) + Z_L Z_C (n + n\varepsilon - \varepsilon)}{Z_L + nZ_C} \tag{7}$$

The impedance of any other phase $i \neq 1$ is:

$$Z_{in,i} = \frac{Z_L^2 (1+\varepsilon) + Z_L Z_C (n + n\varepsilon - \varepsilon)}{Z_L (1+\varepsilon) + Z_C (n + n\varepsilon - \varepsilon)} \tag{8}$$

In the absence of the sharing capacitors, the various phase voltages will share according to the ratios of their impedances, found by dividing (7) by (8) to yield

$$\frac{Z_{in1}}{Z_{in,i}} = \frac{v_1}{v_i} = \frac{Z_L (1+\varepsilon) + Z_C (n + n\varepsilon - \varepsilon)}{Z_L + nZ_C} \tag{9}$$

At dc, the impedance of the sharing capacitors is infinite, so dc sharing is determined entirely by (9). Also at dc, the impedance of the output capacitor is infinite. The dc limit of (9) gives

$$\lim_{s \to 0} \frac{v_1}{v_i} = 1 + \frac{n-1}{n} \varepsilon \tag{10}$$

Since the transformer equivalents are all identical, sharing on the secondary implies sharing on the primary. So a phase whose inductor impedance is ε away from the nominal will have a voltage that is less than ε away from the nominal. Typically n is small (for example, $n = 4$ in Fig. 1), so the unbalanced phase voltage will be more balanced than its inductor impedance might indicate.

To complete the analysis, the sharing capacitor impedance must be included. In the high frequency limit, the input impedance of a phase is infinite due to its overall inductive nature. So, defining

$$Z_i = Z_{Cin,i} \,||\, \left(\frac{a}{D} \right)^2 Z_{in,i} \tag{11}$$

as the total impedance of a phase from the input side, one may take the limit of Z_i to examine high frequency sharing:

$$\lim_{s \to \infty} Z_i = R_{Cin,i} \tag{12}$$

To summarize, at dc, sharing is dictated entirely by the series resistance of the inductors (and all the other parasitic resistances in the main current path), while at high frequency, sharing is dictated entirely by the series resistance of the sharing capacitors. For phases that are identical by design, sharing within a few percent is achievable. This is the worst-case condition for a true current source load. In reality, load resistance would improve the sharing. In any case, the sharing is stable, since the relevant impedances have positive real part.

V. Single-Phase Small Signal Model

The complete small signal model of the SIPO system can be derived using the techniques presented in [7]. The small-signal model soon becomes algebraically cumbersome as the number of phases increases, with a high number of poles and zeros. If the phases are nearly symmetric, some poles and zeros cancel, but many more poles and zeros in close proximity remain.

An alternative approach was used to develop a controller:

1. Assume that the voltage sharing on the input is perfect at all frequencies. This will be explored in more detail below.
2. Assume that current sharing on the output is perfect. This follows from voltage sharing and power balance.
3. Collapse the n phases into a single phase switching at $f_{eq} = nf_{sw}$ with an equivalent output inductance of $L_{eq} = L/n$.
4. Refer all voltages and currents to the secondary side of the transformers.

The result is a lower order equivalent SCM controlled buck converter model that can be analyzed to give

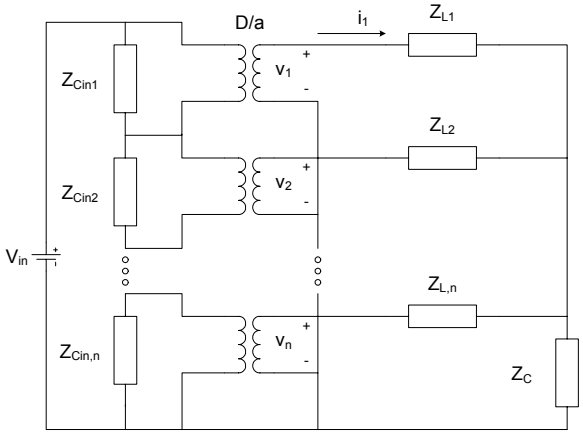

Fig. 3. Averaged model of n-phase SIPO converter.

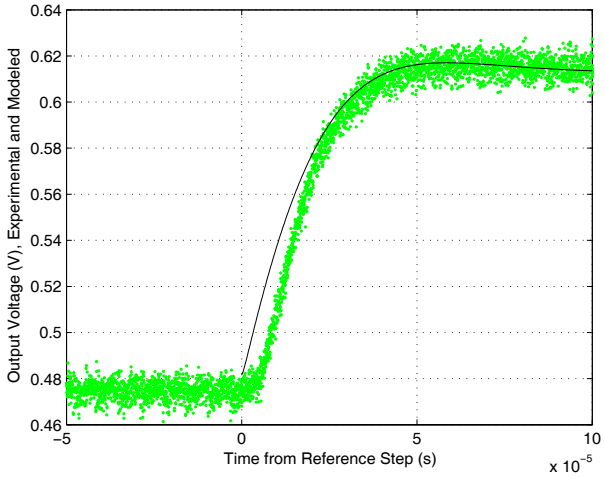

Fig. 4. Output voltage response to a reference step without feedback: experimental and simulated reduced order model response.

$$\frac{v_{out}}{v_{ref}} = \frac{R_{load}\left(1+C_{out}R_{Cout}s\right)\left(2+\left(-1+2D\right)sT\right)V_{in}}{2\left(\alpha_0+\alpha_1 s+\alpha_2 s^2\right)\left(naT_{eq}M_a s+V_{in}\right)} \quad (13)$$

where the coefficients in the denominator are $\alpha_0 = R + R_{Leq}$, $\alpha_1 = \left(L_{eq} + C_{out}R_{Cout}R_{load} + C_{out}\left(R+R_{Cout}\right)R_{Leq}\right)$, and $\alpha_2 = C_{out}L_{eq}\left(R_{load}+R_{Cout}\right)$. The equivalent single-phase inductance parameters are approximated by $R_{Leq} = R_L/n$ and $L_{eq} = L/n$, where L and R_L are the typical inductance parameters in any given phase.

Numerical values of the model parameters are tuned to match experimental results. Fig. 4 shows an experimental reference step command compared to the small signal simulated response. The actual multi-phase converter has more delay, but rise time and overshoot match well. This open-loop model captures enough detail to be used for feedback control design.

VI. Experimental Results

Previously [8], a two-phase 12 V-to-1 V converter was constructed. In the present work, a four-phase 36 V-to-0.7 V converter was built based on the same principles. In the SIPO arrangement, the nominal input voltage per phase is 9 V, so 30 V MOSFETs were used. The reduced-order model (13) whose step response is shown in Fig. 4, is given by

$$\frac{26042\left(s+2.56\times10^6\right)\left(s+8.11\times10^4\right)}{\left(s+1.4\times10^6\right)\left(s^2+1.015\times10^5 s+4.055\times10^9\right)} \quad (14)$$

with model circuit parameters shown in Table 1. A proportional-integral feedback controller was designed with $K_p = 100$ and $K_I = 10^5$. The design phase margin is 75.1° with loop gain crossing 0 dB at 490 kHz, just below the effective switching frequency. Higher gain leads to instability as the underlying small-signal assumptions are violated. Load steps were applied to the closed-loop system. Fig. 5 shows output current and voltage through a 6.8 A/μs transient. The output voltage is nominally 610 mV, with peak overshoot and undershoot of 44 mV, or 7.2%.

Table 1: Single-Phase Equivalent Parameters.

Inductance, L_{eq}	100 nH
Output Capacitance, C_{out}	2.5 mF
Inductor Series Resistance, R_{Leq}	5 mΩ
Capacitor Series Resistance, R_{Cout}	5 mΩ

Section IV showed that the input voltage is balanced dynamically among the phases. Fig. 6 shows experimental results demonstrating near-perfect dc sharing as input voltage is increased. Around 24 V input, the converter begins regulating (duty cycle is at maximum for lower input voltage). Throughout a 2:1 input voltage range, sharing is within 0.66%.

Dynamic current and voltage sharing is shown in Fig. 7 and Fig. 8, respectively, through a load step. Phase current waveforms are nearly identical throughout the step load transient. The digitizing oscilloscope current traces are filtered by averaging to extract the running average from the ripple. Phase voltage waveforms remain constant, near 9 V each, showing dynamic balanced sharing through load transients. Fig. 8 confirms the expected dynamic input voltage balance for both step up and step down load transients.

V. Conclusions

A sensorless current mode control method for a series input-parallel output multiphase converter has been analysed

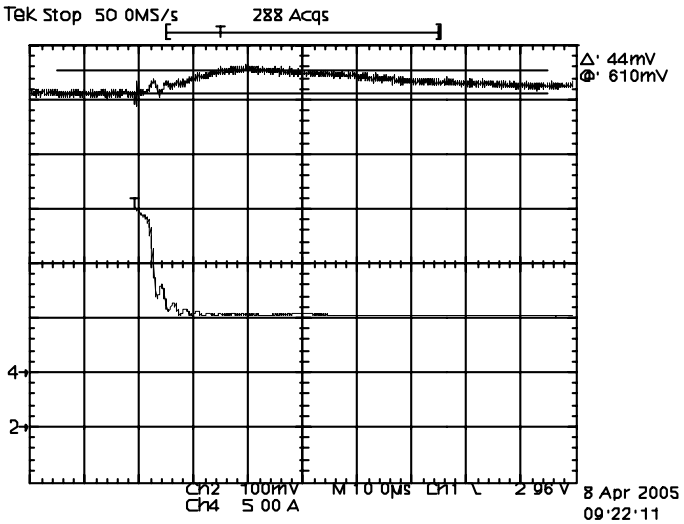

Fig. 5. Output voltage (Channel 2, upper trace) and output current (Channel 4, lower trace) through a 10A step load decrease.

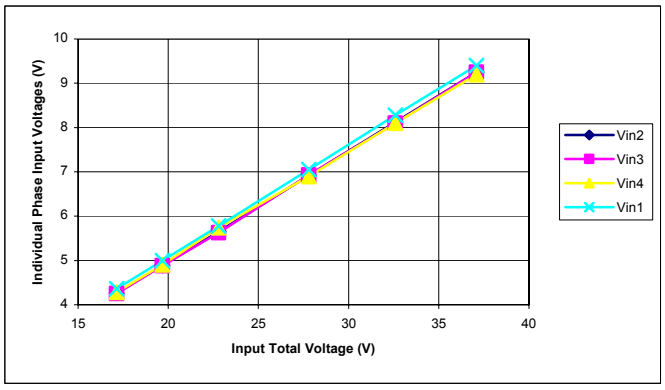

Fig. 6. Dc input voltage sharing.

and demonstrated. Voltage sharing is determined solely by converter construction. Voltage sharing from dc to many kHz has been demonstrated with an experimental four-phase 36 V-to-0.7 V converter. Dynamic phase current sharing has been demonstrated through rising and falling load step transients. While a full-order model is nearly intractable, sufficient symmetry exists to use a reduced order model for controller design purposes. A 6.8 A/µs load step applied to the closed-loop system results in near-perfect matching even through the transient.

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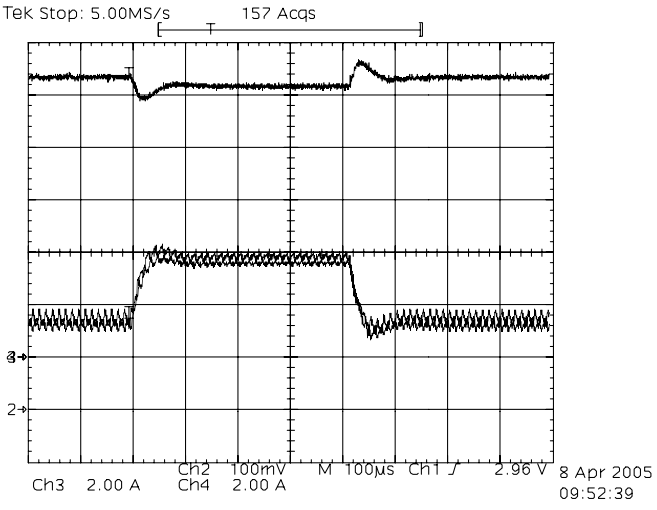

Fig. 7. Output voltage (Channel 2, upper trace) and two phase currents (Channels 3 and 4, lower traces) through a 10A load step, with averaging.

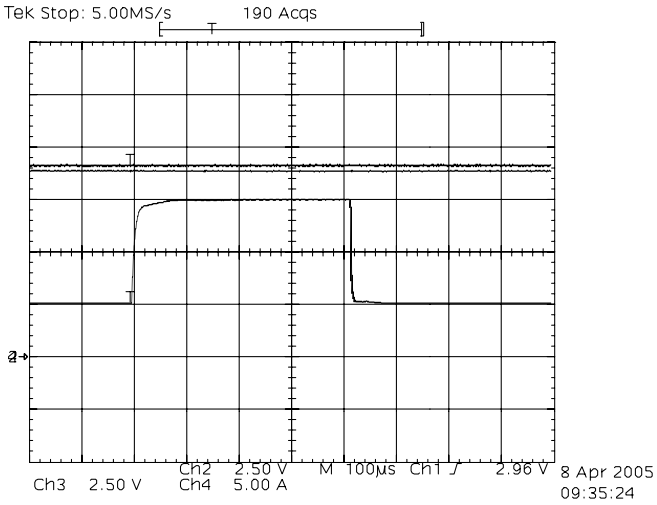

Fig. 8. Input voltage phase voltages (Channels 2 and 3, upper traces) sharing through a10 A load step(Channel 4, lower trace).