01 Jul 2010

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Recommended Citation

T. Feng et al., "Reliability Modeling and Analysis of Clockless Wave Pipeline Core for Embedded Combinational Logic Design," *IEEE Transactions on Instrumentation and Measurement*, vol. 59, no. 7, pp. 1812-1824, Institute of Electrical and Electronics Engineers (IEEE), Jul 2010.
The definitive version is available at https://doi.org/10.1109/TIM.2009.2030917

Reliability Modeling and Analysis of Clockless Wave Pipeline Core for Embedded Combinational Logic Design

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***Abstract*—This paper presents a model for analyzing the reliability of a clockless wave pipeline as an intellectual property (IP) core for embedded design. This design requires different clocking requirements by each embedded IP core during integration. Therefore, either partial or global lack of synchronization of the embedded clocking is considered for the data flow. The clockless wave pipeline represents an alternative to a traditional pipeline scheme; it requires an innovative computing model that is readily suitable for high-throughput computing by heterogeneous IP logic cores embedded in system-on-chip (SoC). A clockless wave pipeline technique relies on local asynchronous operation for seamless integration of a combinational core into an SoC. The basic computational components of a clockless wave pipeline are the datawaves, together with the request signals and switches. The coordination of the processing of the datawaves throughout the pipeline by the request signals is accomplished with no intermediate access in the clock control. Furthermore, the reliability of clockless-wave-pipeline-based cores is of importance when designing a reliable SOC. In this paper, the *reliability* in the clockless operations of the wave pipeline is analyzed by considering the datawaves and the request signals. The effect of the so-called out-of-orchestration between the datawaves and the request signals (which is referred to as a *datawave fault*) is proposed in the reliability analysis. A clockless-induced datawave fault model is proposed for clockless fault-tolerant design.**

***Index Terms*—Asynchronous circuit, embedded intellectual property (IP) core, fault tolerance, reliability, system-on-chip (SoC), wave pipeline.**

I. Introduction

ONE of the major hurdles encountered in the design of a system-on-chip (SoC) arises from the different clocking requirements of the embedded intellectual property (IP) cores at integration. Either partial or global asynchronous operation of the cores is considered as a possible solution to resolve issues related to the so-called orchestration of data flow with respect to clocking. A clockless wave pipeline utilizes local asynchronous operation to accomplish seamless integration into an SoC by a heterogeneous number of IP cores. Each core is usually procured from different IP providers with different clocking requirements.

There has been extensive research on the asynchronous integration of embedded IP cores [1]. Most of these works have focused on the interconnection bus structures and the protocols for intercore on-chip communication. This is required to orchestrate partly asynchronous cores with other embedded synchronous cores to meet timing constraints. However, reliability is also of importance for asynchronous control of SoC. This must be addressed at the intracore level to ensure proper operation.

A clockless wave pipeline is an alternative to a traditional pipeline and a promising computing model for attaining ultrahigh throughput and speed. The basic computational components of a clockless wave pipeline are the data waves (together with the request signals and switches). In a clockless wave, coordination of the processing of datawaves throughout the pipeline is performed without relying on any intermediate access points under clocked control. Due to the complexity in clockless operations, an efficient method for modeling and analyzing the confidence level (referred to as *reliability* or *yield*) of the clockless operation in a wave pipeline is required, but it has not yet been adequately addressed. The confidence level is primarily determined by the reliability of the clockless orchestration of datawaves and the request signals under various switching arrangements for alignment. Out-of-orchestration between datawaves and request signals, which is referred to as a delay fault, is a major concern for the reliability of the pipeline. New faults, which are referred to as *intrawave fault*, *interwave fault*, and *request signal faults*, are proposed in this paper and extensively characterized. The proposed faults reveal novel characteristics of the clockless wave pipeline; intra/interwave faults are used as primary drivers for evaluating the impact of a fault with respect to delay-sensitive features, such as delay distribution, delay variation, crosstalk noise, and intra/interwave of datawaves. By establishing its reliable operation, the proposed method has great *potential* to *significantly impact* the realization of computer-aided design tools for clockless circuit design.

The specific objectives of this paper are given as follows: 1) to characterize a fault model for clockless wave pipeline operation; 2) to demonstrate a theoretical yet detailed *characterization* of these faults (such as intrawave fault, interwave

Manuscript received November 26, 2008; revised April 30, 2009; accepted May 1, 2009. Date of publication October 23, 2009; date of current version June 9, 2010. This work was supported in part by NSF-0340949.

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Digital Object Identifier 10.1109/TIM.2009.2030917

fault, and request signal fault); 3) to conduct a parametric evaluation of those parameters identified in the proposed fault model; and 4) to propose fault-tolerant design methods for the request signal and datawave faults.

This paper is organized as follows: Section II introduces the background of clockless architectures and, in particular, wave pipelines. The proposed fault model and evaluation are described in Section III. In Section IV, reliable techniques are described to handle such request signals and datawave faults. Conclusion and discussion are addressed in the last section.

II. Clockless Wave Pipeline

Wave pipeline is a pipeline processing technique that can increase the throughput without increasing internal storage space and power consumption [2], [20]. Multiple datawaves can simultaneously propagate through the wave pipeline from the primary input (PI) to the primary output (PO) without internal latching. It can ideally achieve the theoretical maximum performance and draws much attention in the industry today.

A wave pipeline can be built in either a synchronous or an asynchronous manner. A synchronous wave pipeline uses a clock signal to synchronize the movement of datawave bits. It has successfully been deployed in several commercial processors, such as the floating-point unit of IBM 360/91 [3] and the external caches in the HP PA8000 [4]. An asynchronous wave pipeline uses request and acknowledgement signals (or only a request signal), instead of a global clock, to serve as a reference signal. (Note that the asynchronous wave pipeline with the request signal only is referred to as *clockless wave pipeline* in this paper.) An asynchronous wave pipeline is relatively more difficult to deploy than a synchronous wave pipeline due to its explorations and a few technological hurdles, as mentioned before. Clockless wave pipeline circuits have only been experimented in noncommercial sectors such as the two-phase clockless wave pipeline, which uses only a single request signal line [5], [6]. The specific architectural model investigated in this paper is the two-phase clockless wave pipeline [6] since it is ideally supposed to yield [23], [24] the theoretical maximum performance.

In a conventional pipeline, there are registers or latches between any two stages, and there is only one datawave active in any stage at any time. The clock cycle time is determined by the maximum stage path delay, i.e., $T_{\rm ck} \geq D_{\max}$. Wave pipelines remove all of the internal registers or latches, and let multiple datawaves simultaneously propagate through the circuit. This way, the throughput is greatly enhanced. The clock cycle time of a wave pipeline with clock is determined not by the maximum path delay but by the difference between the maximum and the minimum path delay, and its clock cycle [21] is $(T_{\max}/N) < T_{\rm ck} < (T_{\min}/(N-1))$, where N is the number of waves in the circuit (degree of the wave pipeline).

A clockless wave pipeline is an asynchronous circuit. A *two-phase asynchronous wave pipeline* was proposed by Hauck *et al.* [6], which has the two-phase operation by alternating positive and negative switches, and it employs a request signal as the signal control component.

As shown in [6], two types of switches, i.e., positive and negative switches, logically and physically partition the circuit into several pipeline stages for datawave progress alignment purposes, and a request signal controls the switches. A pair of a datawave and a request signal level (either a high or a low pulse of the request signal) enters the clockless wave pipeline at the same time in full association, and they must stay so throughout the propagation of the datawave.

The switch can be *opaque* or *transparent* to the datawaves. If opaque, the switch latches the datawave, and if transparent, the datawave passes the switch without latching. Specifically, n-type switches (negative switches) are made to be opaque to the datawaves associated with a low request signal and transparent to those associated with a high request signal. Symmetrically, p-type switches (positive switches) are made to be transparent to the datawave associated with a low request signal and opaque to those associated with a high request signal. The propagation of the datawave within a pipelined circuit is intermittent. Once the datawave enters the circuit, it is assigned a request signal, at either high or low level. Then, by the design rule, as defined, the datawave associated with a high request signal propagates through n-switches without stopping for alignment but has to be latched at p-switches. Symmetrically, the datawave associated with a low request signal propagates through the p-switch without stopping but has to stop and be latched at the n-switches.

Ideally, there are multiple datawaves simultaneously populated and propagating through the combinational circuit, and traditional delay-fault testing, modeling, and assurance techniques are not readily able to handle and evaluate the faults of successive transitions at the datawave level in the circuit. Therefore, assurance and optimization of delay-oriented yield and reliability is exigently demanded and a key to the success of the clockless wave pipeline technique. Ideally, all path delays from the PI to the PO are to be equally or near-equally balanced. However, equal balancing of path delays is hard to realize, even with the help of extensive tuning [22], for various fabrication and runtime variations (such as power consumption, thermal distribution, and design errors, to mention a few) to account for delay variations. Furthermore, clock skews due to variations in the rise/fall time and the setup and hold times of the storage elements will limit the clock frequency to within an increase only by a factor of 2 to 3, even with the use of the best-known design tuning method [7].

Two most representative delay-fault models for *synchronous wave pipeline* are given here.

1) Wave delay fault [8]: The timing constraint in the synchronous wave pipeline is two-sided, such that each datawave must obey the *setup* and *hold* time constraints at each end of its current clock cycle for correct synchronization. Violation of the two-sided clock-timing constraint, such as setup or hold time error, is referred to as a wave delay fault.
2) Wave fault [8]: In order for successive datawaves to propagate and stay in correct operation back to back, it is required that each datawave must stay within the time range of the clock cycle period associated with it. Thus, a

wave delay fault may create further wave faults. A wave fault is very likely to cause signal invalidation, such as spikes or absent signals.

These fault models provide an important basis and guidance to theoretical characterization and parameterizations of delay faults for the *clockless* wave pipeline in this paper, as well as that of wave pipelines in general. There have been a few works proposed on synchronous wave pipeline design for reliability [8], [9], in which testing, characterization, and parameterizations of datapath-oriented delay faults were proposed. *However*, there are no adequate and extensive characterization and parameterizations of the faults and yield for synchronous wave pipelines or clockless wave pipelines. This is a *great hurdle* for reliable wave pipelines to be realized. Therefore, it is *imperative* to develop formal methods for adequate and extensive modeling of delay faults precisely from the datawaves' standpoint and at an integrated datawave level to be able to assure and optimize the yield in the early design stage. Without such theoretical reliability assurance and optimization methods, which are precisely on the integrated system level with focus on the datawaves, there is no efficient and effective way of designing a reliable wave pipeline with fault tolerance.

III. Fault Models and Yield Modeling/Assurance

To efficiently and effectively depart from the delay fault models of conventional synchronous wave pipelines, we propose two new fault models. The proposed *intrawave fault model* is based on the *pulse fault model*, as proposed in our previous work [10]. Based on the intrawave fault model, we further propose the *interwave fault model* to provide a comprehensive yet essential understanding of the fault mechanism of a clockless wave pipeline. The proposed fault models are used as the theoretical basis for the proposed yield modeling, assurance, and optimization method. In addition, we take into account a synergistic fault model, in which, specifically, delay faults on request signal lines are modeled, together with the datawave delay faults, because correct association between datawaves and their request signals primarily determines the delay-oriented yield and reliability.

A. Intrawave Fault and Yield

The path delay of a circuit with fabrication variations can be modeled using an interval, instead of a single value. Thus, we may model the path delay of a partial path as x. Suppose that there are n such partial paths (i.e., $x_1, \ldots, x_n$), and assume that those partial paths are assumed to be well balanced in the clockless wave pipeline under investigation. In addition, without loss of generality, we may assume that the path delay for x_i follows a *normal distribution* with a mean μ and a standard deviation σ as follows: $x \sim N(\mu\sigma^2)$, relying on each path being composed of at least several logic elements contributing delay [11], [12]. Let $\bar{x}$ be the sample mean and s be the sample standard deviation. Then, μ and σ can be substituted by $\bar{x}$ and s, respectively, because $\bar{x}$ and s are unbiased estimators of μ and $\sigma x \sim N(\bar{x}s^2)$. Suppose that $f(x)$ is the probability density function (pdf) of x as follows: $f(x) = (1/\sqrt{2\pi}s)e^{-((x-\bar{x})^2/2s^2)}$. By definition, the intrawave fault is the probability that some bits in the data wave proceed too fast and then overstep their associated request level (i.e., the probability of a setup time fault) or some bits in the datawave are so slow that they lag behind the associated request level (i.e., a hold time fault), leaving some bits out of the range of the supposed-to-be-associated request level interval.

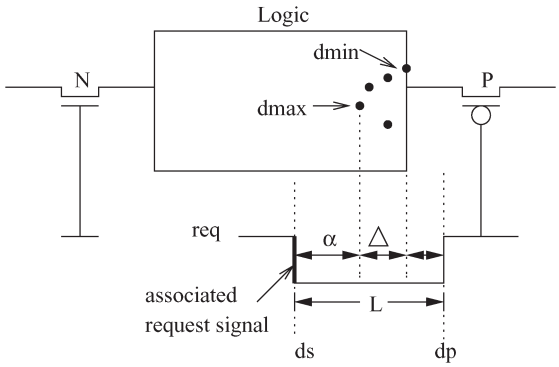

Fig. 1. Relative position between the request signal and data wave.

The request signal and all the data bits enter the circuit at the same time, and for proper operation, the request signal should be slower than the slowest bit of the data wave and reach the switch after the slowest bit. Likewise, the previous request signal should reach the switch before the fastest bit of the associated data wave. The data skew (represented by $\triangle$ in Fig. 1) is supposed to be properly covered by the associated request level. Therefore, the coverage of $\triangle$ by the request level, i.e., the relative position between the datawave and its associated low or high request level, may influence the intrawave fault rate to a great extent.

α refers to the difference in propagation time between the slowest bit of the datawave and the request level, as shown in Fig. 1. Thus, the associated request signal propagation delay (which is denoted as d_s) can be expressed as $d_s = d_{\max} + \alpha$. The propagation delay of the request signal pulse through the switch (which is denoted as d_p) is $d_p = d_{\min} - (L - \alpha - \triangle)$. Thus, $L = d_s - d_p$.

Placing n switches in the circuit, each of which has P_i (i.e., the intrawave fault rate at each switch), where $1 \le i \le n$, the *total intrawave fault rate* P_{total} is given as follows:

$$P_{\text{total}} = 1 - \prod_{i=1}^{n}(1 - P_i) = 1 - \prod_{i=1}^{n}\left(1 - \int_{d_{\min_i} - (L - \alpha_i - \triangle_i)}^{d_{\max_i} + \alpha_i} \frac{1}{\sqrt{2\pi}s} e^{\left(-\frac{(x-\bar{x})^2}{2s^2}\right)} dx\right). \quad (1)$$

Therefore, the overall *yield* $Y = 1 - P_{\text{total}}$. In addition, note that, using the proposed yield model, at each switch i, we see that theoretical optimum is achieved by setting α_i to $(1/2)(L - \Delta_i)$.

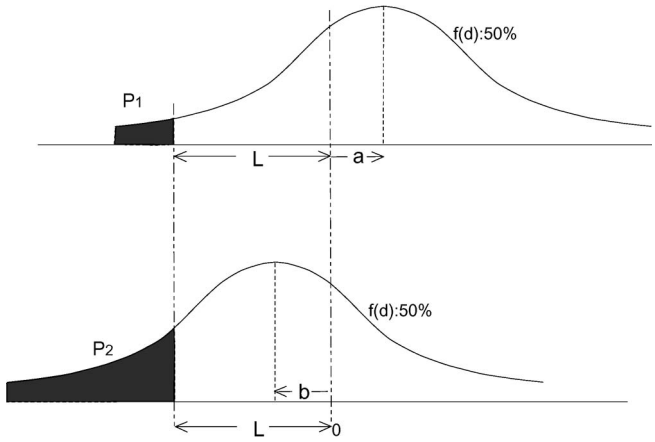

Fig. 2. Probability for two bits on the same datapath to cause an interwave fault.

B. Interwave Fault and Yield

To extensively assure and optimize the reliability of the clockless wave pipeline, delay faults between datawaves must be characterized and parameterized beyond the scope of the intrawave fault. A preliminary result was reported in [13]. The proposed interwave fault model reveals the effect of the proposed intrawave fault in association with other primary delay-oriented factors, such as the request signal and inter-datawave relation.

Delay faults can either vertically or horizontally be viewed and modeled at the moment when the bits of a datawave reach the opaque switches. Vertically, datawave-delay faults can occur within the scope of a datawave if its associated request signal goes out of association; this has the effect of an intrawave fault. Horizontally along each data path, if path-delay faults occur, then the data bits of two adjacent datawaves may collide and get invalidated across the scopes of the datawaves; this type of fault is referred to as *interwave fault*. The interwave fault observes the bits of datawaves at each switch and thus facilitates the controllability and observability of datawave testing.

Fig. 2 shows the pdfs for interwave fault. Notice that the pdf on top represents the probability distribution of having the two bits A and B getting farther from each other due to an arbitrary delay variation, as indicated by the shift of the average point in the positive direction from the original point at 0 by a, whereas the pdf on the bottom represents the probability distribution of having the two bits A and B coming closer to each other due to another arbitrary delay variation, as indicated by the shift of the average point in the negative direction from the original point at 0 by b. L indicates the maximum difference, or the maximum value d, between bits A and B, in either the positive or negative direction. In addition, note that each pdf accounts for 50% of the entire probability, because, without loss of generality, we can assume that the probabilities for the two bits to get farther or closer are equal, unless otherwise specified. The dark area in the pdf on top (i.e., P_1) represents the probability that bit B is going beyond the left edge of its request level in the negative direction and thus will intersect and overlap with bit A, and *vice versa* (i.e., P_2) in the pdf on the bottom. Thus, it shows that the farther the two bits get away, the smaller the probability for interwave fault, and *vice versa*. Therefore, summation of the dark areas of each pdf represents the total probability for the interwave fault, i.e., $\Pr(Interwave\ fault/switch)$ at each switch. Thus, P_1 and P_2 are given as follows: $P_1 = \int_{-\infty}^{-L-a}(1/\sqrt{2\pi}S_{d_1}) \times e^{-((d_1-\bar{d_1})^2/2S_{d_1}^2)}dd_1$, and $P_2 = \int_{-\infty}^{-L+b}(1/\sqrt{2\pi}S_{d_2}) \times e^{-((d_2-\bar{d_2})^2/2S_{d_2}^2)}dd_2$.

Therefore, the total probability $\Pr(Interwave\ fault/switch) = P_1 + P_2$. Suppose that there are n such paths in a partial circuit; then, the total probability for the interwave fault in each partial circuit [i.e., $\Pr(Interwave\ fault/partial\ circuit)$] can be expressed as follows: $\Pr(Interwave\ fault/partial\ circuit) = \prod_{i=1}^{n} P_i$, because the delays on each datapath are independent. Furthermore, suppose that there are m such partial circuits, and let $\Pr(Interwave\ fault/partial\ circuit)$ be P_j; then, the total probability for the interwave fault in the whole clockless wave pipeline can be expressed as $\Pr(Interwave\ fault/pipeline) = 1 - \prod_{j=1}^{m}(1 - P_j)$. Therefore, the resulting yield $Y = 1 - \Pr(Interwave\ fault/pipeline)$.

C. Request Signal Fault and Yield

Correct operation of a clockless wave pipeline is mainly determined not only solely by intra/interwave fault but also by the request signal faults. Datawaves are guided by the request signal and aligned at and by the p- and n-switches; hence, the request signal determines the correct propagation of datawaves. Therefore, the request signal is the primary signal in control of the clockless wave pipeline processing. Any incorrect control over datawaves by the request signal may cause a fatal error leading to data corruption. Hence, ensuring a fault-free request signal is a key to the successful realization of a reliable clockless wave pipeline.

The *request signal fault* of our interest is a *glitch* hit on the request signal due to crosstalk or power pulse noises [19]. In [6], it was reported that glitches can hit on the request signal created by a request signal generator. A glitch on a request signal breaks the datawave in association with it (either transient, permanently, or intermittently); the faulty request signal may instantaneously break the datawave at the instant the glitch hits and let the head portion of the broken datawave propagate through the next switch where the broken datawave will be released earlier than the normal switch-blocking period of time. This broken datawave will consequently proceed toward the datawave ahead of that and result in an interwave fault. Likewise, the tail portion of the broken datawave may suffer from any glitch hit on the request signal associated with the following datawave, also resulting in another interwave fault. The yield with consideration of the interwave fault caused by request signal faults can be evaluated by extending the proposed interwave fault model in the previous section. In this context and based on the proposed fault models and yield modeling/assurance methods, a solid method for ensuring a fault-free request signal is proposed in the next section.

TABLE I
FAULT INSTANCES CAUSED BY REQ. SIG. FAULT

	N-switch	P-switch
Glitch on High Req. Sig.	Faulty	Fault-Free
Glitch on Low Req. Sig.	Fault-Free	Faulty

TABLE II
PROPOSED FAULT MASKING

A (Normal)	B (Glitch)	A OR B (N Switch)	A AND B (P Switch)
High	Low	High	X
Low	High	X	Low

IV. PROPOSED DESIGN FOR RELIABILITY

We propose two design-for-reliability methods: one targeting *request signal faults*, because the request signal is the most critical element for correct control over the datawaves and overall computation, and one targeting *datawave faults*, because intra/interwave faults may still hit on the datawaves due to delay variations that are independent of request signal faults. The efficiency and effectiveness will be demonstrated by the proposed novel reliability and yield modeling and assurance techniques.

A. Fault-Tolerant Design for Request Signal Faults

Based on our preliminary work on a fault-tolerant method for request signal faults, as reported in [14], we propose a method for ensuring fault-free request signals. In practice, a request signal is highly sensitive and vulnerable to electronic crosstalk or power pulse noise (which is referred to as *glitch*). As the technology allows ultra-smaller device geometries, millions of closely spaced interconnections, and higher switching speeds, electronic crosstalk noise is very likely to occur, and it appears to be a major problem in the development of next-generation high-speed integrated circuits [16], [17]. In general, the request signals are caused by various electrical and environmental factors, such as voltage, temperature, and humidity. Crosstalk noises on request signals could be permanent, transient, or intermittent. Any type of glitch on the request signal is deleterious and may result in fatal datawave corruption.

In Table I, we give a comprehensive characterization of four possible types of faulty behavior due to the interaction between switches and request signal faults.

The proposed method for ensuring a fault-free request signal is *fault masking*. The fault-masking method is to employ redundant request signal lines and an AND and an OR gate at each p- and n-switch, respectively. An AND gate at a p-switch will control the incoming datawave such that any low-glitch hit on the request signal is masked to the normal (i.e., high) value, unless every request signal is hit by a low glitch exactly at the same time (as shown in the upper row in Table II), and *vice versa* in the case of an OR gate at an n-switch (as shown in the lower row in Table II). Note that the probability for an original request signal and all redundant request signals to be hit by the glitches exactly at the same time is practically negligible. Hence, the proposed simple yet powerful fault-tolerant request signal method using the fault-masking technique is efficient and effective.

We propose a reliability model to thoroughly verify the effectiveness of the proposed fault-masking method. The model employs the *mean time to glitch* (MTTG) to take into account and demonstrate the effect of the fault masking on request signals at different levels of redundancy. Assume that λ is the rate at which a glitch hits on a request signal line during the period of time from the instant of time when the signal was submitted into the PI of the circuit to the instant of time when the signal arrives at the PO of the circuit. In addition, assume that the primary request signal line and redundant request signal line(s) have the same glitch rate without loss of generality. Having the redundant request signal line(s) employed, the glitch can be masked off, except when the glitches hit on all the request signals, respectively, at the same time.

Thus, the overall fault rate of the primary and redundant request signal(s) is $\lambda_{\text{effective}} = (\lambda \times (l/L))$, where l is the mean time width of a glitch's effect and L is the length of the request signal, and the relative width l/L of a glitch hit on the request signal pulse L is practically considered. Therefore, the effective reliability of N request signals, inclusive of the primary and redundant request signal(s), is $R(t) = e^{-(\lambda\times(l/L))^N \times t}$. MTTG is the mean time for a high or low signal to propagate normally through the circuit before the first glitch hits. Hence, the MTTG can be modeled as follows:

$$\text{MTTG} = \int_0^{kL} e^{-\lambda t} dt = -\frac{1}{\lambda} e^{-\lambda kL} - \left(-\frac{1}{\lambda} e^{-\lambda(0)}\right) = \frac{1}{\lambda}(1 - e^{-kL\lambda}) \tag{2}$$

where k is the *depth of the wave pipeline*, i.e., the number of request signal cycles needed for a data signal to propagate through a partial circuit before being aligned at a switch; thus, kL is the total length of a request signal path within the partial circuit. Note that, according to (2), the glitch rate can significantly impact MTTG, and L can be derived as $L = \ln(\lambda \times \text{MTTG} - 1)/k\lambda$. The expression for L can be used as a theoretical bridge between MTTG-induced request signal faults and intra/interwave faults, and is used as a primary driver to optimize the intra/interwave fault rate with respect to a request signal fault.

Having MTTG theoretically identified, the reliability of a single request signal at MTTG [18] can be expressed as follows:

$$R(\text{MTTG})_{\text{single}} = R\left(\frac{1}{\lambda}(1 - e^{-kL\lambda})\right) = e^{-\lambda\left(\frac{1}{\lambda}(1-e^{-kL\lambda})\right)} = e^{(e^{-\lambda kL}-1)}. \tag{3}$$

Therefore, the overall reliability with respect to N request signal lines is $R_{\text{overall}} = \sum_{i=1}^{N-1} \times N \times R^{N-i} \times (1-R)^i \times (1-P)$, where $P = \lambda^N$ to account for the instance when all the request signals are hit by a glitch at the same time. Hence

$$R(\text{MTTG})_{\text{overall}} = \sum_{i=1}^{N-1} \times N \times \left(e^{(e^{-\lambda kL}-1)}\right)^{N-i} \times \left(1 - \left(e^{(e^{-\lambda kL}-1)}\right)\right)^i \times (1 - \lambda^N). \tag{4}$$

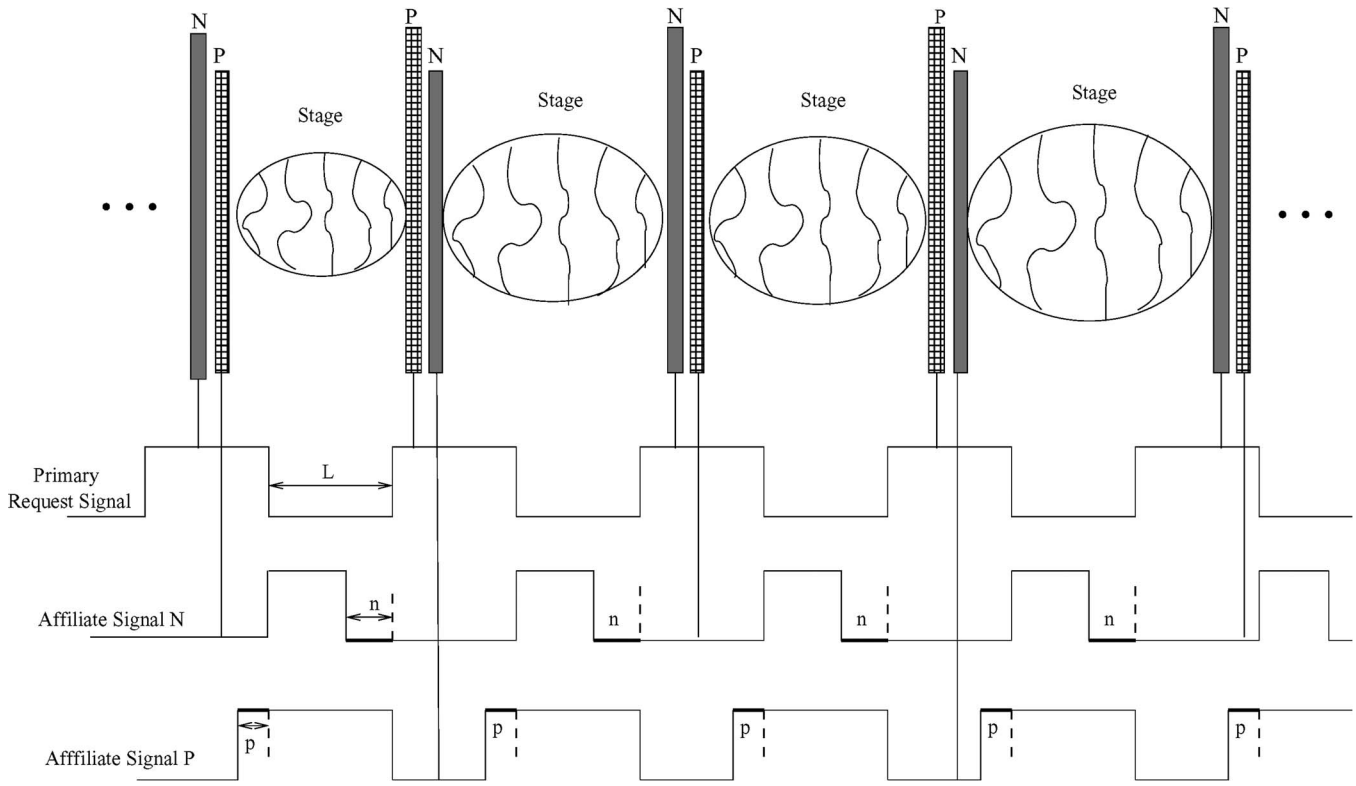

Fig. 3. Architecture of the reliability enhanced two-phase clockless wave pipeline.

The design-for-reliability modification curtails the impact of low (high) glitches at p-switches (n-switches) through the use of the OR and AND gates. However, the opposite form of glitch is made worse in that there are now multiple sources (multiple request signal lines) that can initiate the glitch. The glitch in the opposing direction is somewhat less of a concern, unless it occurs near a planned edge to the request signal.

Several methods can be used to counter this problem. One method involves the insertion of a buffer in advance of the control input to each switch; the buffer must be designed to be insensitive to brief glitches. A similar effect can be had by ensuring that the gate capacitance of the switch is quite high. A second method involves a cascade of AND and OR gates at each switch (e.g., effectively creating a majority gate). A third method involves a more direct implementation of the majority gate using ratio logic. The first and third methods can be combined.

B. Fault-Tolerant Design for Datawave Faults

Having ensured that the request signal is near fault-free, the proposed method must still deal with a request signal fault in which all request signal lines are hit by a glitch exactly at the same time; we have presented a preliminary result of a fault-tolerant design technique for datawave faults in [15], and in this paper, we further present the design-for-reliability technique in full detail and the reliability analysis relevant to it to facilitate the reliability optimization process. The proposed technique will reduce or possibly completely tolerate the modeled intra- and interwave faults. As an intrawave fault is a necessary but insufficient condition for an interwave fault to occur, we focus our modeling and fault tolerance on the improvement of intrawave-fault-related yield. Interwave-fault-related yield improvement can also be realized by relating the interwave fault model to the intrawave fault model.

The main concern of the proposed method is to control the shape of the datawaves to maintain their width (i.e., $d_{\max} - d_{\min}$) within L (i.e., the length of the request signal pulse in association). The proposed basic framework for reliability optimization employs a novel idea of *bipolar switches* in association with *affiliate request signals*.

The proposed bipolar switch, as shown in Fig. 3, consists of two switches connected in series where the switches have opposite polarity. There are two types of bipolar switches, i.e., *pn-switch* (i.e., a series connection of p- and n-type switches) and *np-switch* (i.e., a series connection of n- and p-type switches). The bipolar switches can be deployed such that each type of bipolar switch is alternately placed through the circuit. The alternate placement of bipolar switches enables the proposed *double alignment method*, i.e., datawaves are given another chance for alignment in place. Hence, there are two possible arrangements to consider in demonstrating the double alignment methods, i.e., pn–np–pn and np–pn–np. As the two arrangements are symmetric, we will demonstrate only the first arrangement of pn–np–pn, as shown in Figs. 4–6.

In Fig. 4, we show a datawave propagating through the stage in between the first pn and np; the datawave, which was initially supposed to be completely aligned (i.e., the first alignment) at the p-switch in the first pn-switch, is then getting out of alignment during the propagation due to the variation in path delays; the datawave is associated with its primary request signal with low level; and the affiliate request signal with low level in length

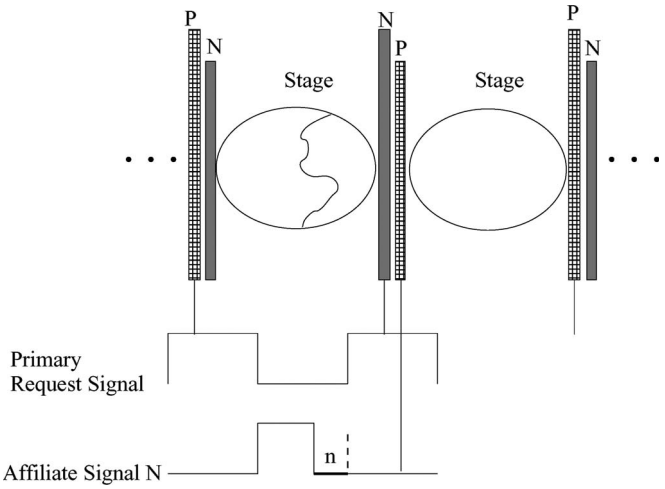

Fig. 4. Before passing the middle n-switch and p-affiliated switch.

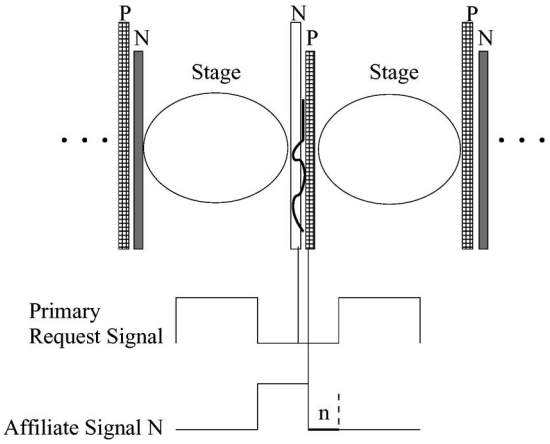

Fig. 5. Passing the middle n-switch and p-affiliated switch.

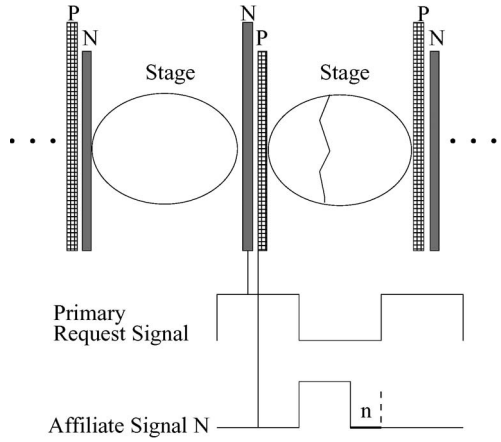

Fig. 6. After passing the middle n-switch and p-affiliated switch.

n is provided to control the double alignment. Fig. 5 shows the double alignment method: At the np-switch, the datawave just passes through the n-switch, because the datawave is associated with a high-level primary request signal and the n-switch is transparent to high-level request signal; passing through the n-switch, the datawave then gets aligned at the p-switch (i.e., the second-chance alignment) in association with the low-level affiliate request signal for the n period of time, because the p-switch is opaque to high-level request signal; and the second-chance alignment period n can be determined by the expected extent of the misalignment. (Note that, in the symmetric case of np–pn–np, the high-level affiliate request signal extends p period of time.) In Fig. 6, it is shown that the datawave has realigned after passing through the double alignment.

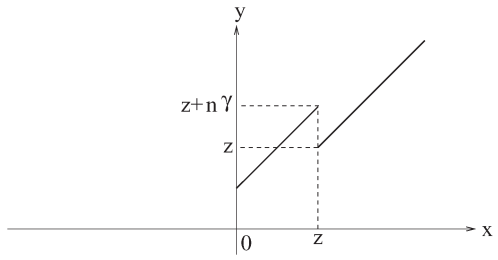

Fig. 7. Path delay with bipolar switches.

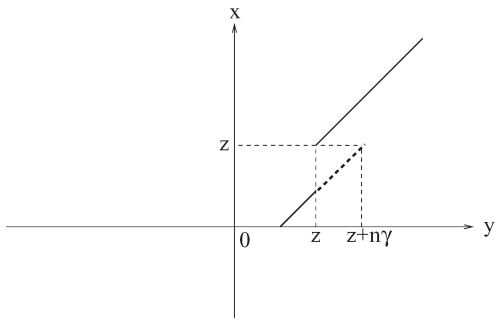

Fig. 8. Inverse function.

To demonstrate the validity of the proposed fault tolerance method for the datawave faults, we use a modeling and assurance method as follows:

Assume a random variable x with a normal distribution to represent the path delay of a bit in a datawave without the bipolar switches, and similarly, assume a random variable y with a normal distribution to represent the path delay of a bit in a datawave with the bipolar switches. The *pdf* of x can be expressed as follows: $f_x(x) = (1/\sqrt{2\pi}\sigma)e^{(-((x-\mu)^2/2\sigma^2))}$, where μ represents the mean and σ represents the standard deviation. To manipulate the extra delay induced by the double alignment, we introduce a parameter γ such that the value of the effective extra delay is $n \times \gamma$ (or, symmetrically, $p \times \gamma$), i.e., $0 \leq \gamma \leq 1$. y is the random variable of concern since this represents the new delay variable with the bipolar switches employed and is to be formalized in terms of the path-delay variable without the bipolar switches (i.e., x). In the analysis, there is a specific path-delay value z of x at which the bipolar switch has the effect of increasing y from z to $z + n\gamma$, as shown in Fig. 7. In this context, y and x can be expressed as follows: $y = x$ if $x \geq z$ or $x + n\gamma$ if $x < z$. The inverse function of this is given as $x = y$ if $y \geq z$ or $y - n\gamma$ if $y < z$, and shown in Fig. 8.

The expected resulting *pdf* of y, i.e., $f(y)$, is shown in Fig. 9 (bottom).

As shown in Fig. 9, $f_y(y)$ can be derived range by range as follows: In the range $(-\infty, z)$, $f_y(y)$ is shifted downward, resulting in the reduced shaded area beyond L to the left; this is an obvious indication of the *reduced intrawave fault rate*. Likewise, in the range of $(z, z + n\gamma)$, $f_y(y)$ is shifted upward,

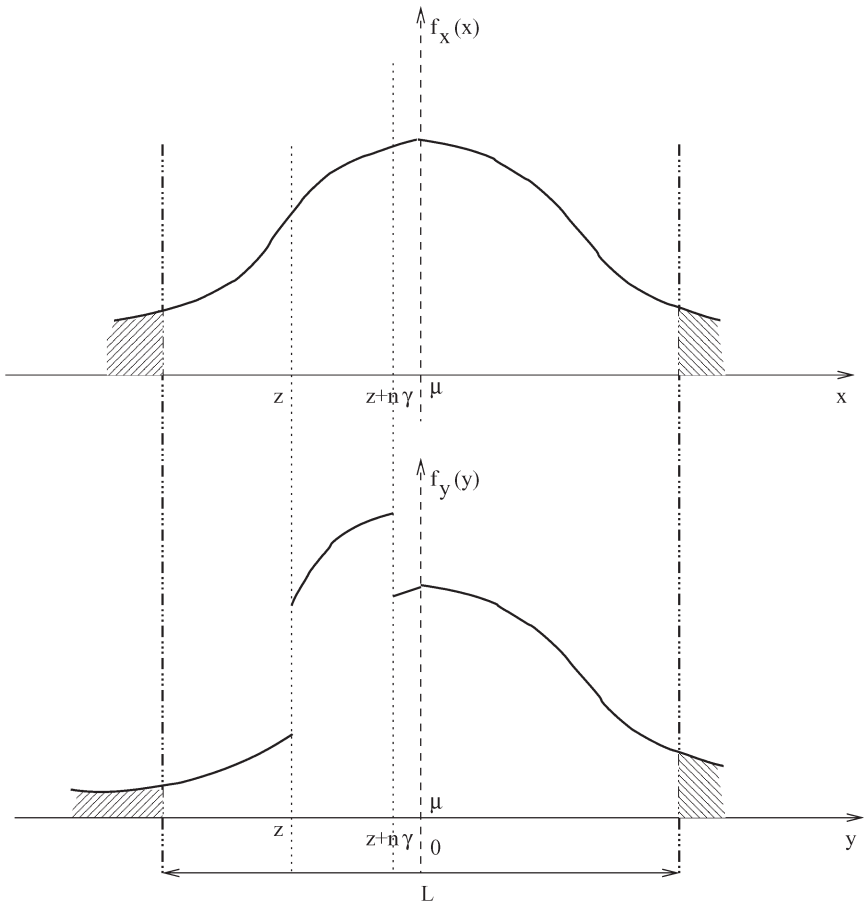

Fig. 9. PDF of the path delay with bipolar switches.

resulting in a new pdf, and the remaining portion of the pdf remains unchanged for $(z + n\gamma, +\infty)$.

1) If $y \in [-\infty, z]$ and $F(y)$ is the cumulative distribution function of random variable y

$$f_y(y) = \frac{d}{d_y}F(y) = \frac{d}{d_y}\left[\int_{-\infty}^{y} f_y(t)dt\right] = \frac{d}{d_y}\left[\int_{-\infty}^{x} f_x(t)dt\right]$$
$$= \frac{d}{d_y}\left[\int_{-\infty}^{y-n\gamma} \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(t-\mu)^2}{2\sigma^2}\right)} dt\right] = \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-n\gamma-\mu)^2}{2\sigma^2}\right)}. \quad (5)$$

2) If $y \in [z + n \times \gamma, +\infty]$, $x = y$ in Fig. 8. Thus, $f_y(y) = (1/\sqrt{2\pi}\sigma)e^{(-((y-\mu)^2/2\sigma^2))}$.
3) If $y \in [z, z + n \times \gamma]$, there are two linear functions; the first one is $x = y$, and the other one is $x = y - n\gamma$ (i.e., dotted line segment). Therefore, $f_x(y)$ and $f_x(y - n\gamma)$ should be calculated and then added together to find $f_y(y)$ for this range, i.e.,

$$f_x(y) = \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-\mu)^2}{2\sigma^2}\right)}$$
$$f_x(y - n \times \gamma) = \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-n\times\gamma-\mu)^2}{2\sigma^2}\right)}$$

and thus

$$f_y(y) = f_x(y) + f_x(y - n\gamma)$$
$$= \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-\mu)^2}{2\sigma^2}\right)} + \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-n\times\gamma-\mu)^2}{2\sigma^2}\right)}. \quad (6)$$

Putting the $f_y(y)$'s from each range together, the overall $f_y(y)$ is given as follows and verifies the correctness of the proposed model:

$$\int_{-\infty}^{+\infty} f_y(y)dy = \int_{-\infty}^{z-n\times\gamma} \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-\mu)^2}{2\sigma^2}\right)} dy + \int_{z-n\times\gamma}^{z+n\times\gamma} \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-\mu)^2}{2\sigma^2}\right)} dy + \int_{z+n\times\gamma}^{+\infty} \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-\mu)^2}{2\sigma^2}\right)} dy$$
$$= \int_{-\infty}^{+\infty} \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-\mu)^2}{2\sigma^2}\right)} dy = 1. \quad (7)$$

Without loss of generality, we assume functional independence between pn bipolar switches and np bipolar switches, and then, based on the shaded area in the *pdf* in Fig. 9 (bottom), the

TABLE III
TIMING OF ISCAS C432 ORIGINAL DESIGN (PS)

# of Stages	Mean	Variance	S.D.	D_{max}	D_{min}	Δ
3	275.4943	1530.4559	39.121	323.6667	41.5053	282.1613
4	206.6207	860.8814	29.3408	242.75	31.129	211.621
5	165.2966	550.9641	23.4726	194.2	24.9032	169.2968
6	137.7471	382.614	19.5605	161.8333	20.7527	141.0807
7	118.069	281.1041	16.7662	138.7143	17.788	120.9263
8	103.3104	215.2204	14.6704	121.375	15.5645	105.8105
9	91.8314	170.0507	13.0403	107.8889	13.8351	94.0538
10	82.6483	137.741	11.7363	97.1	12.4516	84.6484
11	75.1348	113.8356	10.6694	88.2727	11.3196	76.9531
12	68.8736	95.6535	9.7803	80.9167	10.3763	70.5403
13	63.5756	81.5036	9.0279	74.6923	9.5782	65.1142
14	59.0345	70.276	8.3831	69.3571	8.894	60.4631
15	55.0989	61.2182	7.8242	64.7333	8.3011	56.4323
16	51.6552	53.8051	7.3352	60.6875	7.7822	52.9052

intrawave fault rate for each type of bipolar switch (i.e., the ith n-type for a pn bipolar switch and the jth p-type for an np bipolar switch) can be expressed as follows respectively:

$$P_{i'\text{th}-\text{ntype}} = \int_{-\infty}^{d_{\min_i}-(L-\alpha_i-\triangle_i)} \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-n\times\gamma-\mu)^2}{2\sigma^2}\right)} dy + \int_{d_{\max_i}+\alpha_i}^{+\infty} \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-\mu)^2}{2\sigma^2}\right)} dy \quad (8)$$

$$P_{j'\text{th}-\text{ptype}} = \int_{-\infty}^{d_{\min_j}-(L-\alpha_i-\triangle_j)} \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-p\times\gamma-\mu)^2}{2\sigma^2}\right)} dy + \int_{d_{\max_j}+\alpha_j}^{+\infty} \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{(y-\mu)^2}{2\sigma^2}\right)} dy. \quad (9)$$

Thus, assuming that there are n number of n-type bipolar switches and p number of p-type bipolar switches, the overall intrawave fault rate P_{overall} can be expressed as $P_{\text{overall}} = 1 - \prod_{i=1}^{n}(1-P_i) \times \prod_{j=1}^{p}(1-P_j)$. Therefore, the overall yield Y is given by $Y = 1 - P_{\text{overall}}$.

V. SIMULATION

The simulation and validation of the proposed fault-tolerant model and design are conducted against the delay information obtained from ISCAS benchmark circuit [25] C432, C499, and C880, from which 83 926, 9440, and 8642 paths with delay information are extracted, respectively. The statistical analysis of the path delays is implemented with or without the bipolar switch design, respectively. The simulation results demonstrate that the proposed fault tolerance technique using the bipolar switches has a great impact on the intrawave fault rate. Note that the simulations are conducted only with respect to the intrawave fault, because the interwave fault functionally depends on the intrawave fault.

The circuit paths are extracted from the benchmark circuit netlist specification. Then, the delay information of the wires and gates, which is stored in the file in the stand delay format, is applied to those paths. Because the delay information specified in this benchmark circuit is all static worst-case delay, the upper delay bound of each path can directly be obtained by adding up the gate delay through the longest port for every gate and all the wire delays along the path. The lower delay bound of each path is obtained by adding up the gate delay through the shortest port for every gate and all the wire delays along the path.

The benchmark circuits themselves are distributed as non-pipelined. Thus, at this point, the maximum and minimum path delays are the bound for the whole path from the PI to the PO. The benchmark circuits are virtually designed into clockless wave pipeline circuits and clockless wave pipeline circuits with bipolar latches for the theoretically simulation purpose in this paper. The whole paths from the PI to the PO are ideally equally divided into multiple fractions, and each fraction fits in to one stage. In the real case, the functional dependence has to be considered when designing a pipelined circuit. Thus, the whole path is usually not divided into equal fractions. However, how the pipelined circuit is designed does not affect the simulation experiment results since, generally, the bipolar latch fault-tolerant design works on all clockless wave pipelined circuits.

In the original clockless wave pipeline design, there is only one latch (n or p) in between stages. The delay of the latch is not counted in this paper since it is negligible, compared with the whole path delay. According to the clockless wave pipeline architecture, the partial paths are calculated as part of the path on any two attached stages. All the partial path delays are considered as sample and are statistically analyzed. Their results are listed in the table.

In the bipolar latch fault-tolerant design, the only difference is that there are two latches in between stages, instead of one latch. The partial paths are still the part of the path on any two attached stages. Since the added latches extended the faster paths, all the partial paths that have longer path delay remain unchanged, whereas all the partial paths that have shorter path delay are extended into a certain point. The value of this certain point depends on how the parameters (γ and np) are set. All the newly generated partial paths are considered as a sample and are statistically analyzed. Their results are listed in the tables as well.

Table III shows the statistical analysis results of the benchmark circuit C432 clockless wave pipeline without bipolar design. Table IV shows the statistical analysis results of the same circuit with bipolar design. They clearly manifest the effectiveness of the bipolar design by increasing the values of $D_{\min}$. For example, the value of $D_{\min}$ increased from 41.5053 to 109.2241 when the circuit has three stages, whereas $D_{\max}$

TABLE IV
TIMING OF ISCAS C432 FAULT-TOLERANT DESIGN WITH $np = 0.6$ AND $\gamma = 0.6$

# of Stages	Mean	Variance	S.D.	D_{max}	D_{min}	Δ
3	275.542	1512.6147	38.8923	323.6667	109.2241	214.4426
4	206.6379	855.7118	29.2526	242.75	69.2208	173.5292
5	165.305	548.8563	23.4277	194.2	49.2819	144.9181
6	137.7523	381.5238	19.5326	161.8333	37.6823	124.151
7	118.0723	280.4876	16.7478	138.7143	30.2261	108.4882
8	103.3126	214.8549	14.6579	121.375	25.0874	96.2876
9	91.833	169.8152	13.0313	107.8889	21.3594	86.5295
10	82.6495	137.5813	11.7295	97.1	18.5463	78.5537
11	75.1358	113.7177	10.6638	88.2727	16.3566	71.9162
12	68.8744	95.5639	9.7757	80.9167	14.6088	66.3079
13	63.5763	81.434	9.0241	74.6923	13.1845	61.5078
14	59.0351	70.2212	8.3798	69.3571	12.0035	57.3536
15	55.0993	61.1741	7.8214	64.7333	11.0098	53.7235
16	51.6556	53.7691	7.3327	60.6875	10.163	50.5245

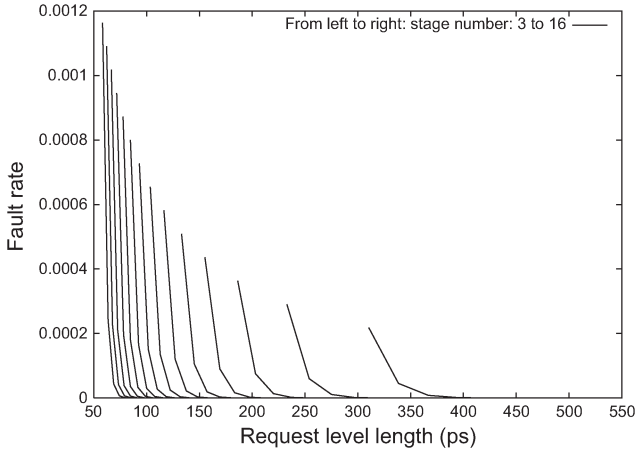

Fig. 10. $c432$ intrawave fault rate in the original design.

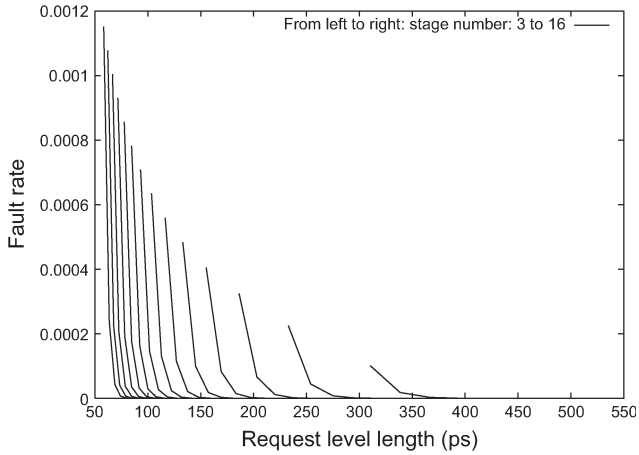

Fig. 11. $c432$ intrawave fault rate in the fault-tolerant design with $np = \gamma = 0.8$.

remained unchanged. As a result, Δ decreased from 282.1613 to 214.4426. The mean and variance both have no significant change. If L and α remained the same, $d_{\min_i} - (L - \alpha_i - \delta_i)$ and $d_{\min_j} - (L - \alpha_j - \delta_j)$ became smaller. Therefore, according to (8) and (9), the intrawave fault rate of the design with bipolar switches theoretically reduced.

To further clearly demonstrate the difference in the intrawave fault rate between the designs with and without bipolar switches, the intrawave fault rates for the benchmark circuit $c432$ are calculated in the original design and the design with bipolar switches when np and γ are set to 0.8. The results are shown in Figs. 10 and 11. In both designs, the intrawave fault rates dramatically decrease as the request signal length L increases, and as the circuit is divided into more stages, the intrawave fault rate increases. The intrawave fault rate with the bipolar switches of the clockless wave-pipelined circuit is significantly lower than the equivalent circuit without bipolar switches. For example, the intrawave fault rate is 0.0218% if the circuit has three stages, and the request signal level is 310.377 ps long in the original design, whereas the intrawave fault rate of the new design drops to 0.01009% under the same circuit circumstance.

As illustrated in (8) and (9), the parameters α, n, p, and γ all play very important roles in the bipolar switch-based design. Thus, an experiment is designed to explore the effectiveness of those parameters on the intrawave fault rate of the benchmark circuit c432. The experiment is carried out, with focus on the following three analyses: 1) to analyze the effectiveness of the request signal length on the intrawave fault rate; 2) to analyze the effectiveness of $np \times \gamma$ on the intrawave fault rate; and 3) to separately analyze the effectiveness of np and γ on the intrawave fault rate. They are shown in Figs. 12–15.

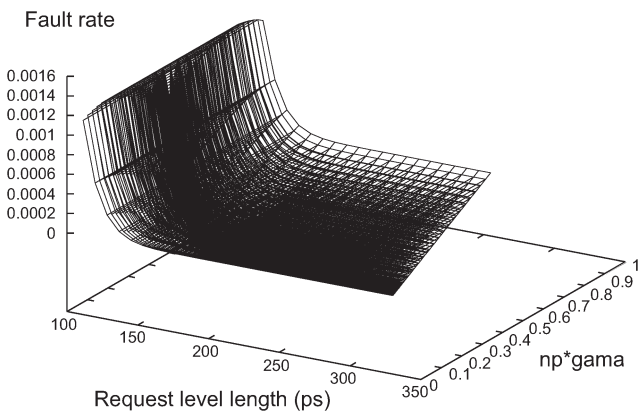

Fig. 12. $c432$ intrawave fault rate analysis in the fault-tolerant design with stage number $= 5$.

In Fig. 12, the effectiveness of parameters α and $np \times \gamma$ on the intrawave fault rate is evaluated. Since $L = \Delta + 2\alpha$ and Δ is static, once the number of stages in the circuit is fixed, the value of α is determined by the length of the request signal level. As shown in the figure, the intrawave fault rates are significantly reduced as the request signal length changes from 100 to 350 ps if the circuit has five stages. This can indirectly

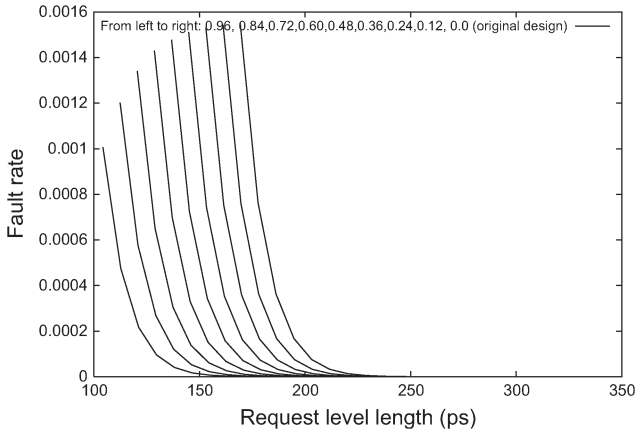

Fig. 13. Effectiveness of $np \times \gamma$ in the fault-tolerant design of $c432$ with stage number $= 5$.

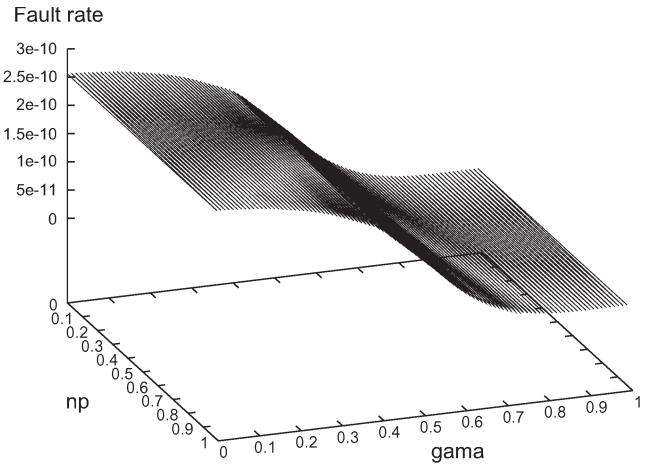

Fig. 14. Effectiveness of np and γ in the fault-tolerant design of $c432$ with stage number $= 3$ and $\alpha = 0.8\Delta$.

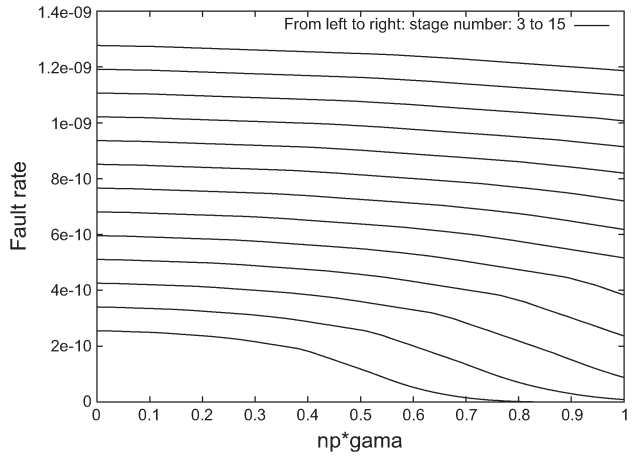

Fig. 15. $c432$ intrawave fault rate analysis in the fault-tolerant design of $c432$ with $\alpha = 0.8\Delta$.

be accounted for the effectiveness of α on the intrawave fault rate. The parameter $np \times \gamma$ is also very critical to the intrawave fault rate, whereas its effectiveness is not very visible, as shown in this figure. Thus, in the next figure, they are further investigated.

Fig. 13 shows the effectiveness of $np \times \gamma$ as the intrawave fault rates when the stage number is 5 and the request signal length is in the range of 100–350 ps. The higher the value of $np \times \gamma$, the lower the intrawave fault rate. As shown in the figure, the intrawave fault rate is 0.0075399% when $np \times \gamma$ is equal to 0.96 and the request signal level is equal to 203.15616 ps, whereas the intrawave fault rate is 0.0000229% when $np \times \gamma$ is equal to 0.24 at the same request signal level length. The situation of $np \times \gamma = 0$ is actually the case where there is no bipolar switches. As shown in the figure, the intrawave fault rate is the highest when $np \times \gamma = 0$. This is another evidence of the effectiveness of the bipolar switch-based fault-tolerant design.

Fig. 14 shows a 3-D figure that serves the purpose of further illustrating how the parameters of np and γ individually affect the intrawave fault rate when the circuit has three stages and α is 0.8. As shown in the figure, γ has significant effects on the intrawave fault rate. The intrawave fault rate greatly drops as γ increases from 0 to 1. np also considerably affects the intrawave fault rate such that the intrawave fault rate drops as np increases.

Fig. 15 shows the effectiveness of parameter $np \times \gamma$ on the intrawave fault rate with designs with respect to different stage numbers when $\alpha = 0.8$. The intrawave fault rate greatly increases as the stage number increases and significantly reduces as $np \times \gamma$ increases.

VI. Conclusion and Discussion

This paper has presented comprehensive theoretical yet practical methodologies to model, assure, and optimize the reliability of clockless wave pipeline-based embedded IP combinational logic cores in their early design stage for seamless integration along with heterogeneous embedded IP cores.

The specific architectural model referenced in this paper is the two-phase clockless asynchronous wave pipeline. The intrawave fault model has been proposed and thoroughly identified as the unique fault of the clockless wave pipeline, compared with the wave and wave delay faults of conventional wave pipelines. The intrawave fault rate is statistically yet practically modeled and extensively studied with respect to various design parameters, such as yield, fault coverage, defect level, and request level length. In addition, it has been analyzed and revealed that placing $\triangle$ in the middle of L or dividing d and $\triangle_{\max} - \triangle$ equally to stride at both sides of $\triangle$ can drastically reduce the intrawave fault rate.

The interwave fault, in addition to the intrawave fault model, has been proposed for comprehensive characterization and optimization of the fault rate and yield. The relation between the two fault models is such that an interwave fault is a subset of an intrawave modeled fault, i.e., an intrawave fault is a necessary but insufficient condition for an interwave fault. Thus, functionally, intrawave and interwave faults comprehensively cover the whole fault domain, based on which an optimization of fault rate and yield has been conducted by finding the optimal value of α (i.e., the difference in propagation time between the slowest data bit of a datawave and its associated request signal)

for the intrawave fault model and a/b for the interwave fault model.

To realize a reliable clockless wave pipeline, the fault tolerance for request signal and datawave approaches have been proposed under the proposed fault models. It was demonstrated that a low-level glitch hit on a high request signal line may cause a broken datawave (i.e., intrawave fault on p-switches) with no fault on the n-switches assumed. In addition, a high-level glitch hit on a low request signal line may result in a broken datawave (i.e., intrawave fault on n-switches) with no fault on the p-switches assumed. Based on this principle, an AND gate was used to mask the high-level glitch hit on a low request signal to a p-switch, and an OR gate was used to mask the low-level glitch hit on a high request signal to an n-switch. This simple yet effective approach can mask all the glitches on the request signal lines, except when every redundant request signal line is impaired by glitch at the same time.

It has been demonstrated that the reliability of the clockless asynchronous wave pipeline is exponentially increased as more redundant request signal lines are incorporated. In addition, the reliability with respect to MTTG, λ (glitch rate), and L (request signal level length) has been analyzed. It was demonstrated that the proposed bipolar switch two-phase clockless wave pipelines with redundant affiliate request signals cause the reduction on the data skew along the datapaths. As the intrawave fault is caused by the data skew on different data paths, the bipolar switches in association with the affiliated request signals can effectively slow down the propagation speed of the faster data bits without affecting the propagation of the slower data bits. Therefore, the data skew rate has been reduced, and consequently, the intrawave fault rate is effectively reduced as well. Numerical experiments and simulations have demonstrated and verified the efficiency and effectiveness of the proposed reliability modeling and assurance methods, and fault-tolerant design for reliability.

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