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Characterization of Human Metal ESD Reference Discharge Event and Correlation of Generator Parameters to Failure Levels—Part II: Correlation of Generator Parameters to Failure Levels

Kai Wang, David Pommerenke, Ramachandran Chundru, Tom Van Doren, *Fellow, IEEE*, Federico Pio Centola, and Jiu Sheng Huang

***Abstract*—Most electrostatic discharge (ESD) generators are built in accordance with the IEC 61000-4-2 specifications. It is shown, that the voltage induced in a small loop correlates with the failure level observed in an ESD failure test on the systems comprised of fast CMOS devices, while rise time and derivative of the discharge current did not correlate well. The electric parameters of typical ESD generators and ESD generators that have been modified to reflect the current and field parameters of the human metal reference event are compared and the effect on the failure level of fast CMOS electronics is investigated. The consequences of aligning an ESD standard with the suggestions of the first paper, of this two-paper series, are discussed with respect to reproducibility and test severity.**

***Index Terms*—Electrostatic discharge (ESD) generator, fast CMOS system, induced loop voltage.**

I. INTRODUCTION

THIS IS Part II of a two-paper series. In Part I, a reference human metal electrostatic discharge (ESD) event was derived and characterized by current, current derivative, fields, and induced voltages. This article applies the parametric characterization for analyzing the failure level in fast CMOS circuits. The objective is to reveal the reasons for the bad reproducibility of test results observed in systems containing fast digital logic. Such circuits will experience vastly different failure levels during ESD tests, depending on the brand ESD generators [1]–[7]. Understanding the underlying reasons allows for the revision of ESD generators and to adopt the ESD standards like IEC 61 000-4-2 to improve test result uncertainties.

Numerous parameters have been suggested to define the "severity" of an ESD generator with respect to fast logic circuits. Some of them are: 1) discharge current derivative ("smoothness of the waveform") [8]; 2) spectral density of the discharge current [9]; and 3) transient fields [10], [11]. Using identical CMOS systems setups, this paper presents data on failure level variations, as large as 1 : 5, due solely to changing the ESD generator while only using generators that fulfill the present IEC 61 000-4-2 specifications. The induced loop voltage data generated by the reference event and different generators is presented and compared in Section II. From this and the failure levels, it is shown that the voltage induced in a small loop correlates well to the failure levels, shown in Section III. Finally, the consequences of aligning the 61 000-4-2 [12] standard with the suggestions of this paper are discussed with respect to reproducibility and test severity in Section IV.

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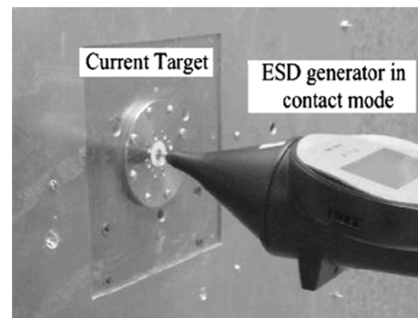

Fig. 1. Photo showing one of the ESD generators used to measure the data shown in Figs. 2 and 3.

II. INDUCED VOLTAGES OF PRESENT ESD GENERATORS RELATIVE TO THE REFERENCE ESD EVENT

In Part I, the voltage induced by multiple reference ESD human metal events was presented. To compare this data with ESD generators, a set of ESD generators has been discharged in contact mode to a current target mounted within the metallic sidewall of a shielded room. The semiloop was mounted on the wall, Fig. 1. The average voltage induced by the human metal reference ESD is compared to voltages induced by three different ESD generators in Fig. 2.

All nine commercial generators investigated showed strong high-frequency components in the induced voltages. Additionally, the voltage is often strongly dependent on which side of the generator is facing the loop; most generators exhibit no symmetry of rotation. The reference does as long as the arm is fully extended, as the fast changing fields are mainly caused by the hand–arm structure. Figs. 2 and 3 also include induced voltage data of a generator especially designed to provide currents and

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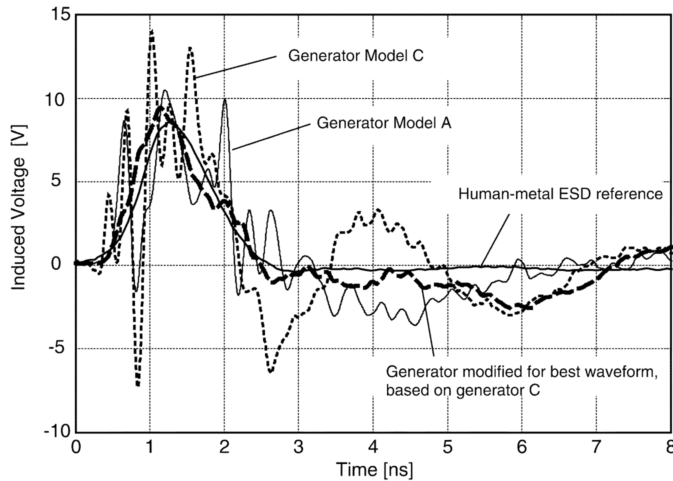


Fig. 2. Voltage induced in a 28-mm diameter semiloop at a distance of 0.1 m from the discharge point for the average of the human metal reference events, two commercial ESD generators and a modified ESD generator. The data is shown for 5-kV charging voltage.

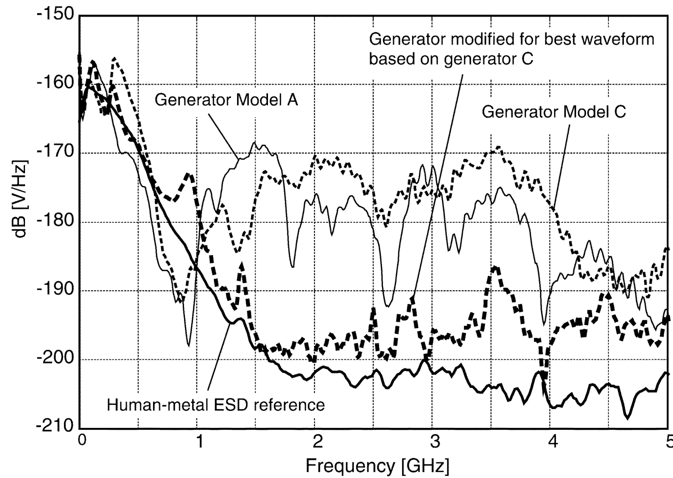


Fig. 3. Comparison of the spectral density of the induced loop voltages produced by human metal ESD with the discharges from ESD generators. The dynamic range of the 8-bit 4 Ghz, 20 G samples/s oscilloscope limits the noise floor to about -200dB (V/Hz).

fields as close to the reference event as possible. Its induced voltages are lower and show little ringing. The induced voltage is close to the dynamic range limit of the measurement system.

The modified ESD generator did not withstand the 5-kV charging voltage, as it had not been potted in epoxy resin. For that reason, the data has been taken in contact mode at 1 kV and scaled to 5 kV. The scaling assumes linearity. In general, linearity is given, but the voltage collapse inside the relay will be somewhat slower at 5 kV relative to the 1 kV measurements. Based on data presented in the discussion section, it can be estimated that, due to deviations from the linear relationship, the spectral density values at 5 kV are less than 3 dB below the values shown.

Up to about 500 MHz the differences are small. Beyond this frequency, larger differences become visible. For the commercial ESD generators, the spectral densities shown in Fig. 3 are often 20 dB above the human metal reference event. The spectral density of the modified generator is still above the noise floor. Relative to the commercial generators, its spectral density is improved by 10–20 dB. By the spectral density information, it can be expected that this will not impact slower circuits, i.e., circuits that cannot respond to very narrow induced voltage pulses, but that fast circuits will be strongly affected by the differences observed about 1 GHz.

It is noteworthy to analyze two extreme cases for illustrating the cause of the voltage induced in a small loop. In the first hypothetical case, the generator is constructed in such a way that the discharge current at its tip is zero. In this case, only the fast currents from the relay would cause an induced voltage. The other extreme case uses a relay having an internal voltage collapse time of about 1 ns, but in contrast to the first case a discharge current close to the IEC specification. In this case, there would be no fast changing currents within the structure, only currents of about 1 ns rise time would induce a voltage in the loop.

In reality, both effects contribute to the loop voltage. For marketed generators the fast changing currents dominate the induced loop voltage, such that the induced loop voltage does not correlate well with the rise time. If these fast changing currents would be shielded, the rise time as well as the peak current derivative would correlate to the induced voltage. For such a case, one would expect that rise time would be predictive for the response of fast EUTs. But for now, the generators contain too much unshielded currents that overwrite the correlation between discharge current rise time at the tip and the EUT response. Such a correlation has often been expected.

III. Correlation of Failure Threshold to Voltages Induced in the Small Loops

To determine which parameters need to be standardized in an ESD generator, one needs to understand which electrical parameters cause the EUT to fail. The answer depends on the EUT and the location of the discharge. As long as the parameters are similar between the ESD generators and the EUT, repeatable test results will be achieved. For the cases in which the test results vary strongly between ESD generators, different explanations have been proposed [12], e.g., current derivative, ringing in the waveform, transient fields, time dependence of the EUT, etc. Here we disregard the time dependence of the EUT and assume that a sufficiently large number of discharges has been applied, i.e., only one for an EUT that has a time invariant susceptibility but many for a PC-like system. A significant effort has been placed into determining and reducing the measurement uncertainty of the ESD current and designing new current targets [13]–[15]. While this is important from a metrology point of view and required via accreditation, it may not solve the repeatability problem faced in ESD testing. The parameter causing the large test result variations needs to be identified and controlled.

Different brand simulators have been used as well as modified simulators. The failure levels and the peak-to-peak voltages induced in a 5-mm radius loop are shown in Table I. To allow the analysis of possible other correlation, e.g., between failure level and rise time, also the rise times and the peak current derivatives are included in Table I.Different EUTs have been tested for nondestructive failures. The setup was similar to the one given by [12]. For EUTs comprising of slow CMOS-logic the failure levels were only weakly affected by the ESD generator used.

TABLE I
ESD FAILURE LEVELS, RISE TIMES, PEAK CURRENT DERIVATIVES, AND THE CORRESPONDING INDUCED VOLTAGES IN A SMALL LOOP (4-GHZ BANDWIDTH MEASUREMENT) FOR DIFFERENT BRAND ESD GENERATORS AND MODIFIED GENERATORS. THE LOOP HAD A RADIUS OF 5 MM AND WAS PLACED AT A DISTANCE OF 0.4 M. THE LOOP VOLTAGE MEASUREMENT WAS DONE ON A LARGE GROUND PLANE WITHOUT THE EUT

ESD generator	**EUT ESD Failure level (kV)**	**Induced loop voltage, Peak to peak value normalized to 1 kV (V)**	**Rise time (10% - 90% of the peak value) (ps)**	**Maximum Current Derivative A/(kV*ns)**
ESD A	1.3	0.56	1000	5.37
ESD B	6.2	0.29	1000	5.87
ESD C	2.6	0.49	900	7.55
ESD D	1.3	0.56	860	5.25
ESD E	4.8	0.18	990	5.10
Optimized ESD C1	3.8	0.29	580	10.70
Optimized ESD C2	1.9	0.43	440	14.50
Optimized ESD C3	3.8	0.30	400	11.64
Optimized ESD C4	4.4	0.20	1030	7.32
Optimized ESD C5	1.0	0.62	200	18.30

Note: Optimized ESD C1: 600 ps rise time, very smooth waveform. Optimized ESD C5: about 200 ps rise time, designed to achieve very strong high-frequency components.

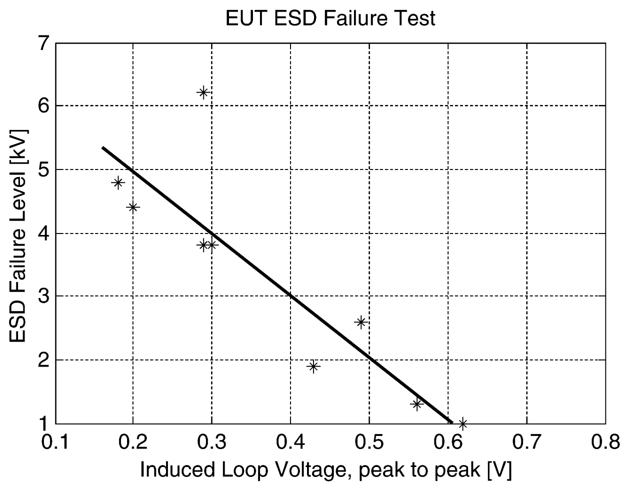


Fig. 4. Correlation between ESD failure level and induced voltage data. The data is from Table I. The induced voltage is normalized to 1 kV.

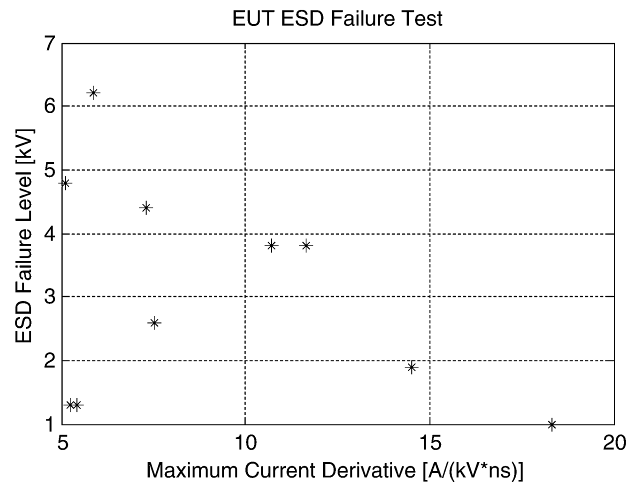


Fig. 5. Correlation between ESD failure levels and the maximum current derivatives. The data is from Table I.

However, for fast CMOS devices the picture changed dramatically. In this testing, a system containing CMOS ICs, operating above 1.5-GHz clock, and manufactured in less than 1.5-μm technology has been used. Contact mode discharges were applied in proximity to the system or on grounded metallic structures of the system while it was observed for soft errors.

While the correlation between failure levels and induced peak-to-peak voltages is shown in Fig. 4, the correlation between failure levels and maximum current derivatives is presented in Fig. 5.

To illustrate the meaning of the data presented in Table I, it compares the data in the first row "ESD A" to the data in the second row "ESD B." Both generators have a similar rise time and a similar maximum current derivative. This indicates that both have about the same waveform for at least the fast initial rise. But the failure level differs a lot: at 1.3 kV, the EUT fails if ESD A is used but it takes 6.2 kV to fail the EUT if ESD B is used. If the normalized peak to peak induced loop voltages are compared, we see that ESD A induces 0.56 V at 1 kV charging voltage, while ESD B only induces 0.29. This is about a 2 : 1 difference. The failure level varied about 4.5 : 1, not fully reflecting the 2 : 1 variation of the induced voltage, but illustrating the principle effect: an induced loop voltage correlates better to the observed failure level than any other property measured.

Another data set worth analyzing is "optimized C5." This simulator has a fast rise time of 200 ps and a large current derivative of 18.3 A/(ns $*$ kV) but the level at which the EUT fails (1 kV) is similar to the value obtained from "ESD A" which has a much slower rise time of 1 ns. This again emphasis the fact that rise time and current derivative do not predict the failure level well.

It is important to note that this ESD test result is repeatable in the sense that if the same ESD generator is used, the results will repeat well. Three important conclusions can be drawn.

1) A 1 : 5 variation of ESD failure level is introduced by differences between the first nine ESD generators. These generators fulfill or are very close to the specifications spelled out in IEC 61 000-4-2. If "optimized ESD C5 " is taken into consideration (it rises in 200 ps), a 1 : 6 variation is observed.

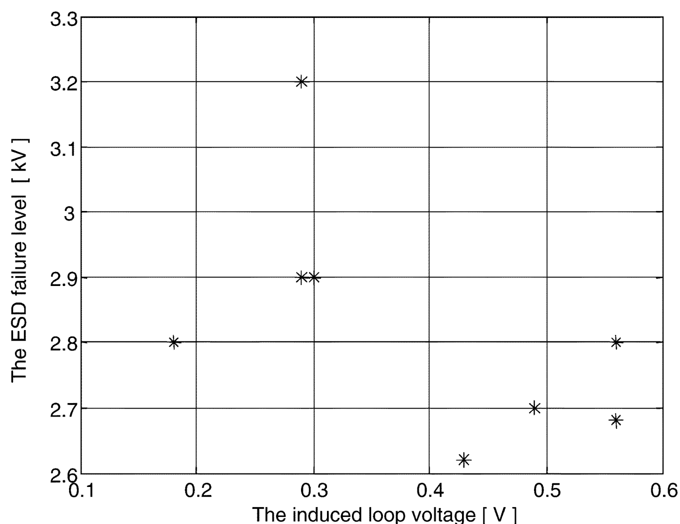


Fig. 6. Correlation between the induced loop voltage and the failure level for a 20-MHz clock CMOS device, having > 3ns signal rise and fall times.

2) There is good correlation between the ESD failure levels and the induced loop voltages.
3) The peak current derivative and the rise times do not correlate well to the failure level. A failure level variation of 1 : 5 was observed for generators having rise time variations of only between 0.7–1 ns, i.e., rise time alone can not explain the variations.

The analysis of the data showed that there is at most a weak correlation to the rise times or peak current derivatives. Of all the parameters, rise time, current derivative of the discharge current, and induced voltage, the induced voltage in a loop is the best indication for the failure level of very fast CMOS devices. No other parameter varies as much as the failure level observed during the contact mode testing.

The ESD test is on a very fast CMOS device. The same test is also applied to some slow digital devices which operate below 20 MHz. The correlation between the induced loop voltage and the ESD failure level of this slow device is show in figure.

By comparing Figs. 4–6, we realize a small spread of the failure levels for the slow CMOS device: it is 2.6–3.2 kV and no obvious correlation to the induced loop voltage. The discrepancies between both figures make sense; qualitatively, we can understand the difference as such: that the slow CMOS device is not susceptible to the rapidly changing components. Its slow inputs cannot react fast enough. In contrast, the fast CMOS device will be able to respond to pulses as narrow as 50 ps, i.e., it will be disturbed by the rapidly changing components. As the induced loop voltage is a measure for the fast components, we do not see a correlation to the failure level for slow CMOS but it correlates to the fast CMOS device.

As the fraction of devices that use fast CMOS is increasing, and going to continue to increase in the future, changes in the ESD standard are needed. Without such changes, the growing fraction of devices that can respond to pulses having widths of tens to hundreds of picoseconds will lead to an increased dependence of the test result on the ESD generator selected, such as shown in Fig. 4.

IV. Discussion

The data of the first paper showed that human metal ESD at 5 kV having 0.85-mm arc length yields current values close to the IEC specifications. Consequently, and constrained by the fact that the IEC TC77b will not accept changes to the present peak value and rise time specifications, these ESDs have been selected as reference events. But it does not answer the question: how likely are such events? How many of the ESDs will have a larger severity than the reference event? Due to the strong dependence on factors like humidity, personal activity, clothing, etc, there is no final answer. Generally, for lower voltages the typical rise times are much shorter and the rate of occurrence of ESD is larger, but fast rising ESD having less than 300 ps rise time can also occur under dry conditions and fast approach speeds at voltage as high as 15 kV.

A. Which Part of the Waveform Is Responsible for the System Failure?

The data presented in Fig. 4 showed a good correlation between the induced voltage and the failure level for the fast CMOS VLSI IC. Will that correlation be valid in general? This is unlikely since the input of digital EUTs can be approximated as a low-pass filter followed by an infinitely fast threshold detector. In a rough approximation, neglecting resonances, the coupling to the IC has a high-pass characteristic if we consider that the ESD current is injected into some well grounded part of the system, e.g., a metallic enclosure.

The induced voltage of a typical present day ESD generator is the superposition of the voltage caused by the more or less smooth discharge current and the induced voltage by fast changing currents within the generator. Depending on the low-pass 3-dB frequency of the input of the digital IC, the IC may respond only to the smooth contribution, as it integrates over the fast changing components. The response will be related to the rise and fall times of the initial current peak. This relationship has been given in [8], [9], [16], and [17]. However, the authors did not consider faster reacting digital systems, as there were only slower systems at the time of the publications.

The effect of using various ESD generator models will be smaller than the observed 1 : 5 ratio of EUT failure voltages, as the ESD standard limits the rise time to 0.7–1 ns. The falling edge of the initial rise varies from being as fast as the rise (similar current derivative) to about three times slower for most commercial ESD generators. For a EUT that reacts to the lower frequency $(< 1$ GHz$)$ current components, the effect of changing the ESD generator model should not be larger than 1 : 3. In fact, we have not observed any ratio of EUT failure voltages above 1 : 2. In contrast, modern CMOS circuits with less than 0.15-μm technology can react to pulses as narrow as 50 ps. These circuits will respond to the fast changing (unintended) components of the induced voltage. The effect of changing the ESD generator model may be as large as 1 : 10, as the spectral density varies by more than 20 dB, as shown in Fig. 3. Our observations showed a 1 : 5 variation.

With the introduction of more and faster CMOS circuits, the large influence of the ESD generator model, shown in Fig. 4, will occur more often if the ESD standard is not improved.

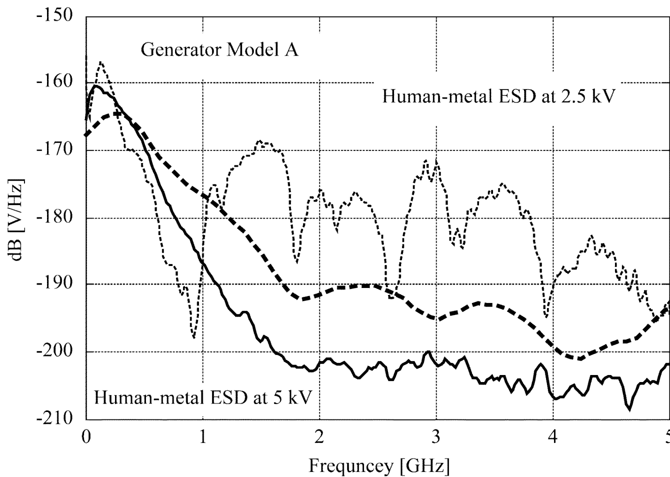


Fig. 7. Spectral density of the induced voltage for an ESD generator and two reference events.

B. How Will the Severity Averaged Over All ESD Generator Models Change if the Reference Event Is Adopted by All Generators?

The data presented in Fig. 7 indicates that most of the present ESD generators yield transient field spectral densities that are significantly above the human-reference event. The revision of the IEC 61 000-4-2 standard intends to bring the generators in line with the reference event.

If one would modify all ESD generators such that their induced voltages would match the reference event, two consequences need to be considered.

1) The test repeatability will be improved by a large amount. This is the most significant outcome, as the lack of repeatability is the driving force for revising ANSI C63.16 and IEC 61 000-4-2 standards.
2) For many but not all ESD generators, the test severity will be significantly reduced for electronic systems that are susceptible to the > 1 GHz spectral components. Examples are fast CMOS VLSI ICs. This may be a desired effect as it leads to cost reduction, but it might lead to field failures due to ESD. A low-voltage ESD is much more likely than ESDs at high voltages.

Those low-voltage ESDs and higher voltage ESDs having short arc lengths show short rise times, as low as 50 ps, thus, their high-frequency content is much stronger. Up to now some widely used ESD generators not only covered the spectral content of the proposed reference event, but also tested for fast rising ESDs. They did not do so intentionally, but as a result of their design, which was based on incomplete understanding of the failure mechanisms in fast electronic systems and insufficient specifications.

As a consequence standardization bodies or manufacturers could adopt a second ESD test having a faster rise time. Do present ESD generators emulate the induced voltage of such a fast rise time test? For answering this question a hypothetical reference event of 2.5 kV, 250 μm arc length was taken. Its rise time is about 250 ps and the peak current is about 17 A (at 2.5 kV). Using the same methodology as for the 850-ps rise time reference event described above, the currents and the induced voltages have been measured. The spectral content of these induced voltages were compared.

The data in Fig. 7 indicates that present day simulators provide too much energy above about 1 GHz even if a faster reference event would be adopted. This shows that the risk of having many field failures as a consequence of an improved ESD generator specification is not large. Of course, if one would consider a reference event of 50-ps rise time, its spectral content would extend into the multiple gigahertz range.

C. Is the ESD Generator Linear in Contact Mode?

In contact mode, the arc discharge is confined to a relay. In most generators, pressurized gas relays are used. If the time needed for the voltage collapse would be independent of the applied voltage, the discharge current and all field components would be linear with respect to voltage. Upon observing the discharge current while varying the voltage, typically no nonlinearity are observed.

The current will flow inside the relay before the contacts meet. If the distance is reduced sufficiently explosive emission processes on the surface will initiate the breakdown. Both injection of metal from the surface and gas ionization will provide the needed charge carriers. It is expected that at higher voltages the contribution of gas ionization to the overall current though the gap between the contacts will increase due to that larger gap distance over which the breakdown will occur (the breakdown is initiated if a certain surface field strength is reached, i.e., the larger the voltage the larger the gap will be).

For that reason, one would expect that the voltage collapse fall time increases with the applied static charge voltage prior to the breakdown. We are not aware of any method to measure the voltage across the contacts with sufficient bandwidth, but observing the spectrum of the voltage induced in a small loop allows to indirectly concluding on the processes within the relay.

The process was as follows.

1) The induced voltage has been measured for different charging voltages between 500 and 8000 V in contact mode. A couple of discharges have been taken at each voltage and the spectral density has been averaged. The pulses repeated very well, so the averaging had little overall effect.
2) The effect of changing the voltage from 500 to 8000 V and the effect of changing the voltage from 1000 to 5000 V have been analyzed at frequencies that contain a sufficient spectral density (avoiding nulls in the spectrum, but selecting maxima).

The data shows a nearly linear rise. A perfect linear rise would increase the spectral density by going from 500 to 8000 V by 24 dB. To visualize the effect better the deviation from the linear rise has been plotted in Fig. 8. For example, instead of the 24-dB increase, only an increase of 16 dB was observed at 4.8 GHz. Of course, at lower frequencies, e.g., 0.5 GHz a nearly 24-dB increase is observed. The results are shown in Fig. 8.

If the voltage is increased from 500 to 8000 V, the spectral density at 3 GHz is increased by 21 dB, i.e., about 3 dB less than a linear relationship would provide.

While the data for the 500 to 8000 V increase can be approximated by a straight line, it is noteworthy to analyze why this

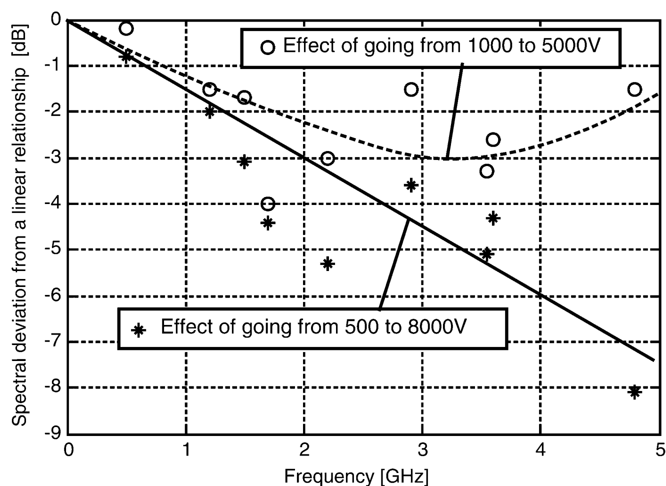


Fig. 8. Deviation from a linear increase of the spectral density of the induced voltage (28-mm loop, 0.1 m) as a function of charge voltage. Data from ESD generator model A and C. Both use the HC-5 relay from kilovac.

cannot be done for the 1000–5000-V data: At 4.8 GHz, the increase of the voltage from 500 to 1000 V already caused a strong deviation from the linear relationship, a further increase of the voltage to 5000 V had only an effect of 1.5 dB.

It is possible to estimate the voltage fall time within the relay using this data. We will assume the following.

- Voltage collapse waveform can be represented by a step function having the waveshape of an integrated Gauss-impulse. The step function is negative to represent the voltage collapse. It is characterized by its fall time. This is a reasonable assumption, but measured fast breakdowns often show a quick initial collapse for the first 70% of the voltage and a slower process thereafter [18].
- For 500 V discharges the spectral density of the step function is not affected by the fall time for frequencies up to 5 GHz, i.e., the spectral density follows $1/f$, with f being the frequency up to 5 GHz. Or, applying the same assumption for the nonintegrated Gauss pulse, its spectral voltage density is flat up to 5 GHz.

Using these assumptions the data presented in Fig. 8 is analyzed. The deviation from the linear increase of about -7.5 dB when raising the voltage from 500 to 8000 V would be matched by an integrated Gauss pulse having a fall time of about 100 ps. This can be taken as a rough estimate of the voltage collapse fall time within the pressurized relay at 8 kV. A 50 ps fall time would only result in a -1.8 dB deviation at 5 GHz.

It needs to be noted that the data shown in Fig. 8 will depend somewhat on the ESD generator used and that there is significant scatter in the data points. It mainly provides a qualitative idea on the deviation from the linearity.

However, within the frequency and voltage range observed, the deviation from the linearity is not very strong. For comparison one needs to note that for air discharges, above a voltage threshold that depends on the speed of approach and time lag, the spectral density generally goes down with voltage [5], [19]–[21], i.e., the process inverts from a linear process. For ESD generators that allow contact-mode discharge voltage up to 30 kV further investigations are needed, as they might show a much stronger deviation from linearity due to different relay designs.

D. Changes to the ESD Standard for Reducing the Effect of the ESD Generator Model on the Test Results

In our opinion, the ESD standard should be revised such that ESD generator performance is as similar to the reference events as possible in all their parameters. But manufacturers and users need to be aware that the standard does not cover all possible ESD events. For example, medical equipment might need to be tested using a shorter rise time to cover a larger portion of the real ESDs, notwithstanding furniture ESD or other ESD types. The standard needs to be understood as a minimum requirement, passing it does not protect against ESD related field failures.

V. Conclusion

The two paper series derived a reference ESD event for human metal ESD from measured discharges. It is characterized by current, current derivative fields, and induced voltages. Further, it is shown that the peak-to-peak value of the voltage induced in a small loop correlates with the failure level in fast CMOS devices. The peak-to-peak voltages and the spectral content of the induced voltages vary greatly between different brand ESD generators. This correlates well with failure level variations in fast CMOS electronic systems of up to 1 : 5. The data supports that a revised ESD standard will reduce the test result uncertainty if current derivative and most of all, the induced voltage are included as specifications for the design of ESD generators. As unintended radiations from the ESD generators would be reduced, the change might reduce the test severity for very fast digital systems.

References

[1] J. Maas and W. Rhoades, "New ANSI ESD standard overcoming the deficiencies of world wide ESD standards," in *Proc. IEEE Int. Symp. EMC*, vol. 2, 1998, pp. 1078–1082.

[2] J. S. Maas and D. J. Pratt, "A study of the repeatability of electrostatic discharge simulators," in *Proc. IEEE Int. Symp. EMC*, 1990, pp. 265–269.

[3] K. Hall, "Tests with different IEC 801.2 simulators have different results," in *Proc. EOS/ESD Symp.*, Las Vegas, NV, Sept. 1994, pp. 161–163.

[4] K. Hall, D. McCarthy, D. Dale, D. Smith, J. Nuebel, J. Barth, and H. Hyatt, "Steps taken to determine why different IEC 61000-4-2 ESD generators produce different results," in *Proc. Int. Zurich Symp. EMC*, 1997, pp. 105–108.

[5] D. Pommerenke, "ESD: Transient fields, arc simulation, and rise time limit," *J. Electrostatics*, vol. 36, no. 1, pp. 31–54, Nov. 1995.

[6] D. Pommerenke and M. Aidam, "ESD: Waveform calculation, field and current of human and simulator ESD," *J. Electrostatics*, vol. 38, no. 1–2, pp. 33–51, Oct. 1996.

[7] D. Pommerenke, "ESD: What has been achieved, what is less well understood?," in *Proc.13th Int. Zurich Symp. Technical Exhibition Electromagnetic Compatibility*, Zurich, Switzerland, Feb. 16–18, 1999, pp. 77–82.

[8] B. Daout and H. Ryser, "The reproducibility of the rising slope in ESD testing," in *IEEE Int. Symp. EMC*, 1986, pp. 467–474.

[9] C.-Y. Wu, "On the frequency domain specification of ESD waveforms," *J. Electrostatics*, vol. 24, pp. 197–206, 1990.

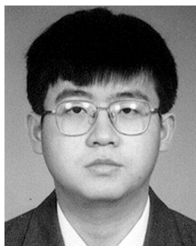
[10] K. Wang, D. Pommerenke, and R. Chundru, "Numerical modeling of electrostatic discharge generators," *IEEE Trans. Electromagn. Compat.*, vol. 45, pp. 258–271, May 2003.

[11] M. Mardiguian, *Electrostatic Discharge: Understand, Simulate and Fix ESD Problems*. Warrenton, VA: Don White Consultants, 1986.

[12] *Electromagnetic Compatibility (EMC)—Part 4-2: Testing and Measurement Techniques—Electrostatic Discharge Immunity Test*, IEC 61 000-4-2, 1995.

[13] J. Sroka, "Insertion loss as transfer coefficient for the calibration of ESD generators. Is it sufficient to cope with?," in *Proc. IEEE Int. Symp. EMC*, vol. 2, 2001, pp. 838–840.

[14] ——, "Contribution of the target in the measurement uncertainty by calibration of the ESD generator," in *Proc. 14th Int. Zurich Symp. EMC*, Feb. 2001, pp. 189–192.
[15] Y. Braem, W. De Ketelaere, L. Martens, and Y. Vlietinck, "Calculation of the ESD-pulse parameters and associated uncertainty for ESD-gun calibration," in *Proc. IEEE Int. Symp. Electromagnetic Compatibility*, vol. 1, 2000, pp. 449–452.
[16] R. K. Keenan and L. A. Rosi, "Some fundamental aspects of ESD testing," in *IEEE Int. Symp. EMC*, 1991, pp. 236–241.
[17] ——, "Some fundamental aspects of ESD testing: Part II," in *IEEE Int. Symp. EMC*, 1992, pp. 469–473.
[18] S. Bonisch, D. Pommerenke, and W. Kalkner, "Broadband measurement of ESD rise times to distinguish between different discharge mechanisms," *J. Electrostatics*, vol. 56, no. 3, pp. 363–383, Oct. 2002.
[19] B. Daout, H. Ryser, A. Germond, and P. Zweiacker, "The correlation of rising slope and speed of approach in ESD testing," in *Int. Zurich Symp. EMC*, Zurich, Switzerland, Mar. 1987.
[20] P. Richman, "Progress report on a different kind of ESD standard," in *Proc. Int. Zurich Symp. EMC*, 1989, pp. 349–354.
[21] M. Honda, "The characteristics of low-voltage ESD and its threat," in *Proc. EOS/ESD Symp.*, 1991, pp. 18–25.



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