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Pulse Regulation Control Technique for Flyback Converter

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***Abstract*—Pulse Regulation, a fixed frequency control technique, is introduced and applied to flyback converter operating in discontinuous conduction mode (DCM). The control parameters are designed in a way that the converter operates as close as possible to the critical conduction mode. In contrast to the conventional pulse width modulation (PWM) control scheme, the principal idea of Pulse Regulation is to achieve output voltage regulation using high and low-power pulses. Pulse Regulation is simple, cost effective, and enjoys a fast dynamic response. The proposed technique is applicable to any converter operating in DCM. However, this work mainly focuses on flyback topology. In this paper, the main mathematical concept of the new control algorithm is introduced and simulation as well as experimental results are presented.**

Keywords-critical conduction mode; DC-DC power converters; discontinuous conduction mode; flyback converter; switch-mode power supplies.

I. INTRODUCTION

Due to high efficiency and high power density as well as reduced costs, switch-mode power supplies (SMPS) are now becoming more popular compared to the linear power supplies [1]. Since the number of semiconductor and magnetic components of flyback converter is less than other SMPS and furthermore, it provides input/output isolation; therefore, this topology perfectly suits off-line low-cost power supply applications.

Flyback converter has been employed operating both in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) as well as critical conduction mode, i.e., at the boundary between CCM and DCM [2], [3]. Critical conduction mode enjoys benefits such as zero current turn-on of the switch and zero current turn-off of the freewheeling diode. These soft switching transitions reduce the switching losses as well at the electromagnetic interference (EMI) noise [4]. Critical conduction mode has less current stress compared to DCM. Furthermore, the transfer function of flyback converter operating in critical conduction mode is first-ordered; thus, the feedback compensation is simplified compared to CCM. However, despite the advantageous benefits of critical conduction mode, its major drawback is the variations of the switching frequency as the output load changes.

This paper introduces Pulse Regulation, a fixed frequency control technique, which regulates the output voltage based on the presence and absence of high-power and low-power pulses and makes the flyback converter operate as close as possible to the critical conduction mode. This control scheme offers a faster dynamic response compared with pulse width modulation (PWM) control method [5]-[7]. Pulse Regulation is simple, cost effective, and robust against the variations of the parameters of the converter.

In this paper, Section II introduces the basic concepts of the new control algorithm. Section III investigates the stability of the proposed control scheme. In Section IV, a comprehensive analysis of the output voltage ripple is presented. Experimental results of applying Pulse Regulation technique on a flyback converter are presented in Section V. Finally, Section VI draws conclusions and presents an overall evaluation of this new control technique.

II. PULSE REGULATION CONTROL SCHEME

Pulse Regulation control algorithm achieves output voltage regulation based on generating high and low-power pulses, rather than employing PWM control technique. If the output voltage is lower than the desired level, the controller chooses D_H to be the duty ratio and therefore, high-power pulses are generated sequentially until the desired voltage level is reached. On the other hand, if the output voltage is higher than the desired level, instead of generating the high-power pulses, the controller chooses D_L ($D_L<D_H$) to be the duty ratio and hence, low-power pulses are generated to descend the level of the output voltage. Fig. 1 depicts the block diagram of the Pulse Regulation control technique. Due to the longer on time of the switch during a high-power pulse, compared to a low-power pulse, more power will be delivered to the load. The switching frequency is constant and D_H is chosen in a way that the converter operates in DCM but as close as possible to the critical conduction mode. Critical conduction mode occurs when the input voltage is at its maximum level. k, the ratio between duty cycle of the switch in a high-power cycle D_H and duty cycle of the switch in a low-power cycle D_L, is chosen by making a compromise between the output voltage ripple and the power regulation range from full load to low load.

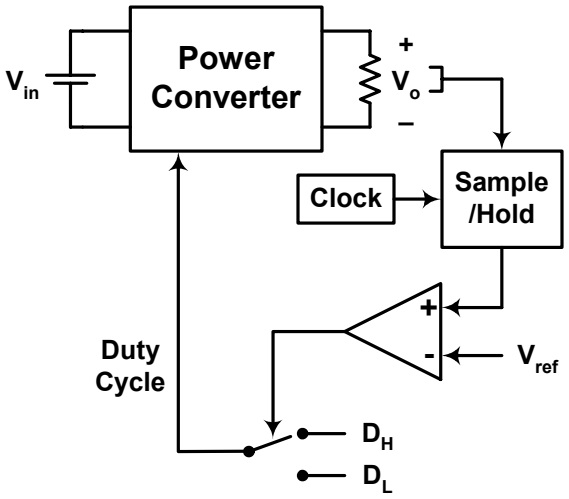

Figure 1. Block diagram of Pulse Regulation control scheme.

Considering a flyback converter, Fig. 2 depicts the current waveform of the magnetizing inductance of the transformer L_m after Pulse Regulation is being applied. At the beginning of each switching cycle, output voltage is being sampled and based on the difference of the measured sample of the output voltage with the desired voltage level, Pulse Regulation controller decides whether a high-power or a low-power cycle needs to be generated. Since the input current ramps linearly with the on-time of the switch, the amount of energy that is drawn from the input power source in a high-power cycle is equal to:

$$\Delta E_{in,HP} = \frac{(V_{in}T)^2}{2L_m} D_H^2 , \quad (1)$$

while the amount of energy that is drawn from the input power source in a low-power cycle is equal to:

$$\Delta E_{in,LP} = \frac{(V_{in}T)^2}{2L_m} D_L^2 = \frac{\Delta E_{in,HP}}{k^2} . \quad (2)$$

Therefore a low-power pulse transfers just $1/k^2$ time as much energy as a high-power pulse. Output voltage sampler and the driver of the switch of the converter are synchronized, therefore the switching frequency is constant and the output voltage is being sampled only once during each switching period.

Fig. 3 shows the simulation results of applying this control method on a flyback converter with parameters defined in Table I. For this specific value of the output power demand, the control scheme generates two high-power pulses and one low-power pulse in each regulation cycle. Since the input voltage is not at it's maximum level, the current of the magnetizing inductor is slightly operating in DCM.

III. Stability Analysis

Considering a general switching period, as shown in Fig. 4,

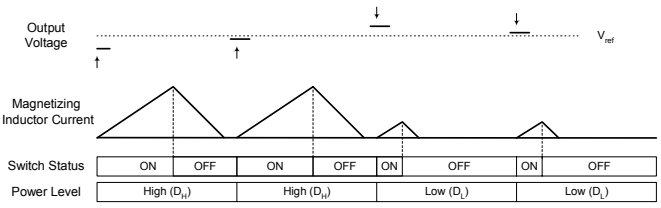

Figure 2. High and low-power pulse cycles.

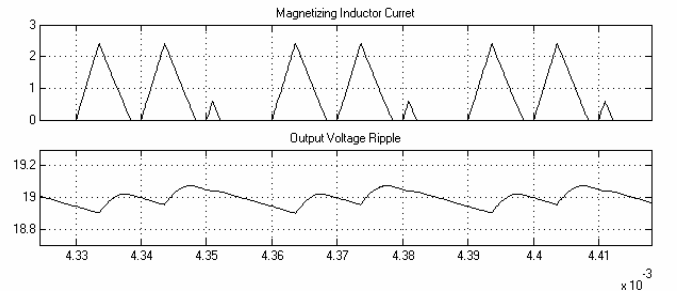

Figure 3. Simulation results of the Pulse Regulation control of flyback converter; (top) magnetizing inductor current (A) and (bottom) output voltage ripple (V) vs. time (sec).

TABLE I. Definition of Variables

Variable	Definition	Value
L_m	Magnetizing inductance	225 µH
C	Output filter Capacitance	100 µF
R	Load resistance	-
V_{in}	Input voltage	150 V
V_{ref}	Output voltage reference	19 V
D_H	Duty cycle of a high-power pulse	-
D_L	Duty cycle of a low power pulse	-
T	Switching period	-
k	D_H / D_L	4
n	transformer turns ratio	6

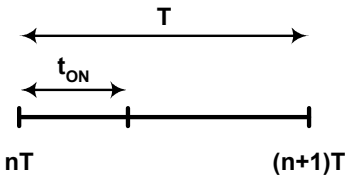

Figure 4. A general switching period.

and based on the energy conservation rule in either a high or a low-power pulse, one can write:

$$\Delta E_{in} = \Delta E_{L_m} + \Delta E_C + \Delta E_{Load} , \quad (3)$$

where ΔE_{in} is the amount of energy that has been drawn from the input power source during the considered switching period. ΔE_{Lm} is the difference of the energy stored in the magnetizing

inductance of the transformer and is equal to zero since L_m de-energizes at the end of each switching period. ΔE_C is the change of the energy stored in the output capacitor during the same switching period, which can be described as:

$$\Delta E_C = E_{C,(n+1)T} - E_{C,nT} \,. \tag{4}$$

And finally, ΔE_{Load} is the amount of energy delivered to load R during the same period. Output capacitor C provides the load current; hence, we can write:

$$\Delta E_{Load} = \frac{1}{R} \cdot \int_{nT}^{(n+1)T} V_C^2 \cdot dt \,. \tag{5}$$

In (5), using the trapezoidal rule instead of integration, we can approximate ΔE_{Load} as:

$$\Delta E_{Load} \cong \frac{T}{2R}\left(V_{C,(n+1)T}^2 + V_{C,nT}^2\right). \tag{6}$$

Moreover, the energy stored in a capacitor at each instant is equal to the squared value of the voltage that appears across the capacitor divided by twice the value of the capacitor; hence, (6) can be rewritten as:

$$\Delta E_{Load} \cong \frac{T}{RC}\left(E_{C,(n+1)T} + E_{C,nT}\right). \tag{7}$$

Substituting (4) and (7) into (3) and solving for the energy stored in the output capacitor at the end of the desired switching period, one obtains:

$$E_{C,(n+1)T} = M \cdot E_{C,nT} + \frac{1}{1+T/RC}\Delta E_{in}, \tag{8}$$

where

$$M = \frac{1-T/RC}{1+T/RC} < 1 \,. \tag{9}$$

Equation (8) shows the recursive relation of the energy stored in the output capacitor as a function of circuit parameters. We need to note that M is always less than one; therefore, the converter is stable under any pattern of high and low-power pulses in the closed loop system. Using the input current, ΔE_{in} can be described as:

$$\Delta E_{in} = E_{L_m,nT+t_{on}} - E_{L_m,nT} \,, \tag{10}$$

where, for a high-power pulse, we have:

$$\Delta E_{in,HP} = 0.5V_{in}^2\left(D_H T\right)^2 / L_m \,, \tag{11}$$

and for a low-power pulse, we have:

$$\Delta E_{in,LP} = 0.5V_{in}^2\left(D_L T\right)^2 / L_m = \Delta E_{in,HP} / k^2 \,. \tag{12}$$

Therefore, in the closed loop control system, the controller makes the decision of generating a high or low-power pulse, such that:

$$\begin{aligned} &V_{out} < V_{ref} \Rightarrow \Delta E_{in} = 0.5V_{in}^2\left(D_H T\right)^2 / L_m \qquad high-power\ pulse \\ &V_{out} > V_{ref} \Rightarrow \Delta E_{in} = 0.5V_{in}^2\left(D_L T\right)^2 / L_m \qquad low-power\ pulse \end{aligned} \tag{13}$$

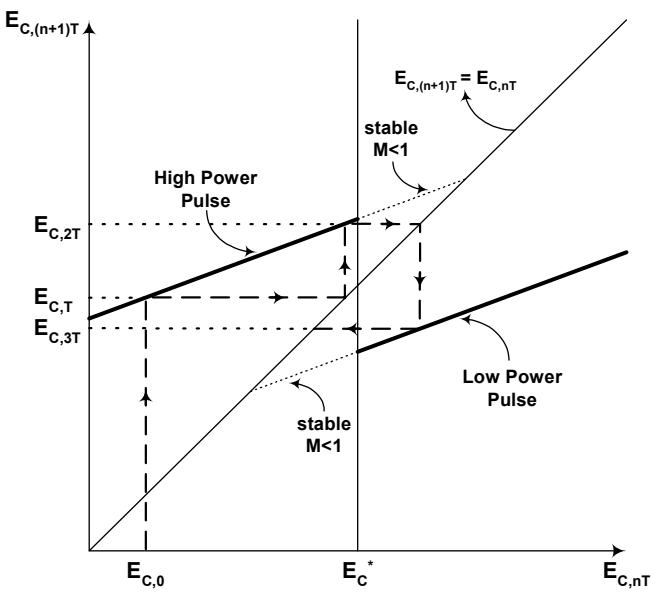

Figure 5. Sequential evolution of high and low power pulses.

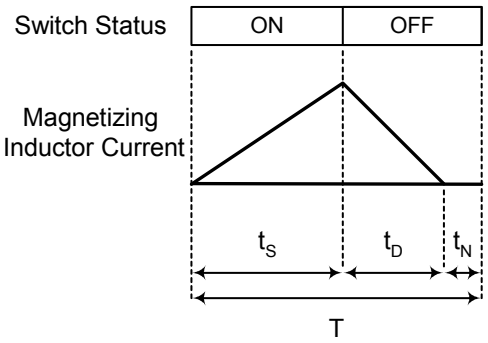

Figure 6. Switching period of a high power cycle.

An example of the time-evolution of the sequence of high and low power pulses, in a closed loop system and based on (8) and (13), is depicted in Fig. 5. In this figure, based on the initial value of the output voltage, two high-power pulses followed by a low-power pulse are generated. The closed loop system is stable under any conditions of the initial energy stored in the output capacitor. In Fig. 5, the energy level corresponding to V_{ref} is depicted as E_C^* and is equal to:

$$E_C^* = 0.5CV_{ref}^2 \,. \tag{14}$$

IV. Output Voltage Ripple

Stability analysis does not determine the output voltage ripple. Hence, the circuit differential equations need to be solved to predict the output voltage ripple. Fig. 6 depicts the switching period of a high-power cycle. The new notations that will be used are; $t_S = t_{on}$ is the time period in which the switch is on, t_D is the time period during which the diode conducts and

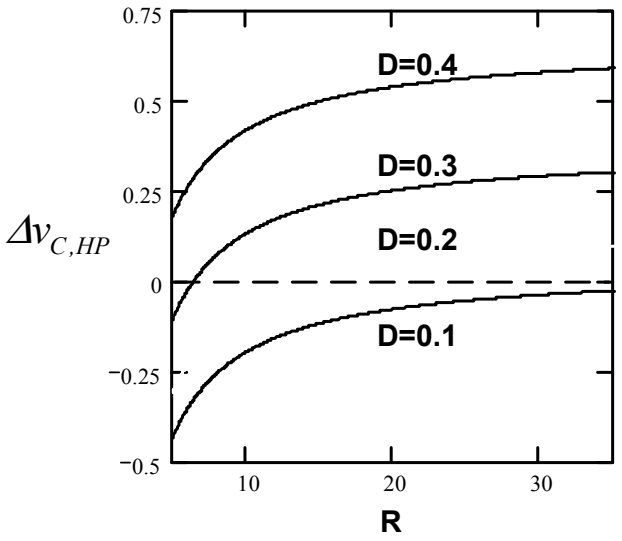

Figure 7. $\Delta v_{C,HP}$ as a function of load for different values of D_H.

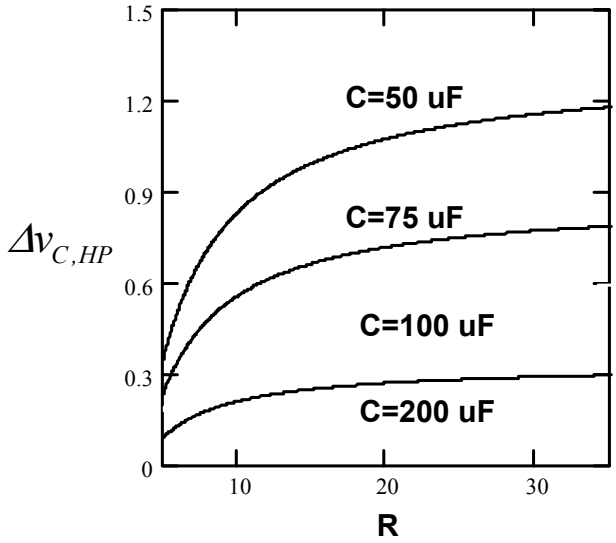

Figure 8. $\Delta v_{C,HP}$ as a function of load for different values of output capacitor C.

$t_N = t_{off} - t_D$ the time period in which both the switch and diode are off.

During time intervals t_S and t_N, diode D is off, hence the output capacitor discharges through the load and the output voltage decreases. In a high-power cycle, assuming that the output voltage is at its desired level $V_o=V_{ref}$, the changes of the output voltage can be written as:

$$\Delta v_{C(-)} \cong -\frac{V_{ref}}{RC}(t_S + t_N) = -\frac{V_{ref}}{RC}(T - \frac{D_H T}{n}\frac{V_{in}}{V_{ref}}) \cdot \quad (15)$$

During time interval t_D, diode D conducts and charges the output capacitor, hence the output voltage increases. Assuming that the magnetizing current decreases linearly and the output voltage variation is small, the increase of the output voltage during on time of the diode t_D can be obtained solving the related differential equation and is equal to:

$$\Delta v_{C(+)} \cong A(e^{-\frac{t_D}{RC}} - 1) - \frac{n^2 R}{L_m} V_{ref} t_D, \quad (16)$$

where $A = V_{ref} - \frac{nRD_H T}{L_m} V_{in} - \frac{n^2 R^2 C}{L_m} V_{ref}$ and $t_D = \frac{D_H T}{n}\frac{V_{in}}{V_o}$.

The total changes of the output voltage after applying a high-power pulse is the summation of the above two extracted values and can be estimated as:

$$\begin{aligned}\Delta v_{C,HP} &\cong \Delta v_{C(-)} + \Delta v_{C(+)} \\ &\cong \left(V_{ref}(1 - \frac{n^2 R^2 C}{L_m}) - V_{in}\frac{nRD_H T}{L_m} \right) \exp(-\frac{D_H T V_{in}}{nRCV_o}) \\ &\quad + V_{ref}(\frac{n^2 R^2 C}{L_m} - \frac{T}{RC} - 1) + V_{in}\frac{D_H T}{nRC}\end{aligned} \quad (17)$$

Equation (17) depicts how different circuit parameters involve in the generation of output voltage ripple. Fig. 7 sketches $\Delta v_{C,HP}$ as a function of the load resistance for different values of D_H. As a high-power pulse, we expect to have positive values of $\Delta v_{C,HP}$ for the entire load range. Therefore, $D_H>0.35$ are good choices for the value of duty cycle in a high-power pulse. As the value of D_H decreases, the functionality of high-power pulses deteriorates and gets similar to a low-power pulse. In order to be in the DCM operating condition, the maximum value of D_H is determined by this equation:

$$D_{H,max} \le \frac{nV_{ref}}{nV_{ref} + V_{in,max}}. \quad (18)$$

Fig. 8 depicts $\Delta v_{C,HP}$ as a function of load resistance R for different values of output capacitor C. Choosing the right value of output capacitor provides the desired range of output resistance in which output voltage regulation is attainable.

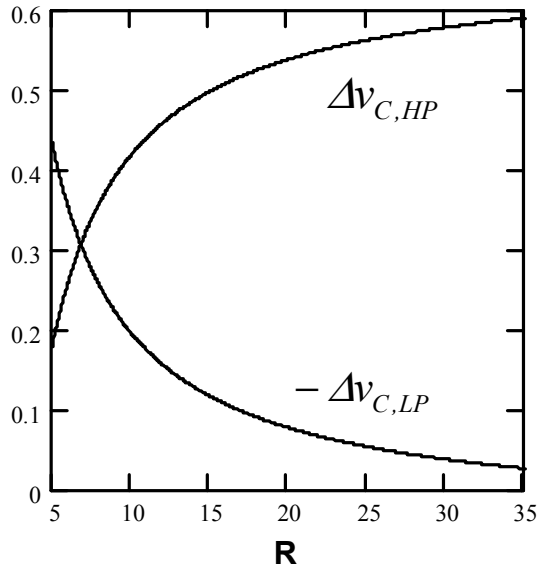

Figure 9. $\Delta v_{C,HP}$ and $-\Delta v_{C,LP}$ as functions of load resistance.

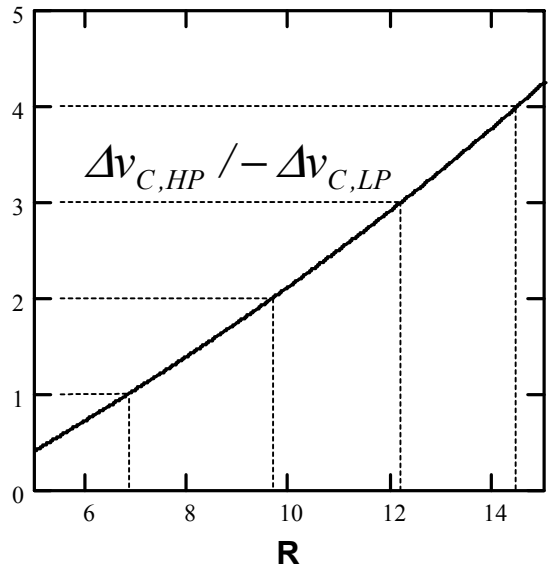

Figure 10. $\Delta v_{C,HP}/-\Delta v_{C,LP}$ as functions of load resistance.

Continuing the same procedure for a low-power cycle, with duty ratio equal to D_L, we can easily obtain that the total changes of the output voltage after applying a low-power pulse is equal to:

$$\Delta v_{C,LP} \cong \left(V_{ref}(1-\frac{n^2R^2C}{L_m}) - V_{in}\frac{nRD_LT}{L_m} \right) \exp(-\frac{D_LTV_{in}}{nRCV_o}) + V_{ref}(\frac{n^2R^2C}{L_m} - \frac{T}{RC} - 1) + V_{in}\frac{D_LT}{nRC} \quad (19)$$

$\Delta v_{C,HP}$ and $-\Delta v_{C,LP}$, for the parameters defined in Table I, as functions of the load resistance are sketched in Fig. 9. As we can observe, the control scheme tries to regulate the output voltage by generating the right number of high-power and low-power pulses in each regulation cycle. As the output power increases, $\Delta v_{C,HP}$ decreases; but $-\Delta v_{C,LP}$ increases. This fact implies that, in each regulation cycle at a higher output power level, the control strategy prefers to have more high-power pulses rather than low-power pulses and vice versa in light loads. The value of the output load resistance at which the two graphs cross each other is the value of the load resistance, which requires one high-power pulse associated with one low-power pulse in each regulation cycle. $\Delta v_{C,HP}/-\Delta v_{C,LP}$ as a function of load resistance is shown in Fig. 10. As the value of the load resistance increases the ratio of $\Delta v_{C,HP}/-\Delta v_{C,LP}$ increase as well. Using Figs. 9 and 10, the patterns of high and low power pulses in a regulation cycle for a specific value of the load resistance can be extracted. Table II shows some examples of this case.

According to Table II, for instance, when R=12.2, we have $\Delta v_{C,HP} \approx 3 * -\Delta v_{C,LP}$ which predicts for this value of load, in each regulation cycle, the controller generates three low-power pulses associated with each high-power pulse. Therefore, first

TABLE II. HIGH AND LOW POWER PATTERN PREDICTION IN ONE REGULATION CYCLE

R	$\Delta v_{C,HP}$	$-\Delta v_{C,LP}$	Predicted Pattern
19.3	0.533	0.082	1*HP - 7*LP - 1*HP - 6*LP
14.5	0.492	0.123	1*HP - 4*LP
12.2	0.461	0.154	1*HP - 3*LP
6.83	0.307	0.307	1*HP - 1*LP
5	0.179	0.434	3*HP - 1*LP - 2*HP - 1*LP

we calculate $\Delta v_{C,HP}$ and $-\Delta v_{C,LP}$ ((17) and (19)) associated with each value of R, then we find two integers as this equation holds.

$$\alpha * \Delta v_{C,HP} = \beta * -\Delta v_{C,LP} \quad (20)$$

where α and β represent the number of high-power and low-power pulses in each regulation period. In a high-power cycle, we can express the average value of the diode current as:

$$\overline{i_{D,HP}} = \frac{V_{in}^2 D_H^2 T}{2nV_o L_m}. \quad (21)$$

The on time of the switch during a low-power pulse is $1/k^{th}$ of the on time of the switch in a high-power pulse and, hence, for a low-power pulse, we can write:

$$\overline{i_{D,LP}} = \frac{\overline{i_{D,H}}}{k^2} = \frac{V_{in}^2 D_H^2 T}{2nV_o L_m}. \quad (22)$$

In the steady state operation, if there are α high-power pulses associated with β low-power pulses in each regulation cycle, then the average value of the diode current is:

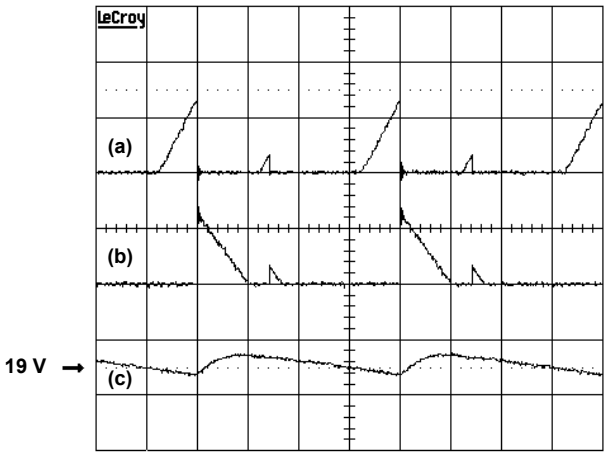

Figure 11. Experimental results of (a) input current (2 A/div), (b) secondary current of transformer (6 A/div), and (c) output voltage ripple (0.1 V/div) vs. time (5 μs/div).

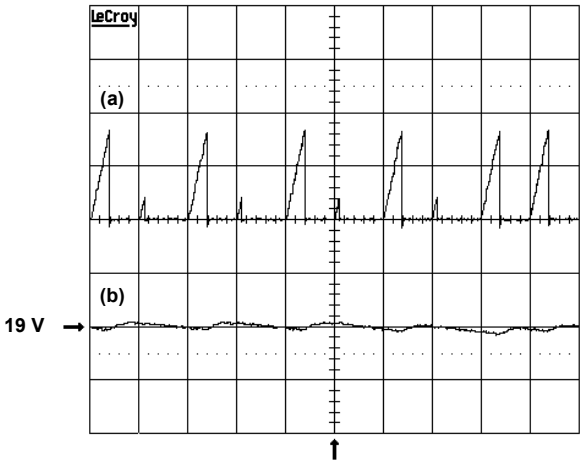

Figure 12. Experimental results of applying a step load change; (a) input current (2 A/div) and (b) output voltage ripple (0.5 V/div) vs. time (10 μs/div).

$$\overline{i_D} = \frac{\alpha * \overline{i_{D,HP}} + \beta * \overline{i_{D,LP}}}{(\alpha + \beta)T}. \quad (23)$$

By noting that $\overline{i_D} = V_o/R$ and, by solving for the load resistance, one obtains:

$$R = \frac{2nL_m k^2}{D_H^2} \frac{V_o^2}{V_{in}^2} \frac{(\alpha + \beta)}{(\alpha k^2 + \beta)}. \quad (24)$$

Equation (24) shows how different parameters like input voltage, output voltage, output load resistance, D_H, and k affect the pattern of high and low power pulses. This equation is being used through the design procedure.

V. Experimantal Results

Using the derived formulation in the previous section, a 90W prototype DC-DC flyback power supply with V_{in}=135~165V, V_o=19V, and switching frequency of 100 KHz was designed and developed.

Fig. 11 depicts the experimental results of the primary and secondary currents of the transformer as well as the output voltage ripple. In this figure, one low-power pulse follows each high-power pulse. Fig. 12 depicts the experimental results of the input current and output voltage ripple for a 30% to 65% step load change. The vertical arrow specifies the instant at which the step change is applied. As we can observe, the pattern of high and low power pulses changes after the step load change and more high power pulse will be generated upon load demand. The transient response of Pulse Regulation is so fast that no disturbance at the output voltage can be observed after the load step change.

VI. Conclusion

Flyback power converter has found its way into many applications. To address the challenge of designing a simple controller for this type of converters, this paper introduces the new Pulse Regulation control technique. This control method has several advantages over conventional techniques, such as simplicity, accuracy, and fast transient response. Simulation and experimental results completely match with the theoretical concept.

References

[1] R. E. Locher, "Introduction to power supplies," *National Semiconductor Application Note 556,* Nov. 1988.

[2] P. Lidak, "Critical conduction mode flyback switching power supply using the MC33364," *Motorola Semiconductor Application Note AN 1594.*

[3] G. Spiazzi, D. Tagliavia, and S. Spampinato, "DC-DC flyback converters in the critical conduction mode: a re-examination," in *Proc. IEEE Industry Applications Society Annual Meeting,* Rome, Italy, vol. 4, Oct. 2000, pp. 2426-2432.

[4] "Critical conduction GreenLine SMPS controller," *Tech. Rep. MC33364/D,* Motorola, 1998.

[5] M. Telefus, A. Collmeyer, D. Wong, and D. Manner, "Switching power converter with gated oscillator controller," *US Patent No. 6,275,018*, Assignee: iWatt Corporation.

[6] M. Telefus, D. Wong, and C. Geber, "Operating a power converter at optimal efficiency," *US Patent No. 6,304,473*, Assignee: iWatt Corporation.

[7] M. Telefus, A. Shteynberg, M. Ferdowsi, and A. Emadi, "Pulse Train™, a novel digital control method, applied to a discontinuous conduction mode Flyback converter," in *Proc. IEEE 34th Power Electronics Specialists Conference*, Acapulco, Mexico, June 2003.