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Estimating the Noise Mitigation Effect of Local Decoupling in Printed Circuit Boards

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***Abstract*—Local decoupling, i.e., placing decoupling capacitors sufficiently close to device power/ground pins in order to decrease the impedance of power bus at frequencies higher than the series resonant frequency, has been studied using a modeling approach, a hybrid lumped/distributed circuit model established and an expression to quantify the benefits of power bus noise mitigation due to local decoupling developed. In this work, a test board with a local decoupling capacitor was studied and the noise mitigation effect due to the capacitor placed adjacent to an input test port was measured. Closed-form expressions for self and mutual inductances of vias are developed, so that the noise mitigation effect can then be estimated using the previously developed expression. The difference between the estimates and measurements is approximately 1 dB, which demonstrates the application of these closed-form expressions in the PCB power bus designs. Shared-via decoupling, capacitors sharing vias with device power/ground pins, is also modeled as an extreme case of local decoupling.**

***Index Terms*—Closed-form expressions for via inductances, estimation of power-bus noise reduction due to local decoupling, local decoupling, mutual inductance, printed circuit board layer stackup, shared-via decoupling.**

I. Introduction

HIGH-FREQUENCY noise in printed circuit boards (PCBs) results from both simultaneous switching of digital logic within the core, as well as simultaneous switching of device I/O, often referred to as simultaneous switching noise (SSN) and SSO [1]. This high-frequency noise on the dc power bus in PCBs can lead to signal integrity (SI) and electromagnetic interference (EMI) problems. In multilayer PCBs that use entire layers or large area fills for power and ground planes, SI and EMI problems are likely to occur at resonances of the two-dimensional, parallel plate transmission line. The parallel plate structure is designed to have a low impedance, however, a disturbance on the power bus that is initiated by a switching device is easily propagated throughout this low impedance transmission line. This high-frequency noise can couple to a signal transitioning through the power planes [2], or to the power pins of a victim device and contribute to SI problems. For designs with multiple logic levels and power areas on different PCB layers, noise resulting from switching components can easily be coupled among different logic level portions of the design. The high-frequency noise can also be coupled to I/O lines that transition through the power planes and result in EMI problems [2], as well as coupled off the PCB from fringing edge fields. Controlling and mitigating this high-frequency dc power bus noise on a multilayer PCB is a critical aspect of digital design to ensure signal integrity and to reduce the risk of EMI problems.

Critical issues for dc power bus design include:

1) whether to place the power and ground layers on adjacent planes or to sandwich potentially noisy signals between these layers to obtain some "shielding;"
2) whether to locate surface mount technology (SMT) decoupling capacitors close to the IC devices, or to distribute them more uniformly, or globally on the PCB;
3) what values the SMT decoupling capacitors should have;
4) how much total SMT decoupling capacitance is required for a given design.

Approaches that demonstrate the benefits of maintaining closely spaced power and ground layers for minimizing power bus noise have been reported, [3], [4] and are becoming a matter of design experience and practice. SMT decoupling capacitors are commonly used in dc power bus design to mitigate high-frequency noise on the dc power bus [5], [6]. Using the largest value of decoupling capacitor in a given package size is becoming a matter of engineering design practice as well. Quantitative reasons are given for this herein. By contrast, the critical design issues of where to locate SMT decoupling capacitors and how much total SMT capacitance is needed, i.e., how many are required for a specific design, are unresolved questions. While every organization that designs digital electronics has guidelines for "accepted best practices" for these two issues, these guidelines can vary widely. The issue of when locating a decoupling capacitor in proximity to an integrated circuit (IC) can be beneficial is quantified in this paper with regard to estimating the reduction of noise on the parallel plate dc power bus.

Many studies have focused on modeling the power and ground metal layers of the PCB in order to determine the power bus impedance at a specific location. A straight-forward, but fast transmission-line grid method suitable for SPICE implementation demonstrated the distributed behavior and impact of resonances on a parallel-plane power bus [7]. A similar analytical approach using a transmission-line model has also been reported [8]. Full-wave methods have been used as well to model the power/ground layer pair, including FEM [9], partial element equivalent circuit (PEEC) [10], [11], and finite difference time domain (FDTD) [12]. In addition, an analytical method based on the cavity-mode theory developed for microstrip patch antenns [13], has been applied for determining the input impedance and transfer impedance for the

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dc power bus parallel planes [14], [15]. Printed substrates are easily modeled using FDTD [16], including parallel planes.

SMT decoupling capacitors can be included as lumped circuit elements when extracting a network using the cavity theory. PEEC modeling that included numerous capacitors incorporated as lumped elements and uniformly distributed over a mutlilayer PCB agreed well with experimental studies [11]. For decoupling capacitors not placed in proximity to a device, including the capacitor and its interconnect to the power bus as a lumped element in the modeling can be effective. However, when a decoupling capacitor is in proximity to the IC power or ground pins, including it as a lumped element fails to capture the essential physics of the magnetic field coupling between the IC and SMT capacitor vias. This coupling results from the magnetic flux linkage of the current on the two vias between the power and ground planes [17]. Full-wave modeling that includes the vias and planes is necessary to adequately detail the effects that are necessary for quantifying the effect of an SMT decoupling capacitor located in proximity to an IC. Previous studies demonstrated the use of FDTD modeling for including the dispersive effects of FR-4 (glass/epoxy commonly used for PCBs) and the decoupling capacitors with their interconnect vias [18]. PEEC modeling using a layered media Greens function has also been used that included the loss in FR-4 as well as the decoupling capacitors and via interconnects [19]. This work presented curves demonstrating the reduction of the transfer impedance on the dc power bus for certain cases when an SMT capacitor was located close to a noise injection port. While all of these studies provided valuable insight into the essential physics and direction for good modeling of a parallel plane dc power bus, design equations for evaluating the effectiveness of an SMT decoupling capacitor located in proximity to an IC were not provided. Design equations for evaluating the effectiveness of a decoupling capacitor as a function of the spacing between power and ground layers, proximity of the SMT capacitor to the IC and the interconnect inductance to the SMT capacitor are developed in this paper.

An expression for determining the noise reduction impact of local decoupling, i.e., a capacitor placed in proximity to an IC device is developed in Section II in terms of the ratio of portion of the SMT capacitor interconnect inductance above the power ground planes to that between the planes and the mutual coupling between the SMT capacitor and IC vias. This equation is frequency independent, i.e., indicating that the local decoupling capacitor is effective well beyond its series resonant frequency. The frequency independent behavior is demonstrated experimentally in Section III, as well as comparing modeling with the measurements. Closed-form expressions to evaluate the necessary inductances and mutual coupling parameter are given in Section IV. The local decoupling behavior is shown and discussed for three different classes of board geometries in Section V and the closed form expressions compared with full-wave modeling. Finally, dc power bus design implications are discussed in Section VI.

II. Power Bus Noise Reduction Due to Local Decoupling

Local decoupling capacitors, i.e., SMT decoupling capacitors placed adjacent to the power/ground pins of IC devices, can be beneficial in mitigating high-frequency power bus noise. Local decoupling capacitors can be effective up to the gigahertz range. Global decoupling capacitors, which can be effective to frequencies as high as 200 MHz, are restricted by the parasitic inductances associated with the interconnects and package of the capacitors. This work addresses the reduction of noise transmission from a noise source switching circuit (IC) to a receptor point on the PCB power bus by examining the performance of SMT decoupling capacitors on the PCB. This work does not address the reduction of the noise source itself (the IC switching circuit), which can depend on the package inductance of the IC.

TABLE I
Parameter Description for (1)

L_2	the portion of the self inductance of the via between the power/ground planes associated with the local decoupling capacitor;
L_3	the remaining inductance of the interconnect to the local capacitor package and its parasitics;
M	the mutual inductance between the two vias associated with the local decoupling capacitor and its adjacent IC device;
Z'_{11}	the distributed input impedance for the power bus structure excluding the local decoupling capacitor and the IC device, when the output port is open. The input port is where the local capacitor/IC pair is located.

This noise mitigation effect of local decoupling was modeled using a mixed-potential integral equation formulation with circuit extraction [19]. It was found that, as compared to the cases without local decoupling, the inclusion of local decoupling decreased the $|Z_{21}|$ between two ports on the power bus and this $|Z_{21}|$ decrease was approximately frequency-independent from 100 MHz to 2 GHz. A hybrid lumped/distributed circuit model was established from physics and a closed-form expression was developed to characterize this phenomenon as

$$|Z_{21}|\text{decrease(dB)} = 20^* \log_{10}\left[\frac{j\omega\,(L_2 + L_3 - M)}{j\omega\,(L_2 + L_3) + Z'_{11}}\right] \quad (1)$$

where the parameters L_2, L_3, M and Z'_{11} are detailed in Table I. Note that L_2 also includes the power/ground plane inductance. For a large power/ground plane pair, the inductance due to the flux wrapping the planes is negligible [20]. However, currents in the planes congest in the vicinity of vias, resulting in extra "plane" inductance [21]. The inductance is included into the via inductance herein, since it results from the vias. As demonstrated in [19], it is typically the case that $|Z'_{11}| \ll \omega(L_2 + L_3)$ for a PCB dc power bus structure. Therefore, (1) can be approximated as

$$|Z_{21}|\,\text{decrease(dB)} \approx 20^* \log_{10}\left(\frac{L_2 + L_3 - M}{L_2 + L_3}\right). \quad (2)$$

Notice that, in (2), the approximate $|Z_{21}|$ decrease is independent of frequency, which is consistent with the modeled results observed in [19]. This frequency-independent behavior makes it possible to quantify the local decoupling benefits using a simple $|Z_{21}|$ decrease value. Design curves have been generated from modeling to relate the average $|Z_{21}|$ decrease to capacitor/IC spacing and power/ground layer separation in [19].

Via diameters in typical PCB designs are usually constant across the PCB, which means that the self inductances associated with the decoupling capacitor via and its adjacent device

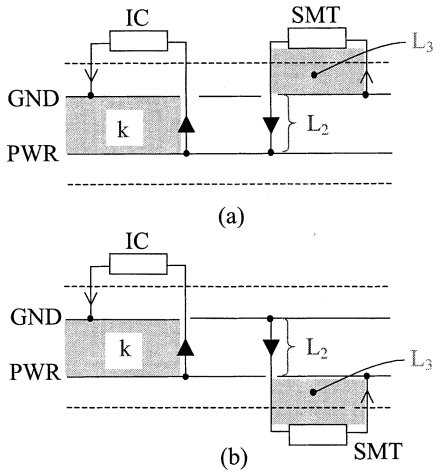

Fig. 1. Schematic representation of the physics associated with the decoupling effect and the lumped circuit element parameters for (a) the SMT decoupling capacitor on the same side of the board and (b) on opposite sides of the board.

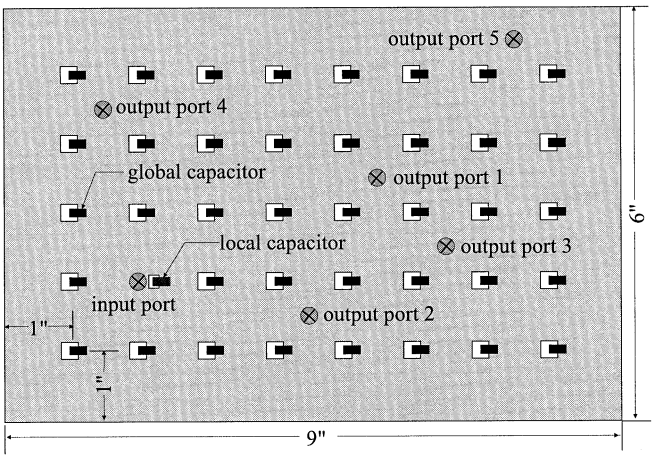

Fig. 2. Test board geometry (top view).

power/ground pin via are approximately the same. Therefore, the mutual inductance between them, M, can be approximated as $M \approx kL_2$, where k is the coupling coefficient, and the mutual inductive coupling between the loop portions outside the power/ground pin via is neglected. In this case, (2) can be further simplified as

$$|Z_{21}|\,\text{decrease(dB)} \approx 20^* \log_{10}\left[\frac{L_2(1-k)+L_3}{L_2+L_3}\right] = 20^* \log_{10}\left[\frac{(1-k)+\left(\frac{L_3}{L_2}\right)}{1+\left(\frac{L_3}{L_2}\right)}\right]. \quad (3)$$

The potential benefits of local decoupling can then be extracted from (3). In particular the relevant factors are the mutual coupling between the local decoupling capacitor and IC vias and the ratio of the portion of the interconnect inductance above the planes, relative to that in the planes. The portion of the inductance above the planes represented by L_3 is comprised of both the portion of the capacitor via above the power/ground plane pair and interconnect trace and the equivalent series inductance (ESL) of the capacitor. In (3), the mutual inductance between the local decoupling capacitor via above the power planes and the IC interconnect above the planes is neglected. While this can easily be accounted for by splitting M into the two components, the mutual inductance between the planes will be dominant. When it is not dominant, the ratio of L_3/L_2 is greater than one and little benefit from local decoupling can be achieved.

The mutual coupling physics and the associated lumped element parameters are illustrated schematically in Fig. 1. In the development of (3), the mutual coupling between the local decoupling capacitor and IC vias occurs between the power and ground plane pair to which the components are attached and the coupling is between the current segments of each component that penetrate through the plane and connect to the plane opposite the component [19]. Referring to Fig. 1(a) for example, if both the capacitor and IC are located on the same side of the board and the ground layer is the closest layer toward the components in the power/ground plane pair, then the mutual inductance that is being exploited for the local decoupling effect is between the power pins of each component, which penetrate the ground plane and connect to the lower power plane. The portions of the physical layout associated with the lumped circuit model are also illustrated in Fig. 1.

The modeling approach used to characterize L_2, k, and L_3 in this work is denoted *c*ircuit *e*xtraction approach based on a *m*ixed-*p*otential *i*ntegral *e*quation (CEMPIE) and is a formulation [22]. It is a PEEC method applied to a general multilayer dielectric medium [23]. In the CEMPIE modeling, Rao-Wilton Glisson (RWG) triangular patches were used to model the planar metallization surfaces [24], rectangular patches were used to model the vertical via interconnect and mixed basis functions at the via/plane junction were used to ensure current continuity [22]. In this manner, all aspects of the geometry were considered in order to evaluate the constituent factors in (3).

III. Test Board Geometry and Results

A test board was built to verify the results from modeling reported in [19]. It was a two layer PCB with the top layer shown in Fig. 2 and its bottom layer was a solid copper ground. The dielectric layer was ordinary FR-4 (Fiberglass/expoy) material with a dielectric constant of $\varepsilon_r = 4.5$, loss tangent of $\tan\delta = 0.02$ and a thickness of 44 mils. As shown in Fig. 2, 39 global SMT decoupling capacitors were uniformly placed on the board on a 1 in grid. One end of each capacitor was soldered to the top layer, while the other end was connected to the bottom layer through a via. All via diameters were 20 mil. An input port, made from semi-rigid coaxial cable and an SMA connector, was located on the board with a spacing from the left and bottom edges equal to 2 in. A local SMT decoupling capacitor was added to the right of the input port and the spacing between the via walls of the input port and the local capacitor was varied from 50 to 500 mil. Five output ports, with the same geometry as the input port, were placed such that the peak and null locations of the low-order board resonances could be avoided. The decoupling capacitors placed on the board were 0805 package size SMT capacitors. One of them was measured using an Agilent 4291A Impedance Analyzer. The measured ESL, equivalent

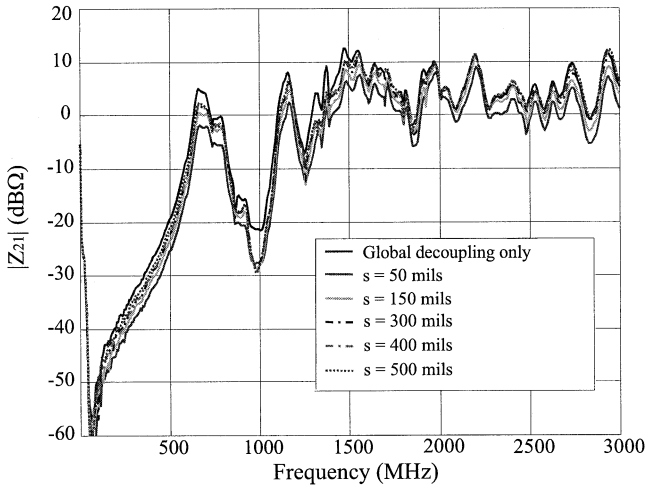

Fig. 3. Measured $|Z_{21}|$ averaged over the five output ports for the test board shown in Fig. 2.

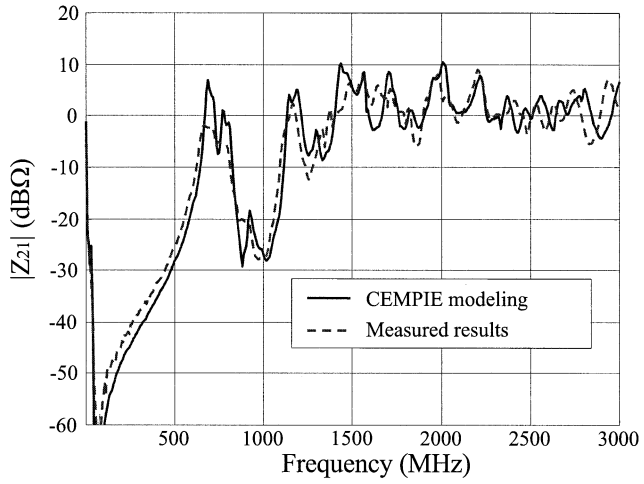

Fig. 4. Comparison between the CEMPIE modeling and the measured results for the test board shown in Fig. 2.

series resistance (ESR), and capacitance values were 0.5 nH, 85 mΩ, and 7.3 nF, respectively.

The S-parameters between the input and an output ports were measured and transformed to a corresponding $|Z_{21}|$ [25]. An Agilent 8753D Network Analyzer was used in the measurements. The 12-term calibration procedure was performed using an open, short and load. Reference planes were rotated from the calibration planes to the test port terminals looking into the PCB. The $|Z_{21}|$ results, which were averaged over the five output ports, are shown in Fig. 3, where they are compared with the case with only 39 global decoupling capacitors placed on the board. The CEMPIE modeling for the case of 39 global decoupling capacitors plus one local decoupling capacitor located at $s = 50$ mils is compared to the measured results in Fig. 4. In general, the agreement between the measurements and modeling is good. The discrepancies are due in large part because of the construction by hand of the board. The capacitors were mounted by hand soldering and the via connections made with wires inserted into drilled holes. Also, only one SMT capacitor component was characterized for ESL, ESR, and capacitance and these values used for modeling every capacitor.

TABLE II
CALCULATED AVERAGE $|Z_{21}|$ DECREASES (IN DECIBALS) VERSUS OUTPUT PORT LOCATION AND IC/CAPACITOR SPACING

IC/capacitor Spacing	Port 1	Port 2	Port 3	Port 4	Port 5	Average
50 mils	4.6	4.6	4.5	4.4	4.4	4.5
150 mils	2.5	2.7	2.7	2.4	2.8	2.6
300 mils	1.4	1.7	1.7	1.2	1.5	1.5
400 mils	1.2	1.5	1.5	0.9	1.2	1.3
500 mils	1.0	1.5	1.3	0.6	0.9	1.1

Fig. 3 indicates that adding a local decoupling capacitor decreases the $|Z_{21}|$ over a frequency range from approximately 100 MHz to 3 GHz and that as the IC/capacitor spacing decreases, the $|Z_{21}|$ decreases. Furthermore, the $|Z_{21}|$ decrease is approximately frequency independent over the entire frequency range. The decrease in the $|Z_{21}|$ with regard to the baseline case that only the 39 global decoupling capacitors were present on the board were then calculated and averaged over all frequency points. They are listed in Table II. The values listed in the last column are those averaged over the five different output ports.

IV. CLOSED-FORM EXPRESSIONS FOR INDUCTANCE

According to (3), the average $|Z_{21}|$ decrease due to a local decoupling capacitor can be estimated, if the values of L_2, L_3, and k are known. In the test board shown in Fig. 2, L_3 is approximately the package parasitic inductance of the local SMT decoupling capacitor. In other words, $L_3 \approx 0.5$ nH. In order to calculate L_2 and k, two different approaches were developed.

A. CEMPIE Modeling Approach

L_2 is the self inductance associated with the via portion between the power and ground planes. A general procedure was developed to extract lumped circuit elements based on CEMPIE and a physics-based circuit prototype in [26], where calculation of via inductances in dc power bus structures is an example application of this general procedure [27]. Further, the closed-form expression of the self inductance of a via portion between the power and ground planes in a rectangular power bus, as illustrated in Fig. 5, was derived based on curve-fitting [26]. The derived expression is

$$\begin{aligned} L_2 = & \frac{\left(60893d^2 - 273.622d + 1.952\right)\mu_0 d}{4\pi} \ln\left(\frac{1}{\sqrt{\pi}}\sqrt{\frac{ab}{r}}\right) \\ & \times \left[0.96 + 0.033k_d + 0.007k_d^2\right] \\ & \times \left[1 + \left(\frac{0.0045}{ab} + 0.6\right) xk^{0.4} \right. \\ & \quad \left. + \left(\frac{1.58}{ab} - 11.3\right)\left(\frac{x}{k^{0.05}}\right)^2\right] \\ & \times \left[1 + \left(\frac{0.0045}{ab} + 0.6\right) yk^{0.3} \right. \\ & \quad \left. + \left(\frac{1.58}{ab} - 11.3\right)\left(yk^{0.3}\right)^2\right] \end{aligned} \tag{4}$$

where

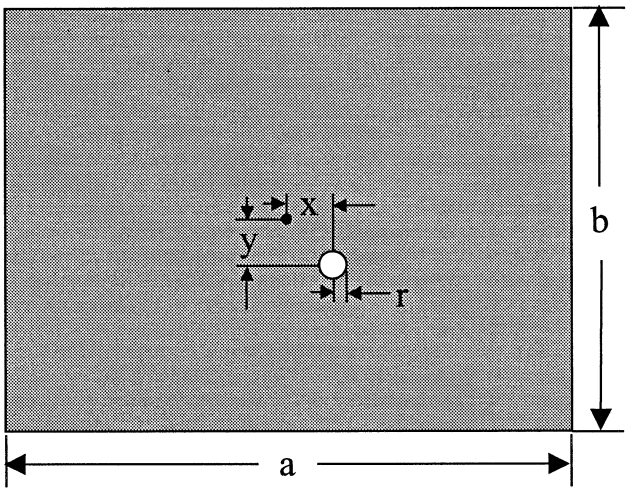

Fig. 5. Via at an arbitrary location in a rectangular power bus.

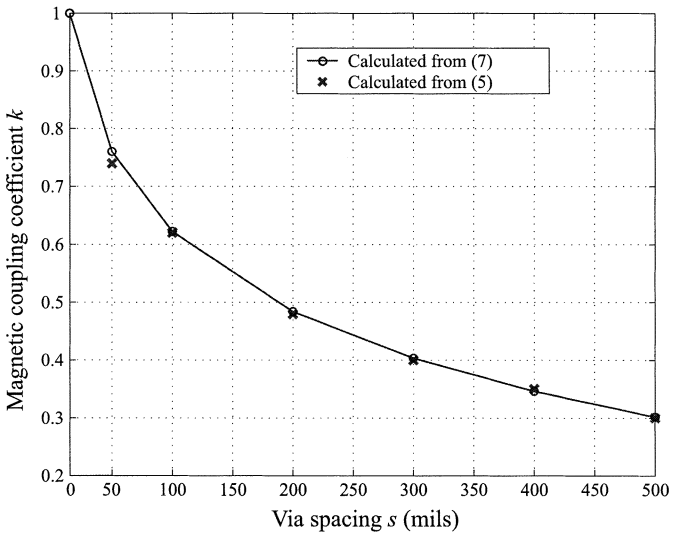

Fig. 6. Magnetic coupling coefficient k as a function of the via spacing.

a, b length of the longer or shorter edge of the rectangular power bus, in meters;
d separation between the power and ground planes, in meters;
x, y distance between the centers of the via and the power bus, in meters;
r radius of the via, in meters;
k_d dimension ratio, $k_d = a/b$;
μ_0 permeability of air.

The coupling coefficient, k, can be extracted from the full-wave CEMPIE modeled results. The $|Z_{21}|$ with and without a local decoupling capacitor can be determined using the CEMPIE modeling approach and the average $|Z_{21}|$ decrease due to the local capacitor calculated. The coupling coefficient k can be solved from (3) as

$$k \approx \frac{L_2 + L_3}{L_2}\left[1 - 10^{|Z_{21}|\text{decrease}(dB)/20}\right]. \tag{5}$$

Then, by determining the $|Z_{21}|$ decrease as a function of the decoupling capacitor via spacing with respect to the IC via, the value of k can be extracted as a function of this spacing. Since the mutual coupling of interest is between the planes, the CEMPIE modeling used to extract k as a function of capacitor/IC spacing was for a two layer structure, where the inductance between the planes was dominant and only a nominal value of ESL for the capacitor was included as the portion for L_3.

B. Simplified Physical Models

Closed-form expressions for L_2 and k can be derived based on physics and some approximations. First, consider a circular power bus with a via at its center. The radius of the power bus is R and d is the separation between the power and ground planes. The radius of the via is r. If the power bus is sufficiently large, the magnetic field due to a current flowing through the via is approximately inversely proportional to the distance to the center of the via. Then, the self inductance associated with the via can be approximated as

$$L_2 = \frac{\mu_0 d}{2\pi}\left[\ln\left(\frac{R}{r}\right) - 0.75\right] \tag{6}$$

where 0.75 is a factor used to compensate for the edge effects of the finite power bus. For other shapes of power bus, an equivalent R, such as the average distance to the board edges, can be used in (6) to estimate the L_2 value. Specifically, for a rectangular power bus with length a and width b, an approximated R can be

$$R_{\text{rec}} = \frac{a+b}{4}.$$

Similarly, the mutual inductance between two vias can be approximated as

$$M = \frac{\mu_0 d}{2\pi}\left[\ln\left(\frac{R}{s+r}\right) - 0.75\right]$$

where s is the spacing between the two via centers and the two vias are assumed to have the same radius r. If a pair of two closely spaced vias is located in the center of a power bus, the self inductance of each via is approximately the same, provided that $s \ll R$. Then, the coefficient k can be obtained as

$$k = \frac{M}{L_2} = \frac{\left[\ln\left(\frac{R}{s+r}\right) - 0.75\right]}{\left[\ln\left(\frac{R}{r}\right) - 0.75\right]}. \tag{7}$$

Both (6) and (7) were derived based on the assumption that the via/via pair is located in the center of the power bus. However, the change of via inductance in a power bus due to its location has been found to be insignificant in most of the board region, except for the small areas in proximity to board edges [28]. Therefore, (6) and (7) should be sufficiently accurate for many engineering calculations.

The two approaches to calculate the magnetic coupling coefficient k, using CEMPIE modeling and (5) and the analytical expression (7), were applied for the 6 in $\times$ 9 in two-sided modeling geometry shown in Fig. 2. The results using (5) and (7) are compared in Fig. 6. In general, the two equations give comparable results. As suggested by (7), k is not a function of power/ground layer separation and it is not expected to be.

TABLE III
ESTIMATES VERSUS MEASUREMENTS OF THE AVERAGE $|Z_{21}|$ DECREASE DUE TO THE LOCAL DECOUPLING CAPACITOR FOR THE TEST BOARD SHOWN IN FIG. 2

Via spacing	50 mils	150 mils	300 mils	400 mils	500 mils
Measured average |Z21| decrease (dB)	4.5	2.6	1.5	1.3	1.1
Calculated average |Z21| decrease* (dB)	5.3	3.4	2.3	1.9	1.6
Calculated average |Z21| decrease** (dB)	5.9	3.7	2.5	2.0	1.7

* L2 was calculated from (6);
** L2 was calculated from (4).

C. Estimation With the Developed Expressions

With the developed closed-form expressions for L_2 and k, the average $|Z_{21}|$ decrease due to a local decoupling capacitor was estimated for the test board shown in Fig. 2 using (3), where $L_3 \approx 0.5$ nH as discussed before. The L_2 values using (4) and (6) were 1.51 and 1.18 nH, respectively. The coupling coefficient k was obtained from (7). The calculated and measured results are compared in Table III. The difference between the measured and estimated results is approximately 1 dB for all cases. This difference is due in part to the assumption in (3) that $Z'_{11} = 0$ and partly due to possible measurement errors. However, the estimated results are sufficiently accurate for typical engineering designs.

V. DISCUSSION

In (3), L_3 is a portion of the self inductance associated with the local decoupling capacitor. It is the inductance of the interconnects above the power/ground layer to the capacitor package plus the package parasitic inductance as illustrated in Fig. 1. In the two-sided test board, L_3 was the package parasitic inductance only. However, in practical multilayer PCB designs, L_3 will also typically include additional interconnect inductance. The effects of this L_3 value on local decoupling benefits will be discussed further in this section. The limiting case for local decoupling is to let the decoupling capacitor share a common via with the IC power or ground pin. In that case, the via spacing s is zero and, the maximum mutual inductive coupling is achieved. This will be also discussed in this section.

A. Modeling Multiple Layers Using CEMPIE

The previously reported CEMPIE results were all for the two-layer boards with one solid ground that was included in the calculation of Green's functions in the modeling and one power/signal layer that was meshed using RWG triangular patches. The multilayer Green's functions are general and can handle multiple power/signal layers [2]. As an example, a test board with two connected power areas on different layers was modeled with CEMPIE. The three-layer board had a dimension of 8 cm $\times$ 5 cm, as shown in Fig. 7. The entire bottom layer was used as the ground plane. There was a 4.3 cm $\times$ 5 cm power area (PWR1) on the left top layer; and another power area (PWR2) with a dimension of 4.1 cm $\times$ 5 cm on the right hand portion of the second layer. A via at (40, 25) mm from the lower left corner connected the two power areas. The layer spacing was 45 mils and the total board thickness was 90 mils. The relative dielectric constant of the board material was $\varepsilon_r = 4.5$. Two test ports were placed on the test board

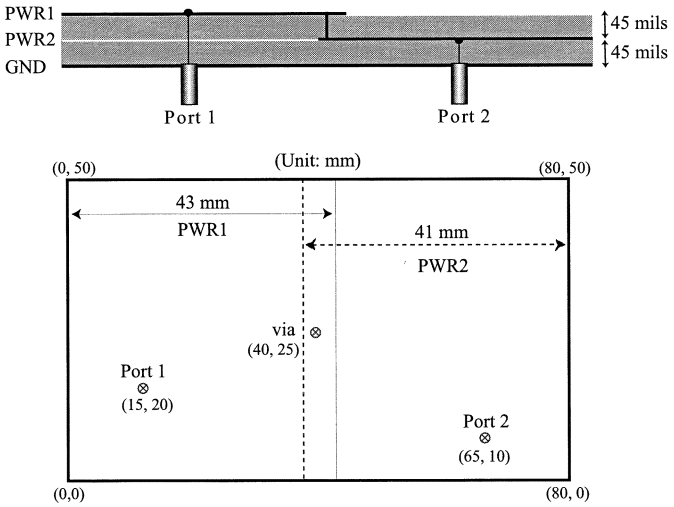

Fig. 7. Test board with two connected power areas on different layers.

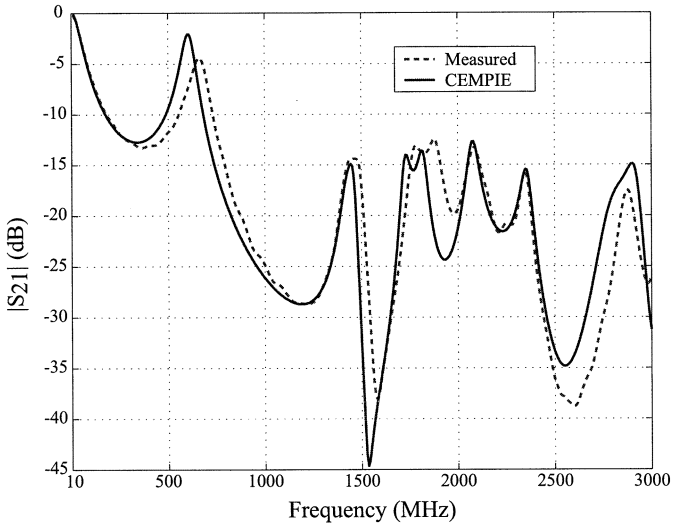

Fig. 8. Modeled and measured $|S_{21}|$ for the test geometry shown in Fig. 7.

with SMA connectors. Port 1 was located at (15, 20) mm and Port 2 at (65, 10) mm from the lower left corner of the board. Ports 1 and 2 were connected to the PWR1 and PWR2 power areas, respectively. The center conductors of these ports had a diameter of 50 mils. The $|S_{21}|$ between the two ports was measured with an Agilent 8753D Network Analyzer and modeled using the CEMPIE approach. The results are compared in Fig. 8. In the CEMPIE modeling, $|S_{21}|$ was calculated at 401 frequency points from 10 MHz to 3 GHz. The total number of unknowns was approximately 1400, with a fine discretization of the power areas surrounding the connecting via. Dielectric

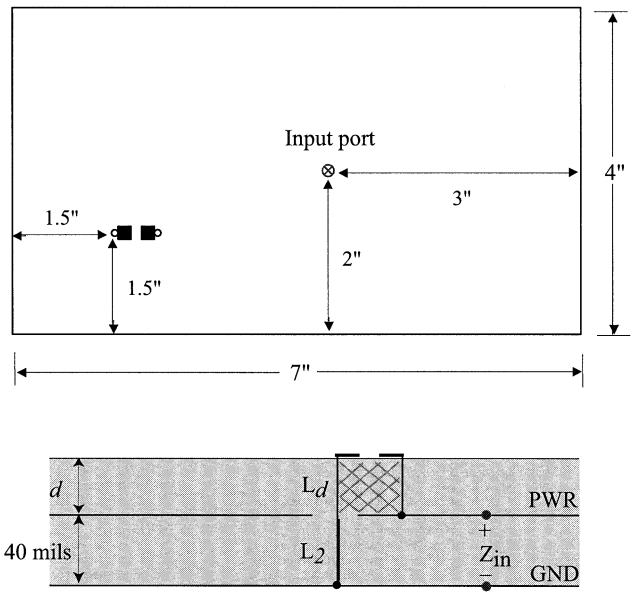

Fig. 9. Board configuration for determining the inductance associated with the via interconnects between and above the power/ground plane pair.

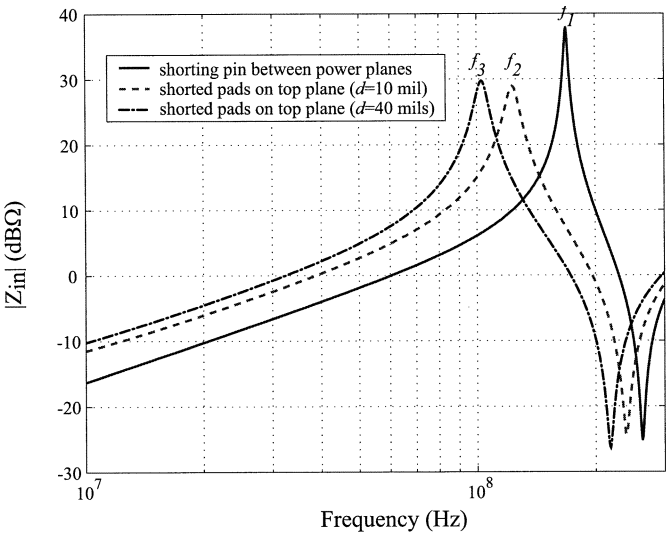

Fig. 10. Modeled $|Z_{\rm in}|$ for the test geometry shown in Fig. 9.

loss was included in the modeling with a loss tangent of $\tan\delta = 0.02$. The vertical discontinuities associated with the test ports were also included in the modeling. The first peak of $|S_{21}|$ at approximately 600 MHz was due to the connecting via inductance and the parallel capacitances between the power areas and the ground plane. In constructing the test board, a thin wire with a diameter of 20 mils was soldered to both power areas at the location (40, 25). Any extra solder in the hole at the wire connection would decrease the equivalent wire inductance in the measurements, but was not accounted for in the CEMPIE modeling. This is evident at the lumped element resonances at both approximately 600 and 1550 MHz, which are impacted by the via inductance connecting the two power areas. As a result, the measured $|S_{21}|$ resonances were shifted to approximately 650 and 1660 MHz. The $|S_{21}|$ peak at approximately 1.4 GHz was a resonance related to the board's short edge dimension. At frequencies higher than 1.6 GHz, the test board exhibited distributed characteristics. Overall, the agreement between the measurements and the modeling is satisfactory, supporting the CEMPIE modeling of multiple layers.

B. Determining L_3

The parasitic inductance associated with the interconnects of a decoupling capacitor can be determined from the resonant frequency of the PCB [29]. This inductance resonates with the inter-plane capacitance of the power/ground plane pair. Since the inter-plane capacitance can be easily measured or calculated, the inductance value can then be obtained from the resonant frequency.

A test configuration, shown in Fig. 9, was modeled as an example. The PCB was a three-layer board with a dimension of 44 in $\times$ 7 in. The relative dielectric constant was $\varepsilon_r = 4.7$ and the loss tangent was $\tan\delta = 0.02$. The second and bottom planes were power and ground planes and two mounting pads were placed on the top plane. The 1.2 mm $\times$ 1.2 mm pads had the approximate size for mounting an 0805 SMT capacitor with a spacing of 0.8 mm. The 0805 SMT capacitor is 79 mil long, 48 mil wide and 50 mil high. Two vertical vias with a diameter of 30 mils were placed in the middle of the pad edges and connected the capacitor to the power/ground planes. The spacing between the power and ground planes was 40 mils. As defined before, the inductance associated with the via portion between the power and ground planes is L_2. The inductance associated with the rest of the vias above the power/ground plane pair and the bonding pads, is L_d. L_3 is the sum of L_d and the parasitic inductance of the capacitor package.

The L_2 and L_d values were determined by calculating the input impedance $|Z_{\rm in}|$ of the test structure. To calculate L_2, a shorting post with the same diameter as the via portion between the power and ground planes shown in Fig. 9, was used to replace the via portion. The shorting post connected the power and ground planes together and the input impedance looking into the input port was modeled. The modeled results are shown as the solid curve in Fig. 10. The peak at $f_1 = 168.775$ MHz was due to the inter-plane capacitance (C_p) and L_2. The power/ground planes were modeled again with the shorting post removed. Since the input impedance in this case was approximately the impedance of the inter-plane capacitance at low frequencies, the C_p was determined from the CEMPIE modeling to be 0.78 nF, which is comparable to 0.74 nF using a simple parallel plate capacitor model. Then, L_2 was determined from f_1 and C_p as $L_2 = 1/[(2\pi f_1)^2 C_p] = 1.14$ nH. Again, as discussed before, the L_2 value includes the plane inductance as well. The closed-form expressions developed in the previous section were also used to estimate this inductance value and (4) and (6) gave the results of 1.08 and 0.96 nH, respectively.

The value of L_d was calculated by shorting the bonding pads on the top plane shown in Fig. 9 using an ideal inductance $L_s = 0.82$ nH and modeling the input impedance. Two cases were studied with the spacing between the top and middle planes to be 10- and 40-mil. The modeled results are shown in Fig. 10 and exhibit a resonant frequency of $f_2 = 123.1$ MHz and $f_3 =$

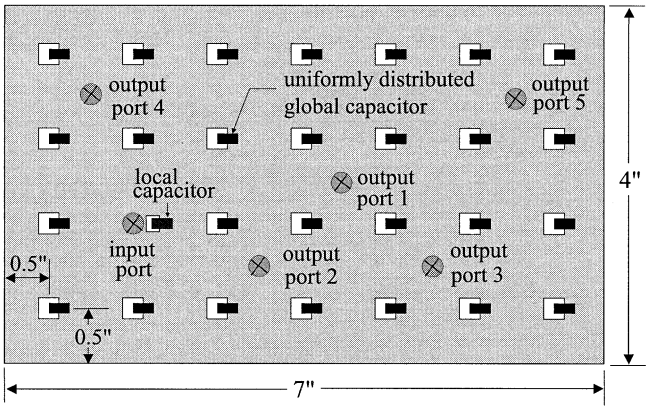

Fig. 11. Test board configuration (top view) for the shared-via decoupling study.

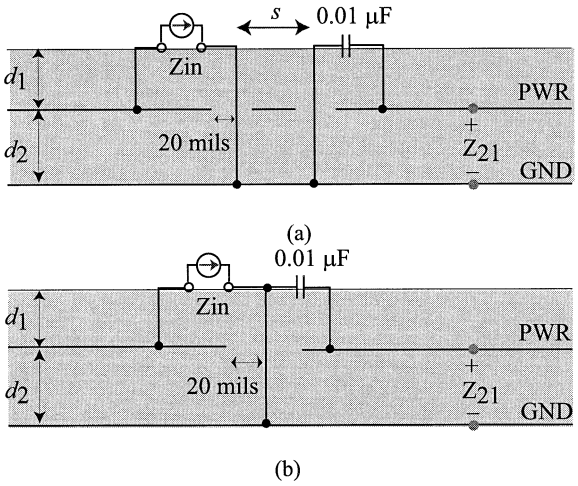

Fig. 12. Local decoupling study of (a) the capacitor ground via is placed in adjacent to the port ground via with a spacing of s and (b) the capacitor and the port share a common ground via.

102.8 MHz for the 10 and 40 mil cases, respectively. This resonant frequency is due to the total inductance ($L_2 + L_d + L_s$) combined with C_p. Therefore, L_d was determined to be 0.19 and 1.12 nH for the 10- and 40-mil cases, respectively. Then, the corresponding L_3 values are 1.01 and 1.94 nH. These L_3 values are used in the next section to compare the estimate (3) to rigorous full-wave modeling.

The above approach to extract L_3, the portion of the interconnect inductance above the plane, using CEMPIE modeling is one possibility. However, for engineering design, a full-wave simulation to obtain L_3 to use in (3), the estimate of the noise mitigation effects of a local decoupling capacitor is undesirable. In particular since design equations have been developed for L_2 and k. An alternative for calculating L_3 is to use inductance equations available for square loops [30].

C. Modeling Shared-Via Decoupling

As a limiting case of local decoupling, shared-via decoupling is studied herein as an extension of the work reported in [19]. Also, the modeled geometry is changed from two-layer to three-layer, so that the effects of L_3 on local decoupling benefits can be investigated. Shared-via decoupling refers to the design that the decoupling capacitor shares a common via with the IC power or ground pin.

The modeled test board is shown in Fig. 11. The three-layer board had a dimension of 4 in $\times$ 7 in. The second and bottom planes were power and ground planes, respectively. The board dielectric material had a dielectric constant of $\varepsilon_r = 4.7$ and loss tangent of $\tan\delta = 0.02$. There were 27 decoupling capacitors uniformly distributed on the board on a 1 in grid for global decoupling. An input port was placed 1.5 in from the left and bottom edges, simulating an IC ground via. A local decoupling capacitor was placed close to the input port. As shown in Fig. 12, the decoupling capacitor was mounted between two bonding pads on the top plane and connected to the power and ground planes with vias. In Fig. 12(a), the local capacitor was located from the input port at a distance of s; while in Fig. 12(b), it shared a common via to the ground plane with the input port, modeling the shared-via decoupling. An ideal current source was applied between the two bonding pads of the input port on the top plane, as shown in Fig. 12, to generate a frequency-domain response. The bonding pads had a dimension of 1.2 mm $\times$ 1.2 mm and were separated by 0.8 mm. The vertical vias were located at the pad edges with a diameter of 30 mils. Five ideal voltage probes were placed on the board, as output ports, to monitor the voltages between the power and ground planes.

The signal layer thickness (from the top to the middle plane) was d_1 and the power/ground plane spacing was d_2, as shown in Fig. 12. Several values of d_1 and d_2 were selected to compare the effectiveness of local decoupling. In particular, the modeled test configurations were as follows.

1) Board #1 ($d_1 = 40$ mils, $d_2 = 40$ mils).
2) Board #2 ($d_1 = 10$ mils, $d_2 = 40$ mils).
3) Board #3 ($d_1 = 10$ mils, $d_2 = 10$ mils).

For each test configuration, four placements of local decoupling were studied with the CEMPIE approach.

1) Only global decoupling capacitors were placed, no local decoupling.
2) A local decoupling capacitor was placed at a relatively far location with $s = 300$ mils.
3) A local decoupling capacitor was placed close to the input port with $s = 75$ mils.
4) A local decoupling capacitor shared a ground via with the input port.

The global decoupling capacitors were placed on the board for all test cases. All capacitors had a value of 0.01 μF and an ESR of 120 mΩ, ESL of 0.82 nH. The $|Z_{21}|$ between the input port and five output ports was modeled at 401 frequency points from 1 MHz to 3 GHz. The modeled results averaged over the five output ports are shown in Figs. 13–15 for Boards #1–#3, respectively.

For Boards #1 and #2 where a 40-mil thick power/ground layer was used, the $|Z_{21}|$ decreases as the local decoupling capacitor was placed closer to the input port, with the case without the local decoupling capacitor having the highest magnitude. The mutual inductance between the vias of the input port and the decoupling capacitor was beneficial for extending the effectiveness of the local decoupling capacitor to higher frequencies far higher than its series resonant frequency. When the decoupling

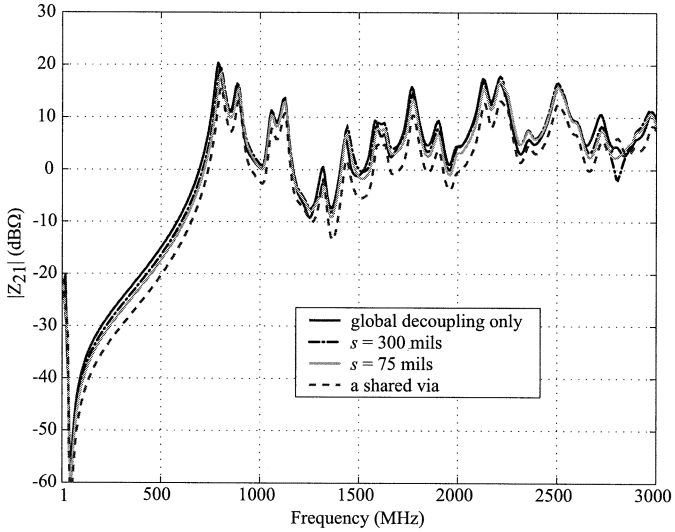

Fig. 13. Modeled $|Z_{21}|$ averaged over the five output ports for Board #1.

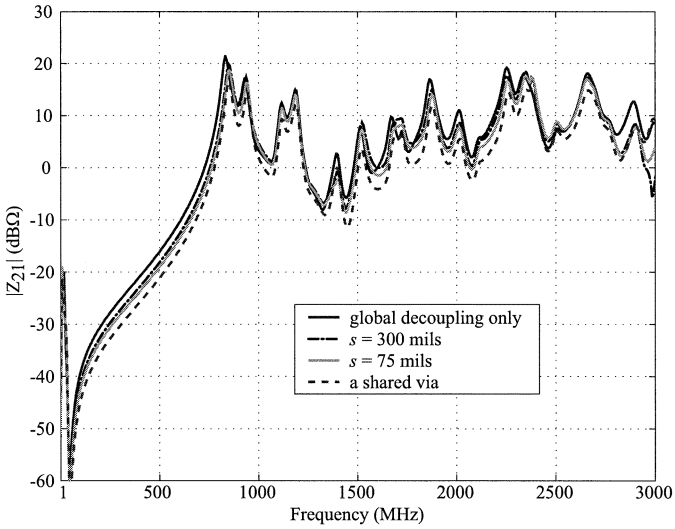

Fig. 14. Modeled $|Z_{21}|$ averaged over the five output ports for Board #2.

capacitor shared a common ground via with the input port, the mutual inductance was maximized and it is clear from Figs. 13 and 14 that the $|Z_{21}|$ decrease in this case is the largest. The average $|Z_{21}|$ decreases for the shared-via case over frequency points and output ports were obtained from the CEMPIE modeled results and are listed in Table IV, where they are compared with the corresponding estimates using (3). In the rough estimation, L_2 and L_3 values were obtained in the previous discussion. The magnetic coupling coefficient k was set to be 0.8 as calculated from CEMPIE as shown in Fig. 6, as opposed to $k \approx 1$ from (7). The decrease of k may be due to the diminished mutual coupling above the power/ground plane pair that is not accounted for in the closed-form expression (7).

L_3 is a limiting factor for local decoupling in (3). When its value is considerably greater than L_2, which sometimes is true for a PCB with many layers or interior power/ground layers, the noise mitigation benefit of local decoupling is negligible. In order to achieve any potential local decoupling benefit, minimum parasitic inductance above the power/ground plane pair (eliminating traces between bonding pads and

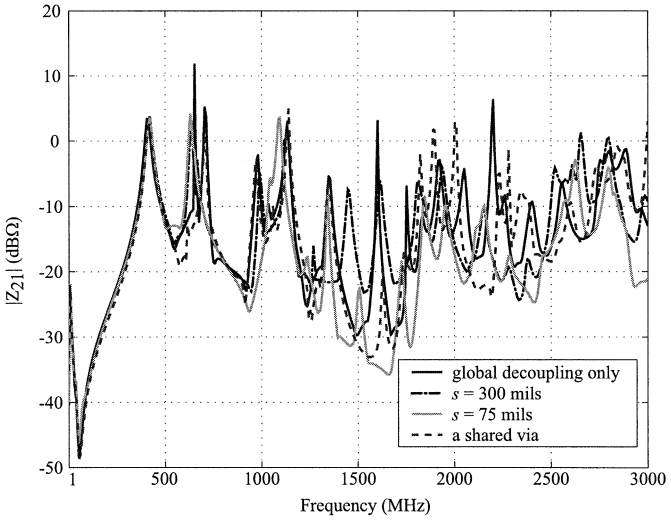

Fig. 15. Modeled $|Z_{21}|$ averaged over the five output ports for Board #3.

vias, small package parasitics, applying multiple vias, etc.) is required. Boards #1 and #2 studied here demonstrate the effect of L_3. The value of L_3 for Board #1 was 1.94 nH and it decreased to 1.01 nH for Board #2 since the thickness above the power/ground plane pair was reduced from 40 mils to 10 miles. The L_2 value remained the same for the two boards. Therefore, Board #2 achieved a greater average $|Z_{21}|$ decrease accordingly, as shown in Table IV.

Board #3 behaved differently as compared to Boards #1 and #2. As shown in Fig. 15, the overall $|Z_{21}|$ changes due to the local decoupling, even the shared-via decoupling, are negligible, though the resonant peaks shift in frequency. Board #3 had a 10 mil thick power/ground plane pair, compared to 40 mil for both Boards #1 and #2; therefore, the values of L_2 and M were much smaller, resulting in little $|Z_{21}|$ decrease as suggested in (3). It is worthy to point out that the overall $|Z_{21}|$ for Board #3 is approximately 10 dB lower than Boards #1 and #2. This is beneficial for power bus noise reduction. The impedance of a power/ground plane pair is nearly proportional to the thickness [14], [18]; therefore, a thin power/ground plane pair always has superior performance for power bus noise, which impacts signal integrity and EMI, as compared to a thick power/ground plane pair [18].

VI. DC Power Bus Design Implications for Multilayer PCBs

The physics and design equations quantifying the benefits of local decoupling detailed in the previous sections, together with previous work reported in the literature, allow for a more complete design methodology of dc power buses in multilayer PCBs. Of particular interest herein are those designs that use entire layers or large area fills for power/ground plane pairs. Specifically, a design approach is

1) to minimize the plane separation between the power/ground layers so as to maximize the inter-plane capacitance;
2) to evaluate the power bus noise mitigation benefits as in (3), which is dominated by the ratio of the portion of the

TABLE IV
AVERAGE $|Z21|$ DECREASE FOR THE SHARED-VIA DECOUPLING IN THE TEST BOARD SHOWN IN FIG. 11

	Average $\|Z_{21}\|$ decrease* from the CEMPIE modeling (dB)	Average $\|Z_{21}\|$ decrease* estimated from (3) (dB)
Board #1	3.9	3.0
Board #2	4.5	4.6

*compared with the baseline case where only global decoupling capacitors were present on the board

decoupling capacitor interconnect inductance above the plane to that in the power/ground plane pair and determine if local decoupling can be beneficial and if so to minimize the separation between the SMT capacitor and IC;

3) to use the largest value of SMT capacitor available in a given package size;
4) to attach the SMT capacitor to the power/ground plane pair through minimal interconnect inductance for both global and local decoupling capacitors.

The first, third, and fourth items are becoming accepted practice as a matter of experience for many designers of leading edge high-speed digital circuits. However, the present work allows the potential benefits of local decoupling to be quantified within engineering accuracy and is an essential piece of a more complete dc power bus design strategy.

The first design priority for a power bus that uses entire planes is to minimize the spacing between the planes, which also maximizes the inter-plane capacitance (though this is not the reason for minimizing the spacing). In short, *thin* is best. By minimizing the plane pair spacing, the input impedance seen looking into the power bus at the IC terminals is reduced. In fact, the power bus input impedance Z_{in} and Z_{21} are proportional to thickness [14], [18], [28] and minimizing the impedance reduces the noise voltage on the planes.

The estimate for power bus noise reduction with (3) is dominated by the ratio of the inductance above the planes to that in the planes for the SMT capacitor interconnect, as well as the via spacing between the capacitor and IC. For PCBs with many layers, where the power/ground layer pairs may be several layers into the planes and following the first priority of thin is best, there may be no benefit derived from local decoupling. Two cases in particular where the power/ground layer pair might be sufficiently thick to obtain some benefit from local decoupling is the case of four-layer boards where a thick core is used for the ground and power planes on layers two and three, or a six-layer board where each of four signal layers must have controlled impedance signal lines and so the ground and power planes are on layers two and five. In these cases, the power and ground planes may be sufficiently thick and benefits of local decoupling can be achieved. There may be other types of special cases where design constraints limit the ability to maintain a thin power/ground plane pair and power bus noise mitigation from local decoupling achieved because the power/ground pair is thick, e.g., a multilayer board that may have several logic levels on different layers, but only a single ground layer. A case where there may also be benefits of local decoupling that is not indicated by (3) is placing many decoupling capacitors in the unused area beneath an application-specific integrated circuit (ASIC) (on the opposite side of the board) in which the pins or balls are only on the periphery of the package. The power and ground planes may be on adjacent layers and so the power bus is thin and the ratio of the portion of the inductance above the plane to that in the plane for a single capacitor is on the order of one or greater, however, for many capacitors placed close together, there is the mutual coupling through the magnetic field among all the capacitors and then to the ground/power pins of the ASIC that may provide some benefit of local decoupling. Finally, a critical aspect when striving to achieve some noise mitigation benefit from local decoupling is that the current on the via segments coupling the capacitor and IC must be coupled between the power/ground plane pair as illustrated in the two examples of Fig. 1. This dictates whether the capacitor is placed in proximity to the power or ground pin of the IC.

The value of the decoupling capacitor for local decoupling does not appear in (3) because it is assumed sufficiently large so that the impedance of the capacitor is small relative to the impedance associated with the interconnect inductance, which is typically the case in practice. Then, beyond this, using the largest value in any given package size is beneficial in providing charge for maintaining signal fidelity and reducing power bus noise at lower frequencies below the board resonances. For global decoupling, the effectiveness of the SMT decoupling capacitor is dictated by the impedance seen looking into the SMT as compared to the power bus at the SMT location. The impedance seen looking into the SMT at high frequencies is dominated by the interconnect inductance, because the impedance associated with the capacitance is very small with respect to the impedance associated with the interconnect inductance plus ESL. Then, a larger capacitance value in a particular package size does not limit any performance and again is beneficial for signal fidelity and lower-frequency power bus noise.

Finally, as indicated by (3) and for the reasons indicated in the previous paragraph, minimizing the interconnect inductance achieves the best performance and in practice is a common habit among most high-speed digital designers.

VII. CONCLUSION

A test board was investigated to support the previously reported modeling studies on local decoupling. Closed-form expressions for via inductance and the magnetic coupling coefficient were developed and used to estimate the average $|Z_{21}|$ decrease due to an added local decoupling capacitor. The approximately 1 dB difference between the estimates and measurements demonstrates the application of these closed-form expressions in practical engineering for power bus design and decoupling.

The IC/capacitor spacing, as well as the power/ground plane separation, determines whether the capacitor is local or global. For a fixed IC/capacitor spacing, the thicker the power/ground plane separation is, the greater the $|Z_{21}|$ decrease that can be achieved in a frequency band up to several gigahertz. Previous studies concluded that, for a power/ground plane pair with a thickness of 30 mils or more, placing a decoupling capacitor closely enough to an IC power/ground pin can effectively reduce the power bus noise. However, for a thin power/ground plane pair with a thickness of 10 mils or less, it is not easy to achieve local decoupling benefits by simply placing the capacitor physically close to the device power/ground pin. In this case, decoupling capacitors are normally global. In other words, it is not necessary to put capacitors near devices; rather, they can be placed where space is available on the PCB, though should be connected through minimal interconnect inductance.

The shared-via decoupling was studied in this work as a limiting case of local decoupling. It demonstrated the possible maximum benefits that a local decoupling capacitor can achieve. The modeling results again corroborated the previous conclusions. For a 10-mil thick power/ground plane pair, the noise reduction exceeded that of the widely spaced planes with good local decoupling by 10 dB. The shared-via decoupling for the 10-mil thick plane pair resulted in negligible power bus noise reduction, because the impedance seen looking into the planes at the device terminals was much lower, than that looking into the decoupling capacitor branch, even with the effects of mutual inductance.

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