01 Aug 2005

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Giuseppe Selli

James L. Drewniak
Missouri University of Science and Technology, drewniak@mst.edu

Richard E. DuBroff
Missouri University of Science and Technology, red@mst.edu

Jun Fan
Missouri University of Science and Technology, jfan@mst.edu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/1829

Recommended Citation

G. Selli et al., "Power Integrity Investigation of BGA Footprints by Means of the Segmentation Method," *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility (2005, Chicago, IL)*, vol. 2, pp. 655-659, Institute of Electrical and Electronics Engineers (IEEE), Aug 2005.
The definitive version is available at https://doi.org/10.1109/ISEMC.2005.1513595

Power Integrity Investigation of BGA Footprints by Means of the Segmentation Method

Giuseppe Selli,
James L. Drewniak,
Richard E. Dubroff
EMC Laboratory
University of Missouri-Rolla
gs5xd@umr.edu

Jun Fan,
James L.Knighten,
Norman W. Smith,
Dean McCoy
NCR Corporation
San Diego, CA USA

Bruce Archambeault
IBM Co.
Research Triangle Park,
NC USA

Abstract — **The engineering of the power delivery network is becoming a fundamental issue in the design of high speed digital systems on PCB's. In fact, providing the required power to the different IC's at the specified noise-free voltage levels allows a correct functioning of the overall PCB systems. More over, the ongoing trend of replacing active devices with peripherally located I/O and PWR/GND pins with areally located I/O and PWR/GND pins (BGA packaged) increases the complexity of the models, when power delivery issues need to be studied in a larger contest, such as the overall PCB's. The employment of the powerful, but simple, concept of the segmentation method allows investigation of the power delivery network of the PCB systems in two fundamental stages. During the first stage, a small cut out of the board corresponding to the BGA footprint is modelled with a 3D full wave simulation tool. During the second stage the equivalent impedance network representation corresponding to this cut out is combined, by means of the segmentation method [1-5], with larger pieces of a board, whose network representations can be extracted from the closed form expression of the cavity model approach [6-9].**

Keywords – Power integrity, Ball Grid Array (BGA) footprint, equivalent network representation, segmentation method, cavity mode approach.

I. INTRODUCTION

Power integrity, i.e., the capability of a system to deliver the right amount of power at the desired noise free voltage level, has become a fundamental aspect in the design of high speed digital systems. The employment of IC's with surface located I/O's and PWR/GND pins (BGA footprint) can alter the behavior of the power delivery network constituted by two simple solid planes. Complete models of such geometries with all the holes, as well as the vias and interconnects, are needed in order to quantify the significance of this modification. Self and transfer impedances between PWR/GND pins located within the footprint of the BGA IC's are usually the preferred quantities to investigate in order to establish the voltage drawn associated with each pin or the amount of coupling/decoupling among different pins.

In contrast with a simple pair of solid planes, closed form expressions for the self and transfer impedances for pair of planes with holes and vias are not readily available. Therefore, complete 3-dimesional full wave simulations of these geometries are needed.

The planes constituting the power delivery network are usually much larger than the BGA footprints. Therefore, the modeling of small features associated with the balls, the vias and the remainder of the interconnects necessarily increases the size of the models and the computational effort, given the difference in scale between those small features and the planes constituting the backbone of the power delivery network. The application of the powerful concept of the segmentation method avoids these efforts and also allows a much better versatility.

The method is applied in several steps. Firstly, the overall board corresponding to the power delivery network is segmented in various adjacent pieces corresponding to small cut out's of the BGA footprints and other shapes constituting the solid planes. The cutouts are finely modeled and simulated by means of a 3-dimensional full wave tool and an equivalent network representation is obtained. The self and transfer impedances associated with the other shapes are obtained by means of the closed form expressions from the cavity model method. Finally, all the equivalent network representations are recombined together according to their respective position with one another. Two major improvements result from this methodology. The 3D full wave simulation is focused only to the most complex part of the board, i.e., the footprint, allowing a fine modeling of the geometry itself. The effect of the given footprint within surrounding main power areas of various shape can be investigated very easily without recurring to new lengthy full wave simulations. It is very important, though, to ensure the continuity of the electric and magnetic field between the different patches and this is usually ensured by employing the so called internal ports [1-5].

II. DESCRIPTION OF THE GEOMETRY UNDER INVESTIGATION

The geometry considered is extracted from the multilayer structure shown in Fig.1. The pair of planes constituting the power delivery network of interest, i.e., 1.5 V and GND, is highlighted in the dashed box. The geometry under

investigation is then a 2-layer board, consisting of a ground and a power plane of dimensions 10 cm by 8 cm, where many holes corresponding to a footprint of a BGA package are included. Two hole patterns are localized on the top and bottom plane respectively; these patterns correspond to the antipads for the BGA package pins, which are connected to the 1.5 V plane, GND plane or any other layer. The BGA package in Fig.1 is shown only as an example for the connections.

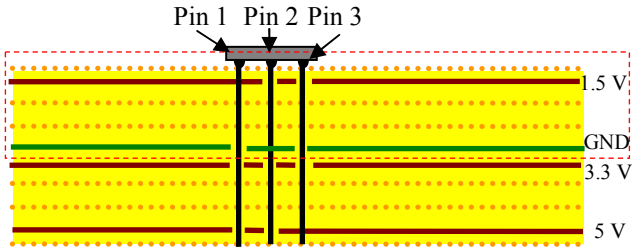


Fig.1. Stack-up of the multi-layer structure from which the power delivery network under investigation is extracted.

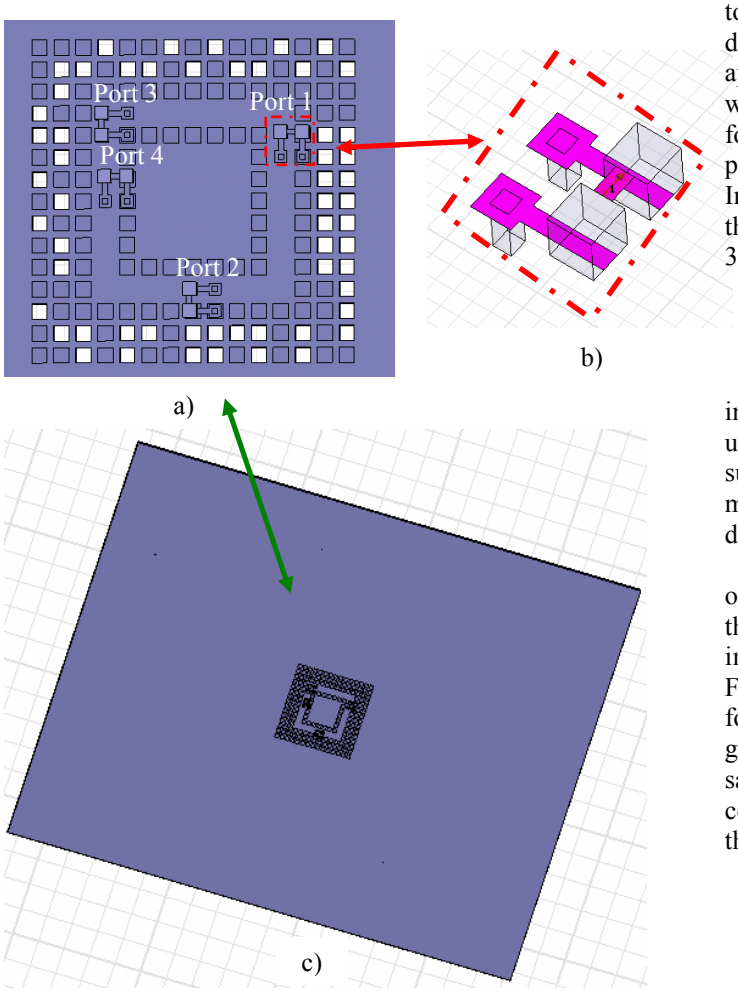


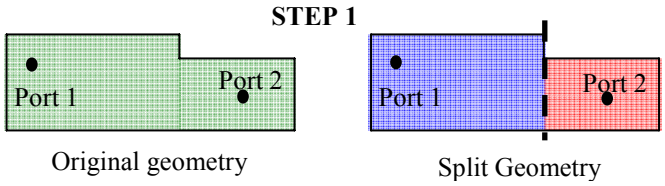
Fig.2. Detailed description of the power delivery network of interest. a) Close up of the central part of the board where the holes due to the footprint of the BGA package are located. b) Close up of the model of the port. c) Overall view of the power delivery network.

A detailed description of the power delivery network under investigation is given in Fig.2a, b and c. The top view of the 2-layer board of interest is given along with a close up of the cut out corresponding to the BGA footprint and a model of port used to excite the structure. The hole pattern on the top layer corresponds to the antipads associated to the pins of the BGA package connected to the bottom layer or any other layer is also given in Fig.2a. When a pin is connected to any of the other layers, antipads are present on both the GND plane and 1.5 V plane (Pin 3 in Fig.1). The model of the port used to excite the power delivery network of Fig.2c is also given in Fig.2b. This model takes into account the entire interconnect from the bottom of the IC package, located on the topmost signal layer, down to the 1.5 or GND layer. Several elements constitute the interconnects, i.e., the balls of the BGA package, which are usually offset with respect to the vias connecting the balls themselves to the ground/power layers, small sections of microstrip lines located on the topmost signal layer and the vias. Due to modeling complexity issues, all the curved surfaces and volumes are replaced by parallelepipeds. However, the net effect of these interconnects is still expected to be an increase in the equivalent inductance of the ports. The distance between the 1.5 V and the GND plane is approximately 21 mils, the square balls have sides of 24 mils, whereas the vias have sides of approximately 10 mils. The footprint employed in the simulation corresponds to the center part of an actual BGA packaged IC with all the pins assigned. In fact, in order to reduce the complexity of the model, only the central 15 x 15 pins of the package are represented in the 3D full wave model of Fig.2c.

III. Description of the Procedure and Results

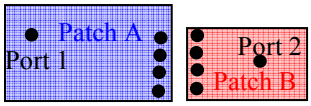
The segmentation method for 2D geometries was introduced by T. Okoshi et al. [1]. This procedure is very useful when closed form expressions of network quantities, such as S-parameter [S], impedance [Z] or admittance [Y] matrices, of complex geometries are not available, but can be derived from simpler ones.

Once the original geometry is split into patches, a number of internal ports [1-5], i.e., fictitious ports, are created along the edges, where the splits took place. Then, different impedance matrices are obtained for the entities realized. Finally, the combination of the matrices is obtained by solving for the external ports, i.e., the real ports of the original geometry. This combination is carried out by enforcing the same voltages and opposite currents to each pair of corresponding internal ports on adjacent patches. A chart of the procedure is outlined below:



STEP 2

$$\begin{bmatrix} Z_{11} & Z_{1Ai} \\ Z_{Ai1} & Z_{AiAi} \end{bmatrix}$$



$$\begin{bmatrix} Z_{22} & Z_{2Bi} \\ Z_{Bi2} & Z_{BiBi} \end{bmatrix}$$

Internal Ports

$$V_1 = Z_{11} I_1 + Z_{1Ai} I_{Ai} \qquad V_2 = Z_{22} I_2 + Z_{2Bi} I_{Bi}$$
$$V_{Ai} = Z_{Ai1} I_1 + Z_{AiAi} I_{Ai} \qquad V_{Bi} = Z_{Bi2} I_2 + Z_{BiBi} I_{Bi}$$

STEP 3

$$V_{Ai} = V_{Bi} \quad \& \quad I_{Ai} = -I_{Bi} \rightarrow \begin{matrix} V_1 = Z_{11}^* I_1 + Z_{12}^* I_2 \\ V_2 = Z_{21}^* I_1 + Z_{22}^* I_2 \end{matrix}$$

$$\begin{bmatrix} Z_{11}^* & Z_{12}^* \\ Z_{21}^* & Z_{22}^* \end{bmatrix} = \begin{bmatrix} Z_{11} - Z_{1Ai} Z_{Ti} Z_{Ai1} & Z_{1Ai} Z_{Ti} Z_{Bi1} \\ Z_{1Bi} Z_{Ti} Z_{Ai1} & Z_{22} - Z_{1Bi} Z_{Ti} Z_{Bi1} \end{bmatrix}$$

$$where \quad Z_{Ti} = (Z_{AiAi} + Z_{BiBi})^{-1}$$

The segmentation method is applied to the geometry described in the previous section by first dividing the power delivery network into a number of adjacent patches as shown in Fig.3. The presence of the holes and the interconnects do not allow a closed form representation of the central patch in terms of an impedance matrix [Z]. Therefore, a simulation by means of a 3D full wave algorithm is needed. On the other hand, an equivalent network representation for all the other patches is achievable by means of the closed form expressions available from the cavity model approach [6-9].

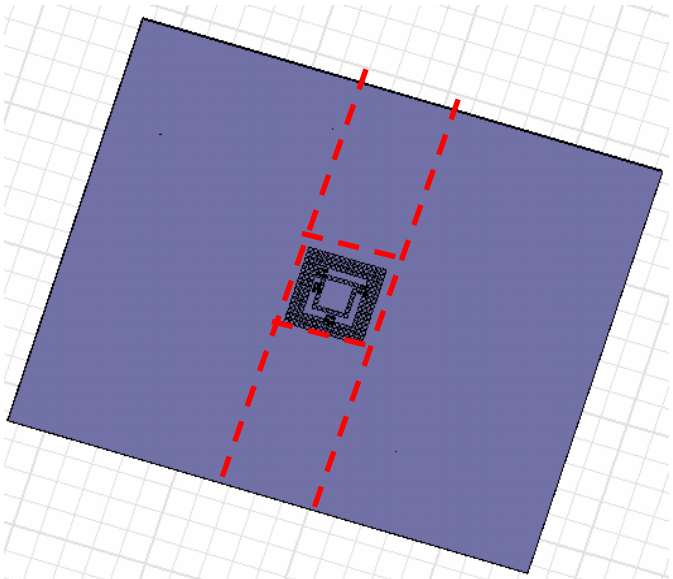


Fig.3. Application of the segmentation method to the board shown in Fig.2 c).

The simulation of the central patch was performed with ANSOFT HFSS. A total number of 28 ports were considered, 4 external ports which are modeled as shown in Fig.2b and 24 internal ports, located along the four edges of the patch in order to have at least ten ports per minimum wavelength, where the minimum wavelength considered corresponds to the maximum frequency of interest, i.e., 5 GHz.

The accuracy of the results, when all the patches are then recombined together, is dependent upon the number of internal ports employed. In fact, too few ports make the procedure less complex, but the enforcement of the continuity of the fields at only a few points modifies the fields themselves inside the overall structure - the lines of surface current are all crunched toward these few discrete points - and the overall results are incorrect. On the other hand, the employment of many ports improves the accuracy of the results. However, when the internal ports are too close one another, it is possible to incur in numerical errors when the matrix ($Z_{AiAi} + Z_{BiBi}$) indicated in STEP 3 is inverted. More over, the complexity of the recombination in the final step of the segmentation method increases. The employment of ten ports per wavelength has been shown by experience to be a good compromise between all these conflicting considerations.

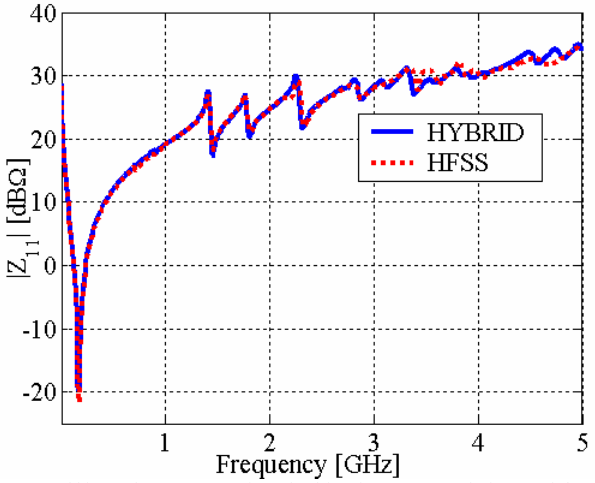


Fig.4. Self impedance comparison looking into Port 1 of Fig.2a of the Hybrid method results and the HFSS simulations.

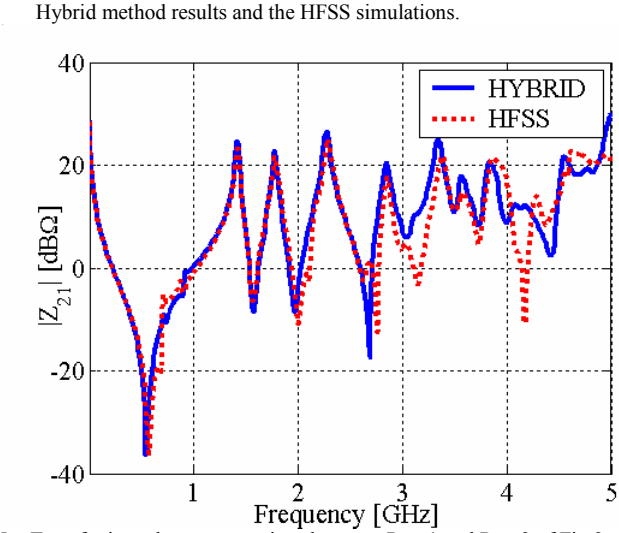


Fig.5. Transfer impedance comparison between Port 1 and Port 2 of Fig.2a of the Hybrid method results and the HFSS simulations.

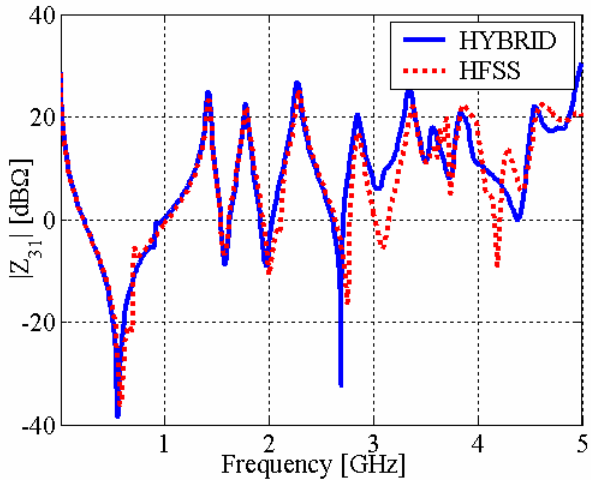


Fig.6. Transfer impedance comparison between Port 1 and Port 3 of Fig.2a of the Hybrid method results and the HFSS simulations.

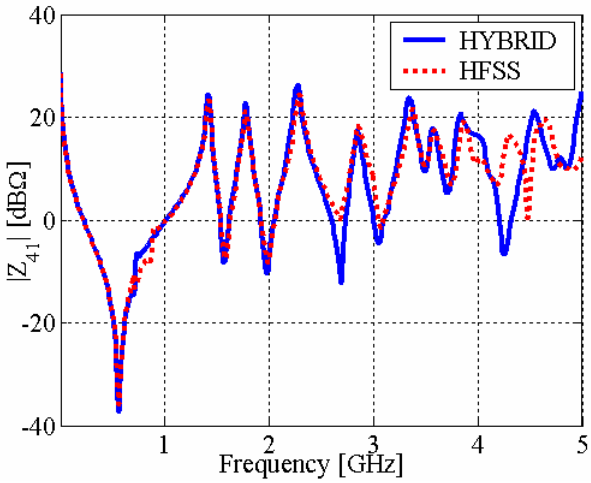


Fig.7. Transfer impedance comparison between Port 1 and Port 4 of Fig.2a of the Hybrid method results and the HFSS simulations.

The self and transfer impedances obtained from the hybrid method described above, i.e., HFSS simulation plus the cavity model and segmentation, are finally compared to an HFSS simulation of the overall structure. The results of the comparison are shown in Fig.4, Fig.5, Fig.6 and Fig.7.

The differences between the hybrid method results and the HFSS simulations are within 1-3 dB up to approximately 3 GHz. Then, larger discrepancies are observed as the frequency is increased. This larger difference is mostly due to the modeling of the internal ports in the HFSS simulation of the central patch, although this claim has to be confirmed by further investigations.

Along with the satisfactory accuracy of the results when compared to 3D full wave simulations, the hybrid method proposed has the great advantage of versatility. In fact, when the equivalent network representation of the cut out of the board corresponding to the BGA footprint is obtained, this can be used in combination with as many rectangles and in any disposition needed, allowing the investigations of different power delivery networks with the same BGA footprint cut out.

IV. CONCLUSIONS

A methodology for investigating complex 2D geometry is proposed. In particular, the power delivery network associated to specified voltage level in a multi-layer structure is investigated. The power network is characterized by many holes due to a BGA footprint located in the middle of the configuration. The employment of the segmentation method to investigate this geometry as an alternative to a complete full wave simulation is shown to be quite accurate and it offers all the advantages of versatility.

In fact, the full wave simulation of only the cutout corresponding to the BGA footprint requires less computational resources than the simulation of the entire power delivery network. In fact, assuming the same computational time for simulating the overall power distribution network or the BGA board, the latter can be simulated once for all and used multiple times in conjunction with the cavity model approach.

More over, this simulation can be performed with a higher degree of accuracy, given that all the features associated with those smaller geometries have comparable dimensions.

Once an equivalent network representation of the cut out is obtained, this representation can be easily embedded in different power delivery networks, avoiding further full wave simulations, when the design needs to be changed or a what-if scenario predicted.

For the specific BGA example examined, the differences between the hybrid method results and the full wave simulations are within 1-3 dB up to approximately 3 GHz.

AKNOWLEDGEMENT

The authors thank the NCR Corporation for all the information regarding the stack-up of the multi-layer geometry and the pin assignment of the BGA packaged IC.

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