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Jun Fan
Missouri University of Science and Technology, jfan@mst.edu

James L. Drewniak
Missouri University of Science and Technology, drewniak@mst.edu

James L. Knighten

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Lumped-Circuit Model Extraction for Vias in Multilayer Substrates

Jun Fan, *Member, IEEE*, James L. Drewniak, *Senior Member, IEEE*, and James L. Knighten, *Senior Member, IEEE*

***Abstract*—Via interconnects in multilayer substrates, such as chip scale packaging, ball grid arrays, multichip modules, and printed circuit boards (PCB) can critically impact system performance. Lumped-circuit models for vias are usually established from their geometries to better understand the physics. This paper presents a procedure to extract these element values from a partial element equivalent circuit type method, denoted by CEMPIE. With a known physics-based circuit prototype, this approach calculates the element values from an extensive circuit net extracted by the CEMPIE method. Via inductances in a PCB power bus, including mutual inductances if multiple vias are present, are extracted in a systematic manner using this approach. A closed-form expression for via self inductance is further derived as a function of power plane dimensions, via diameter, power/ground layer separation, and via location. The expression can be used in practical designs for evaluating via inductance without the necessity of full-wave modeling, and, predicting power-bus impedance as well as effective frequency range of decoupling capacitors.**

***Index Terms*—DC power-bus design, decoupling capacitor design, lumped-circuit model extraction, multilayer substrate, via inductance, via interconnects.**

I. Introduction

INTERCONNECT design is a critical issue in high-speed digital circuit designs [1]. Many signal integrity (SI) and electromagnetic interference (EMI) problems are related to interconnect parasitics in multilayer substrates. For example, effective discrete capacitor decoupling can be a critical dc power-bus design issue in high-speed digital circuits at all levels, on package, and printed circuit board (PCB) [2], [3]. When entire layers are devoted for power supply and current return, via inductance associated with a decoupling capacitor plays an important role in its performance. Typically, decoupling capacitors are effective only when their total impedance is lower than the impedance seen looking into the power/ground planes [4]. The inductance associated with the interconnects (vias, traces/bonding wires, and pads) connecting the capacitors to the power/ground layers determines the frequency range where the decoupling capacitors are effective. Further, decoupling capacitors adjacent to an IC device can have a different behavior than capacitors placed farther away, i.e., local decoupling effects [5]. These local decoupling capacitors can be effective far above the series resonance frequency determined by the interconnect parasitics. It is the mutual inductive coupling between closely spaced vias that accounts for the ability to effectively transfer charge at frequencies higher than the series resonance frequency [6]. The charge needed for device switching is provided directly by adjacent decoupling capacitors through the via mutual inductance. It is desirable to have an approach to quantify the inductance of via interconnects, and the mutual inductance between closely spaced vias, in order to evaluate the local decoupling effects and facilitate design. Further, these lumped element models can be used in full-wave tools to eliminate the need for meshing down to such a fine detail for interconnects.

Full-wave electromagnetic modeling can be used to simulate the impact of interconnects on system performance. However, lumped-circuit models are often preferable for fast and simple prediction of system performance at the design stage. A physics-based lumped-circuit model can be developed based on the interconnect structures, by determining the conduction and displacement current paths. However, a methodical and proven approach to calculate the element values for the lumped-circuit model is also necessary. This paper introduces a procedure to extract lumped-circuit elements based on CEMPIE, a partial element equivalent circuit (PEEC) type method, and a physics-based circuit prototype developed from the physical structure. The CEMPIE method results in an extensive circuit net for interconnect geometries from an integral equation formulation. This circuit net is then simplified to the specified lumped-circuit prototype, by enforcing equality of the admittance matrices looking into the external ports.

The CEMPIE method, a circuit extraction approach based on a mixed-potential integral equation formulation, has been developed and demonstrated as a powerful modeling tool for multilayer substrates [7]. CEMPIE is an application of the PEEC approach for general multilayer media. The ground plane and dielectric layers in the CEMPIE modeling are assumed to be of infinite size, and Green's functions for the grounded dielectric slab are calculated [8]. The power plane, as well as vias, is replaced by equivalent surface currents and charges. A mixed-potential integral equation is formulated when enforcing boundary conditions. It is then discretized using basis functions and tested by testing functions, resulting in an admittance matrix equation. An equivalent circuit is further extracted from this admittance matrix, instead of directly solving the matrix equation. The extracted circuit is then exported to SPICE for simulations in a normal CEMPIE modeling. In this work though, instead of performing the circuit simulations, the lumped-circuit model ex-

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J. Fan and J. L. Knighten are with NCR Corporation, San Diego, CA 92127 USA.

J. L. Drewniak is with the Electromagnetic Compatibility Laboratory, University of Missouri-Rolla, Rolla, MO 65409 USA.

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traction procedure presented herein is applied to get the inductance values associated with the via interconnect. This approach is based on the CEMPIE method, which has been demonstrated by measurements, and is very robust for typical structures on multilayer substrates. Further, it is very efficient and universal in the sense that an inductance matrix, including self and mutual terms associated with all interconnects, is calculated at the same time.

Calculation of via inductance in a microstrip line has been studied using various approaches, and either formulas or design curves for inductance values were generated [9]–[13]. However, if a power plane, instead of a trace, is present in the structure, the portion of the current on the plane that crowds down to the via will also contribute magnetic flux wrapping the via, thus change the via inductance value [14]. A similar contribution of planar current on the ground plane was studied experimentally [15]. In this paper, via self inductance in a rectangular power bus is studied using the developed lumped-element circuit extraction approach, and a closed-form expression which includes the effect of current congestion is derived.

The lumped-element circuit extraction procedure is detailed in Section II. Examples are provided in Section III to demonstrate the procedure. Section IV details the derivation of the closed-form expression for via self inductance in a rectangular power bus, while the application of the expression is discussed in Section V, in the prediction of power-bus impedance and effective frequency range of a decoupling capacitor.

II. Lumped-Element Circuit Extraction Procedure

A lumped-circuit model can be constructed as shown in Fig. 1 for a dc power-bus structure with vias. The power and ground planes can be modeled at low frequencies as an interplane capacitance C_b. Dielectric losses of the power layer can be accounted for by a conductance ωG_b, in parallel with the interplane capacitance. G_b is constant if the loss tangent is constant over the frequency range of interest. All via interconnects are characterized as inductances, with mutual inductances representing the mutual inductive coupling between them. The admittance matrix $[\mathbf{Y}_{\mathbf{lumped}}]$ for this specific lumped-circuit prototype is shown in (1) at the bottom of the page, and N ports are assumed. L_i is the self inductance associated with Via i, and M_{ij} is the mutual inductance between Vias i and j, and

$$[\boldsymbol{Y}_{\mathbf{lumped}}]^{-1}\begin{bmatrix}\boldsymbol{I}_1\\ \vdots\\ \boldsymbol{I}_N\end{bmatrix}=\begin{bmatrix}\boldsymbol{V}_1\\ \vdots\\ \boldsymbol{V}_N\end{bmatrix} \tag{2}$$

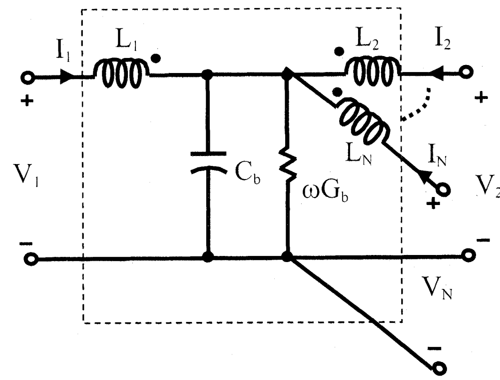

Fig. 1. Lumped-circuit model for a power bus with via interconnects.

where $[I_1, \ldots, I_N]$ are port currents, and $[V_1, \ldots, V_N]$ are port voltages.

For the same geometry, the CEMPIE formulation is applied. Detailed descriptions on the CEMPIE formulation can be found in [7]. Let there be induced surface current and charge densities on the metallization surfaces, then, an electric field integral equation is obtained by enforcing boundary conditions on these metallization surfaces as [16]

$$\hat{\boldsymbol{n}}\times\left[\boldsymbol{j\omega}\int_{\boldsymbol{S}}\overline{\overline{\boldsymbol{G}}}^{\boldsymbol{A}}\left(\vec{\boldsymbol{r}},\,\vec{\boldsymbol{r}}\,'\right)\cdot\vec{\boldsymbol{J}}\left(\vec{\boldsymbol{r}}\,'\right)\,\boldsymbol{ds}'+\nabla\boldsymbol{\phi}\left(\vec{\boldsymbol{r}}\,'\right)\right]=0,\qquad \vec{\boldsymbol{r}}\in\boldsymbol{S} \tag{3}$$

where ϕ is the scalar electric potential; $\vec{\boldsymbol{J}}(\vec{\boldsymbol{r}})$ is the surface current density; S refers to the metallization surfaces; and $\overline{\overline{\boldsymbol{G}}}^{A}(\vec{\boldsymbol{r}},\vec{\boldsymbol{r}}\,')$ is a dyadic Green's function for the magnetic vector potential. Equation (3) is discretized by expanding the unknown current densities $\vec{\boldsymbol{J}}(\vec{\boldsymbol{r}})$ with basis functions, and testing the equation with testing functions. Based on the concept of partial inductance [17], a matrix equation in circuit notation results as

$$\boldsymbol{j\omega}[\mathbf{L}_p][\mathbf{i}]-[\boldsymbol{\Lambda}][\boldsymbol{\varphi}]=0 \tag{4}$$

where $[\mathbf{i}]$ is the unknown edge-current vector; $[\boldsymbol{\varphi}]$ is the vector of unknown cell potentials; $[\boldsymbol{\Lambda}]$ is the connectivity matrix that relates cell quantities to edge quantities; $[\mathbf{L}_p]$ is the branch-wise inductance matrix (partial inductances); and, the scalar potential is assumed to be constant over each mesh cell.

$$[\mathbf{Y}_{\mathbf{lumped}}]=\begin{bmatrix}\boldsymbol{j\omega L}_1+\dfrac{1}{\boldsymbol{\omega}(\boldsymbol{G_b}+\boldsymbol{jC_b})} & \boldsymbol{j\omega M}_{12}+\dfrac{1}{\boldsymbol{\omega}(\boldsymbol{G_b}+\boldsymbol{jC_b})} & \cdots & \boldsymbol{j\omega M}_{1N}+\dfrac{1}{\boldsymbol{\omega}(\boldsymbol{G_b}+\boldsymbol{jC_b})}\\ \boldsymbol{j\omega M}_{21}+\dfrac{1}{\boldsymbol{\omega}(\boldsymbol{G_b}+\boldsymbol{jC_b})} & \boldsymbol{j\omega L}_2+\dfrac{1}{\boldsymbol{\omega}(\boldsymbol{G_b}+\boldsymbol{jC_b})} & \cdots & \boldsymbol{j\omega M}_{2N}+\dfrac{1}{\boldsymbol{\omega}(\boldsymbol{G_b}+\boldsymbol{jC_b})}\\ \vdots & \vdots & \ddots & \vdots\\ \boldsymbol{j\omega M}_{N1}+\dfrac{1}{\boldsymbol{\omega}(\boldsymbol{G_b}+\boldsymbol{jC_b})} & \boldsymbol{j\omega M}_{N2}+\dfrac{1}{\boldsymbol{\omega}(\boldsymbol{G_b}+\boldsymbol{jC_b})} & \cdots & \boldsymbol{j\omega L}_N+\dfrac{1}{\boldsymbol{\omega}(\boldsymbol{G_b}+\boldsymbol{jC_b})}\end{bmatrix}^{-1} \tag{1}$$

Current continuity provides a relationship between charge and current as

$$-j\omega[\mathbf{Q}] = [\mathbf{I}] + [\mathbf{I}^e] \tag{5}$$

if nodal currents are defined as total currents flowing out of the corresponding mesh cells, where Q_n, I_n, and I_n^e are the charge, the surface current, and the externally impressed current associated with Cell n, respectively. The surface nodal currents are related to the surface edge currents by the connectivity matrix as

$$[\mathbf{I}] = [\mathbf{\Lambda}]^T[\mathbf{i}]. \tag{6}$$

It can be shown that the unknown cell potentials are related to cell charges as [7]

$$[\varphi] = [\mathbf{K}][\mathbf{Q}] \tag{7}$$

where

$$K_{pq} = \frac{1}{A_p A_q}\int_{S_p}\int_{S_q} G^{\phi}\left(\vec{r}, \vec{r}\,'\right) ds'\, ds \tag{8}$$

where S_p and S_q indicate a surface integration over Cell p and q, respectively; and, A_p and A_q are the corresponding cell areas.

Using (5)–(7) gives another matrix equation as

$$[\mathbf{\Lambda}]^T[\mathbf{i}] + j\omega[\mathbf{K}]^{-1}[\varphi] = -[\mathbf{I}^e] \tag{9}$$

where

$$[\mathbf{K}]^{-1} = [\mathbf{C}_p] - j[\mathbf{G}_p] \tag{10}$$

where $[\mathbf{C}_p]$ and $[\mathbf{G}_p]$ are both real, $[\mathbf{C}_p]$ is the cell-wise partial capacitance matrix, and $\omega[\mathbf{G}_p]$ is the cell-wise partial conductance matrix that results from the substrate dielectric losses. Based on (4) and (9), a nodal matrix equation (system matrix equation) that relates node potentials to node currents results as

$$[\mathbf{Y}]\begin{bmatrix} V_1 \\ \vdots \\ V_N \\ V_{(N+1)} \\ \vdots \\ V_M \end{bmatrix} = \begin{bmatrix} I_1 \\ \vdots \\ I_N \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{11}$$

where M is the total node number in the CEMPIE extracted equivalent circuit, Nodes 1 to N are external circuit nodes corresponding to the N vias, and $[\mathbf{Y}]$ is the nodal admittance matrix

$$[\mathbf{Y}] = \frac{1}{j\omega}[\mathbf{\Lambda}]^T[\mathbf{L}_p]^{-1}[\mathbf{\Lambda}] + j\omega[\mathbf{C}_p] + \omega[\mathbf{G}_p]. \tag{12}$$

Since all the node currents are zero for inner nodes (Nodes $N+1$ to M) by Kirchoff's Current Law, it is possible to relate external node potentials $[V_1, \ldots, V_N]$ to external node currents $[I_1, \ldots, I_N]$ by matrix manipulation

$$[\mathbf{A} - \mathbf{B}\mathbf{D}^{-1}\mathbf{C}]^{-1}\begin{bmatrix} I_1 \\ \vdots \\ I_N \end{bmatrix} = \begin{bmatrix} V_1 \\ \vdots \\ V_N \end{bmatrix} \tag{13}$$

where

$$[\mathbf{A}] = \begin{bmatrix} Y_{11} & Y_{12} & \cdots & Y_{1N} \\ Y_{21} & Y_{22} & \cdots & Y_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{N1} & Y_{N2} & \cdots & Y_{NN} \end{bmatrix}$$

$$[\mathbf{B}] = \begin{bmatrix} Y_{1(N+1)} & Y_{1(N+2)} & \cdots & Y_{1M} \\ Y_{2(N+1)} & Y_{2(N+2)} & \cdots & Y_{2M} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{N(N+1)} & Y_{N(N+2)} & \cdots & Y_{NM} \end{bmatrix}$$

$$[\mathbf{C}] = \begin{bmatrix} Y_{(N+1)1} & Y_{(N+1)2} & \cdots & Y_{(N+1)N} \\ Y_{(N+2)1} & Y_{(N+2)2} & \cdots & Y_{(N+2)N} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{M1} & Y_{M2} & \cdots & Y_{MN} \end{bmatrix}$$

$$[\mathbf{D}] = \begin{bmatrix} Y_{(N+1)(N+1)} & Y_{(N+1)(N+2)} & \cdots & Y_{(N+1)M} \\ Y_{(N+2)(N+1)} & Y_{(N+2)(N+2)} & \cdots & Y_{(N+2)M} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{M(N+1)} & Y_{M(N+2)} & \cdots & Y_{MM} \end{bmatrix}.$$

The two matrix equations (2) from the physics-based lumped element prototype, and (13) from the integral equation formulation, are then compared, and the values of the lumped-circuit elements in the physics-based model can be extracted. Specifically, first, the capacitance and conductance are determined at very low frequencies. N is set to 1 even if there is more than one interconnect, and ωL_1 is negligible, then

$$\frac{1}{\omega(G_b + jC_b)} = [\mathbf{A} - \mathbf{B}\mathbf{D}^{-1}\mathbf{C}]_{N=1}^{-1}. \tag{14}$$

Thus, values of G_b and C_b can be calculated from (14). Then, at other frequencies, based on (15), as shown at the bottom of the next page, all other element values of self and mutual inductances can be solved.

III. Validation of the Procedure

The procedure for extracting a lumped-circuit model developed in the previous section can be validated by performing the circuit simulations at frequencies where the lumped element model applies, and comparing with CEMPIE modeling as well as measured results. The example shown herein is for a PCB dc power-bus structure. As pointed out before, the interplane capacitance model for the power/ground pair is valid only at low frequencies. At frequencies that cause the substrate to exhibit distributed behavior, the lumped-circuit model cannot fully characterize the power-bus structure. Therefore, comparisons between the lumped-circuit simulations and the CEMPIE modeling/measurements are expected to deteriorate as frequency approaches the substrate's lowest distributed resonance frequency and beyond.

Two examples are demonstrated below. Fig. 2 shows a two-layer PCB, with top and bottom planes representing the

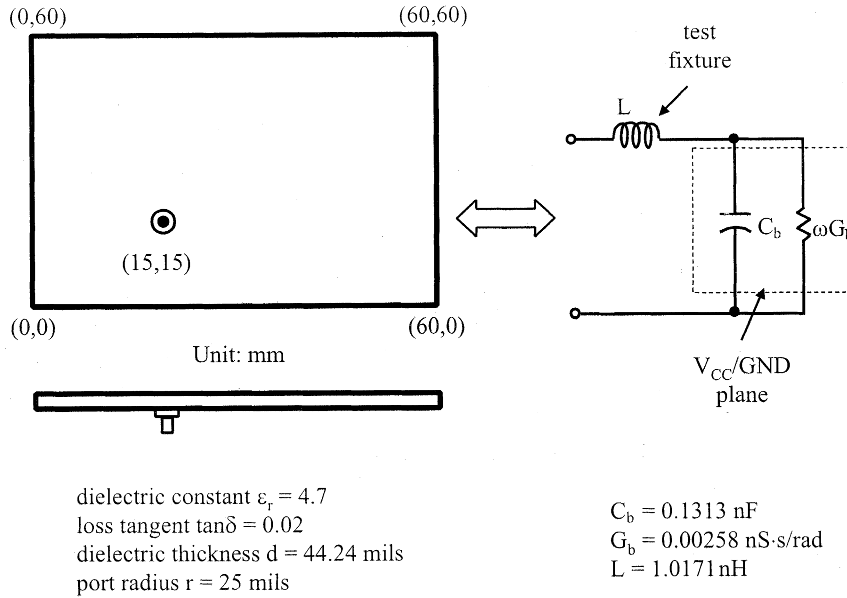

Fig. 2. Extraction of lumped elements from a two-layer PCB with an SMA test probe.

power and ground planes, respectively. A PCB-mounted SMA jack was used as the test probe, which is the only via in this geometry. The equivalent lumped-circuit model was extracted, and the values are listed in Fig. 2. The low-frequency behavior of the input impedance looking into the test port described by the simple lumped-circuit model agrees favorably with the CEMPIE modeling, as well as the measured result, as shown in Fig. 3. Discrepancies arise when the frequency is beyond 700 MHz, which is when the parallel plane geometry starts to exhibit a distributed behavior, and the interplane lumped capacitance does not characterize it well any more.

Fig. 4 shows another test PCB geometry with two vias—a shorting post connecting power and ground planes, as well as a PCB-mounted SMA jack. Again the input impedance looking into the test port was studied. The extraction procedure was applied to extract the lumped element values shown in Fig. 4. The modeled result using the lumped-circuit model is compared with the CEMPIE modeling, as well as measured results in Fig. 5. They compare favorably until the frequency is above 500 MHz, where the distributed behavior of the board is manifested.

IV. Closed-Form Expression for Via Self Inductance

Physically, any inductance is associated with a current loop. In a practical multilayer design, as illustrated in Fig. 6 by a surface mount technology (SMT) decoupling capacitor, the loop inductance that determines the performance of the capacitor is associated with the current loop comprised of both conduction and displacement currents. The conduction currents flow through the two vias connected to the power and ground planes, and traces connecting the capacitors to the vias. The displacement currents complete the current loop from the power plane to the ground plane, and through the capacitor itself. Since the power bus is a two-dimensional (2-D) structure, the portion of the current loop on the power and ground planes cannot be easily determined. However, it will form an area from the via wall to the edge of the substrate, and will be a function of the substrate dimensions, as well as the via location on the substrate.

It is reasonable to assert that thick power/ground layers, most of the loop area lies between the power and ground planes, since the power bus usually has a much bigger scale than the separation between the two vias that determines the rest of the loop area with the trace lengths. For multilayer substrates with thin power/ground separation, the area between the power and ground layers may not be dominant. However, the same procedure can still be used to calculate the total loop inductance. In order to simplify the example, a two-layer power-bus structure with only a via portion between the power and ground planes is studied, and the focus herein is on the inductance associated only with the via portion.

$$\begin{bmatrix} j\omega L_1 + \dfrac{1}{\omega(G_b + jC_b)} & j\omega M_{12} + \dfrac{1}{\omega(G_b + jC_b)} & \cdots & j\omega M_{1N} + \dfrac{1}{\omega(G_b + jC_b)} \\ j\omega M_{21} + \dfrac{1}{\omega(G_b + jC_b)} & j\omega L_2 + \dfrac{1}{\omega(G_b + jC_b)} & \cdots & j\omega M_{2N} + \dfrac{1}{\omega(G_b + jC_b)} \\ \vdots & \vdots & \ddots & \vdots \\ j\omega M_{N1} + \dfrac{1}{\omega(G_b + jC_b)} & j\omega M_{N2} + \dfrac{1}{\omega(G_b + jC_b)} & \cdots & j\omega L_N + \dfrac{1}{\omega(G_b + jC_b)} \end{bmatrix} = [\mathbf{A} - \mathbf{B}\mathbf{D}^{-1}\mathbf{C}]^{-1} \quad (15)$$

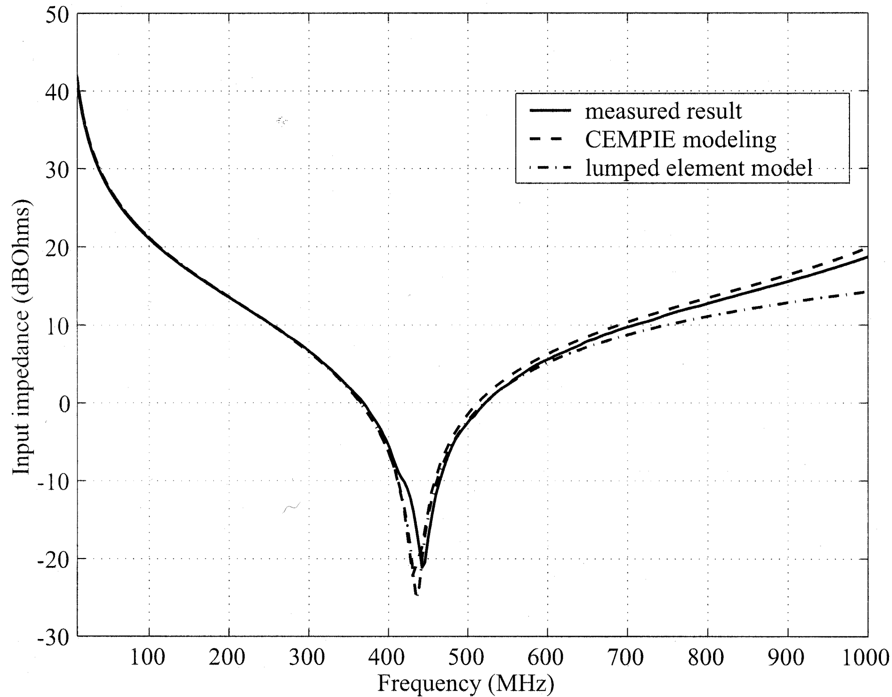

Fig. 3. Comparison between the CEMPIE modeling, measurements, and the lumped-circuit model for the PCB structure shown in Fig. 2.

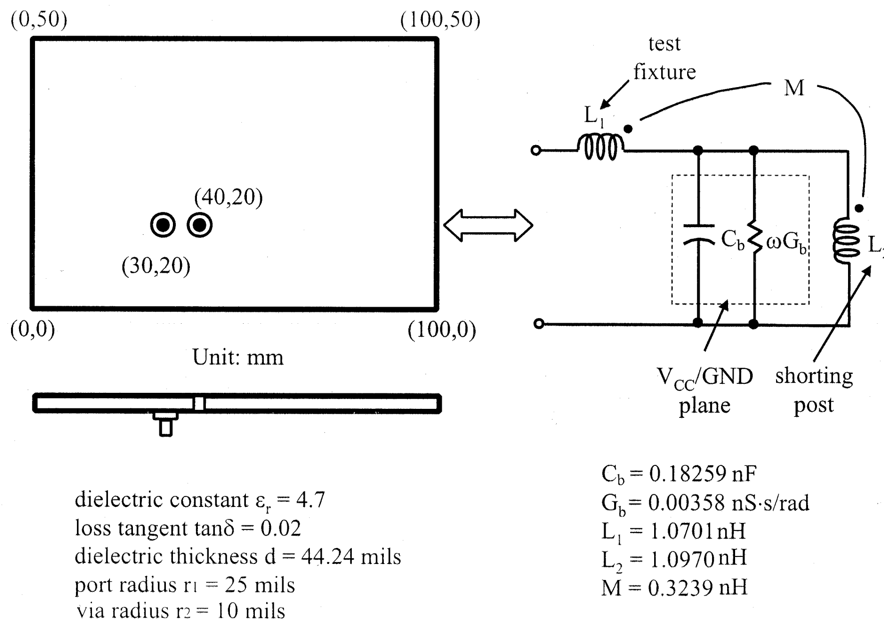

Fig. 4. Extraction of lumped elements from a two-layer PCB with an SMA test probe and a shorting post.

Closed-form expressions for via inductance are particularly useful in practical dc power-bus designs, where full-wave modeling approaches are time-consuming and may be unfamiliar to circuit designers. A practical power plane may have an arbitrary shape, however, most power planes are nearly rectangular. An expression for via inductance in a rectangular power bus can be used to estimate the via inductance for many general power-bus structures.

Power-bus dimensions contribute to the effective via inductance. A circular power bus with a via in the center was studied first because of its perfectly symmetric geometry. In this case, the power-bus contribution can be determined by using its radius in a closed-form expression. According to image theory, if the power bus is infinitely large, the magnetic fields between the two planes due to the current flowing through the via are equal to those resulting from an infinitely long wire with the same diameter of the via. The magnetic field at any observation (field) point is inversely proportional to the distance from that point to the center of the via. The inductance is a function of the magnetic flux associated with the loop from the via

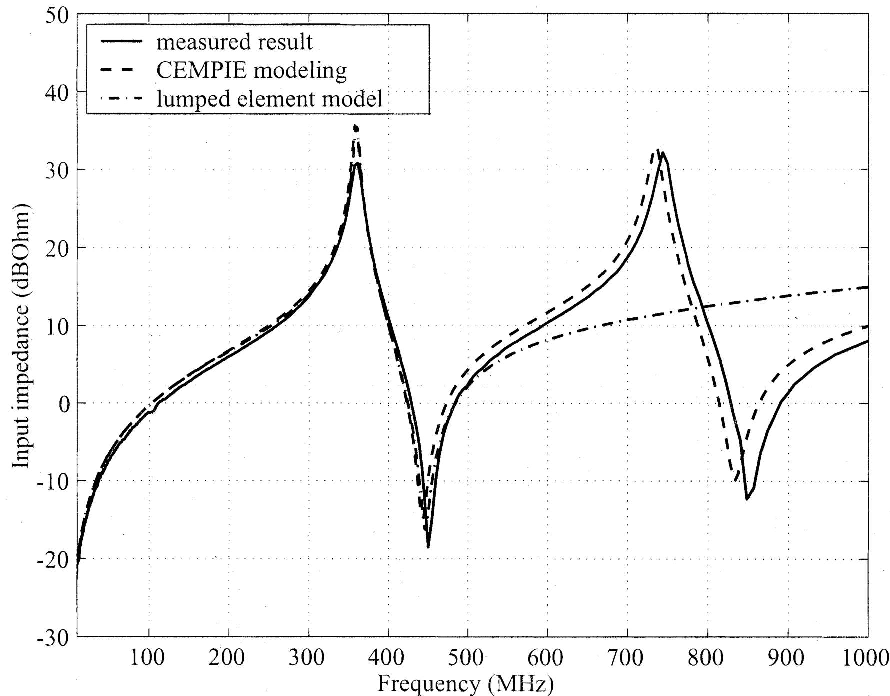

Fig. 5. Comparison between the CEMPIE modeling, measurements, and the lumped-circuit model for the PCB structure shown in Fig. 4.

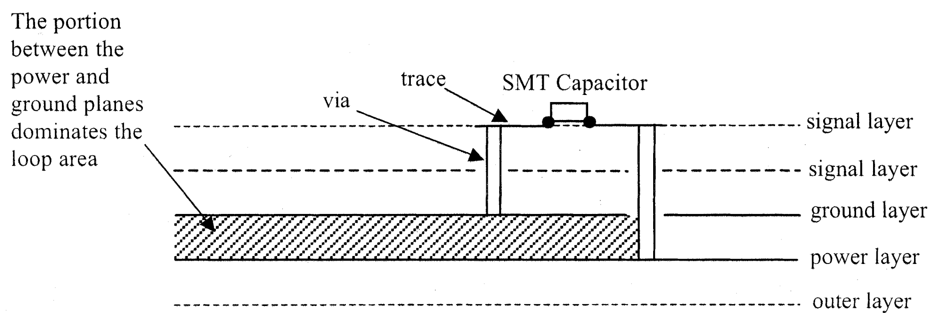

Fig. 6. Current loop for an SMT decoupling capacitor.

wall to the edge of the PCB, which is approximately a function of $d \cdot \ln(R/r)$, where d is the thickness of the power/ground layer, R is the power plane radius, and r is the via radius. This functional dependence provided the basis for a closed-form expression for a rectangular power-bus geometry with appropriate modification factors added. Various scenarios were performed, and the values of the via inductance were calculated from the lumped-circuit extraction procedure. A coefficient that is a function of power/ground separation was obtained by curve fitting. Then, the closed-form expression for a circular power/ground plane pair was modified for a square power bus with a via in its center. Although the power bus does not have radial symmetry with respect to its center, its behavior can be approximated by that of a circular power bus with the same area. As a step further, a rectangular power bus with a via in the center was studied. An additional factor as a function of the ratio between the longer and shorter edges, which was derived by curve fitting, was added to the expression to account for the effect on via inductance due to power plane dimensions.

Via inductance is determined by the current loop of which it is a part, which is complicated in a dc power-bus structure due to its 2-D geometry as described earlier. To form a current loop, the conduction currents flow through a via to the power plane, spread on the plane, and return to the ground plane through displacement current. An equivalent loop can be defined from the via walls to the edge of the board. Obviously, the larger the power bus, the larger the current loop, thus, the larger the via inductance. Furthermore, when a via is located offset from the center of a power bus, some fraction of the current takes the shorter path, i.e., the path to the nearest board edge, while the remaining fraction of the current will take the longer paths to the other edges of the board. The equivalent loop should be an average among all dimensions. Therefore, a larger via inductance, compared to the corresponding case with the via in the center, is

TABLE I
VIA INDUCTANCE FOR THE POWER-BUS STRUCTURE SHOWN IN FIG. 7 WHEN $a = 200$ mm, AND $b = 50$ mm

		x = 50 mm y = 10 mm	x = 30 mm y = 20 mm	x = 10 mm y = 15 mm
d = 20 mils	CEMPIE	0.8833 nH	0.8127 nH	0.6730 nH
	Expression (14)	0.8948 nH	0.8248 nH	0.6852 nH
	Relative difference	1.30%	1.49%	1.82%
d = 40 mils	CEMPIE	1.6870 nH	1.5542 nH	1.2864 nH
	Expression (14)	1.6998 nH	1.5667 nH	1.3016 nH
	Relative difference	0.76%	0.80%	1.19%
d = 60 mils	CEMPIE	2.4503 nH	2.2576 nH	1.8759 nH
	Expression (14)	2.4610 nH	2.2683 nH	1.8845 nH
	Relative difference	0.44%	0.47%	0.46%

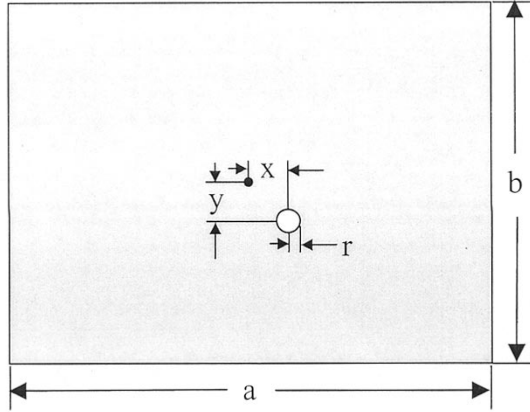

Fig. 7. Via offset from the center of a rectangular power bus.

expected. For an offset via in a rectangular power bus, two additional factors were obtained from curve-fitting to account for the inductance changes due to the offset distances between the centers of the via and the power plane. The closed-form expression for this general case was developed as

$$\begin{aligned} \boldsymbol{L_{ro}} = & \frac{(60893\boldsymbol{d}^2 - 273.622\boldsymbol{d} + 1.952)\boldsymbol{\mu}_0\boldsymbol{d}}{4\pi} \ln\left(\frac{1}{\sqrt{\pi}}\sqrt{\boldsymbol{ab}}/\boldsymbol{r}\right) \\ & \times [0.96 + 0.033\boldsymbol{k_d} + 0.007\boldsymbol{k_d^2}] \\ & \times \left[1 + \left(\frac{0.0045}{\boldsymbol{ab}} + 0.6\right)\boldsymbol{xk_d^{0.4}} \right. \\ & \left. + \left(\frac{1.58}{\boldsymbol{ab}} - 11.3\right)(\boldsymbol{x}/\boldsymbol{k_d^{0.05}})^2\right] \\ & \times \left[1 + \left(\frac{0.0045}{\boldsymbol{ab}} + 0.6\right)\boldsymbol{yk_d^{0.3}} \right. \\ & \left. + \left(\frac{1.58}{\boldsymbol{ab}} - 11.3\right)(\boldsymbol{yk_d^{0.3}})^2\right] \end{aligned} \tag{16}$$

where, as shown in Fig. 7

- a, b length of the longer or shorter edge of the rectangular power bus, in m;
- d separation between the power and ground planes, in m;
- x, y distance between the centers of the via and the power bus, in m;
- r radius of the via, in m;
- k_d dimension ratio, $k_d = a/b$;
- μ_0 permeability of air.

Results from both the lumped-circuit extraction procedure and the closed-form expression, are tabulated in Table I. The via radius was $r = 10$ mils in the tabulated results.

In deriving the closed-form expression, the power/ground layer separation was varied from 10 to 60 mils, the via radius from 2 to 20 mils, the power plane area from approximately 314 to 20 000 mm^2, and the edge ratio from 1 to 5. The relative differences between the results from the lumped-circuit extraction procedure and the closed-form expressions are within 7% for all the studied cases.

V. PREDICTION OF POWER-BUS IMPEDANCE

In practical high-speed digital circuit designs, most implementations of the dc power bus are nearly, though not perfectly, rectangular. Further, some nonrectangular power buses can be approximated into an equivalent rectangular one with the same area. Then, (16) provides a quick and easy way to estimate the via inductance in a general dc power-bus structure, and further gives a good prediction on power-bus impedance at frequencies below distributed resonances, and the effective frequency range of a decoupling capacitor.

Fig. 8 shows an example. The geometry was a two-layer power bus with dimensions of 90 mm × 60 mm. Two SMT decoupling capacitors were added between the power and ground planes. As demonstrated in Fig. 8(b), one end of the capacitors was connected to the ground plane through a via, while the other end was connected to the power plane directly. The input impedance looking into an SMA test port was modeled with two different approaches—the CEMPIE approach, and the lumped-circuit model shown in Fig. 8(c). In both approaches, the capacitor package parasitics were neglected, $C_1 = 0.01$ μF, and $C_2 = 0.25$ μF. For the lumped-circuit model, the via inductances were calculated from the closed-form expression (16), and $L_1 = 1.1878$ nH, $L_2 = 1.1849$ nH, and $L_3 = 1.2032$ nH. The interplane capacitance and conductance were estimated from

$$\boldsymbol{C_b} = \frac{\varepsilon_0\varepsilon_r\boldsymbol{A}}{\boldsymbol{d}} \approx 0.1997 \text{ nF}$$

$$\boldsymbol{G_b} = \frac{\varepsilon_0(\varepsilon_r \tan\delta)\boldsymbol{A}}{\boldsymbol{d}} \approx 0.003\,99 \text{ nS} \cdot \text{s/rad}$$

where A is the area of the power plane, and d is the power/ground layer separation. The input impedance of the lumped circuit was calculated, and compared with the CEMPIE

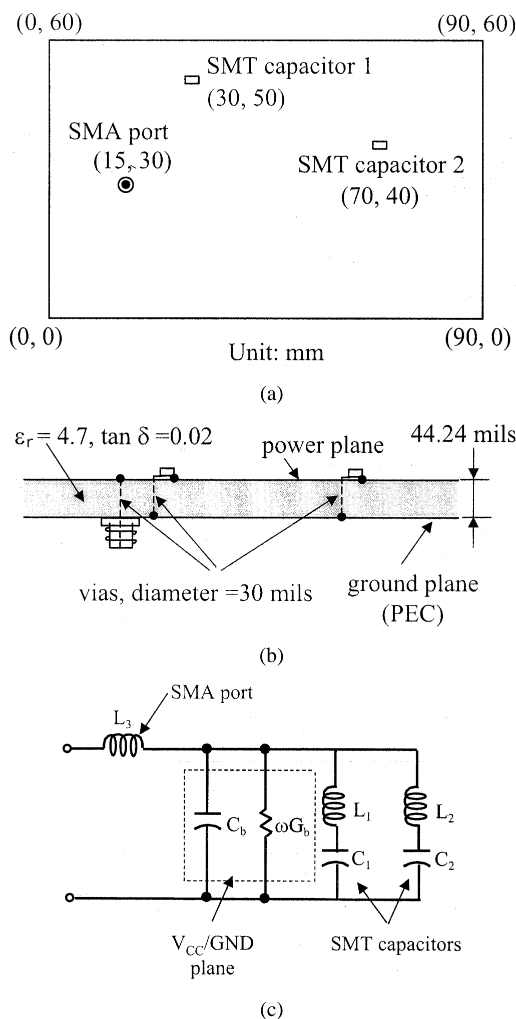

Fig. 8. Prediction of power-bus impedance. (a) Top view of test geometry. (b) Side view. (c) Lumped-circuit model.

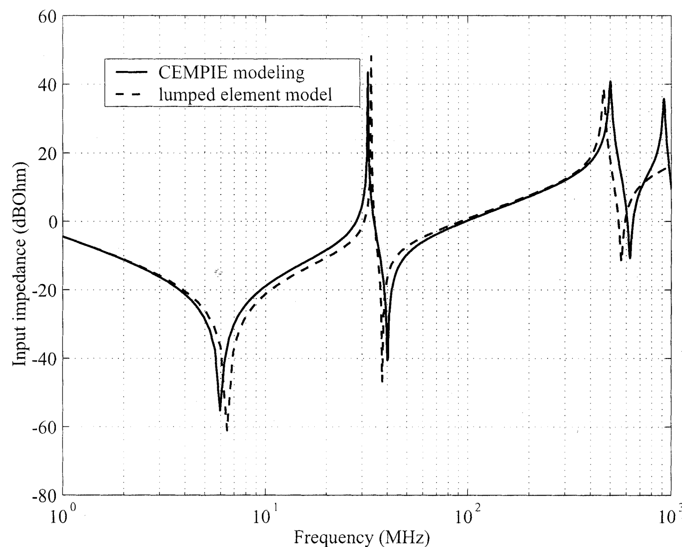

Fig. 9. Comparison of the power-bus impedance results from CEMPIE and the lumped-circuit model.

result in Fig. 9. All interconnects and the test port were modeled in the CEMPIE formulation. The lumped-circuit model gives a good prediction of the power-bus input impedance up to approximately 600 MHz, where the board begins to manifest a distributed behavior. At very low frequencies below the first zero, Capacitor 2 dominates the board impedance (both C_1 and C_b are small relative to C_2). After the first series resonance that is associated with Capacitor 2, the via interconnect inductance dominates C_2, and a parallel resonance occurs due to this inductance and C_1. After the first pole, C_1 becomes dominant. Then, the second zero that is associated with Capacitor 1 occurs, and makes the total impedance of the Capacitor 1 branch inductive. The second pole is due to the interplane capacitance resonating with L_1 in parallel with L_2. At higher frequencies, the interplane capacitance dominates the board impedance, and both SMT decoupling capacitors have lost their effectiveness. The test port inductance series resonating with the interplane capacitance gives the third zero, and then the board-distributed behavior is manifested. From this example, the application of the closed-form expression for via inductance is demonstrated. It can be used for power-bus impedance prediction, and evaluation of decoupling capacitor behavior on PCB and IC package substrates.

VI. Conclusion

A procedure for extracting a lumped-circuit model for via interconnects in multilayer substrates was presented in this paper. The procedure is based on a known lumped-circuit prototype derived from the physics, and an integral equation formulation with circuit extraction. Via inductances in a dc power-bus structure were studied, and the extracted lumped-circuit, with the power/ground planes characterized as an interplane capacitance, captured the low-frequency power-bus behavior quite well when compared with the CEMPIE modeling and measurements. The procedure was also used to develop a closed-form expression for via self inductance in an arbitrary rectangular power bus. This expression worked well with relative differences less than 7% for all the studied cases. It was then used to estimate via self inductance for an example power-bus structure, and further predict the power-bus impedance and effective frequency range of a decoupling capacitor. Although the examples and application were focused on PCB substrates, the procedure itself is applicable for via interconnects in other multilayer substrates.

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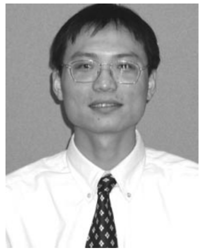

Jun Fan (S'97–M'00) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1994 and 1997, respectively. He received the Ph.D. degree in electrical engineering from the University of Missouri, Rolla, in 2000.

He is currently with NCR Corporation, San Diego, CA, where he works as a Senior Hardware Engineer. His research interests include signal integrity and EMI designs in high-speed digital systems, dc power-bus modeling, PCB noise reduction, and differential signaling.

Dr. Fan received the Conference Best Paper Award from the Applied Computational Electromagnetics Society in 2000. He serves as Secretary of TC-9 Computational Electromagnetics Committee of the IEEE EMC Society.

James L. Drewniak (S'85–M'90–SM'01) received the B.S. (*highest honors*), M.S., and Ph.D. degrees in electrical engineering, all from the University of Illinois, Urbana-Champaign, in 1985, 1987, and 1991, respectively.

In 1991, he joined the Electrical Engineering Department at the University of Missouri, Rolla, where he is a Professor and is affiliated with the Electromagnetic Compatibility Laboratory. His research interests include the the development and application of numerical methods for investigating electromagnetic compatibility problems, packaging effects, and antenna analysis, as well as experimental studies in electromagnetic compatibility and antennas.

He is an Associate Editor of the IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY.

James L. Knighten (S'62–M'77–SM'97) received the B.S. and M.S. degrees in electrical engineering from Louisiana State University, Baton Rouge, in 1965 and 1968, respectively. He received the Ph.D. degree in electrical engineering from Iowa State University, Ames, in 1976.

He is currently with NCR Corporation, San Diego, CA, and serves as a Technical Consultant. Since 1996, he has worked in the field of electromagnetic research interests including the EMI and signal integrity issues related to design of digital computing systems that employ high-speed signaling. Prior to joining NCR, he was with Maxwell Technologies, Inc. and, earlier, with IRT Corporation, San Diego, CA, where he held management positions and was engaged in the study and mitigation design of the lightning, and high-powered microwaves on electronic systems. He has presented numerous technical papers on topics involving various aspects of electromagnetics and taught short courses on electromagnetic pulse effects and electronics survivability both in the USA and in Europe.