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Seven-Level Shunt Active Power Filter for High-Power Drive Systems

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***Abstract*—In high-power adjustable-speed motor drives, such as those used in electric ship propulsion systems, active filters provide a viable solution to mitigating harmonic related issues caused by diode or thyristor rectifier front-ends. To handle the large compensation currents and provide better thermal management, two or more paralleled semiconductor switching devices can be used. In this paper, a novel topology is proposed where two active filter inverters are connected with tapped reactors to share the compensation currents. The proposed active filter topology can also produce seven voltage levels, which significantly reduces the switching current ripple and the size of passive components. Based on the joint redundant state selection strategy, a current balancing algorithm is proposed to keep the reactor magnetizing current to a minimum. It is shown through simulation that the proposed active filter can achieve high overall system performance. The system is also implemented on a real-time digital simulator to further verify its effectiveness.**

***Index Terms*—Active filters, harmonic analysis, power conversion, power electronics.**

I. Introduction

ADJUSTABLE-SPEED motor drives (ASDs) have found extensive application in a variety of high-power systems. One example is the electric propulsion system used in modern naval ships, the power ratings of which can be tens of megawatts. Typically, the front-ends of such ASDs employ a diode or a thyristor rectifier. In spite of their simple control and robust operation, these devices can generate voltage and current harmonics that might affect the operation of other devices in the same ac system. Conventionally, passive LC filters are used to mitigate harmonic-related problems. However, due to their large size and inflexibility, passive filters are gradually being replaced by active filters that utilize power electronic inverters to provide compensation for harmonics [1].

Among various active filter configurations, the shunt active filter systems have a number of advantages and constitute the optimal harmonic filtering solution for ASD rectifier front-ends [2]. In general, the ratings of shunt active filters are based on the rms compensating current and the rms filter terminal voltage. For high-power applications such as ship propulsion systems, the large compensation current often requires parallel operation of two or more switching devices or active filters.

In recent years, multilevel converters have shown some significant advantages over traditional two-level converters [3]–[5], especially for high-power and high-voltage applications. In addition to their superior output voltage quality, they can also reduce voltage stress across switching devices. Since the output voltages have multiple levels, lower $\mathrm{d}v/\mathrm{d}t$ is achieved, which greatly alleviates electromagnetic interference problems due to high-frequency switching. Over the years, most research work has focused on converters with three to five voltage levels [4], [5], although topologies with very high number of voltage levels were also proposed [6]. In general, the more voltage levels a converter has, the less harmonic and better power quality it provides. However, the increase in converter complexity and number of switching devices is a major concern for a multilevel converter. It has been shown that although more voltage levels generally mean lower total harmonic distortion (THD), the gain in THD is marginal for converters with more than seven levels [7].

This paper presents a shunt active filter configuration that uses tapped reactors for harmonic current sharing. It reduces current stress of the switching devices by distributing the compensation current between two parallel legs of an H-bridge topology. It also reduces voltage stress across the switches by utilizing a conventional three-level flying capacitor topology. Overall, the configuration is capable of producing seven distinct voltage levels, and thus, greatly reduces switching ripple in the compensating currents. The concept of the configuration was introduced in a previous conference publication [8]. Herein, more detail of the topology and control are presented. Additional simulation studies are also carried out as well as corresponding studies using a real-time digital simulator (RTDS). The studies herein are also conducted on a full motor drive system, whereas in the previous work, the system was supplying a resistive load.

The rest of this paper is organized as follows. The active filter topology is briefly described in Section II. The control algorithm of the active filter is discussed in Section III. Simulation results are presented in Section IV to evaluate the proposed configuration and control. In addition, the system is implemented on RTDS hardware to further validate the proposed active filter, and the results are also presented in Section V. Finally, the conclusions are given in Section VI.

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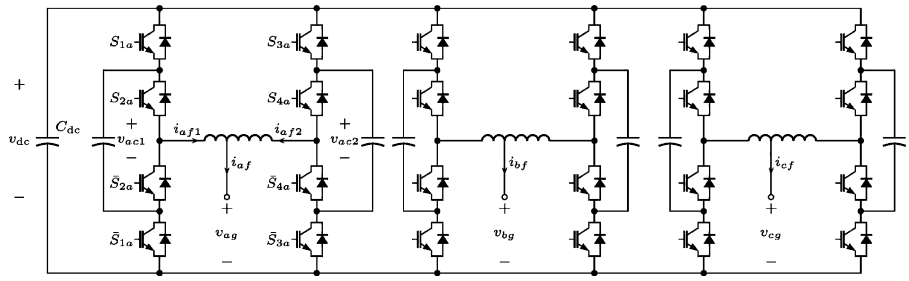

Fig. 1. Proposed seven-level active filter topology.

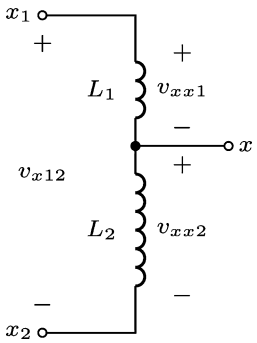

Fig. 2. Ideal tapped reactor model.

TABLE I
ACTIVE FILTER LINE-TO-GROUND VOLTAGES

s_a	v_{a1}	v_{a2}	v_{ag}
0	0	0	0
1	0	$v_{dc}/2$	$v_{dc}/6$
2	$v_{dc}/2$	0	$v_{dc}/3$
2'	0	v_{dc}	$v_{dc}/3$
3	$v_{dc}/2$	$v_{dc}/2$	$v_{dc}/2$
4	$v_{dc}/2$	v_{dc}	$2v_{dc}/3$
4'	v_{dc}	0	$2v_{dc}/3$
5	v_{dc}	$v_{dc}/2$	$5v_{dc}/6$
6	v_{dc}	v_{dc}	v_{dc}

II. ACTIVE FILTER TOPOLOGY

The proposed active filter topology is shown in Fig. 1. It consists of an H-bridge configuration made from three-level flying capacitor branches. Essentially, it is a voltage-source inverter (VSI) with capacitive energy storage ($C_{\rm dc}$) shared by all three phases. A total of eight switching devices are used in each phase.

A tapped reactor is used to connect the two legs of the H-bridge. Typically, the reactor is wound to be center tapped, making the output line-to-ground voltages (v_{ag} for example) the average of the voltages from each side of the H-bridge. Then, the line-to-ground voltages will have five distinct voltage levels [9]–[12]. However, with this topology, the tap is set at 1/3. This results in seven distinct output voltages, and therefore, improves the power quality. The switching operation is described next, wherein all seven levels are clearly illustrated.

A. Tapped Reactor Model

Unlike the center-tapped interphase reactor [9]–[12], the reactor in the proposed topology has a tap terminal at its one-third position, as shown in Fig. 2. For the convenience of analysis, the reactor can be divided into two parts. In Fig. 2, part one, denoted as L_1, consists of the portion from terminal $x1$ to the tap and has a number of turns $N_1 = N$; part two, denoted as L_2, consists of the portion from the tap to terminal $x2$ and has a number of turns $N_2 = 2N$. Terminals $x1$ and $x2$ are defined as the input terminals while the tap terminal is defined as the output terminal x.

To derive the relationship between the input voltages and the output voltage, an ideal model of the tapped reactor is considered first in which there are no losses and no leakage flux. The following assumptions are made.

1) The core of the reactor is highly permeable in a sense that it requires vanishingly small magnetomotive force to set up the flux.
2) The core does not exhibit any eddy current or hysteresis loss.
3) All the flux is confined in the core, so there is no leakage flux.
4) The resistance of the reactor is negligible.

Suppose that voltages v_{x1} and v_{x2}, with respect to a common ground, are applied to the input terminals $x1$ and $x2$, respectively. For this ideal model, it is straightforward to determine the voltage between the output terminal x and terminal $x2$

$$v_{xx2} = \left(\frac{N_2}{N_1 + N_2}\right)(v_{x1} - v_{x2}) = \frac{2}{3}(v_{x1} - v_{x2}). \quad (1)$$

The voltage at the output terminal with respect to the common ground is therefore

$$v_{xg} = v_{xx2} + v_{x2} = \frac{2}{3}v_{x1} + \frac{1}{3}v_{x2}. \quad (2)$$

In the general analysis presented earlier, x represents a phase, and the phase may be a, b, or c. Each leg of the H-bridge has a voltage-clamping capacitor, and the voltages at the two input terminals of the reactor can be 0, $v_{\rm dc}/2$, or $v_{\rm dc}$, where $v_{\rm dc}$ is the nominal voltage of the capacitor $C_{\rm dc}$, as shown in Fig. 1. For each phase, there are nine different switching states, corresponding to nine terminal voltage combinations. These combinations can produce a line-to-ground voltage at the output terminal that has seven distinct voltage levels. For phase a, these states are detailed in Table I.

In Table I, s_a is the switching state that is defined as being 0 for the lowest possible line-to-ground voltage. The voltages v_{a1}

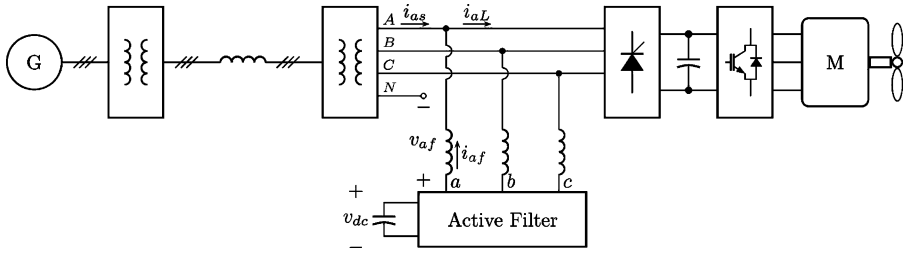

Fig. 3. Active filter connection to a shipboard power system.

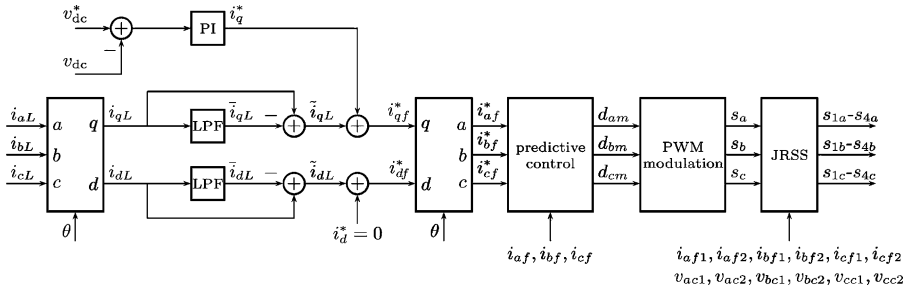

Fig. 4. Active filter control diagram.

and v_{a2} are the line-to-ground voltages applied to the left and right side of the reactor in Fig. 1, respectively. The voltage v_{ag} is as defined in Fig. 1 and calculated using (2). Note that there are two redundant states $2'$ and $4'$ that produce the same voltage as states 2 and 4, respectively. However, these are not desirable, and will be ignored, because the voltages applied across the reactor are twice as high as the other states. The output current for each phase is split between the two legs of the H-bridge structure. Ideally, two-thirds of the current will come from $x1$ and one-third from $x2$ so that the magnetizing current is zero. The control given later discusses the regulation of the reactor currents so as to minimize the magnetizing current.

B. Active Filter Interface

As shown in Fig. 3, the active filter is connected to the power system via a three-phase inductor L_f. The filtering function is achieved by injecting a compensating harmonic current into the point of common coupling of the utility–load interface, which in this case is the secondary side of the rectifier load transformer. The reference harmonic currents are extracted from the load currents so that the sum of the load currents and the injection currents has a THD that meets required specifications. The seven-level inverter can produce an output voltage that contains much less switching frequency ripple than a conventional two-level inverter; thus, the generated injection currents are smoother and the coupling inductor can be reduced.

According to the inverter equations, the line-to-neutral voltage v_{af} depicted in Fig. 3 can be related to the inverter line-to-ground voltages by [13]

$$v_{af} = \frac{2}{3}v_{ag} - \frac{1}{3}v_{bg} - \frac{1}{3}v_{cg}. \tag{3}$$

Having established the model for the proposed active filter, the following section describes the details of the control.

III. Active Filter Control

To effectively compensate the load harmonic currents, the active filter controller should be designed to meet the following three goals:

1) extract and inject load harmonic currents;
2) maintain a constant dc capacitor voltage;
3) avoid generating or absorbing reactive power with fundamental frequency components.

A. Harmonic Current Extraction

For diode or thyristor rectifier loads, the most common harmonic currents are of the 5th, 7th, 11th, and 13th order. Although a high-pass filter can be used to extract these components directly from the line currents, it is not feasible to obtain high attenuation at the fundamental frequency due to the high current amplitude. The synchronous q–d reference frame controller developed for shunt active filter systems is used to generate the reference compensating current [2]. As shown in Fig. 4, the measured load phase currents (i_{aL}, i_{bL}, and i_{cL}) are first transformed into the synchronous reference frame to obtain i_{qL} and i_{dL}. The synchronous reference frame phase angle can be obtained by processing the measured system voltage with a phase-locked loop circuit or algorithm. Low-pass filters are then used to extract the dc components, which correspond to the fundamental frequency components of the load currents. The dc component is removed by a simple subtraction of the filtered components ($\bar{i}_{qL}$ and $\bar{i}_{dL}$) and the transformed components (i_{qL} and i_{dL}).

B. DC Capacitor Voltage Control

For the active filter to operate effectively, it is important to maintain the dc capacitor voltage at a constant value. Since the active filter topology is essentially identical to that of an active

rectifier, similar control strategies for the active rectifier are applicable.

The dc capacitor voltage is directly affected by the real power transferred across the active filter. To keep the voltage constant, ideally, no real power should be transferred. However, due to losses in switching devices and other components, a small amount of real power is needed. In the synchronous reference frame with the q-axis aligned with the voltage at the point of common coupling, the real power transferred can be expressed as

$$P = \frac{3}{2} v_{qs} i_{qf} \tag{4}$$

which means that by adjusting the q-axis filter current, the real power can be effectively controlled. The capacitor voltage regulation is then handled by a simple proportional-integral (PI) control adding to the q-axis filter current, as shown in Fig. 4.

C. Reactive Power Control

In most cases, a unity power factor for fundamental frequency components is required at the active filter terminals. Since the reactive power can be expressed as

$$Q = \frac{3}{2} v_{qs} i_{df} \tag{5}$$

this goal can be achieved by keeping the average d-axis current at zero, as shown in Fig. 4. The combined control of dc capacitor voltage and reactive power uniquely determines the fundamental frequency component of the active filter output current. This current is then superimposed onto the commanded harmonic currents, and the commanded filter currents i^*_{af}, i^*_{bf}, and i^*_{cf} are obtained by the reverse transformation, as shown in Fig. 4.

D. Harmonic Current Regulator

A current regulator is needed to generate the commanded compensation current. Generally, a hysteresis control provides fast response and is suitable for nonsinusoidal current tracking. However, it suffers from some serious disadvantages such as variable switching frequency and phase interaction problems [1]. In addition, to fully take advantage of the benefits of a multilevel converter, a current regulator that uses a voltage-source pulsewidth modulation (PWM) is desirable. Several frequency-selective harmonic current regulators were proposed in [14]–[17] that achieve zero steady-state error for the dominant harmonics. Nonetheless, they all have to target specific frequencies and require a significant amount of computation time.

In this paper, a predictive current regulator is implemented to track the harmonic currents, which has the advantages of simple structure and less computational requirement. Given the measured system voltages and filter inductor currents, the required phase a filter voltage can be calculated based on the known value of the filter inductance

$$v^*_{af} = \hat{v}_{as} + \frac{(\hat{i}^*_{af} - i_{af}) L_f}{\Delta t} \tag{6}$$

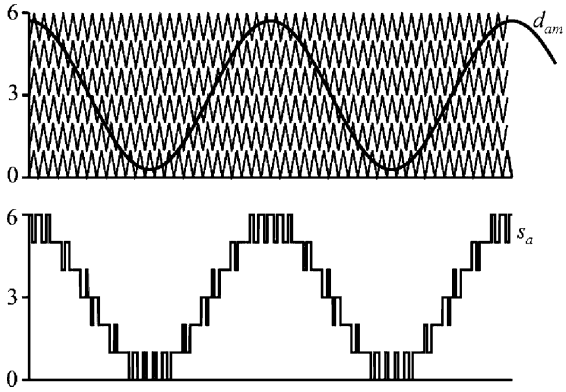

Fig. 5. Seven-level voltage-source modulation.

where Δt is the controller switching period, $\hat{v}_{as}$ is the predicted source voltage and can be calculated through linear extrapolation

$$\hat{v}_{as} = v_{as}(t) + 1.5\Delta t\ [v_{as}(t) - v_{as}(t - \Delta t)] \tag{7}$$

and $\hat{i}^*_{af}$ is the predicted reference harmonic current

$$\hat{i}^*_{af} = i^*_{af}(t) + 2\Delta t\,[i^*_{af}(t) - i^*_{af}(t - \Delta t)]. \tag{8}$$

For accurate current tracking, the prediction takes into account the controller delay due to data acquisition and calculation. Better performance has been achieved when a second-order prediction method is used.

As can be seen, the predictive control effectively turns the commanded currents into commanded voltages suitable for a voltage-source modulator. These commanded voltages are then expressed as PWM duty cycles by normalizing them to the dc voltage and giving them an appropriate range. For phase a, the duty cycle can be expressed as

$$d_{am} = \left(\frac{v^*_{af}}{v_{\rm dc}} + 0.5 \right) (n - 1) \tag{9}$$

where n is the number of voltage levels, which for this topology is $n = 7$. Similar expressions can be written for phase b and phase c. The predictive control is shown in Fig. 4 having outputs to the PWM modulator, which is described next.

E. Multilevel Voltage-Source Modulation

The seven-level voltage-source modulation is accomplished by comparing the duty cycles with a set of six carrier waveforms. This is illustrated for phase a in Fig. 5. The resulting switching state s_a is the number of triangle waveforms that the duty cycle is greater than. Therefore, the switching state has a range of 0–6, and this is in agreement with Table I.

F. Capacitor Voltage Balancing

After carrying out the modulation, the switching states for each phase need to be broken out into transistor signals. In order to have the correct voltage levels, the flying capacitors must remain charged at exactly $v_{\rm dc}/2$. This can easily be assured using the redundancy of the inverter legs.

TABLE II
FLYING CAPACITOR VOLTAGE BALANCING

s_{1a}	s_{2a}	v_{a1}	i_{af1}	Charging
0	0	0	+	0
0	0	0	–	0
1	1	v_{dc}	+	0
1	1	v_{dc}	+	0
0	1	$v_{dc}/2$	+	–
0	1	$v_{dc}/2$	–	+
1	0	$v_{dc}/2$	+	+
1	0	$v_{dc}/2$	–	–

For each leg of the H-bridge structure, there are four switches and a total of four switching states. Two of the switching states can produce the same $v_{\rm dc}/2$ output, which provides great flexibility for capacitor charging and discharging. Table II shows the relationship between switching states, output current direction, and capacitor charging/discharging, where the left leg of phase a bridge is used as an example. The designations of the variables can be found in Fig. 1. The $+$ and $-$ signs for the output current denote the polarity of the current. The charging status of the flying capacitor can be $+$ (charging), $-$ (discharging), or 0 (neither charging nor discharging). It can be seen that for state (s_{1a}, s_{2a}) = (0, 0) and (1, 1), output current does not flow through the flying capacitor; therefore, the capacitor voltage does not change. The two redundant states (1, 0) and (0, 1) produce the same output voltage $v_{\rm dc}/2$. Both can be used to charge or discharge the capacitor, depending on the direction of output current. For example, if the output current is positive, one can pick (1, 0) to charge the flying capacitor, or pick (0, 1) to discharge it. This simple decision is made instantaneously online depending on the state of charge of the flying capacitors.

G. Magnetizing Current Minimization

The current through the reactor consists of two components. One is the compensating current that flows out of the tap terminal and is shared by the two parts of the reactor. The other is the magnetizing current that is generated when an average voltage is applied across the reactor input terminals. The magnetizing current does not contribute to the filtering function and should be minimized to reduce current ratings of the switching devices and avoid reactor saturation. Ideally, the magnetizing current has a zero average component. In practice, however, the magnetization current tends to drift away from zero if uncontrolled because of the differences in component parameters and controller errors. Therefore, it is necessary to monitor and control the magnetizing currents of the reactors in each phase so that their values are within a limited range. Let the magnetizing current in phase a be i_{am}, then the following relationship holds if two-thirds of the filter current is to come from the left side of the reactor

$$i_{am} = 2i_{af2} - i_{af1}. \tag{10}$$

The magnetizing current can be minimized by balancing the average voltage applied across the tapped reactor. Among the seven switching states in Table I, the states ($v_{a1} = 0$, $v_{a2} = 0$), ($v_{a1} = v_{\rm dc}/2$, $v_{a2} = v_{\rm dc}/2$), and ($v_{a1} = v_{\rm dc}$, $v_{a2} = v_{\rm dc}$) have no effect on the magnetizing current, while the other four states can either increase or decrease the magnetizing current. Since states $2'$ and $4'$ are not used, there is no usable per-phase redundant state. Thus, the magnetizing current of each phase cannot be adjusted independently. In this paper, a technique similar to the joint-phase redundant states selection (JRSS) method proposed in [7] is used to minimize the magnetizing currents. The concept behind JRSS is that for a three-phase inverter, the line-to-ground voltages of all phases may be changed simultaneously without affecting the load voltages since the terms that are common in all phases will cancel when looking at the line-to-line voltages or line-to-neutral voltages, as seen by (3).

The magnetizing current minimization procedure is as follows. At the beginning of each switching period, the magnetizing current for each phase is calculated. Suppose the commanded voltage levels are s_i, where $i = a, b, c$, and $0 \le s_i \le 6$. The number of available joint redundant states is

$$k = \min(s_i) + 6 - \max(s_i). \tag{11}$$

Each redundant state specifies the three-phase active filter voltage levels. Based on Table I, the voltage applied across the reactor for each phase and whether the magnetizing current increases, decreases, or does not change can be determined. If the magnetizing inductance L_m is known, the change in the current (for phase a) can be calculated as

$$\Delta i_{am} = \frac{v_{a1} - v_{a2}}{L_m} \Delta t \tag{12}$$

where v_{a1} and v_{a2} are voltages at the two terminals of the reactor and Δt is the duration of the state. The change in current as predicted by (12) is used along with the measured value of magnetizing current to predict the value of magnetizing current at the next controller time step. The switching state that results in the minimum predicted magnetizing current for all three phases is selected.

The calculation block representing the JRSS control is shown at the output of the modulator in Fig. 4. The inputs are taken as switching states from the modulator, which represent commanded voltage levels. The JRSS block performs the calculations as described earlier and determines a new set of states that will lead to minimized magnetization currents. As a practical matter, the flying capacitor voltage regulation is also performed in this block. The outputs are transistor signals, as labeled in Fig. 1. It should be pointed out that this block also reads in analog information of the flying capacitor voltages and the reactor currents to perform this regulation. Therefore, it is a feedback control that compensates to minimize magnetization current.

IV. SIMULATION RESULTS

Numerical simulations have been conducted in the Advanced Continuous Simulation Language (ACSL) to validate the proposed topology. The example naval ship power system has a rated line-to-line voltage of 4.16 kV and a three-phase six-pulse diode rectifier. A three-phase PWM inverter is connected to the rectifier dc bus, and supplies power to a permanent-magnet synchronous motor load. The rated dc capacitor voltage of the

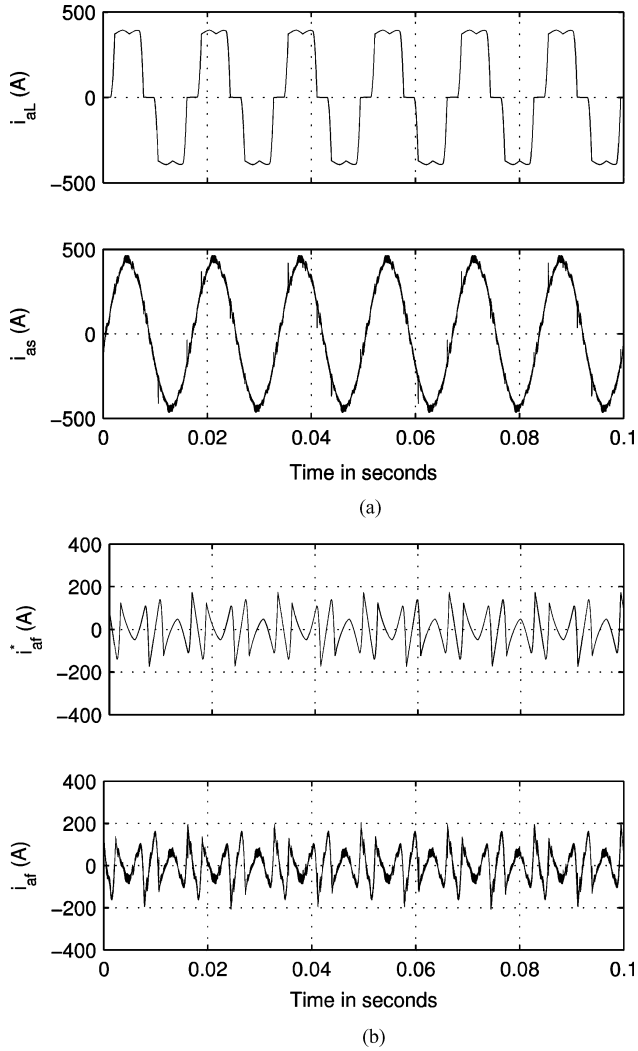

Fig. 6. Active filter detailed simulation results.

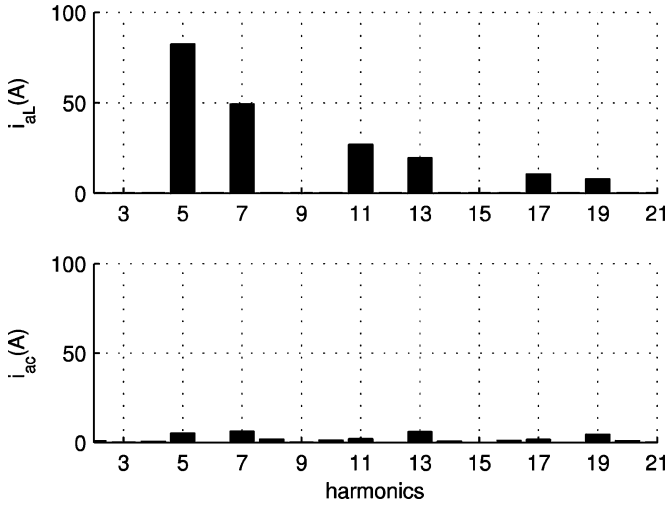

Fig. 7. Harmonic magnitude in load and source currents.

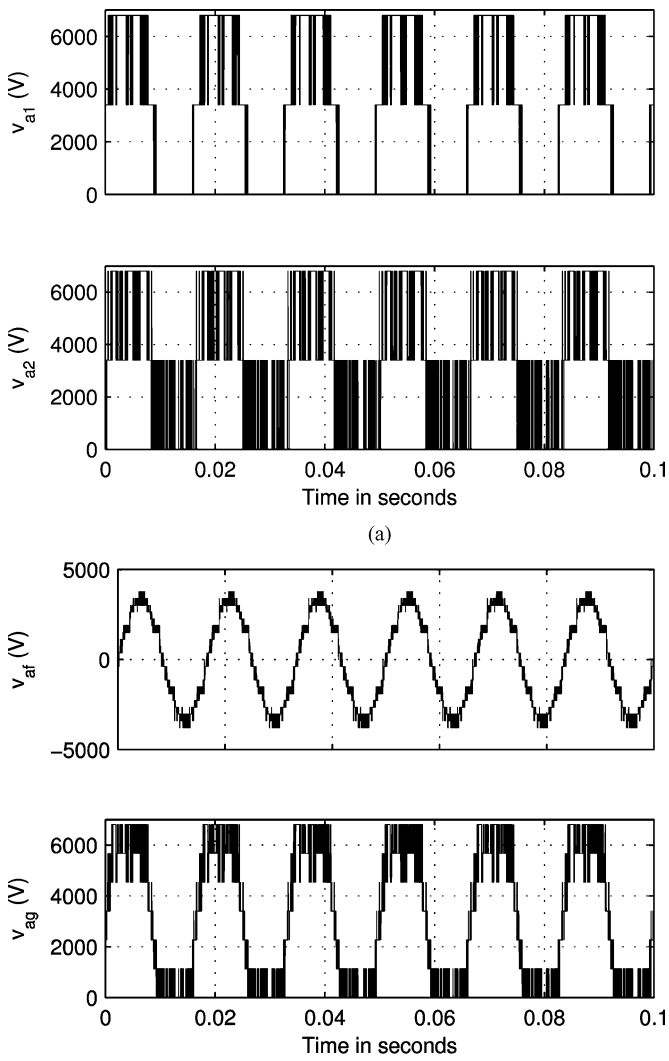

Fig. 8. Reactor terminal and output voltages.

active filter is 6800 V. The three-phase tapped reactor has a leakage inductance of $L_l = 50$ μH, winding resistance $r = 0.1$ Ω, and mutual inductance $L_M = 1$ H. The active filter interface inductance is $L_f = 0.1$ mH.

Fig. 6 shows the phase a operation of the active filter with a rectifier load. As can be seen, the load current i_{aL} contains a significant amount of harmonics. The active filter produces multilevel voltages that generate a current i_{af} to cancel the harmonic contents. The compensated source current i_{as} contains much less harmonics than i_{aL}. The magnitudes of the harmonic spectrum of the load and source currents are shown in Fig. 7. The THD of the load current is 25.1%, which is reduced to about 4.4% in the compensated source current. The source current still contains a certain amount of higher frequency components. However, they are generally not a concern and can easily be removed by passive filters.

To illustrate the generation of seven voltage levels, Fig. 8(a) shows the phase a line-to-dc-ground voltages applied at each end of the tapped reactor. These two voltages are produced by the flying capacitor legs and have three levels. The phase a converter-side line-to-neutral output voltage v_{af} from the ACSL

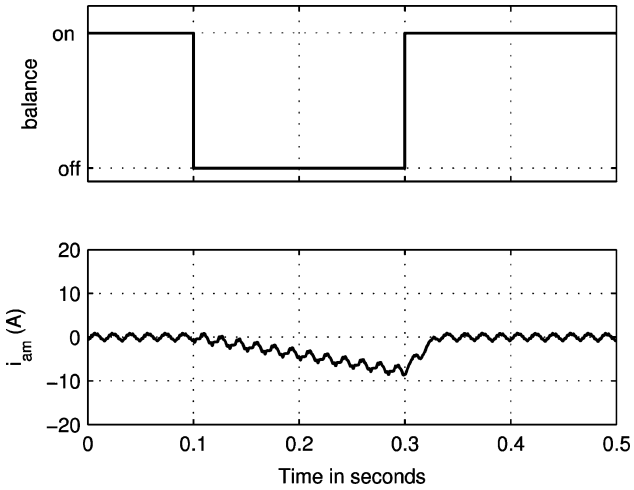

Fig. 9. Magnetizing current with and without the balancing algorithm.

simulation is shown in Fig. 8(b). Multiple voltage levels give the voltage a smooth shape that reduces injection current ripple. Also shown in Fig. 8(b) is the reactor output terminal to dc ground voltage v_{ag}, which has seven distinct levels. Note that because of joint redundant state selection, common-mode components are added to the line-to-ground voltages, which cause the irregular shape of v_{ag}.

The effectiveness of the magnetizing current control is tested in simulation and illustrated in Fig. 9. The top part of Fig. 9 shows whether the JRSS current balancing algorithm is turned on or off, and the bottom part shows the magnetizing current in phase a. Initially, the balancing is ON, and it can be seen that the magnetizing current is kept within a small range with a very low dc component. At time $t = 0.1$ s, the balancing algorithm is turned off, and the magnetizing current drifts away from zero and keeps decreasing. In practice, a large magnetizing current can cause the iron core to saturate and eventually damage the reactor and switching devices. When the balancing method is turned on again, the magnetizing current returns to its minimum value.

V. Validation With RTDS Hardware

To further evaluate the performance of the proposed active filter, a real-time simulation model for the same system described earlier is also implemented. The modeling is based on RTDS hardware [18], which is a fully digital electromagnetic transient power system simulator that operates in real time. Because the solution is in real time, the simulator can be connected directly to a hardware controller or other devices. Thus, real-time simulation provides a convenient way for network-level power system analysis and equipment test. The implementation of the proposed active power filter model in RTDS hardware is quite different from simulation design with regular nonreal-time continuous/discrete simulators. On the one hand, technical difficulties arise due to hardware limitations. The inherent computational delay (75 μs in the setup) may cause instability for the close-loop controller, and the issue must be addressed with appropriate choice of control algorithms. The switch model, which is designed mainly for operation under fundamental frequency

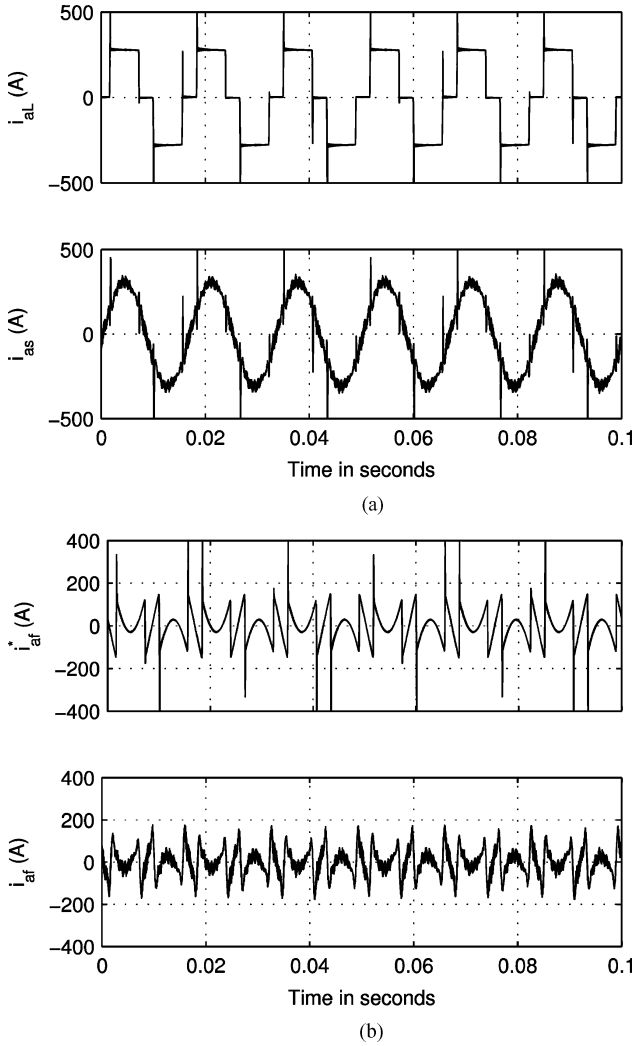

Fig. 10. Active filter RTDS hardware results.

conditions, must be properly configured to work at high switching frequency and pass harmonic currents. On the other hand, the parallel structure of the current regulator makes it suitable to be implemented on the platform, because different harmonic channels can be processed in parallel by multiple processors. Fig. 10 shows the waveforms from the RTDS hardware. As can be seen, these compare well to the detailed simulation results.

VI. Conclusion

A new type of power converter has been introduced in this paper. The converter is based on parallel connection of phase legs through an interphase reactor. However, the reactor has an off-center tap at one-third resulting in an increased number of voltage levels. Specifically, two three-level flying capacitor phase legs are paralleled in this way to form a seven-level power converter. The converter is utilized in an active filter application. The details of the high-level control as well as the switching control have been presented. The control ensures reactor current sharing as well as flying capacitor voltage balance. The proposed active filter has been validated for a naval ship board power system using detailed simulation and RTDS hardware.

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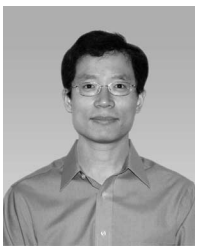

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