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Noise Coupling Between Power/Ground Nets Due To Differential Vias Transitions in a Multilayer PCB

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Abstract— **Due to the increase in board density, routing traces on different layers becomes a widely used strategy. Through-hole vias are often used to connect these traces. Those vias that penetrate power/ground plane pairs could cause noise coupling between signal and power/ground nets. At the same time, the need for clean signal transmitted to receivers results in a wide use of differential signals. This paper studies the noise coupling mechanism caused by a differential pair of vias penetrating power/ground plane pair using a physics-based via-plane model combined with transmission line models for traces. A 26-layer printed circuit board with a pair of differential vias have been modeled. The simulated results clearly demonstrate the impact of ground vias and via stubs on noise coupling.**

Keywords—**Differential signal, noise coupling between signal and power/ground nets, signal via transition, via capacitance, cavity model, ground vias, via stub**

I. INTRODUCTION

Signal vias are extensively used to route signals from one layer to another due to the increasing component density on the printed circuit board surfaces. In addition to the simultaneous switching noise (SSN), signals transitioning through power/ground plane pair can also be a source of power bus noise [1-2].

The noise coupling from the signal to the power/ground nets can be explained by considering the current return path. Even if ground vias and decoupling capacitors are placed adjacent to the signal, a portion of current will return to its source by means of the displacement current between the power/ground planes.

Similarly, noise can also be coupled from power/ground nets to signal nets [7]. The noise from the power and ground planes may affect the integrity (quality) of the high-speed signal that propagates through the vias.

This paper studies the noise coupling problems between the signal and power/ground nets due to differential via transition, using a physics-based via-plane model combined with transmission line models for traces. Noise on power planes generates by signal via transitions as well as time- and frequency-domain effects on signal transmission due to power bus noise are shown in the following sections.

II. MODELING APPROACH AND TEST GEOMETRY

The modeling approach used in this paper is based on the segmentation method [3]. The geometry under study is divided in transmission-line regions and a via-plane region. These regions are modeled separately first, and then are connected by enforcing current and voltage continuities.

The specific test geometry is shown in Figure 1. It includes a 26-layer printed circuit board and two coupled signal vias transitioning a differential signal from the microstrip lines on the top surface of the PCB to striplines on inner layers. The printed circuit board has 12 solid planes for power supply and current return. The dimensions of the printed circuit board are 12″×10″, and the coupled microstrips and striplines with a 100Ohm differential impedance are both 200mils long. All the dielectric layers are assumed to have a dielectric constant of 4.4, and a loss tangent of 0.02. The signal vias are located at (6″, 4″) from the lower left corner of the board, spaced by 60mils center-to-center. The via radius is 11mils. Two ports (Ports 5 and 6 in Figure 1) between two inner planes are chosen to represent the ports in a power/ground plane pair. Ports 1 and 3 are located at the ends of the top microstrip traces, and port 2 and 4 at the ends of the striplines, as shown in Figure 1.

The multilayer PCB geometry is divided into multiple blocks at the middle of each solid plane. This approach is valid since a perfect TEM coaxial mode exists in the antipad regions. This means well-defined voltages and currents exist at every interface between the blocks. Figure 2 illustrates a typical block except the top and bottom ones that are microstrip structures. As clearly shown in Figure 2(a), the geometry of every block includes a pair of planes and multiple via portions that may or may not be connected to the planes. The corresponding equivalent circuit model is shown in Figure 2(b), where a capacitor exists between a via portion and a

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plane if the via portion is not connected to the plane. The plane pair is modeled as a multi- port impedance matrix, where a port is at every via portion. This via-plane model consisting of the cascading blocks is physics-based [4, 6].

The equivalent circuit model for the entire test geometry was established using the previously introduced approach, and is shown in Figure 3. In this simplified model, the ground vias are not shown. There are eleven blocks in the model associated with the eleven plane pair. The via-plane capacitances are between the signals (direct path) and every plane. In this geometry under study, all the solid planes except plane 4 (a power plane) are considered to be ground planes. For the sake of simplicity, only the equivalent circuit for a through transition from the top microstrips to the bottom microstrips thru configuration) is shown in Figure 3.

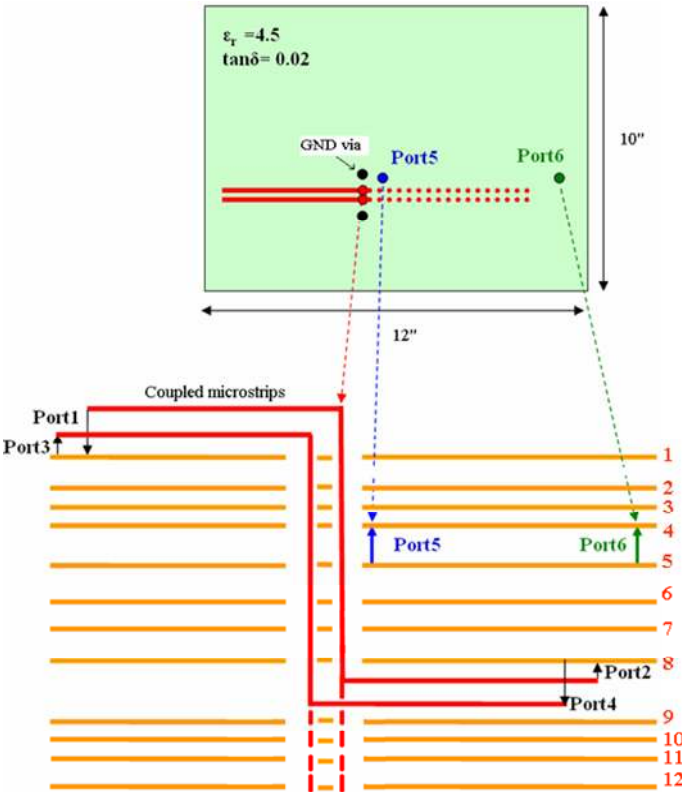

Figure 1. Differential test geometry and stack-up to study noise coupling from signal to power/ground nets.

The capacitance values can be calculated using a quasi-static EM tool or a closed-form expression [4]. The plane pair is modeled as a multi-port impedance matrix that is obtained using the cavity method [5]. Losses in the metal planes and in the dielectric as well as reflections at the plane edges (assumed PMC), are included in the impedance matrix.

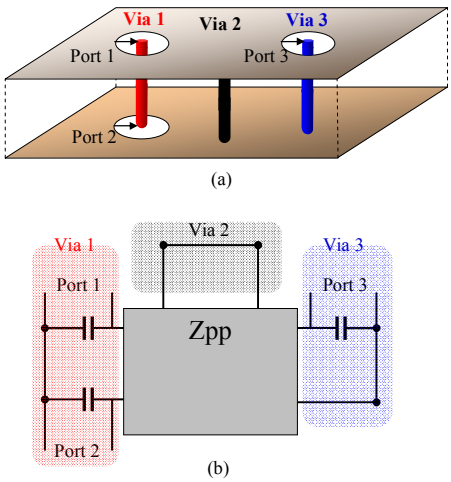

Figure 2. A typical building block.

The inductances associated with the via (evanescent modes) including the mutual ones are accounted for the impedance matrix, as well as the dimension-dependent distributed behaviors of the plane pair. Trace to via transitions, including both microstrip/via and stripline/via transitions, can be combined with the fundamental blocks, as well as other circuit components such as decoupling capacitors and IC devices. This segmentation approach combined with the physics-based via-plane model has been validated to be efficient for common PCB structures [4, 6].

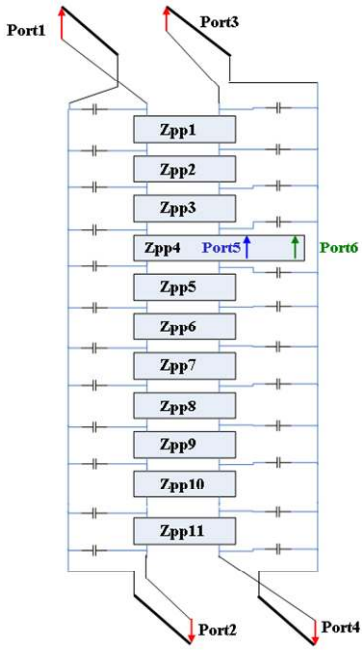

Figure 3. Simplified circuit model for geometry in Figure 1 (thru configuration).

III. The Effects of Via Stubs and Ground Vias

Figure 4 shows the two configurations studied in this paper. Figure 4(a) shows the geometry where the two striplines (associated to Ports 2 and 4) are placed inside the eighth cavities, resulting in a relatively short via stubs. In Figure 4(b) the striplines are located in the fourth cavity with longer via stubs.

As seen in Figure 1, two ground vias are placed 60 mils away from the signal via centers in some cases, so that the impact of these two ground vias can be studied as well.

Both the time- and frequency-domain simulations have been performed to show the impacts of various geometry variations on S-parameters and eye-diagrams.

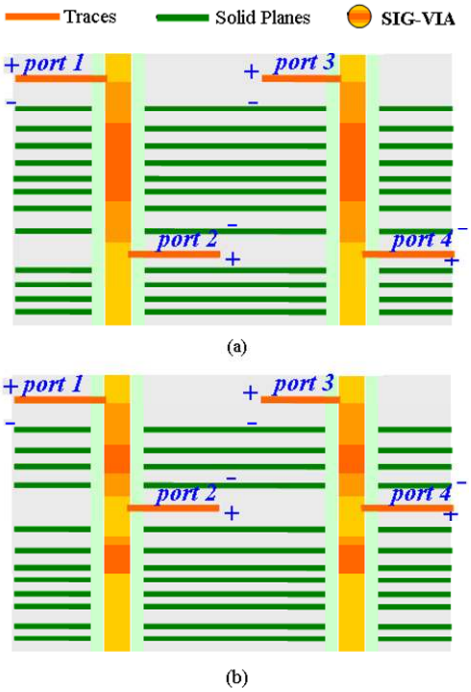

Figure 4. Striplines connection for the (a) short, and (b) the long stub cases.

Figures 5 and 6 show the simulated differential return and insertion losses, respectively, where Ports 1 and 3 in Figure 4 forms the differential Port 1 and Ports 2 and 4 the differential Port 2.

The placement of the GND vias adjacent to the signal does not improve the results a lot, especially in the case of long stubs. For the short stub case, the GND vias are effective in the range between 12 and 20 GHz where the green curve is about 2dB lower than the black one in Figure 6.

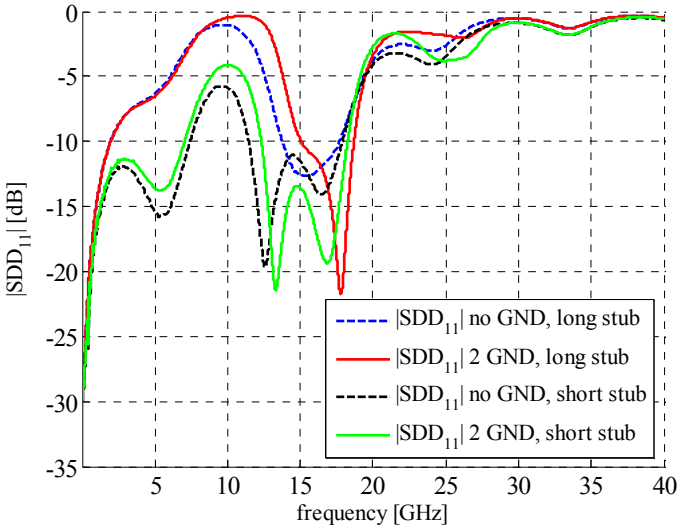

Figure 5. Differential return loss for short and long stub cases with and without GND vias.

It is evident from Figure 6, that the long stub configurations present a deep resonance at around 10GHz. This resonance presents a huge signal transmission loss in the nearby frequency range, and should be avoided for high-speed signals.

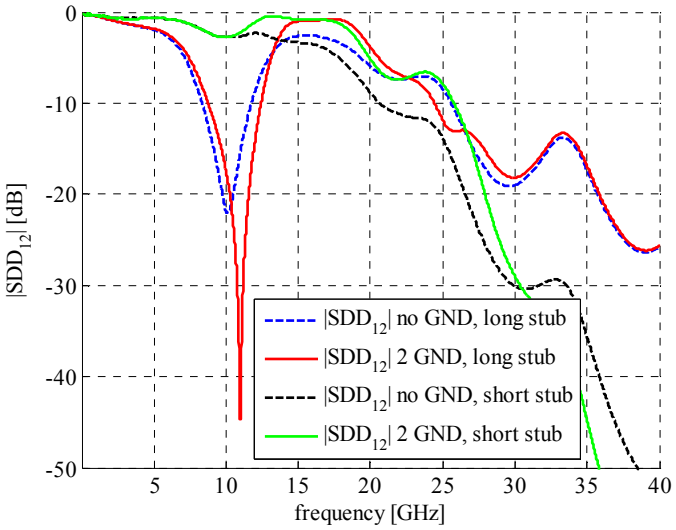

Figure 6. Differential insertion loss for short and long stub cases with and without GND vias.

The reason for this big transmission loss appearing in the black and green curves is that the impedance looking into the stubs is close to zero when frequency is close to the resonant frequency. Adding GND vias can shift the resonance but cannot remove it. The GND vias could, at some cases, provide a lower-impedance return path for current and hence improving the insertion loss at some frequencies.

The impact of stub length is shown in the time-domain as well in Figure 7, where eye diagrams for long and short stubs

are shown in Figure 7(a) and (b), respectively. The data signal has a pattern of a data rate of 20Gbit/s and a rise time of 10ps. As clearly shown, the eye pattern is completely closed for the long stub case and widely open for the short stub case. This dramatic difference is due to the fact that one dominant spectrum component of the signal (10 GHz) is close to the stub resonant frequency shown in Figure 6.

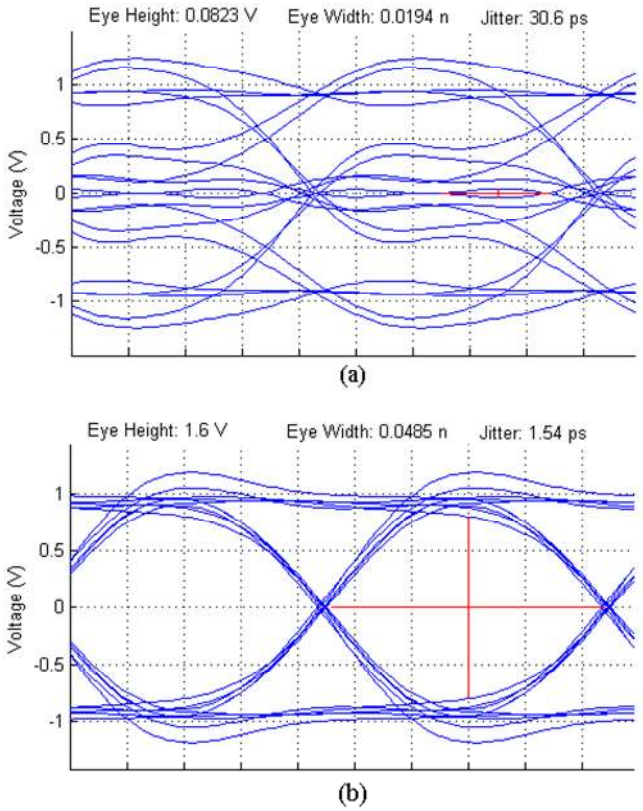

Figure 7. Eye diagrams for a 20GBit/s data pattern for long (a) and short stub (b) configuration without GND vias.

IV. Noise Coupling from Power/Ground to Signal

Noise coupling from power/ground nets to signal in both the frequency- and time-domains was then studied. A redefinition of the ports is necessary to convert the single-ended to the differential mode as illustrated in Figure 8. Since the interest has been focused on the effects of the power bus noise introduced by an IC switching at Port 3' (100 mils from signal vias) or Port 4' (5 inches away from signal vias), two ports, Port 1' and Port 2' are defined in a 100Ohm differential configuration. Again, for simplicity, in Figure 8 the model shown represents a microstrips-to-microstrips through transition.

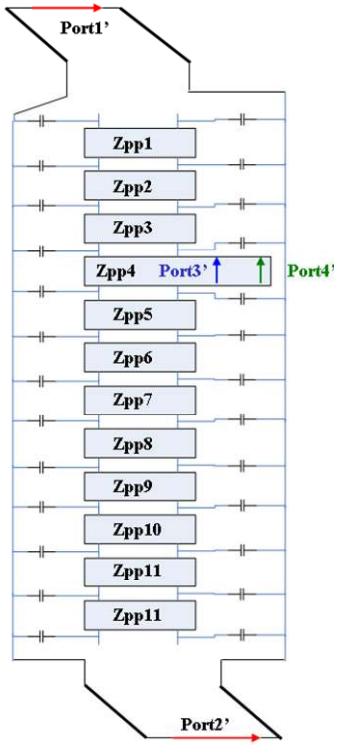

Figure 8. .Simplified equivalent circuit with differential ports.

The circuit model is first investigated in the frequency domain, and the modeled S-parameters among the redefined Ports 1', 3' and 4' are shown in Figures 9 and 10, respectively.

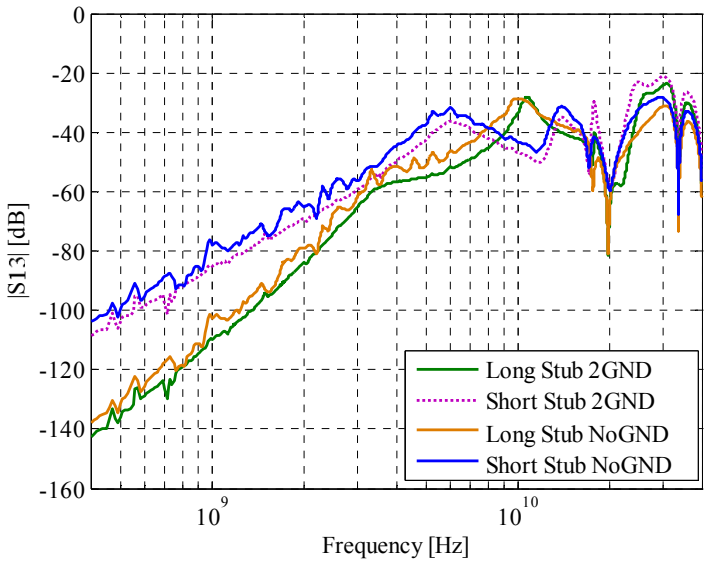

Figure 9. Transfer functions between Ports 1' and 3' in Figure 8 for short and long stubs with and without GND vias.

The $|S_{13}|$, which indicates the noise coupled from Port 3' in the power bus to the top microstrip lines, is below -50dB up to

approximately 3 GHz. This amount of coupling is negligible. Above 3 GHz, the noise coupling could be as high as -20dB.

As clearly shown in Figure 9, the noise coupling is stronger with the shorter stub is short below approximately 8 GHz. It is also noticeable that the presence of the GND vias does not significantly affect the curves.

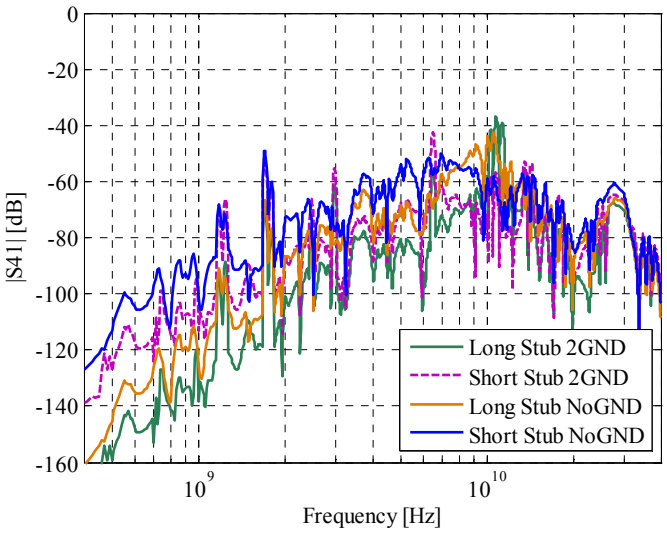

Figure 10. Transfer functions between Ports 1' and 4' in Figure 8 for short and long stub with and without GND vias.

A similar behavior can be observed in Figure 10 where the source of the power bus noise is located five more inches away from the signal vias. Obviously, due to the distance, the coupling is much smaller.

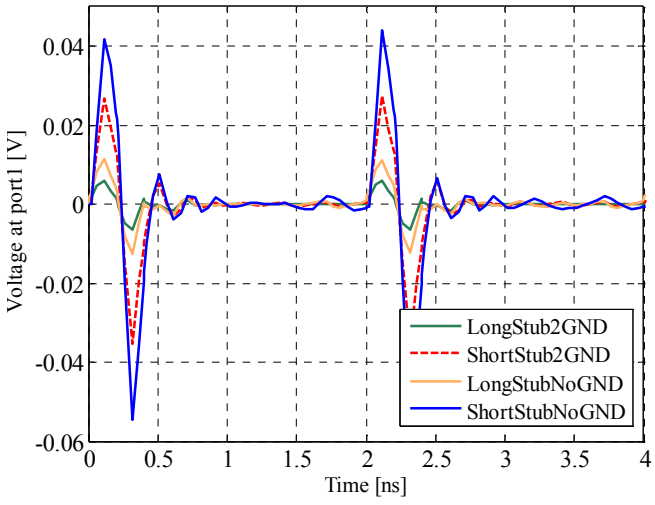

Figure 11.Voltage at Port 1' when noise is applied to Port 3'.

Figure 11 and 12 show the time-domain results. A series of 1Amp triangular current pulses with a fall/rise time of 0.2ns and a period of 2ns are applied to Port 3' and Port 4' to simulate the effect of switching noise on the signal. As clearly shown in these time-domain curves, for this particular setting of data-rate and rise time, a peak voltage noise of about 30 to 50mV is present at the end of the microstrip traces when the noise source is closer. The maximum amplitude is for the case with short stubs and without GND vias, which is consistent to the S-parameter curves. Similarly, moving the noise source farther away, the voltage noise is greatly reduced as shown in Figure 12.

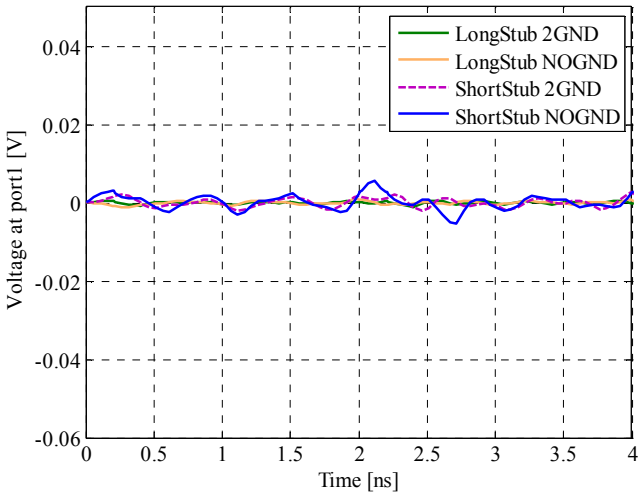

Figure 12. Voltage at Port 1' when the power bus noise is applied to Port 4'

V. Noise Coupling from Signal To Power/Ground

Noise Coupling from signal to power/ground nets was also studied by applying a data signal at Port 1' in Figure 8 and observing noise at Port 3' or Port 4'. Figure 13 shows the time-domain waveforms when Port 1' is excited with a 5V signal with a 100 Ω matching source impedance. The source data rate is 1Gbit/s, and the rise/fall time is 200ps.

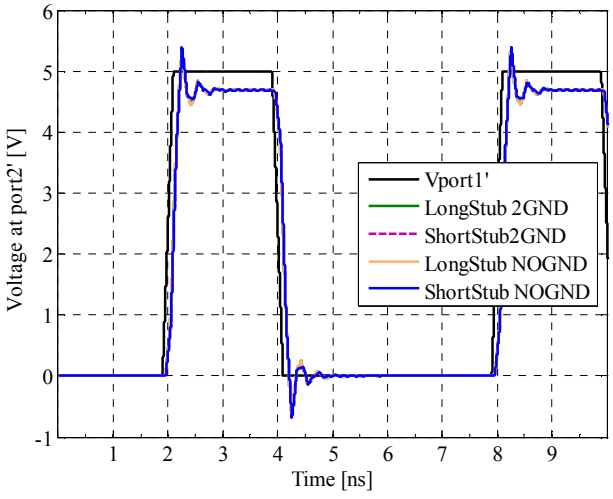

Figure 13. Voltage at Port 2' when a data-stream is applied to Port 1'

The data pattern is "010010001" in repetition. Port 2' is terminated with a 100 Ω load impedance.

As clearly seen in Figure 13, the voltage at Port 2' has a magnitude close to 5V, indicating the signal transmission loss is relatively small at the fundamental frequency. However, the

edges of waveform at Port 2 are significantly slowed due to the high-frequency loss, consistent to the frequency-domain result discussed earlier. The noise voltages at Ports 3 and 4 are much smaller, compared to the Port 2 signal voltage. However, the magnitude gets as high as a few mV. It is interesting to notice that the short stubs, that normally help the propagation of the signals through a via transition, also help the noise to propagate. The noise voltage at Port 4', 5 inches farther away from the signal vias is significantly reduced as clearly seen in Figure 15.

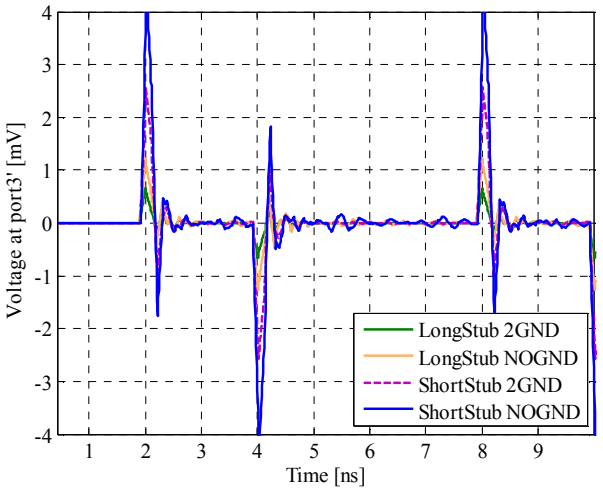

Figure 14. Voltage at port3' when a data-stream is applied to port1'

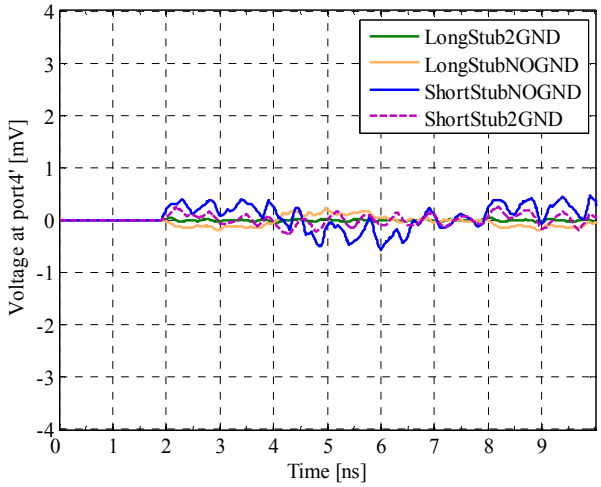

Figure 15. Voltage at Port 4' when a data-stream is applied to Port 1'

VI. CONCLUSION

This paper studies the noise coupling between signal and power/ground nets due to a differential via pair penetrating power and ground planes. The segmentation approach used in combination with a physics-based via-plane model has been proved a suitable and quick method to investigate time and frequency-domain noise phenomena in multilayer PCB.

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