01 Feb 2005

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Recommended Citation

M. Ferdowsi and A. Emadi, "Pulse Regulation Control Technique for Integrated High-Quality Rectifier-Regulators," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 116-124, Institute of Electrical and Electronics Engineers (IEEE), Feb 2005.
The definitive version is available at https://doi.org/10.1109/TIE.2004.841105

Pulse Regulation Control Technique for Integrated High-Quality Rectifier-Regulators

Mehdi Ferdowsi, *Member, IEEE,* and Ali Emadi, *Senior Member, IEEE*

***Abstract*—The Pulse Regulation control scheme is presented and applied to the boost integrated flyback rectifier/energy storage dc/dc (BIFRED) converter as the most popular member of the integrated high-quality rectifier-regulators (IHQRR). In contrast to the conventional control techniques, the principal idea of Pulse Regulation is to regulate the output voltage using a series of high- and low-power pulses generated by the current of the input inductor, which is operating in discontinuous conduction mode (DCM). In this paper, analysis of the BIFRED converter operating in DCM is presented. Fundamentals of Pulse Regulation as well as its stability analysis and the estimation of the output voltage ripple are introduced. Experimental results on a prototype converter are also presented to validate the analytical and simulation results.**

***Index Terms*—AC/DC power converters, boost integrated flyback rectifier/energy storage dc/dc (BIFRED) converter, dc/dc power converters, digital control, discontinuous conduction mode (DCM), integrated high-quality rectifier-regulators, simulation, stability, switch-mode power supplies, voltage regulation.**

I. Introduction

IT is desirable to have switching power converters, which enjoy profitable features such as wide range of output voltage regulation, low-harmonic rectification, small size, low implementation cost, and simple control scheme. It is well proved that it is not simple to achieve these features all at the same time. Integrated high-quality rectifier-regulators (IHQRRs) appear to enjoy most of the desired features to a good extent. The second and third stages of the front-end converters in a distributed power system architecture, depicted in Fig. 1, can easily be replaced by IHQRR converters to improve the design and manufacturing processes and enhance system performance and reliability. They achieve a high level of performance by forcing each energy storage element to change its state as independently as possible from the other elements [1].

Boost integrated flyback rectifier/energy storage dc/dc (BIFRED) and boost integrated buck rectifier/energy storage dc/dc (BIBRED) converters are the most popular members of the IHQRR family. Fig. 2 depicts the block diagram of these two converters. They are capable of doing power-factor correction, electric isolation, and voltage regulation in a single stage using a single switch. The input inductor of these converters is usually employed to operate in discontinuous conduction mode (DCM) to attain the automatic current-shaping characteristic of the boost converter. Without loss of generality, this paper mainly focuses on the BIFRED converter.

As its name suggests, the BIFRED converter is an integration of boost and flyback converters. Due to its topological complications, achieving line and load regulation in a BIFRED converter is not as easy a task as in classical topologies such as buck, boost, or flyback converters. Excessive voltage across the energy storage capacitor under variable load conditions appears to be the major disadvantage of this topology. To alleviate this problem, different solutions have been suggested in the literature [2]–[8]. The authors of [2] represent a variable-frequency control that reduces the voltage stress. In [3], simultaneous phase shift control and duty ratio control is presented to make the output voltage and the voltage across the energy storage capacitor be independently controllable. The authors of [4] and [5] suggest a design in which the flyback part of the BIFRED converter also operates in DCM. In this solution, due to the operation of both stages of the BIFRED converter in DCM, the circuit characteristics, such as voltage transfer ratio, highly become load dependent; therefore, it is extremely difficult to provide a wide output voltage regulation range and/or a fast dynamic response using classical control methods such as pulsewidth modulation (PWM).

In this paper, the Pulse Regulation control technique is proposed to control the output voltage of the BIFRED converter operating in DCM-DCM. This operational mode has the advantages of low voltage level across the energy storage capacitor and, therefore, less voltage stress across the input diode and switch. Pulse Regulation is simple and enjoys fast dynamic response. This control scheme regulates the output voltage based on the presence and absence of high-power and low-power pulses. Pulse Regulation is very simple to implement and does not depend on the small signal model of the converter; therefore, it is cost effective and robust against the variations of the parameters of the converter.

Section II describes the BIFRED converter operating in DCM-DCM. The formulation of DCM-DCM BIFRED is derived in Section III. Section IV presents the application of Pulse Regulation to the input inductance of the BIFRED converter along with the simulation results. Section V investigates the stability of the proposed control scheme. Output voltage ripple is studied in Section VI. Experimental results of applying Pulse Regulation technique to the BIFRED converter are presented in Section VII. Finally, Section VIII draws conclusions and presents an overall evaluation of this new control technique.

Manuscript received November 28, 2003; revised March 18, 2004. Abstract published on the Internet November 10, 2004.

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Digital Object Identifier 10.1109/TIE.2004.841105

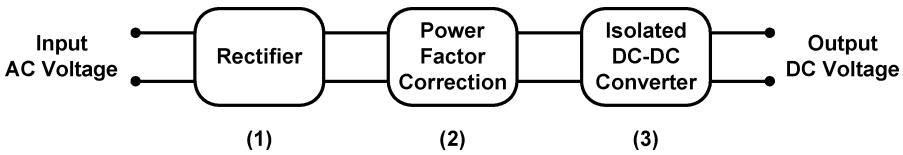

Fig. 1. Block diagram of the front-end converters in distributed power system applications.

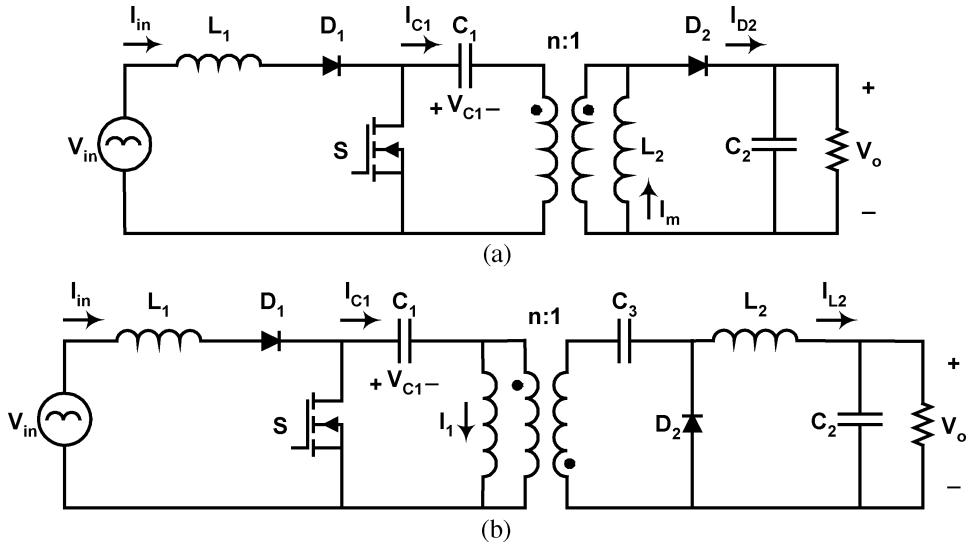

Fig. 2. Block diagram of (a) BIFRED and (b) BIBRED converters.

II. BIFRED Converter

The BIFRED converter initially resulted from integration of a boost converter, operating in DCM, with a flyback converter, operating in continuous conduction mode (CCM) [1]. Inserting a diode in front of an isolated single-ended primary inductance converter (SEPIC) would result in the same topology [5], [9].

In this converter, the input inductor independently operates in DCM and energy storage capacitor C_1 is in the series path of the energy flow. However, the voltage across the energy storage capacitor has a strong dependency on the output load. Reference [5] introduces a new operational mode for this converter, where both boost and flyback converters operate in DCM. With this new mode of operation, large load-dependent voltage variations of the energy storage capacitor no longer exist. Fig. 3 shows four different operating modes of BIFRED converter operating in DCM-DCM. These operating modes can briefly be described as follows.

Mode I: At the beginning of this mode, switch S is turned on; therefore, both switch S and diode D_1 conduct. Input voltage source energizes the input inductor L_1. At the same time, magnetizing inductance of the transformer L_2 receives the energy stored in energy storage capacitor C_1 through the switch S. On the secondary side of the transformer, due to the negative voltage appearance across diode D_2, it gets reverse biased and output capacitor C_2 transfers some of its energy to load R.

Mode II: This mode initiates when switch S is turned off. Therefore, the current of the input inductor L_1 flows through the energy storage capacitor C_1 and the primary side of the transformer delivering its energy to capacitor C_1. Inductor L_1 is completely de-energized at the end of this interval. Secondary diode D_2 is forward biased, which allows the output capacitor to be charged through the secondary winding of the transformer.

Mode III: This mode starts when the input current reaches zero. Switch S and diode D_1 do not conduct while secondary diode D_2 conducts. Therefore, output capacitor C_2 receives all of the energy of the magnetizing inductance of the transformer L_2. Throughout this whole interval, the energy state of input inductor L_1 remains at zero while the energy state of the energy storage capacitor C_1 stays at a constant positive level. This mode ends when magnetizing inductor L_2 is completely de-energized.

Mode IV: In this mode, switch S and diodes D_1 and D_2 do not conduct while the output capacitor delivers energy to the load. During this interval, the energy state of inductors L_1 and L_2 stay at zero while the energy state of the energy storage capacitor C_1 remains at a constant positive level. This mode finishes when the switch is turned on again.

Fig. 4 depicts the typical waveforms of the voltage and current signals of the BIFRED converter operating in DCM-DCM. As this figure suggests, d_1 is the duty ratio of the conduction period of switch S in mode I, d_2 is the duty ratio of the de-energizing period of input inductor L_1 in mode II, and d_3 is the duty ratio of the conduction period of secondary diode D_2 in modes II and III.

III. Formulation Derivation of the BIFRED Converter

The presented formulas in this section are valid if the ac ripple of V_{in} is changing with a frequency much less than the switching

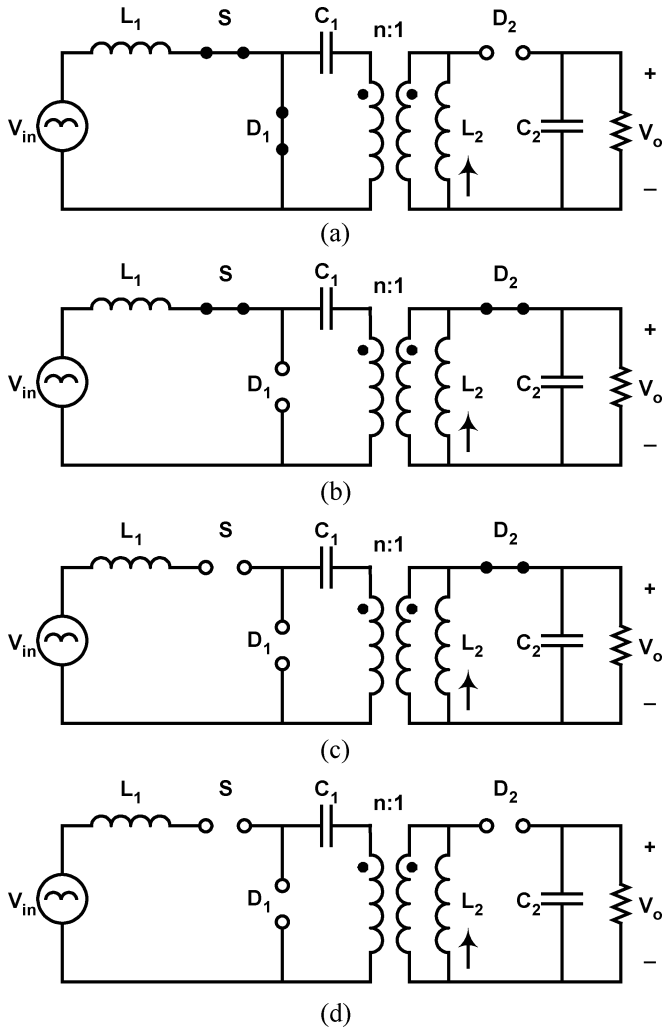

Fig. 3. Four different operational modes of the BIFRED converter operating in DCM-DCM. (a) Mode I (S: on; D_1: on; D_2: off). (b) Mode II (S: off; D_1: on; D_2: on). (c) Mode III (S: off; D_1: off; D_2: on). (d) Mode IV (S: off; D_1: off; D_2: off).

frequency of the converter and the energy storage and output capacitors are large enough to filter out the ripples of energy storage and output voltages.

Current of the input inductor I_{L1} begins the switching period at zero and increase during the first subinterval with a constant slope given by the applied input voltage divided by the value of inductance. Peak input inductor current $I_{L1,\max}$ is equal to the constant slope multiplied by the length of the first subinterval

$$I_{L_1,\max} = \frac{d_1 T V_{\text{in}}}{L_1}. \tag{1}$$

Likewise, for the descending current of the input inductor in the second subinterval, by considering the reflected output voltage to the primary side of the transformer and the voltage across the energy storage capacitor C_1, one obtains

$$I_{L_1,\max} = \frac{d_2 T\left(V_{C_1} + nV_{C_2} - V_{\text{in}}\right)}{L_1}. \tag{2}$$

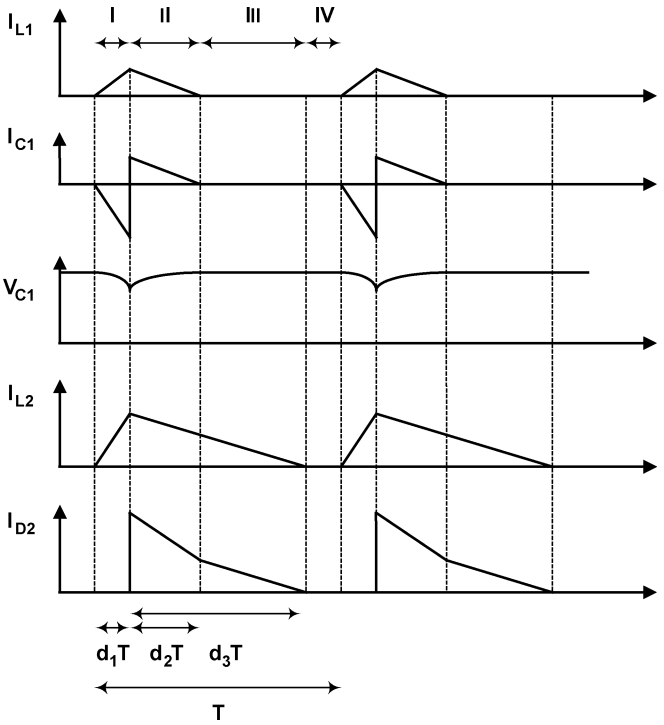

Fig. 4. Typical waveforms of the voltage and current signals of the BIFRED converter operating in DCM-DCM.

Writing the same equation for inductor L_2 in the first subinterval yields

$$I_{L_2,\max} = \frac{d_1 T V_{C_1}}{nL_2}. \tag{3}$$

Furthermore, in the second and third subintervals, based on the descending slope of the magnetizing inductor of the transformer L_2, we can write

$$I_{L_2,\max} = \frac{d_3 T V_{C_2}}{L_2}. \tag{4}$$

Due to the capacitor charge balance in the steady-state operation, including the first and the second subintervals in which the energy storage capacitor conducts, one obtains

$$d_1 \frac{I_{L_2,\max}}{n} = d_2 I_{L_1,\max}. \tag{5}$$

Likewise for capacitor C_2, based on the average value of the current passing through diode D_2, we obtain

$$\frac{1}{2} d_3 I_{L_2,\max} + \frac{1}{2} n d_2 I_{L_1,\max} = \frac{V_{C_2}}{R}. \tag{6}$$

Substitution of (1)–(3) in (5) to eliminate V_{C1} and d_2 yields

$$\frac{n d_1^2 T^2 V_{\text{in}}^2}{L_1} = nL_2 I_{L_2,\max}^2 + d_1 T I_{L_2,\max}\left(nV_{C_2} - V_{\text{in}}\right). \tag{7}$$

Substitution of (1), (4), and (5) in (6) to eliminate d_2 and d_3 yields

$$RL_2 I_{L_2,\max}^2 + Rd_1 T V_{C_2} I_{L_2,\max} = 2TV_{C_2}^2. \tag{8}$$

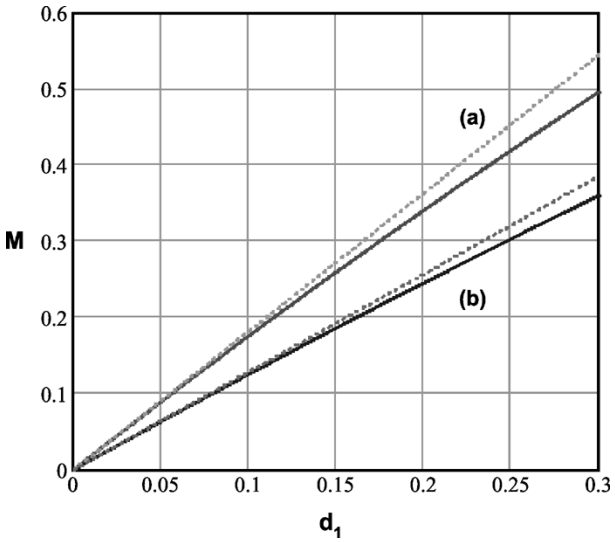

Fig. 5. Exact (solid line) and approximate (dotted line) values of the voltage transfer ratio as a function of d_1. (a) $R = 20\ \Omega$. (b) $R = 10\ \Omega$.

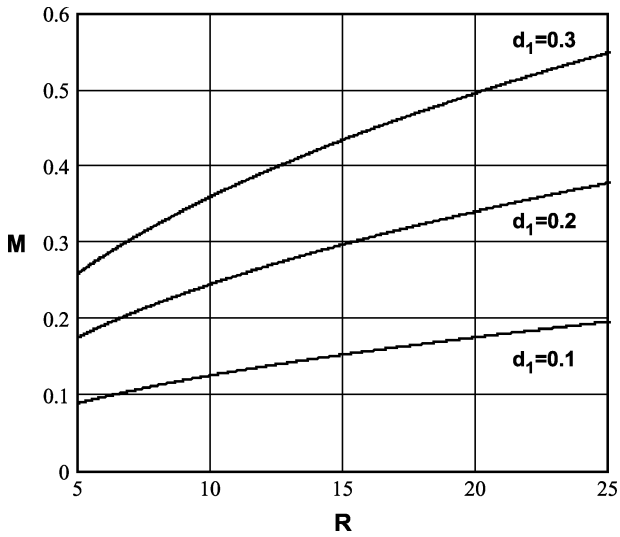

Fig. 6. Voltage transfer ratio as a function of load resistance R.

Solution of (7) and (8) for V_{C_2} leads to the quadratic equation of

$$AV_{C_2}^2 - BV_{C_2} - C = 0 \tag{9}$$

where

$$A = 2nT/R$$
$$B = \frac{T^2 d_1 V_{\text{in}}^2}{L_2}\left(\sqrt{\frac{d_1^2}{4} + \frac{2L_2}{RT}} - \frac{d_1}{2}\right)$$
$$C = nd_1^2 T^2 V_{\text{in}}^2 / L_1.$$

There is not a closed-form formulaic presentation of voltage transfer ratio. However, based on the solution of (9), we can approximate the input to output voltage transfer ratio of the BIFRED converter operating in DCM-DCM ($M = Vo/Vin$) as

$$M \cong \frac{d_1}{4n}\left(\sqrt{\frac{2RT}{L_2} + \frac{8n^2 RT}{L_1}} + \sqrt{\frac{2RT}{L_2}}\right). \tag{10}$$

The exact value of the voltage transfer ratio (solid line) and its approximation using (10) (dashed line) are sketched in Fig. 5 for $V_{\text{in}} = 50$ V, $f = 50$ KHz, $L_1 = 200\ \mu$H, $L_2 = 125\ \mu$H, and different values of the load resistance.

Fig. 6 illustrates the load dependency of the voltage transfer ratio for different values of the duty ratio of the conduction period of switch $S(d_1)$. As we can observe, the load dependency of the voltage transfer ratio increases as d_1 increases.

The voltage across the energy storage capacitor can also be obtained after finding the output voltage based on the solution of (9) for V_{C2}. In Fig. 7, normalized value of the voltage across the energy storage capacitor, using the input voltage, is sketched as a function of load resistance for different values of the duty cycle. As we can see in this figure, the voltage across the energy storage capacitor increases when the load resistance decreases. This increment is less than the case when the BIFRED converter operates in DCM-CCM [5].

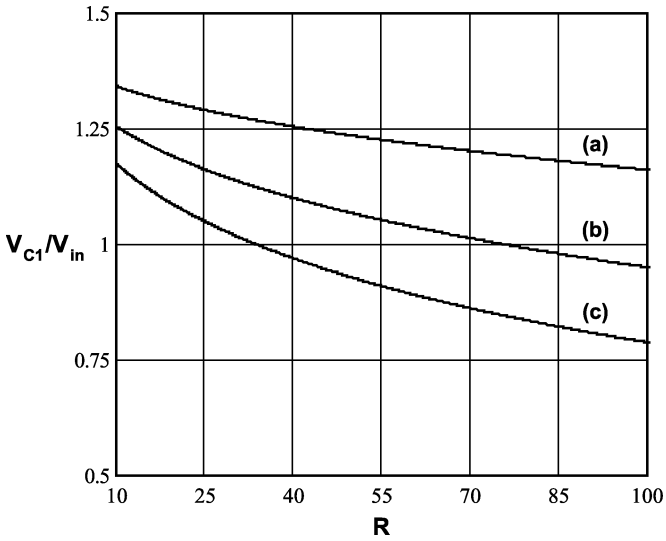

Fig. 7. Normalized value of the voltage across C_1. (a) $d_1 = 0.1$. (b) $d_1 = 0.2$. (c) $d_1 = 0.3$.

Duty ratios d_2 and d_3, as well as $d_1 + d_2$ as a function of d_1 are depicted in Fig. 8. At the point where $d_1 + d_2$ reaches one, the input inductor will no longer operate in DCM. Furthermore, at the point where d_2 and d_3 cross each other, magnetizing inductance of the transformer will be deeply operating in DCM, which causes high output voltage ripple. These two points are desired to happen for the same value of d_1. This can be done by choosing the right values for input inductor L_1 and magnetizing inductance L_2. As can be observed from Fig. 8, the converter needs to operate for the duty ratios of d_1 less than the above-mentioned cross points.

We need to note that our calculations in this section are valid if and only if $d_3 > d_2$. This guarantees that operational modes *I* through *IV* happen in the presumed sequence. If d_3 happens to be smaller than d_2, the order of modes *II* and *III* will be switched, causing the required analysis (1)–(10) to be rewritten. As stated in the previous paragraph, this situation if undesirable due to the high output voltage ripple. Therefore, the best design criteria is to designate the values of L_1 and L_2

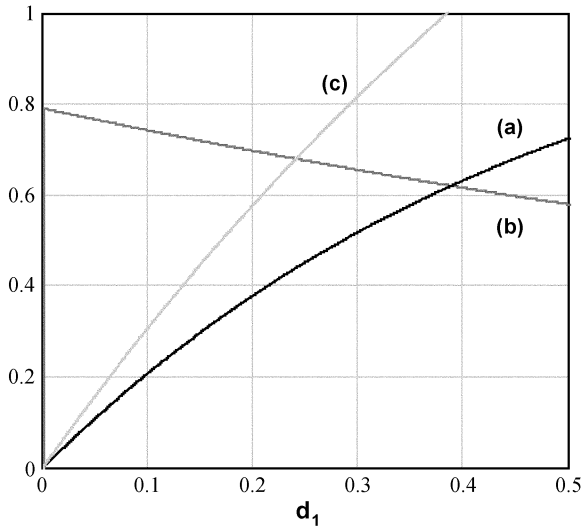

Fig. 8. (a) d_2, (b) d_3, and (c) $d_1 + d_2$ as a function of d_1.

in a way to make sure that continuous conduction operating mode of L_1 starts at the same point where $d_2 = d_3$. In this way, choosing smaller values for d_1 guarantees that L_1 operate in DCM as well as $d_3 > d_2$. Furthermore, magnetizing inductance L_2 nearly operates in critical conduction mode, so that output voltage ripple will be reduced.

IV. Pulse Regulation Control Scheme

The Pulse Regulation control algorithm achieves output voltage regulation based on generating high and low-power pulses, rather than employing PWM control technique. If the output voltage is lower than the desired level, the controller chooses D_H to be the duty ratio and, therefore, high-power pulses are generated sequentially until the desired voltage level is reached. On the other hand, if the output voltage is higher than the desired level, instead of generating high-power pulses, the controller chooses $D_L (D_L < D_H)$ to be the duty ratio and, hence, low-power pulses are generated to descend the level of the output voltage. Fig. 9 depicts the block diagram of the Pulse Regulation control technique. Due to the longer on time of the switch during a high-power pulse, compared to a low-power pulse, more power will be delivered to the load. The switching frequency is constant and D_H is chosen in a way that the converter operates in DCM but as close as possible to the critical conduction mode. Critical conduction mode occurs when the input voltage is at its maximum level. $k = D_H/D_L$, the ratio between duty cycle of the switch in a high-power cycle D_H and duty cycle of the switch in a low-power cycle D_L, is chosen by making a compromise between the output voltage ripple and the power regulation range from full load to low load.

Fig. 10 depicts the current waveform of the input inductance of the BIFRED converter after Pulse Regulation is applied. At the beginning of each switching cycle, based on the difference of the output voltage with the desired voltage level, it will be determined whether a high-power or a low-power cycle needs to be generated. Since the input current ramps linearly with the

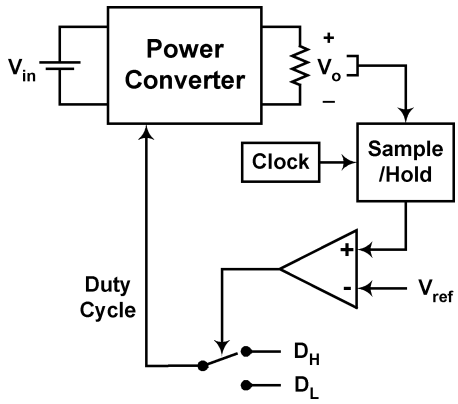

Fig. 9. Block diagram of Pulse Regulation control scheme.

switch on time, a low-power pulse transfers only $1/k^2$ time as much energy as a high-power pulse.

Fig. 11 shows the simulation results of applying this control method on a BIFRED converter with $D_H = 0.3$, $k = 3$, and $V_{\rm ref} = 15$. For this specific value of the output power demand, the control scheme generates three high-power pulses and one low-power pulse in each regulation cycle.

We already discussed that the current of the magnetizing inductance needs to reach zero later than the current of the input inductor $(d_3 > d_2)$. Because of this fact, employment of Pulse Regulation technique might cause the magnetizing inductor current to operate very close to CCM. The circuit parameters can be designed in a way that d_3 is slightly greater than d_2 over a wide load variations. Therefore, the magnetizing inductance will almost operate in critical conduction mode.

Pulse Regulation enjoys online waveform analysis and, hence, fast dynamic response. Fig. 12 compares the speed of response of Pulse Regulation with a typical PWM control to a step load change of 35%–70% of full load. The vertical arrows in this figure mark the time instant at which the step change has applied. As we can observe, Pulse Regulation has a much faster speed of response in contrast with PWM.

V. Stability Analysis

Considering a general switching period, as shown in Fig. 13, and based on the energy conservation rule, one can write

$$\Delta E_{\rm in} = \Delta E_{L_1} + \Delta E_{C_1} + \Delta E_{L_2} + \Delta E_{C_2} + \Delta E_{\rm Load} \quad (11)$$

where $\Delta E_{\rm in}$ is the amount of energy that has been drawn from the input power source during the considered switching period. ΔE_{L1} and ΔE_{L2} are the difference of the energy stored in the input inductor and the magnetizing inductance of the transformer, respectively, and are equal to zero since they both de-energize at the end of each switching period. ΔE_{C1} and ΔE_{C2} are the changes of the energy stored in the energy storage capacitor and the output capacitor during the same switching period, respectively. While ΔE_{C1} is equal to zero, ΔE_{C2} can be described as

$$\Delta E_{C_2} = E_{C_2,(n+1)T} - E_{C_2,nT}. \quad (12)$$

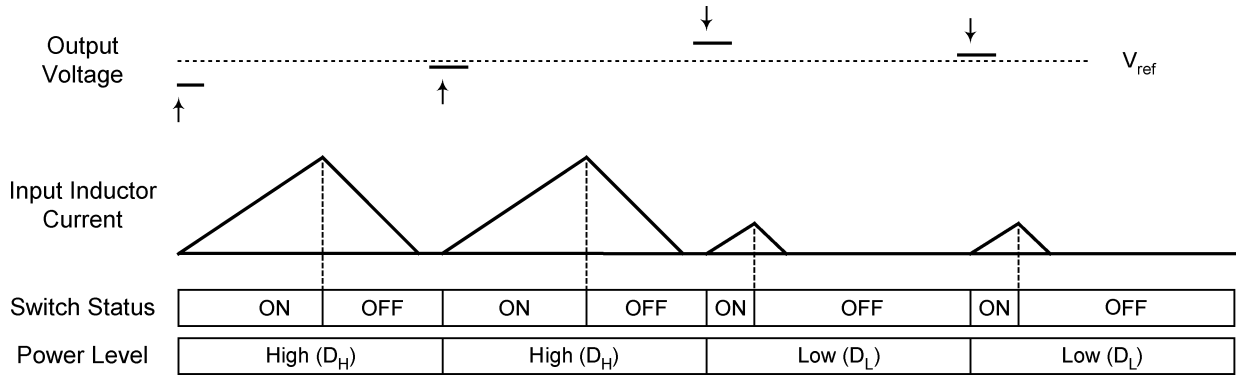

Fig. 10. High- and low-power pulse cycles.

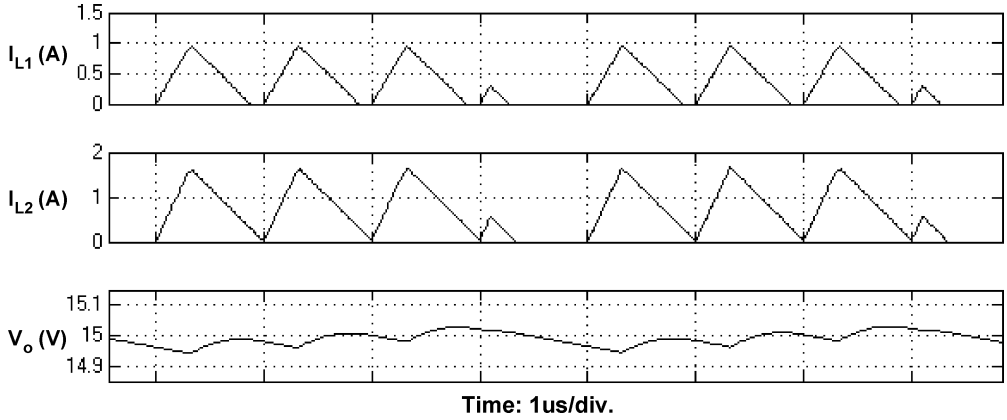

Fig. 11. Simulation results of the Pulse Regulation control of the BIFRED converter.

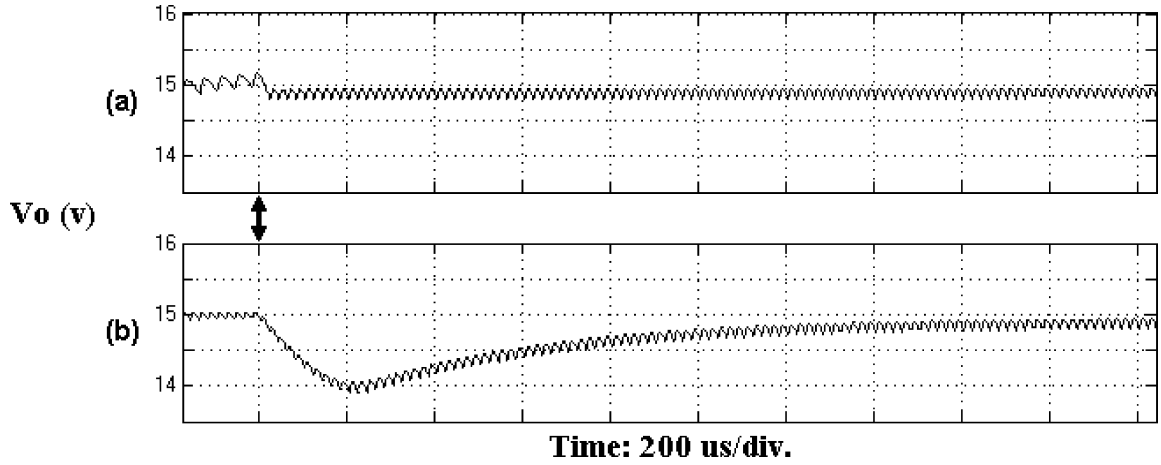

Fig. 12. Simulation results of the output voltage variation after a step load change of 35% to 70% of full-load: (a) Pulse regulation, (b) PWM.

And finally, ΔE_{Load} is the amount of energy delivered to load R during the same period. Output capacitor C provides the load current; hence, we can write

$$\Delta E_{\text{Load}} = \frac{1}{R} \cdot \int_{nT}^{(n+1)T} V_{C_2}^2 \cdot dt. \tag{13}$$

In (13), using the trapezoidal rule instead of integration, we can approximate ΔE_{Load} as

$$\Delta E_{\text{Load}} \cong \frac{T}{2R} \left(V_{C_2,(n+1)T}^2 + V_{C_2,nT}^2 \right). \tag{14}$$

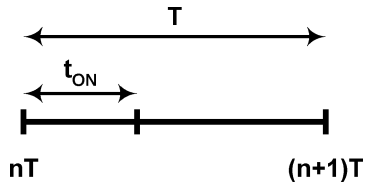

Fig. 13. A general switching period.

Moreover, the energy stored in a capacitor at each instant is equal to the squared value of the voltage that appears across the

capacitor divided by twice the value of the capacitor; hence, (14) can be rewritten as

$$\Delta E_{\text{Load}} \cong \frac{T}{RC_2}\left(E_{C_2,(n+1)T} + E_{C_2,nT}\right). \tag{15}$$

Substituting (12) and (15) into (11) and solving for the energy stored in the output capacitor at the end of the desired switching period, one obtains

$$E_{C_2,(n+1)T} = J \cdot E_{C_2,nT} + \frac{1}{1+\frac{T}{RC_2}}\Delta E_{\text{in}} \tag{16}$$

where

$$J = \frac{1-\frac{T}{RC_2}}{1+\frac{T}{RC_2}} < 1. \tag{17}$$

Equation (16) shows the recursive relation of the energy stored in the output capacitor. We need to note that J is always less than one; therefore, the converter is stable under any pattern of high and low-power pulses in the closed loop system. Using the input current, ΔE_{in} can be described as

$$\Delta E_{\text{in}} = E_{L_1,nT+t_{on}} - E_{L_1,nT} \tag{18}$$

where, for a high-power pulse, we have

$$\Delta E_{\text{in,HP}} = \frac{0.5V_{\text{in}}^2(D_H T)^2}{L_1} \tag{19}$$

and for a low-power pulse, we have

$$\Delta E_{\text{in,LP}} = \frac{0.5V_{\text{in}}^2(D_L T)^2}{L_1} = \frac{\Delta E_{\text{in,HP}}}{k^2}. \tag{20}$$

Therefore, in the closed-loop control, the controller makes the decision of generating a high- or low-power pulse such that

$$\begin{aligned} V_{out} < V_{\text{ref}} \Rightarrow \Delta E_{\text{in}} &= \frac{0.5V_{\text{in}}^2(D_H T)^2}{L_1} \quad \text{high-power pulse} \\ V_{out} > V_{\text{ref}} \Rightarrow \Delta E_{\text{in}} &= \frac{0.5V_{\text{in}}^2(D_L T)^2}{L_1} \quad \text{low-power pulse.} \end{aligned} \tag{21}$$

An example of the time evolution of the sequence of high- and low-power pulses, in a closed-loop system and based on (16) and (21), is depicted in Fig. 14. The closed-loop system is stable under any conditions of the initial energy stored in the output capacitor. In Fig. 14, the energy level corresponding to V_{ref} is depicted as $E^*_{C_2}$ and is equal to

$$E^*_{C_2} = 0.5C_2V_{\text{ref}}^2. \tag{22}$$

VI. Output Voltage Ripple

Assuming that the output voltage is at its desired level ($V_{C2} = V_{\text{ref}}$), we can rewrite (7) like

$$AI_{L_2,\max}^2 + BI_{L_2,\max} - C = 0 \tag{23}$$

where $A = nL_2$, $B = d_1T(nV_{\text{ref}} - V_{\text{in}})$, and $C = nL_1I_{L_1,\max}^2$. Solution of (23) for $I_{L2,\max}$, having $d_1 = D_H$, and using (1), (3) and (5) to find $I_{L1,\max}$, V_{C1} and d_2, respectively, we can calculate the average value of the current passing through D_2

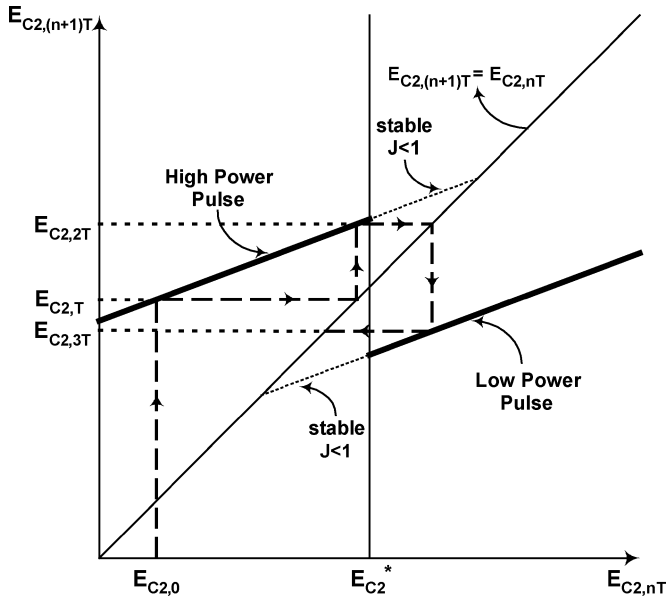

Fig. 14. Sequential evolution of high- and low-power pulses.

$$I_{D_{av}} = \frac{1}{2}d_3I_{L_2,\max} + \frac{1}{2}nd_2I_{L_1,\max}. \tag{24}$$

Neglecting the equivalent series resistance of the output capacitor, total changes of the output voltage after applying a high-power pulse can be estimated as

$$\Delta V_{O,HP} = \frac{T}{C_2}\left(I_{D_{av}} - \frac{V_{\text{ref}}}{R}\right). \tag{25}$$

Fig. 15 sketches $\Delta V_{O,HP}$ as a function of the load resistance for different values of d_1. As a high-power pulse, we expect to have positive values of $\Delta V_{O,HP}$ for the entire load range. As the values of d_1 decreases, the functionality of high-power pulses deteriorates and becomes similar to a low-power pulse.

Likewise, solution of (23) for a low-power cycle ($d_1 = D_L = D_H/k$) leads us to the total changes of the output voltage after applying a low-power pulse ($\Delta V_{O,LP}$). $\Delta V_{O,HP}$ and $-\Delta V_{O,LP}$ as a function of load resistance R are sketched in Fig. 16. As we can observe, the control scheme tries to regulate the output voltage by generating the right number of high and low-power pulses in each regulation cycle. We can observe that as the output power increases, $\Delta V_{O,HP}$ decreases; but, $-\Delta V_{O,LP}$ increases. This fact implies that at a higher output power level, the control strategy prefers to have more high-power pulses rather than low-power pulses in each regulation cycle and vice versa in light loads. The value of the output load resistance at which the two graphs cross each other is the value of load, which requires one high-power pulse associated with one low-power pulse in each regulation cycle. Considering different values for the load resistance, different patterns of high and low-power cycles can be extracted using Fig. 16. Table I shows some examples of the pattern of high- and low-power pulses.

According to Table I, for instance, when $R = 11.1\ \Omega$, we have $\Delta V_{O,HP} \approx 1/3 * -\Delta V_{O,LP}$ which predicts for this value

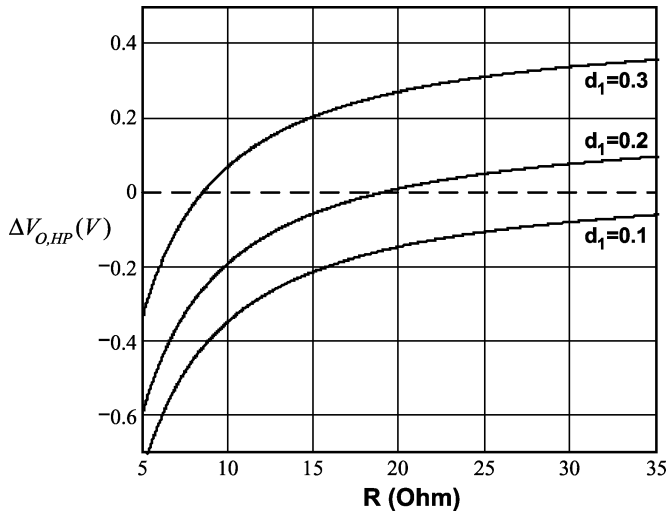

Fig. 15. $\Delta V_{O,HP}$ as a function of load resistance for different values of d_1.

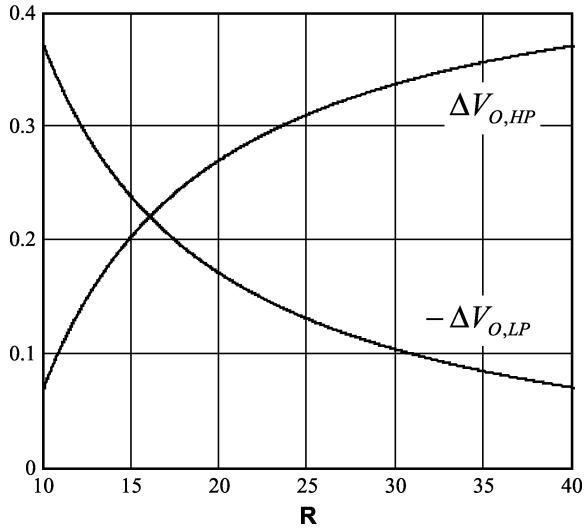

Fig. 16. $\Delta V_{O,HP}$ and $-\Delta V_{O,LP}$ as functions of load resistance.

TABLE I
HIGH- AND LOW-POWER PULSE PATTERN PREDICTION IN ONE REGULATION CYCLE

$R\,(\Omega)$	$\Delta V_{O,HP}(v)$	$-\Delta V_{O,LP}(v)$	Predicted Pattern
11.1	0.11	0.331	3*HP - 1*LP
16	0.221	0.221	1*HP - 1*LP
28.7	0.331	0.11	1*HP - 3*LP

of load, in each regulation cycle, the converter generates one low-power pulse associated with each three high-power pulses. Therefore, first we calculate $\Delta V_{O,HP}$ and $-\Delta V_{O,LP}$ (25) associated with each value of R, then we find two integers as this equation holds

$$\alpha \cdot \Delta V_{O,HP} = \beta \cdot -\Delta V_{O,LP} \tag{26}$$

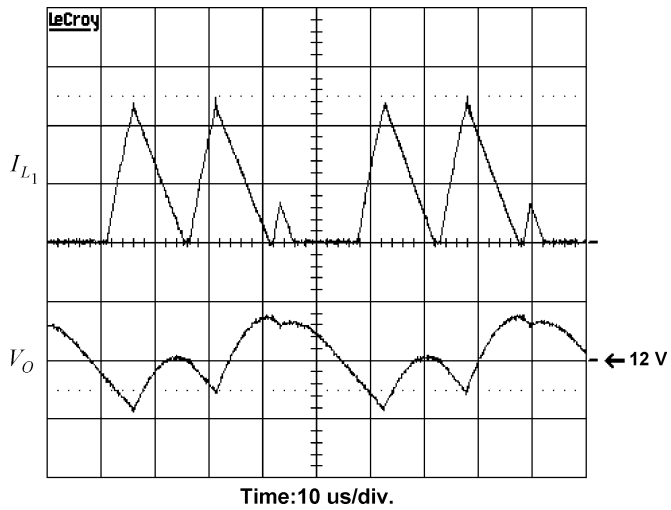

Fig. 17. Measured (a) input current (0.6 A/div) and (b) output voltage ripple (0.1 V/div) for 60% of the full load.

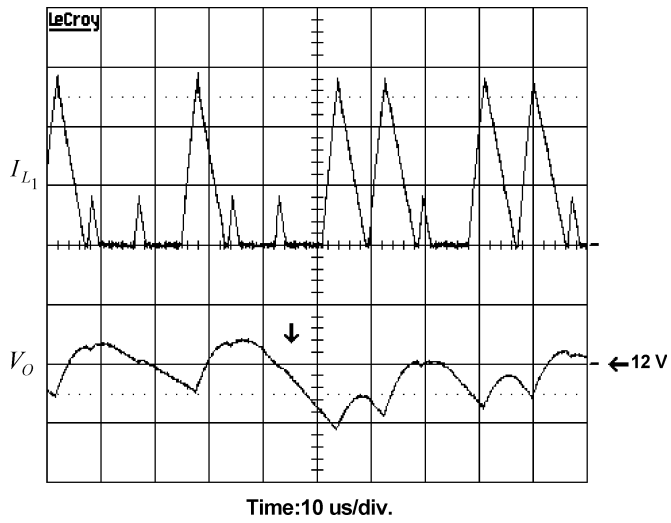

Fig. 18. Measured (a) input current (0.6 A/div) and (b) output voltage ripple (0.1 V/div) for a step load change of 30% to 60% of full load.

where α and β represent the number of high- and low-power pulses in each regulation period.

VII. EXPERIMENTAL RESULTS

A prototype BIFRED converter with output power of 80 W was designed and implemented to provide an output of 12 V. Switching frequency was chosen to be 50 kHz with $L_1 = 210\ \mu$H, $L_2 = 130\ \mu$H, $C = 50\ \mu$F, and $n = 6$. The experimental results of Pulse Regulation control method applied to this converter are shown in Figs. 17 and 18. Fig. 17 depicts the input inductor current and the output voltage ripple for the value of load equal to 60% of the full load, whereas Fig. 18 shows the same waveforms for a 30%–60% step load change. The vertical arrow marks the time instant at which the step change is applied.

VIII. CONCLUSION

The DCM-DCM BIFRED converter has the advantages of low voltage level across the energy storage capacitor and, there-

fore, less voltage stress across the input diode and switch. This converter has found its way into many applications and is the most popular member of the family of integrated high-quality rectifiers-regulators. To address the challenge of designing controllers for this type of converters, this paper has introduced Pulse Regulation control theory. This control method has several advantages over the conventional techniques, such as simplicity, robustness, accuracy, and fast transient response. Simulation as well as experimental results completely match with the theoretical concept.

REFERENCES

[1] M. Madigan, R. Erickson, and E. Ismail, "Integrated high-quality rectifier-regulators," in *Proc. IEEE PESC'92*, vol. 2, Toledo, Spain, Jun. 1992, pp. 1043–1051.

[2] M. M. Jovanovic, D. M. C. Tsang, and F. C. Lee, "Reduction of voltage stress in integrated high-quality rectifier-regulators by variable-frequency control," in *Proc. IEEE APEC'94*, vol. 2, Orlando, FL, Feb. 1994, pp. 569–575.

[3] M. A. Johnston and R. W. Erickson, "Reduction of voltage stress in the full bridge BIBRED by duty ratio and phase shift control," in *Proc. IEEE APEC'94*, vol. 2, Orlando, FL, Feb. 1994, pp. 849–855.

[4] M. J. Willers, M. G. Egan, J. M. D. Murphy, and S. Daly, "A BIFRED converter with a wide load range," in *Proc. IEEE 20th Int. Conf. Industrial Electronics, Control, and Instrumentation*, vol. 1, Bologna, Italy, Sep. 1994, pp. 226–231.

[5] K. Schenk and S. Cuk, "A single-switch single-stage active power factor corrector with high quality input and output," in *Proc. IEEE PESC'97*, vol. 1, St. Louis, MO, Jun. 1997, pp. 385–391.

[6] M. Telefus, A. Collmeyer, D. Wong, and D. Manner, "Switching power converter with gated oscillator controller," U.S. Patent 6 275 018.

[7] M. Telefus, D. Wong, and C. Geber, "Operating a power converter at optimal efficiency," U.S. Patent 6 304 473.

[8] M. Telefus, A. Shteynberg, M. Ferdowsi, and A. Emadi, "Pulse Train, a novel digital control method, applied to a discontinuous conduction mode flyback converter," in *Proc. IEEE PESC'03*, Acapulco, Mexico, Jun. 2003.

[9] Z. Nie, A. Emadi, J. Mahdavi, and M. Telefus, "SEPIC and BIFRED converters for switch-mode power supplies: a comparative study," in *Proc. IEEE 24th Int. Telecommunications Energy Conf.*, 2002, pp. 444–450.

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