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Validation of Circuit Extraction Procedure by Means of Frequency and Time Domain Measurement

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Abstract — **Aim of this paper is the validation in both frequency and time domain of the procedure to extract fully H-Spice compatible equivalent circuits of structures on printed circuit boards. The procedure is initiated by standard measurement of scattering parameters between 40MHz to 20GH. After the extraction of the equivalent circuit, the computed scattering parameters are compared with those measured. The same equivalent circuit is also used for transient analysis in order to compare TDR measurement and eye-pattern to a pseudo-random bit sequence with those coming from the simulations.**

Keywords- Equivalent circuit extraction, SPICE, TDR, eye pattern.

I. INTRODUCTION

The actual design process of high-speed digital systems pays more and more attention on the simulations of the electrical performances of the system. Reliable simulations allow the designer to predict the system's behavior, to perform a what-if analysis and to anticipate design's changes before the physical construction of the board.

In the field of Signal Integrity (SI) full wave three dimensional (3D) numerical simulations are often used to characterize signal and noise propagation paths or discontinuities. They allow tacking into account of complex geometries and features in the result space, at the expenses of computational resources and time. Equivalent circuit models for these structures are more interesting from an engineering point of view. They use require less computing and time resources and they can be easily integrated in larger circuit simulations incorporating the description of the active parts of the digital system that can not be described (at least without considerable theoretical and programming efforts) in 3D simulations.

Multiple techniques for the extraction of equivalent circuits of on-board discontinuities are present in the scientific literature ([1-4] are among the more recent and significant). The authors have developed [5] and applied [6-7] a procedure based on the rational fitting of network parameters such as Scattering parameters (S-parameters), or the admittance (Y) or impedance (Z) matrices. They have been obtained by numerical simulations before the definitive design of the board's structure. Another real world scenario is when one wants to characterize an existent discontinuity in terms of an equivalent circuit avoiding a lengthy numerical simulation but resorting to direct measurements.

In this work, the above mentioned procedure is applied for the characterization of a plated through hole (PTH) via with feeding traces by means of the extraction of an equivalent SPICE circuit from the measurement of the S-parameters in frequency domain.

The obtained circuit is validated both in frequency and time domain. In frequency domain the measured S-parameters are compared in magnitude and phase with those computed by using the extracted equivalent circuit; in time domain the computed step response and output voltage due to a pseudo-random bit sequence (PRBS) are compared with the measured data from a time-domain reflectometer (TDR) and an eye pattern (EP) respectively.

In SECTION II the circuit extraction procedure is briefly recalled; in SECTION III the test board is described and the results from measurement compared with those coming from the simulation of the equivalent circuit. Finally, SECTION IV offers some conclusions.

II. PROCEDURE FOR EQUIVALENT CIRCUIT EXTRACTION

The most used characterization of the passive structures (such as interconnects) in digital systems is by means of the S-parameters easily available from network analyzer measurements. The structure to be characterized is considered as an n-port network at which ports the S-parameters are measured. They do not allow a direct circuit interpretation of the network but, by transforming the S-parameter matrix **S** into the admittance matrix **Y**, an equivalent circuit can be obtained. The **S**-to-**Y** matrix conversion is [8,9]

$$\mathbf{Y} = \left\{ \left[\frac{\mathbf{Z}_0^*}{\sqrt{\mathbf{R}_0}} \right] + \mathbf{S} \left[\frac{\mathbf{Z}_0}{\sqrt{\mathbf{R}_0}} \right] \right\}^{-1} \{\mathbf{U} - \mathbf{S}\} \left[\frac{1}{\sqrt{\mathbf{R}_0}} \right] \qquad (1)$$

Where **U** is the unitary matrix, $\mathbf{Z_0}$, $\mathbf{Z_0}^*$, are the matrices of the complex reference impedance and its conjugate and $\mathbf{R_0}$ the matrix of the real part of $\mathbf{Z_0}$. From the admittance matrix **Y** in (1) (whose entries are y_{ij}) can be obtained the associated admittance based circuit whose elements are related to **Y** by the following expressions [10] for the self-terms.

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$$y_{i0} = \sum_{j=1}^{n} y_{i,j} = y_{i1} + y_{i2} + y_{i3} + y_{i4} \tag{2}$$

and for the mutual terms:

$$y_{ij} = -y_{i,j} \tag{3}$$

In the simple case of a four-port network, the topology of the admittance based circuit described by (2) and (3) is shown in Fig. 1a. The nodal admittance matrix corresponding to this circuit is:

$$\mathbf{Y_n} = \begin{bmatrix} y_{10} & y_{12} & y_{13} & y_{14} \\ y_{21} & y_{20} & y_{23} & y_{24} \\ y_{31} & y_{32} & y_{30} & y_{34} \\ y_{41} & y_{42} & y_{43} & y_{40} \end{bmatrix} \tag{4}$$

At this stage a Vector Fitting procedure (VF) [11-13] is applied to the entries in (4), in order to compute their rational approximation in the form:

$$y_{ij}(s) = \sum_{k=1}^{Np} \frac{res_{k,ij}}{(s - p_k)} + d_{ij} + se_{ij} \tag{5}$$

being $s = j\omega$ the complex frequency, $res_{k,ij}$ (i,j=1,..,4) and p_k the kth residue and pole, d_{ij} and e_{ij} two constant terms. Np is the number of poles corresponding to the order of the approximation. In [7] it has been shown as at each term in (5) can be associated to passive lumped circuit. Each real pole/residue pair in the first term of the summation in (5) can be represented as a RL series circuit (Fig.1b).

For the previous equivalent circuit the corresponding admittance is

$$y(s) = \frac{\bar{I}(s)}{\bar{V}(s)} = \frac{1}{(R + sL)} = \frac{\frac{1}{L}}{\left(s + \frac{R}{L}\right)} \tag{6}$$

Given a real pair of a pole and residue extracted by the fitting procedure it is straightforward obtaining the corresponding *R* and *L* parameters:

$$L = \frac{1}{res_{RL}}$$
$$R = -p_{RL} L = -\frac{p_{RL}}{res_{RL}} \tag{7}$$

For complex pole/residue pair an equivalent circuit is represented in Fig. 1c and the equivalence admittance is:

$$y(s) = \frac{1}{L} \frac{\left(s + \frac{1}{R_2 C}\right)}{\left(s^2 + \left(\frac{R_1}{L} + \frac{1}{R_2 C}\right)s + \left(\frac{R_1}{L}\frac{1}{R_2 C} + \frac{1}{LC}\right)\right)} \tag{8}$$

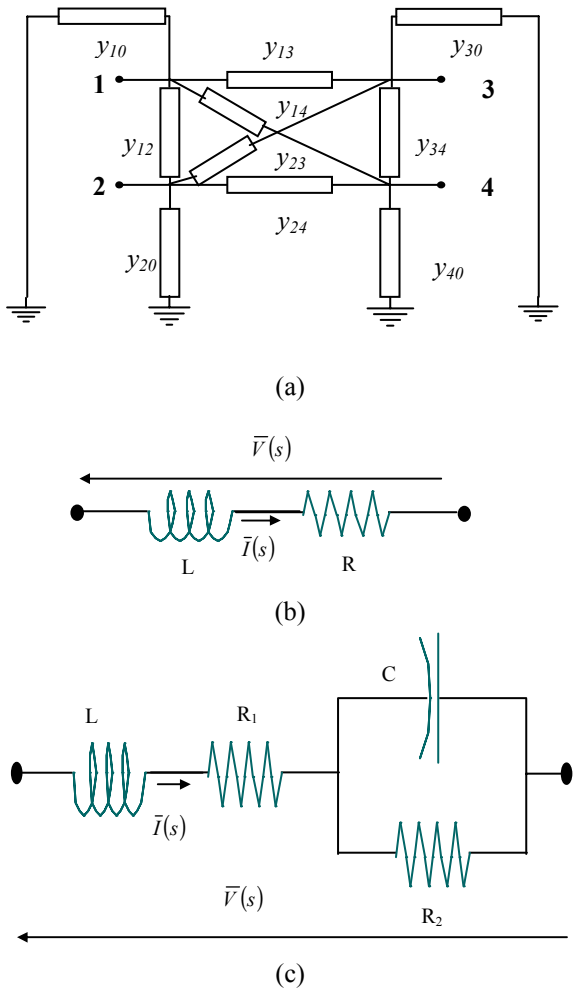


Figure 1. Equivalent circuit for: (a) admittance based representation (b) real pole and (c) complex pole.

For the previous expression the following relations hold:

$$L = \frac{1}{(res_1 + res_2)}$$
$$R_1 = \frac{1}{(res_1 + res_2)}\left[-(p_1 + p_2) + \frac{1}{(res_1 + res_2)}(res_1 p_2 + res_2 p_1)\right] \tag{9}$$
$$C = \frac{(res_1 + res_2)}{p_1 p_2 + \left[-(p_1 + p_2) + \frac{1}{(res_1 + res_2)}(res_1 p_2 + res_2 p_1)\right]\frac{(res_1 p_2 + res_2 p_1)}{(res_1 + res_2)}}$$
$$R_2 = -\frac{1}{C}\frac{res_1 + res_2}{res_1 p_2 + res_2 p_1}$$

The passivity of the rational approximation is enforced as outlined in [13]. It should be noted that the enforcement of passivity should be done at the external ports from which S-parameters are measured and hence from which the whole system is characterized. This enforcement does not strictly imply all the lumped elements'value be greater than zero. Although, in principle, negative values are allowed, some commercial circuit solvers do not accept circuit elements with negative values.

In order to overcome this limitation and making the extraction procedure more exportable an all-positive equivalent circuit for a negative element can be obtained by putting an appropriate current-controlled current-source in parallel with it [6]. The controlled source forces a current twice as much the original one, and the net contribution at the external node is kept unaltered, as demonstrated in Figs. 2.

In Fig. 2a $V = (-Z)(-I) = ZI$ and in Fig. 2b one has $I' = 2I - I,\ V' = (+Z)I' = ZI = V$. The drawback of this approach is the increasing of the complexity of the circuit.

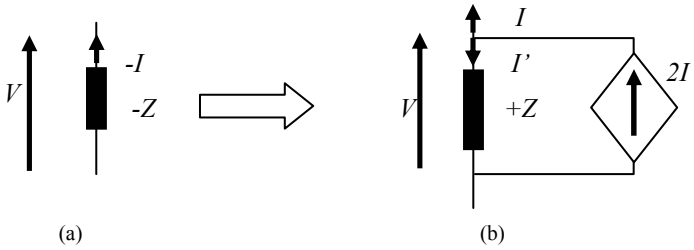
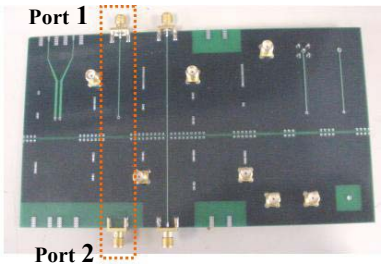


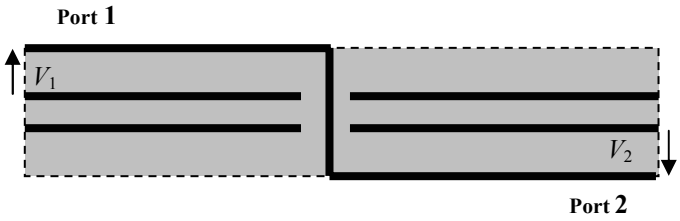
Figure 2. From original negative "Z" element (a) to equivalent circuit with positive one (b).

III. Test Board, Measurement and Results

The test board on which the above procedure has been applied is illustrated in Fig. 3a. It is a four layers board of total thickness t =1.63 mm and dimensions 18 cm x 10 cm; the dielectric material is FR-4 with nominal relative electric permittivity 4.5. The dotted inset indicates the specific structure considered: two 50Ω microstrips (one on the TOP layer and one on the BOTTOM) 5cm long, connected by a plated through hole (PTH) via passing the two reference planes, not connected between them. The two traces are accessible by two edge mounted SMA connectors and the stack-up of the structure is in Fig. 3b.



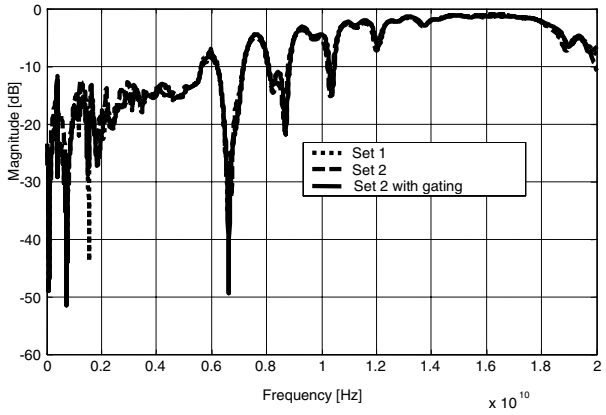
(a)



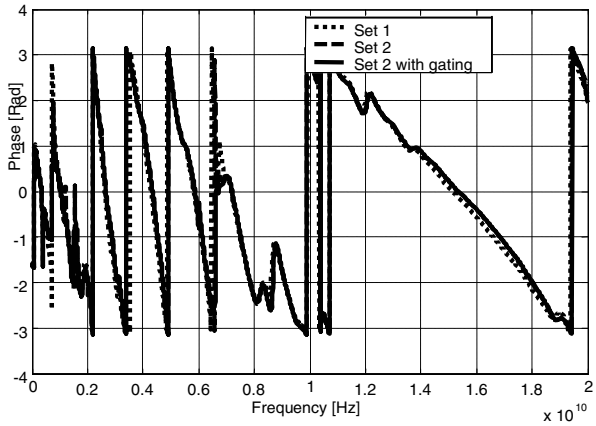
(b)

Figure 3. Test board: (a) general view and (b) its stack-up.

Two identical samples of the board are available. In order to cross-validate the values of the measured S-parameters (starting point of the overall technique) two independent measurements (Set 1 and Set 2) have been performed and the results compared. In the frequency range 40 MHz to 20 GHz three different sets of S-parameters measurements have been performed, each one of 1600 frequency points and then combined in order to cover the complete range with 4800 frequency samples. The comparison of magnitude and phase S_{11} and S_{21} are shown in Fig. 4. To get rid from the S-mesurement of the artefacts due to the mismatch of the adapters connecting the traces to the vector network analyzer (VNA Anritsu 37247C) a windowing and gating procedures is applied. Windowing is a frequency filter that is applied to the data. This filtering rolls off the abrupt transitions at the ends of the frequency range. An IFFT algorithm is then applied to each one of the measured S-parameters; after the transformation, a second window between t_{START} and t_{STOP} is selected on the time domain transformed signal (this is referred as gating). This action removes unwanted time-domain responces. The gated time domain signal is then transformed back in frequency domain by means of an FFT algorithm.



(a)



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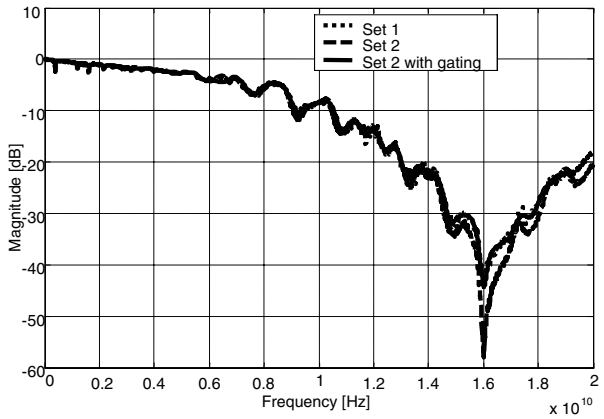

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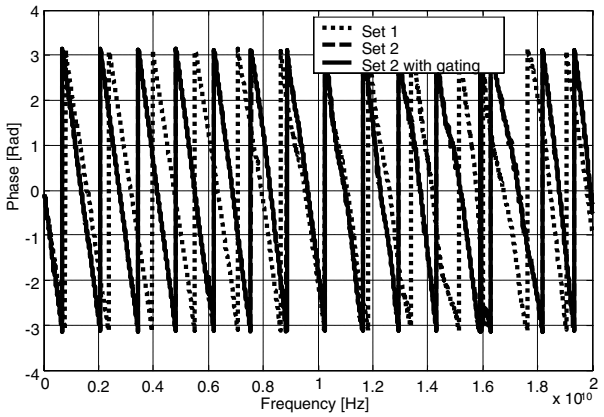
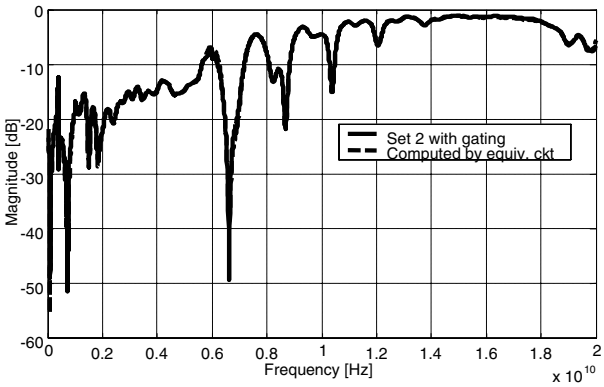


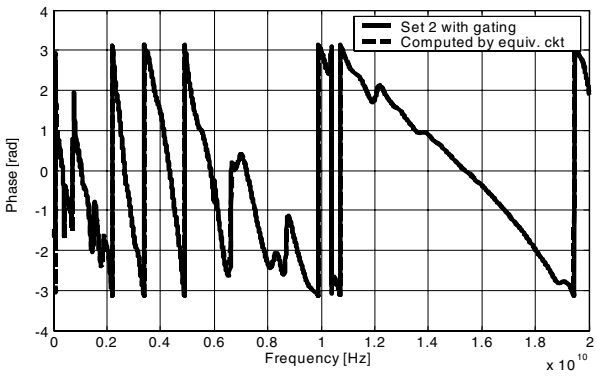
(d)

Figure 4. Measured S-parameters in UAq and UMR: (a) S_{11} magnitude, (b) S_{11} phase, (c) S_{21} magnitude, (d) S_{21} phase.

In this work the selection of t_{START} and t_{STOP} is based on a visual inspection of the measured data and carried out on an heuristic fashion. When the discontinuities to be removed are not small, windowing and gating can provide only a first order approximation because in presence of multiple reflections, gated out effects may easily show up in the main data-set as reflections. However these have small amplitudes and their effects on the time domain waveforms is often negligible as indicated in Figs. 4 and 5 for this case. In order to take into account also this aspect a more systematic procedure is object of investigation. In Fig. 4 are also reported the measured S-parameters Set 2, at which have been applied this gating procedure with t_{START} = 0.0 ns and t_{STOP} = 2.2828 ns (Set 2 with gating). Starting from the measured and gated S-parameters at ports 1 and 2 (see Fig.3) the equivalent circuit extraction technique described in the previous SECTION is applied: 230 poles/residues pairs for a total of 800 lumped elements, that become 1400 when the negative values are converted to positive one, as described in Fig. 2. Fig. 5 shows the agreement of the measured S-parameters with those computed by using the extracted equivalent circuit: both magnitude and phase almost overlap giving confidence on the reliability of the proposed procedure. It is experience that minor or negligible differences between the measured and computed network response in frequency domain can result in significant discrepancies when the comarison is done considering time domain responses of the same network. This is even more true when the system and its equivalent circuit are excited by a voltage step with fast rise time. In order to check the robustness of the extracted circuit, the test board has been used for a TDR measurement. The TDR equipment (TEKTRONIX CSA 8000 OS) has a nominal voltage step of 0.5 V and a nominal rise time of 50 ps. Fig. 6a shows the comparison between the measured and the computed transient voltage at Port 1 (with Port 2 open) for a time window of about 9 ns. The increasing of the voltage for late time is due to the open condition of Port 2 and to the fact that the two reference planes are not connected between them.



(a)



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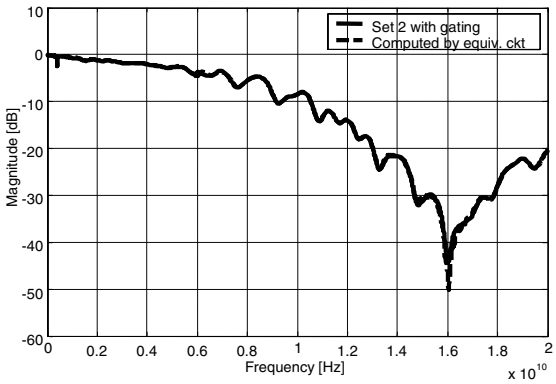

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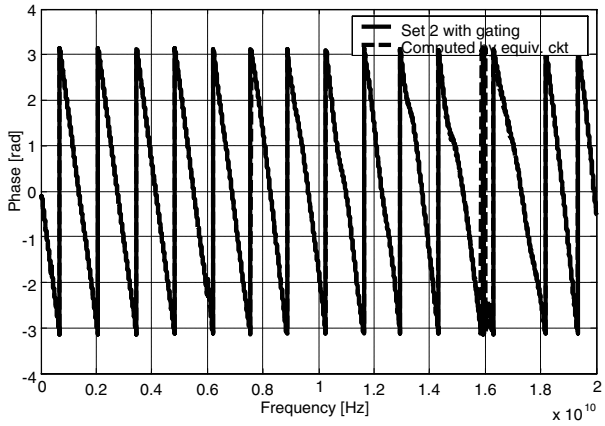
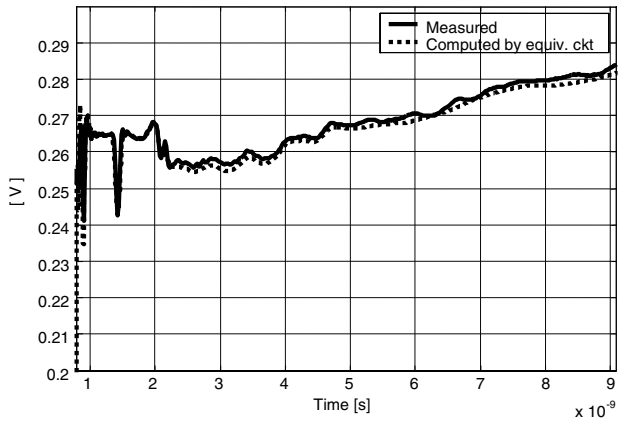


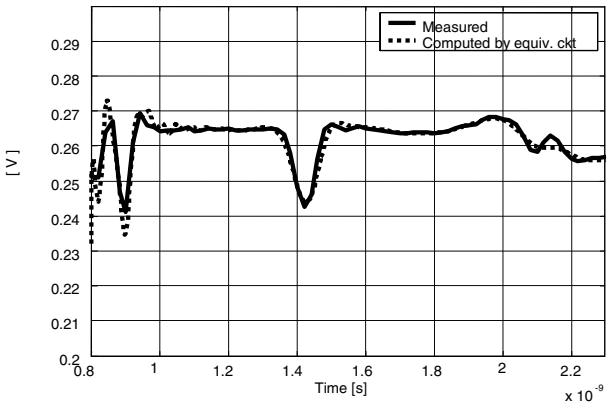
(d)

Figure 5. Comparison between measured and simulated by equivalent circuit S-parameters: (a) S_{11} magnitude, (b) S_{11} phase, (c) S_{21} magnitude, (d) S_{21} phase.

Fig. 6b shows a detailed view of the early time behaviour of the measured and computed voltage waveforms. It allows one to appreciate the similarity of the two waveforms both in amplitude and timing.



(a)



(b)

Figure 6. Measured and simulated by equivalent circuit TDR response at Port 1: (a) complete time window, (b) early time detail.

The eye pattern (EP) diagram is a common tool for SI analysis in order to quantify the performances of the data-link. At Port 1 of the test board a 2.5 Gbps NRZ-coded Pseudo-Random Bit Sequence (PRBS) 2^7-1 bits long is applied. Each bit swings between $\pm$ 400 mV with nominal rise and fall time of $\tau_r = \tau_f = 100$ ps. The used PRBS has nominal 0 (zero) DC component. This is done to mitigate, in the equivalent circuit, the lack of information on the frequency response of the board at frequencies lower than the starting one at 40 MHz. A digital oscilloscope is used at Port 2 to record the EP of the transmitted signal. In Fig. 7 are compared the measured EP and the computed one by means of the above extracted equivalent circuit.

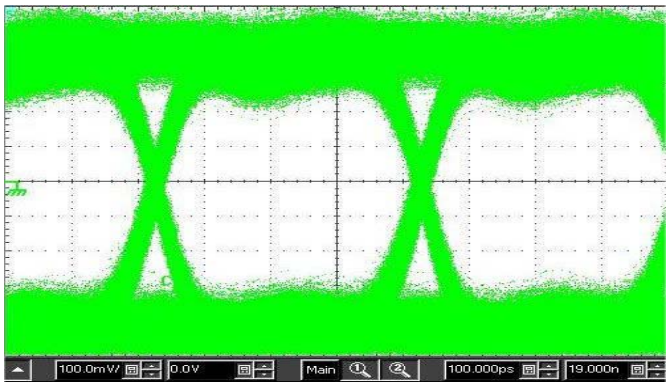


Figure 7a. Measured EP (100 ps/div, 100 mV/div).

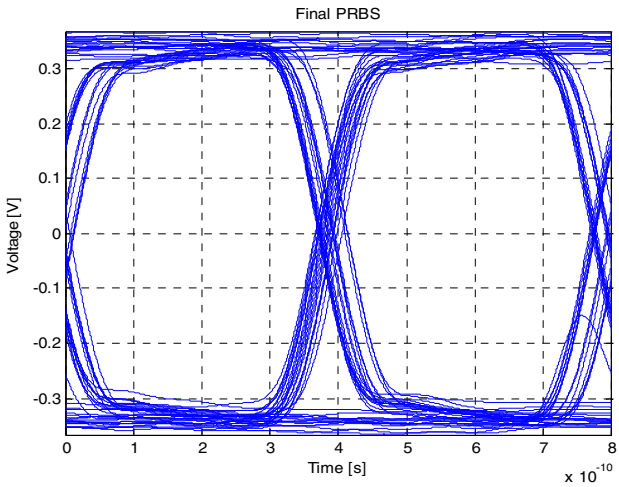


Figure 7b. Computed EP by using the equivalent circuit (100 ps/div, 100 mV/div).

The values of the Maximum Eye Opening (MEO) and the Maximum Eye Width (MEW) [14] computed in Fig. 7a and 7b are in good agreement as shown in TABLE I.

TABLE I – COMPARISON OF MEASURED AND COMPUTED MEO AND MEW.

	Fig. 7a Measured	Fig. 7b Computed
MEO [mV]	560	610
MEW [ps]	365	355

IV. CONCLUSIONS

In this work the procedure for the extraction of an equivalent circuit, based on the rational fitting of measured network parameters in frequency domain and subsequent interpretation of each pole/residue pair has been validated in frequency and in time domain. It has been noted as two main actions make possible the good performances in both domain of the extracted circuit: 1) the use of a suitable number of sample points for the measured S-parameters, starting values for the extraction procedure. In this case 1600 frequency samples per decade have been used; and 2) the use of gating to get rid of unwanted reflections that corrupt the true frequency response of the structure under test.

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