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Large Scale Signal and Interconnect FDTD Modeling for BGA Package

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Abstract—This paper introduces a Finite-Difference Time-Domain (FDTD) approach to modeling portions of Ball Grid Array (BGA) package interconnect circuits. A fullwave circuit model including vias, trace segments, and ground vias was generated, using a computer gridding tool, and fed into the FDTD [1] program. The simulated results were correlated with TDR measurements.

I. INTRODUCTION

The BGA package is one of the most commonly used package type. It is important to understand the fullwave electro-magnetic effects on the package. As the signal transmission speed increases, the design of the BGA package becomes more critical. Fullwave tools are essential to simulate and estimate the transmission, reflection, and coupled RF signal from die to the solder ball. However, there are two major obstacles for fullwave modeling: it is very difficult to model the fine structure of the circuits, which include hundreds of traces and vias, and it usually takes a large amount of cells for the full wave tools to be able to represent the physical geometry, which leads to a large computation time.

A parallel compatible FDTD program [2] offers a solution for large scale models. The parallel FDTD program is based on the Message Passing Interface (MPI) [3] and has been verified on a cluster with 130 machines. A standalone program was implemented to generate the FDTD mesh from an allegro board file. The mesh program was able to create an approximate model for each circuit layer, generate vias and antipads, and add the source and load. With such extended ability, the parallel FDTD program can handle a sophisticated packaging and interconnects model with many million. In our experiments, the cross-talk model of four signal traces, twenty-eight vias, and hundreds of ground vias consists of 60 million cells. A single trace transmission model takes about 17 million cells. and takes approximately 24-48 hours for the cluster to get sufficient simulation results.

The typical circuit structures in a BGA package model include signal traces and vias. This work is focused on the transmission line effect of the signal traces and wave propagation in large scale FDTD modeling.

II. APPROACH

The BGA package in the experiment consists of eight layers: TOP, FC3, FC2, FC1, BC1, BC2, BC3 and the bottom layer. The thickness of each layer and substrate is shown in Figure 2. Twenty traces, a differential clock pair and 18 data traces, were selected. The signal was connected to traces residing on layer FC3 by via, and then routed to solder points through 6. Most of the traces propagate on the layer of FC3. The metallization is copper and the dielectrics used are ABF-GX13 and BT-679FG.
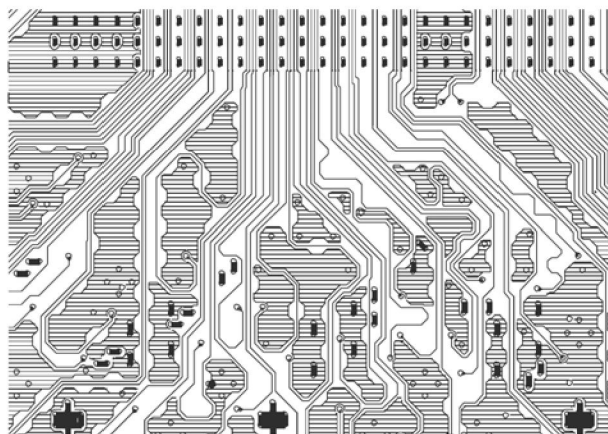

Figure 1 Twenty traces of interests in the BGA package in layer FC3.
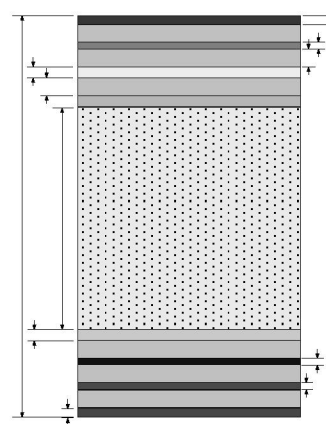

Figure 2 Twenty traces on different layers

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o verify the simulation results, a TDT/TDR measurement is performed on the package. A step source of 194.5 mV is induced on the die side and probe is attached to the BGA side. The input rise time is 39.5 ps and the output delay is about 118.6 ps for DAT02, and the output rise time is 81.5 ps as shown in Figure 4.
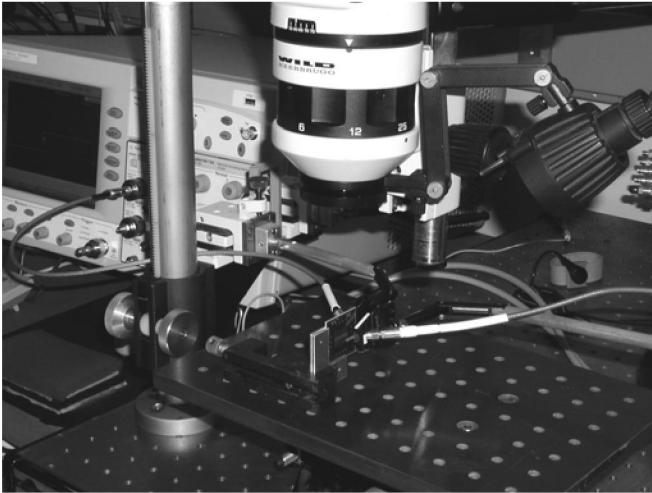

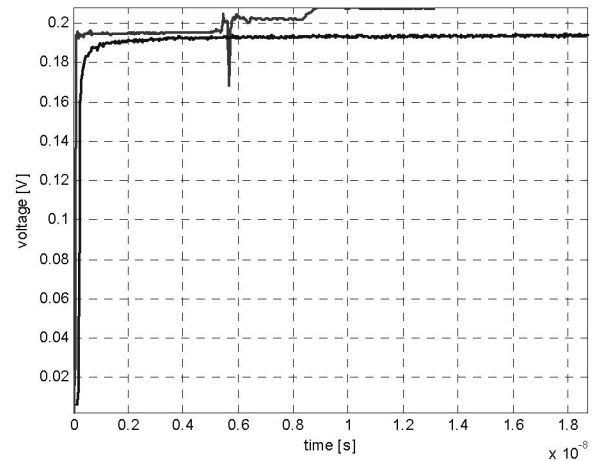Figure 3 TDR measurement setup.

Figure 4 Measured signal propagation on DAT02

To be able to model the circuit, a script file was implemented to extract a text file from the allegro board. The extracted text file was then parsed to get the information for layer, substrate, trace segments and vias. The program divided the physical geometry by a designated cell size and creates discrete plate location. The vias, traces and plane islands were represented by the PEC plates of different size and location. A single trace, L3_CP_PP_CL3_CLK3_DAT_02 (DAT_02) was used to generate the first FDTD model. The typical trace widths were about 20 to 40 um. The cell size was set at 10 um X 20 um X 10 um according to the trace width and the total number of cells was 17 million. Normal dielectrics were used between the layers. Since EZ-FDTD only takes rectangle shapes, the diagonal traces have to be segmented into small pieces of rectangles. The model file generated about 1000 lines of geometry description. Figure 5 shows DAT_02 (fifth trace from left) and its relative position compared to the rest of the traces.
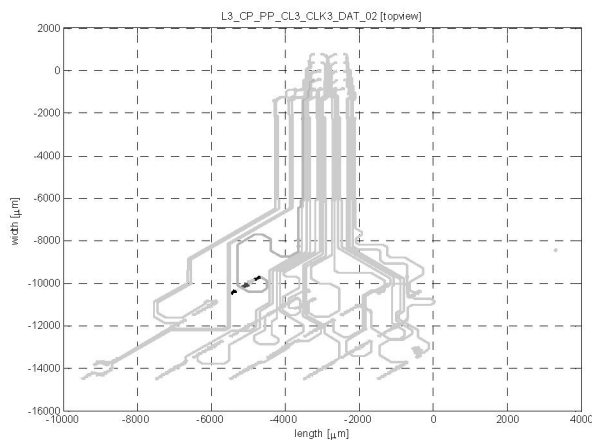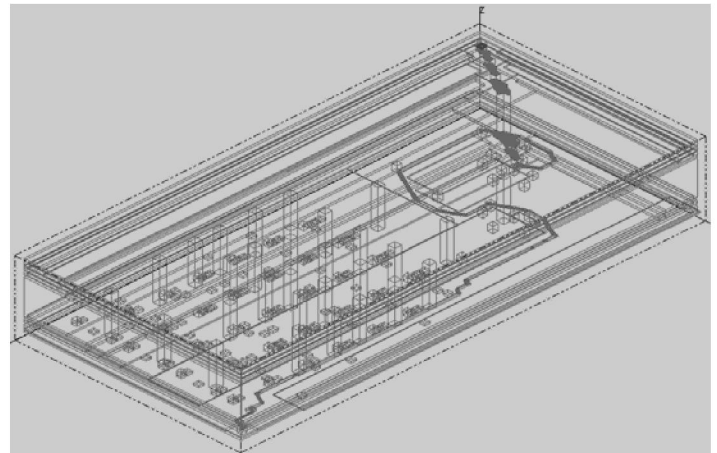

Figure 5 L3_CP_PP_CL3_CLK3_DAT_02 (DAT_02)

Figure 6 EZ-FDTD model for DAT_02

A step source of 0.194 V was added between layer FC3 and layer FC2. A thin wire connected the rest of the ground planes together. Twenty 1-K Ω resistors were added to the edge of the via above the bottom plane, shown as small purple cubes in the upper right corner of the Figure 7. The boundary condition is set to be Perfect Matched Layer (PML). The number of the white cells is ten and the number of PML cells is eight.
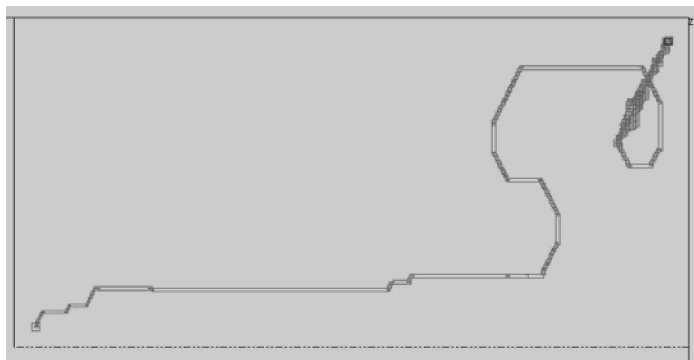
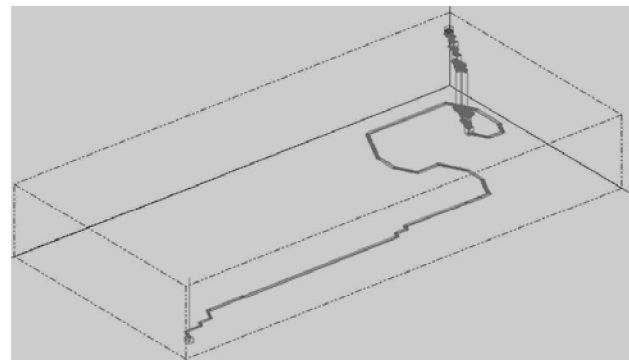**300**

Figure 7 Topview of the trace DAT_02

Figure 8 3D view of the trace DAT_02

After the geometry was built, (many slightly different models were simulated to ascertain the gridding effects on the method of termination, source impedance and reflection.) The material properties for the non-conductive layers are shown in Table 1.

Table 1 Material properties

Material Type	Relative permittivity	Relative permeability	Conductivity
ABF-GX13	3.2	1.000	0.0202
BT-679FG	4.8	1.000	0.0202

The simulated results are correlated with the measured results. There is some ringing in the waveform, the ring frequency is on the order of delay time. More results will be presented at the conference.
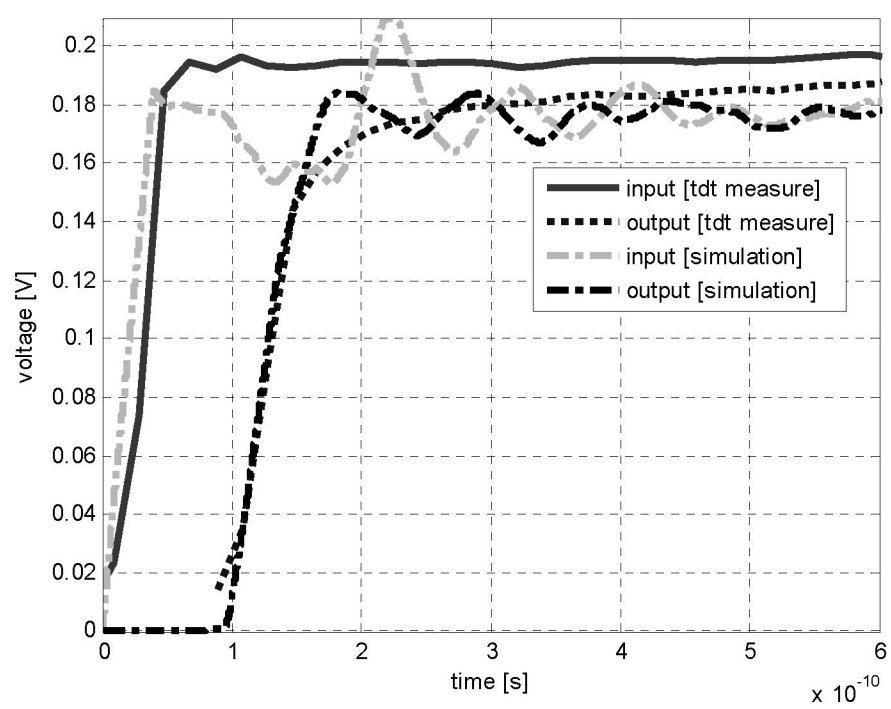

Figure 9 Simulation for single signal trace transmission

III.   APPLICATION AND FUTURE WORK

The BGA package modeling capability could be useful in many aspects of circuitry simulation such as cross-talk analysis, signal transmission and reflection.

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A. Cross-talk

The FDTD program will be able to model and simulate the cross-talk models. The fullwave cross-talk model in Figure 10 used approximately 60 million cells and a total of 7 GB memory.
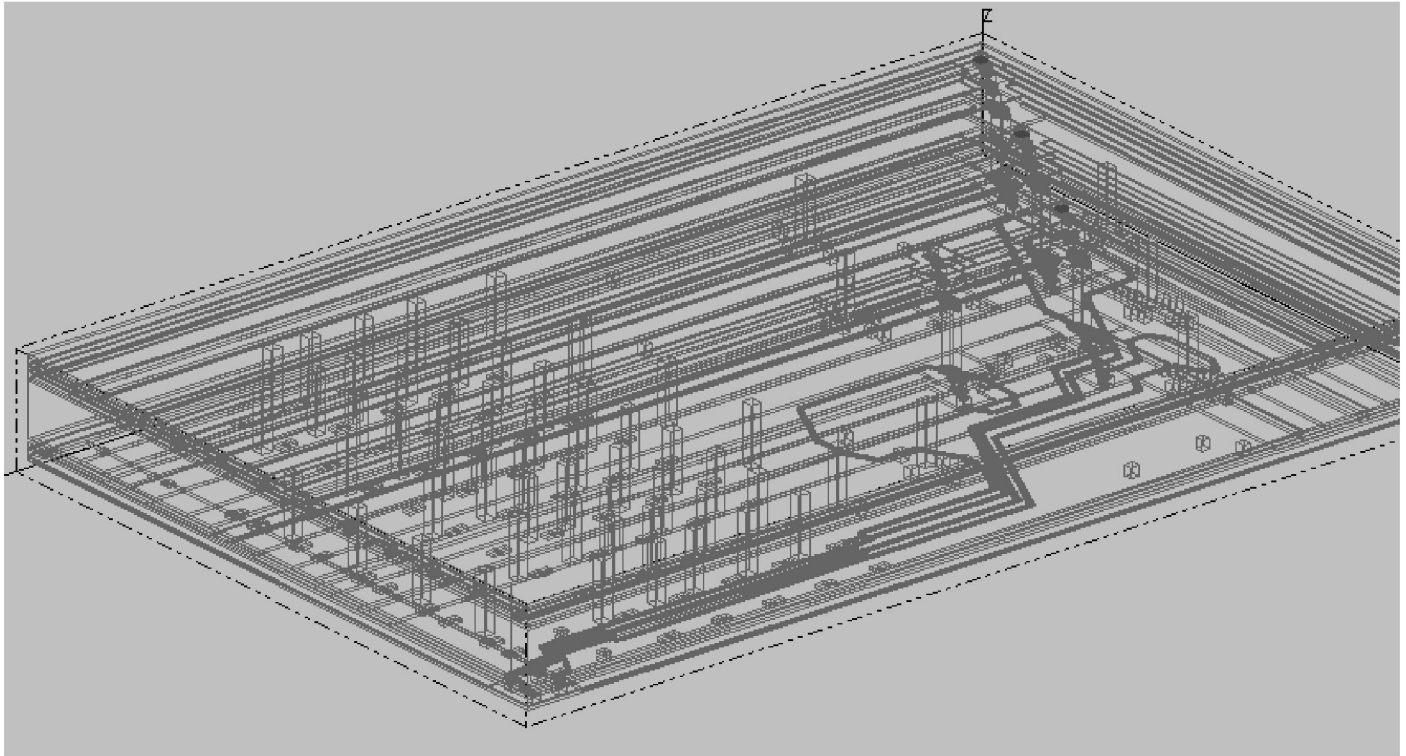

Figure 10 Cross-talk model of DAT_02, 03, 06 and 07

B. Future work

The only limit on the problem size that the parallel FDTD program can simulate is the computational ability of the cluster. IBM BlueGene® now has 131,000 IBM PowerPC processors and can compute 280.6 trillion operations per second. However, as the model increase, it is more difficult to check the trace and ground connectivity in the model. A cross-talk model can easily have more than 4000 lines of cell configuration.

IV. SUMMARY AND CONCLUSIONS

A parallel compatible FDTD program was used to model a part of the BGA package including a differential clock pair and eighteen data traces. This approach used automatic model generation program to create FDTD model geometry. Simulated results compared correlatively with the TDR measurements, demonstrated that large scale package circuitry can be modeled by an FDTD tool. For the single trace propagation example, the simulated results agree within 10% of the measured results.

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