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Overdistention Operation of Cascaded Multilevel Inverters

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***Abstract*—In the past decade, the multilevel power converter has transitioned from an experimental concept to a standard product of many medium-voltage drive manufacturers. By utilizing small voltage steps, the multilevel topology offers higher power quality, higher voltage capability, lower switching losses, and improved electromagnetic compatibility over standard topologies. Recently, several researchers have focused on the cascaded multilevel inverter whereby two multilevel inverters are series connected to a motor load by splitting the neutral connection. The resulting performance is exceptional in terms of power quality since the overall number of voltage levels is effectively the product of the two cascaded inverters. This paper demonstrates that it is possible to extend this performance to an even higher number of voltage levels referred to as overdistended operation. This further improves the power quality that is significant in applications that have stringent total harmonic distorsion requirements, such as naval ship propulsion. A new control is introduced for overdistention operation and is validated with computer simulation and laboratory measurements.**

***Index Terms*—Multilevel converter, multilevel inverter, pulsewidth modulation, space vector.**

I. Introduction

ONE OF THE most significant recent advances in power electronics is the multilevel inverter. Using this concept, the power conversion is performed in small voltage steps, resulting in better power quality. Although this requires more power transistors, they are of lower voltage and operate with a low frequency so that the switching losses are also reduced. Further advantages include higher voltage capability and better electromagnetic compatibility (due to lower dv/dt transitions). Some of the fundamental multilevel topologies include the diode-clamped [1], flying capacitor [2], and series H-bridge [3], [4] structures. Recently, there has been much interest in combinational topologies such as the cascaded multilevel inverter [5]–[9] structure shown in Fig. 1. Therein, a standard multilevel inverter (having n_1 voltage levels) supplies a motor load from a dc source $v_{\rm dc1}$. The motor neutral is opened up so that a second multilevel inverter may be effectively placed in series. The second inverter is supplied from an isolated source $v_{\rm dc2}$ and is capable of producing n_2 voltage levels. It is important to point out that the ground points of the dc sources $g1$ and $g2$ are not connected. If they were, the topology would effectively operate as an H-bridge structure. With the sources isolated, the inverters operate in series and there is a multiplying effect in the number of voltage levels. Specifically, it can be shown that the effective number of voltage levels supplied to the load is the product of n_1 and n_2 if the ratio $v_{dc1} : v_{dc2}$ is set appropriately [6]. This results in exceptional power quality. Another interesting feature of the cascaded multilevel inverter is the natural split between a higher voltage inverter operating at a low switching frequency and a lower voltage inverter operating at a high switching frequency. The higher voltage inverter supplies the bulk of the power and the lower voltage inverter performs waveform conditioning (much like an active filter). In this case, higher voltage low-frequency devices [such as integrated gate commutated thyristors (IGCTs)] can be mixed with lower voltage high-frequency devices [such as insulated gate bipolar transistors (IGBTs)].

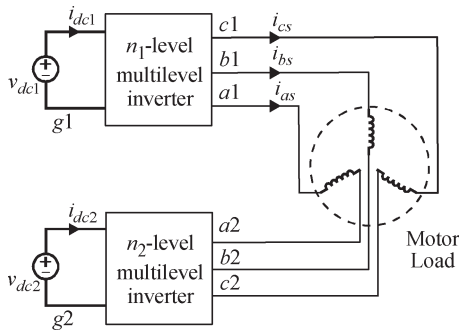

Fig. 1. Cascaded multilevel inverter topology.

The cascaded topology also has several advantages over a traditional multilevel structure which are of particular interest in Naval propulsion applications. Besides, high power quality, the dual nature of the topology allows for incorporation of commercial-off-the-shelf components. For example, the bulk inverter may be supplied by a commercial drives manufacturer; requiring only the lower-power conditioning inverter to be custom made. Also, the dual structure provides some redundancy which will increase survivability. In the case where the bulk inverter is disabled, points $a1$, $b1$, and $c1$ can be shorted together and the motor could be-driven by the lower-power inverter (keeping in mind that only a fraction of the power is required to operate at half speed for propulsion loads).

In this paper, a cascaded multilevel inverter involving two three-level inverters is studied. The typical voltage ratio allows

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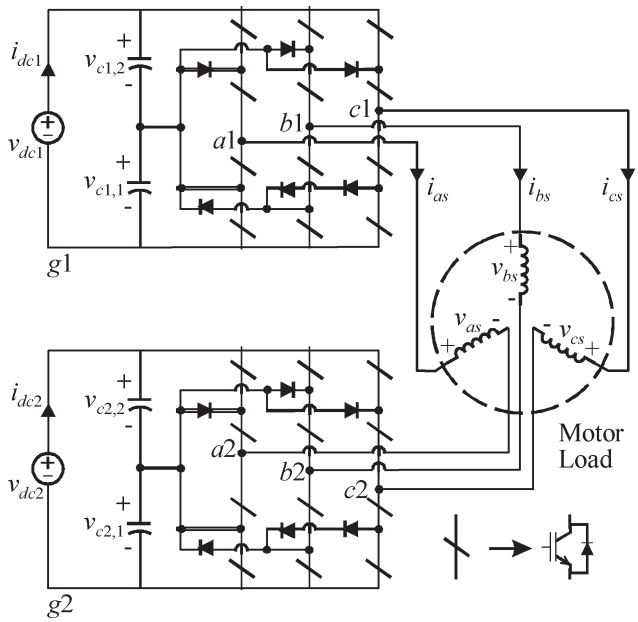

Fig. 2. Cascade-3/3 multilevel inverter topology.

nine-level performance and this is referred to as maximal distention. Previous simulation and laboratory work has shown that this combination is capable of achieving 9% voltage total harmonic distortion (THD) without filtering [6]. The analysis is then extended by changing the dc voltage ratio so that 11-level performance is achieved. This condition is referred to as overdistention. The penalty for operating in overdistention is that there are missing voltage levels in the high modulation index region. However, the simulation and laboratory measurements herein, show that the voltage THD is approximately 7.8% even with the absent voltage levels. In Naval ship propulsion applications, the decrease in THD amounts to smaller and lighter weight filtering requirements to meet the stringent specifications (frequently 2%–3%). In a ship application, size and weight are of primary concern so a slight change in THD could be significant. This paper contains the details of the modulation control for overdistention operation including the method for operation with omitted voltage levels.

II. Cascaded Multilevel Inverter

Fig. 2 shows the topology considered herein. Since it is a cascaded connection of two three-level diode-clamped [1] inverters, it is referred to as a cascade-3/3 inverter. The individual inverters will be referred to as inverter 1 (upper inverter) and inverter 2 (lower inverter).

A. Fundamental Operation

The most important concept is the relation of switching states (typically output from a controller) to voltage levels. As an example, the a-phase line-to-ground voltages of inverter 1 are related to a controller switching state by

$$v_{a1g1} = \frac{s_{a1}}{2} v_{dc1} \tag{1}$$

$$v_{a2g2} = \frac{s_{a2}}{2} v_{dc2}. \tag{2}$$

By definition, (1) and (2), are voltages from nodes $a1$ to $g1$ and $a2$ to $g2$ (shown in Fig. 2), respectively. The controller switching states s_{a1} and s_{a2} are defined so that their lowest state is 0. Since this is a three-level inverter topology, the states may have values of 0, 1, and 2 indicating a line-to-ground voltage of zero, half, and full-dc voltage. Equations (1) and (2) are accurate if the capacitors split the dc voltage evenly (or $v_{c1,1} = v_{c1,2}$ and $v_{c2,1} = v_{c2,2}$). This is true for the three-level inverter in steady-state operation, and can also be readily ensured by the controller [6]. Similar expressions to (1) and (2) can be written for the b- and c-phases.

From (1) and (2), it can be seen that the controller directly determines the line-to-ground voltages. However, the load phase voltages v_{as}, v_{bs}, and v_{cs} are usually of interest in a higher-level motor vector control. These can be computed from the line-to-ground voltages in the following way. By KVL, a voltage equation for each phase may be developed as

$$v_{a1g1} = v_{as} + v_{a2g2} + v_{g2g1} \tag{3}$$

$$v_{b1g1} = v_{bs} + v_{b2g2} + v_{g2g1} \tag{4}$$

$$v_{c1g1} = v_{cs} + v_{c2g2} + v_{g2g1}. \tag{5}$$

By adding (3)–(5) and noting that $v_{as} + v_{bs} + v_{cs} = 0$ for standard motor loads [10], an expression for the voltage between the two grounds may be obtained as

$$v_{g2g1} = \frac{1}{3}(v_{a1g1} + v_{b1g1} + v_{c1g1} - v_{a2g2} - v_{b2g2} - v_{c2g2}). \tag{6}$$

By substitution of (6) into (3)–(5), the load phase voltages can be computed in terms of the line-to-ground voltages as

$$v_{as} = \frac{2}{3}(v_{a1g1} - v_{a2g2}) - \frac{1}{3}(v_{b1g1} - v_{b2g2}) - \frac{1}{3}(v_{c1g1} - v_{c2g2}) \tag{7}$$

$$v_{bs} = \frac{2}{3}(v_{b1g1} - v_{b2g2}) - \frac{1}{3}(v_{a1g1} - v_{a2g2}) - \frac{1}{3}(v_{c1g1} - v_{c2g2}) \tag{8}$$

$$v_{cs} = \frac{2}{3}(v_{c1g1} - v_{c2g2}) - \frac{1}{3}(v_{a1g1} - v_{a2g2}) - \frac{1}{3}(v_{b1g1} - v_{b2g2}). \tag{9}$$

From (7)–(9), it can be seen that the phase voltages are made up of a combination of all six line-to-ground voltages which are related to the controller switching states as outlined in (1) and (2). It can also be seen by the differential terms in (7)–(9) that the effect of the series connection is a subtraction of the voltage levels of inverter 2 from inverter 1.

B. Global Voltage Levels

In the cascaded connection, the number of overall (or global) voltage levels is a function of the voltage ratio between the two dc sources. To illustrate this, Table I shows the complete set of a-phase switching states when the dc voltage ratio is set to $v_{dc1} : v_{dc2} = 3 : 1$. This is accomplished by setting $v_{dc1} = 6E$

TABLE I
CASCADE-3/3 GLOBAL SWITCHING STATES
(DEMONSTRATING MAXIMAL DISTENTION)

s_a	s_{a1}	s_{a2}	v_{a1g1}	v_{a2g2}	v_{a1g1}-v_{a2g2}
0	0	2	0	$2E$	$-2E$
1	0	1	0	E	$-E$
2	0	0	0	0	0
3	1	2	$3E$	$2E$	E
4	1	1	$3E$	E	$2E$
5	1	0	$3E$	0	$3E$
6	2	2	$6E$	$2E$	$4E$
7	2	1	$6E$	E	$5E$
8	2	0	$6E$	0	$6E$

and $v_{dc2} = 2E$; where E is a constant dc value. The line-to-ground voltages v_{a1g1} and v_{a2g2} are related to the switching states s_{a1} and s_{a2}, respectively as depicted in (1) and (2). In the far right column, the difference in the line-to-ground voltages of inverter 1 and 2 are shown. This term was seen to be a governing term in (7)–(9). As can be seen, this voltage has nine even steps of voltage level E. This allows the definition of a global switching state for the a-phase s_a as in Table I. Since nine unique voltage levels are obtained, the global number of voltage levels is the product of the number of levels in each inverter. This is referred to as maximal distention since it is the maximum number possible while maintaining even separation of voltage levels.

In practice, Table I can be used as a breakout table. A nine-level pulsewidth modulator (PWM) outputs a global switching state with nine-levels which can then be directly converted to individual switching states s_{a1} and s_{a2} for inverters 1 and 2, respectively. For a multilevel inverter the specific transistors are then a direct function of these switching states (or levels) [1].

Although the nine-level case is the maximally distended, it is possible to operate in overdistention. This can be demonstrated by setting the voltage ratio to $v_{dc1} : v_{dc2} = 4 : 1$. This case is shown in Table II where $v_{dc1} = 8E$ and $v_{dc2} = 2E$. As with the maximal distended case, the voltage levels are evenly spaced. However, it is not possible to make up some of the voltage levels. In particular, global switching states $s_a = 3$ and $s_a = 5$ cannot be obtained.

In the next section, it will be theoretically shown that the inverter can operate in overdistention with 11-levels despite the absent switching states. A modulation scheme will then be developed to demonstrate overdistention operation.

C. Voltage Vector Analysis

Analysis of the voltage vectors provides a convenient way of understanding the inverter operation. The voltage vectors are created by first transforming the phase voltages to the $q-d$ stationary reference frame [10] using

$$v_{qs}^s = v_{as} \tag{10}$$

$$v_{ds}^s = \frac{1}{\sqrt{3}}(v_{cs} - v_{bs}). \tag{11}$$

Next, a plot of v_{ds}^s versus v_{qs}^s is created for all possible combinations of inverter 1 and 2 switching states. Fig. 3

TABLE II
CASCADE-3/3 GLOBAL SWITCHING STATES
(DEMONSTRATING OVERDISTENTION)

s_a	s_{a1}	s_{a2}	v_{a1g1}	v_{a2g2}	v_{a1g1}-v_{a2g2}
0	0	2	0	$2E$	$-2E$
1	0	1	0	E	$-E$
2	0	0	0	0	0
void					
4	1	2	$3E$	$2E$	$2E$
5	1	1	$3E$	E	$3E$
6	1	0	$3E$	0	$4E$
void					
8	2	2	$6E$	$2E$	$6E$
9	2	1	$6E$	E	$7E$
10	2	0	$6E$	0	$8E$

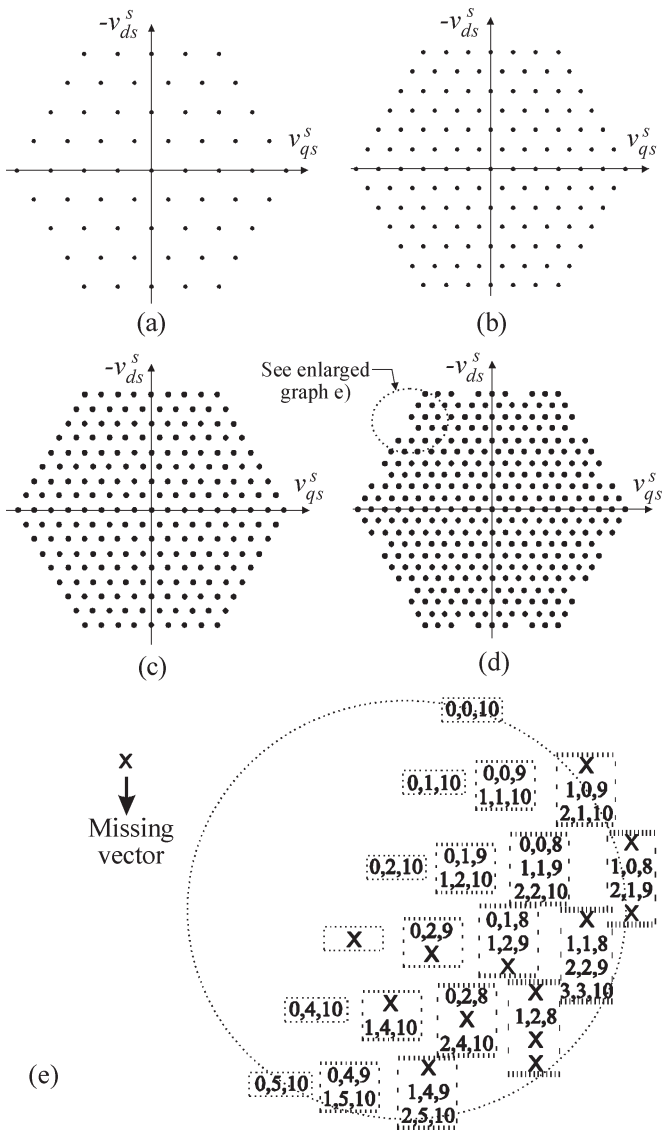

Fig. 3. Voltage vector plots for the cascade-3/3 inverter. (a) $v_{dc1} : v_{dc2} = 1 : 1$. (b) $v_{dc1} : v_{dc2} = 2 : 1$. (c) $v_{dc1} : v_{dc2} = 3 : 1$ (maximal distention). (d) $v_{dc1} : v_{dc2} = 4 : 1$ (overdistention). (e) Enlarged detail space-vector plot.

shows the voltage vector plots for various dc voltage ratios. In Fig. 3(a), the dc voltages are equal. In this domain, an ideal set of sinusoidal voltages appears as a perfect circle and the modulator will attempt to form this circle from the available

discrete voltage vectors (dots). Therefore, with a higher density of vectors, the inverter can track commanded voltages with a lower THD. For the case in Fig. 3(a), the cascaded inverter is operating as a five-level inverter (incidentally, this can be determined by counting the number of vectors on one side of the hexagon). If the voltage ratio is set to $v_{dc1} : v_{dc2} = 2 : 1$, as in Fig. 3(b), the pattern changes. This case can be seen to operate as a seven-level inverter and the density of voltage vectors is increased. In Fig. 3(c), the dc voltage ratio is set to $v_{dc1} : v_{dc2} = 3 : 1$ and the cascaded inverter is operating as a nine-level inverter. The density of vectors is even greater and therefore the resulting THD will be lower than the cases of Fig. 3(a) and (b).

Fig. 3(d) shows the vector plot for the case where $v_{dc1} : v_{dc2} = 4 : 1$. In this case, the density of voltage vectors is further increased. However, since the operation is beyond maximal distention, there are missing vectors on the outside of the hexagon. According to this vector analysis, if the commanded voltage is in the region where the vectors are evenly spaced, normal operation is possible. When the commanded voltage is high, it enters the region where the vectors are missing. In this region, it is still possible to track the reference, but the nearest vectors are further apart degrading the performance slightly. As an example of this, Fig. 3(e) shows a zoomed in portion of the vector plot of Fig. 3(d). Therein, each vector is indicated by a dashed box which contains all of the switching states. The notation is the global switching states for all three phases. For example, the vector {0,0,10} represents $s_a = 0$, $s_b = 0$, and $s_c = 10$. In fact, the vector plot was created by indexing through all possible combinations of switching states and calculating the q- and d-axis stationary voltages accordingly. Several switching state combinations result in the same voltage vector. These redundant states can be identified by increasing or decreasing the switching states in all three phases at the same time. For example, switching states {0, 0, 9} and {1, 1, 10} produce the same voltage vector.

As seen in Fig. 3(d), the cascaded-3/3 inverter has an equivalent 11-level space vector plot in overdistention except for some missing vectors near the outside. As it turns out, there are missing switching state combinations for inner vectors as well, which are not seen in Fig. 3(d). Since redundant state combinations produce the same vector, these missing vectors can be classified into non-redundant missing vectors (NRMV) and redundant missing vectors (RMV) depending on whether the vectors have redundancy. To be clear, it is helpful to define $s_{\max}$, $s_{\min}$ and rd (redundant degree) as

$$s_{\max} = \max(s_a, s_b, s_c) \tag{12}$$

$$s_{\min} = \min(s_a, s_b, s_c) \tag{13}$$

$$rd = nl - (s_{\max} - s_{\min}) \tag{14}$$

where the max function returns the maximum switching state among the three-phase joint switching states s_a, s_b, and s_c and the min function returns the minimum. The variable nl represents the number of the equivalent switching levels (11 in the overdistended case). For NRMVs, the rd is always equal to one and one of the switching states among s_a, s_b, and s_c includes the missing level (3 or 7). For RMVs, rd is greater than one and some switching states among s_a, s_b, and s_c are 3 or 7. There are 12 NRMVs are located around the outer loop of Fig. 3(d). For example, there should be a vector determined by the joint switching states {0, 3, 10} in the space vector plot of the conventional 11-level inverter. However, due to the missing level 3, caused by overdistention operation, this vector is absent. Since the redundant degree of NRMVs is 1, there is no remedy for these missing vectors, and this leads to the empty vector spots in the outer loop as shown in Fig. 3(e). For RMVs, it is easy to see from Fig. 3(e) that there is always redundancy available. For example there should be a vector determined by the joint switching states {0, 3, 9} in the space vector plot of the conventional 11-level inverter. However, due to the missing switching level 3, caused by overdistention operation, {0, 3, 9} is absent. Since the rd of this joint switching state is 2, there is a group of joint redundant switching state {1, 4, 10} available to generate the same space vector, and this state can be regarded as the remedy for the missing vector when performing the modulation.

In summary, the overdistention operation of the cascade-3/3 inverter generates two void line-to-ground converting levels compared to the nine converting levels under maximal distention operation. Furthermore, from Table II and Fig. 3(d) and (e), it can be seen that the two missing switching levels (3 and 7) have undesirable influences on the space vector plot. Twelve outer voltage vectors are missing and the cascaded inverter cannot work equivalently as a conventional 11-level inverter when the commanded voltage is higher than 91.7% of the maximum voltage and the performance will be degraded slightly in this scenario. However, the power quality will still be better than that of maximal distention (nine-level) operation. To minimize the negative influences, special care needs to be taken when performing the modulation techniques as described below.

III. Overdistention Modulation Techniques

The concluding purpose of the modulation technique is to control the transistor gate signals so that power semiconductor may switch on/off as desired. The gate signals are directly related to the switching states (or levels) s_a, s_b, and s_c. As shown in (1) and (2), these switching states may be computed by normalizing the commanded line-to-ground voltage to the dc voltage. The PWM switching is typically accomplished by defining duty-cycles based on the normalized commanded line-to-ground voltages which may be expressed as

$$d_{am} = \frac{10}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \tag{15}$$

$$d_{bm} = \frac{10}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \tag{16}$$

$$d_{cm} = \frac{10}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right]. \tag{17}$$

In (14)–(16), the modulation index determines the amplitude of the commanded phase voltages and has a range of 0–1.15

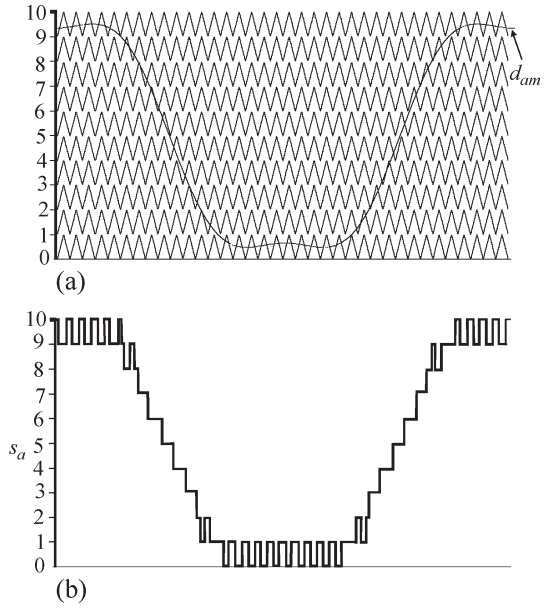

Fig. 4. Overdistention sine-triangle modulaton technique $(m < 1.05)$. (a) Modified duty cycle and triangle waveforms. (b) Switching state.

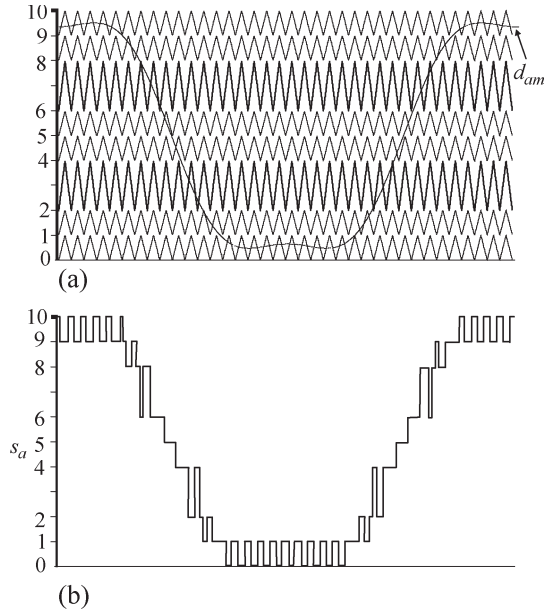

Fig. 5. Overdistention sine-triangle modulation technque $(m > 1.05)$. (a) Modified duty cycle and triangle waveforms. (b) Switching state.

since a third harmonic term is included [11]. The angle θ_c is the converter angle which is $2\pi f_e t$ for a constant fundamental frequency f_e. The inverter switching states can be determined by comparing the duty-cycles to multiple triangle waveforms [11], [12]. Alternatively, some drive systems utilize a digital signal processor (DSP) implementation in which definition of the triangle waveforms is not necessary [11]. These methods can also be applied to the overdistended cascade-3/3 inverter. However, when cascaded inverters are working in overdistention mode, some missing switching levels will occur as discussed before and special care needs to be taken due to this anomaly.

A. *Typical Modulation* $(m \leq 1.05)$

When the modulation index is lower than 91.7% of its maximum value $(m \leq 1.05)$, the overdistended cascade-3/3 inverter has the vector density of an 11-level inverter. Fig. 4 demonstrates the 11-level sine-triangle modulation technique when $m = 1.05$. For this modulation index (and any modulation index lower), the duty cycle is compared to a set of ten triangle waveforms ($nl - 1$ in a general sense). The switching state is then equal to the number of triangle waveforms that the duty cycle is greater than. Fig. 4 shows this process for the a-phase. The b- and c-phase duty cycles are compared to the same set of triangle waveforms to produce global switching states for all three phases.

Even though the levels 3 and 7 do not exist, from a space vector point of view, those missing levels result in RMVs as shown in Fig. 3(d) and (e). Therefore, the 11-level sine-triangle modulation technique can be applied directly except that a redundant states selection (RSS) procedure for RMVs needs to follow the modulation. the RSS procedure amounts to shifting all phases (up or down) whenever a void switching state is encountered. In general, a redundant state may be found for a given switching state by incrementing or decrementing the states for all three phases since this results in changing the zero-sequence line-to-ground voltage, which does not affect the load voltages. The boundary states are the joint states with the highest switching level or the lowest switching level involved in some certain phases. For instance, if the converting levels range from 0 to 10, the redundancy of the joint switching states 3, 7, 8 can be found by continuously adding 1 to or subtracting 1 from each state so as to find {0, 4, 5}, {1, 5, 6}, {2, 6, 7}, {4, 8, 9}, and {5, 9, 10}, all of which refer to the same space vector. The boundary states are {0, 4, 5} and {5, 9, 10} in this example. Therefore, if the modulation process described above commands state {3, 7, 8} at some time, it can be replaced with one of the redundant states that do not involve levels 3 and 7.

B. *Extended Modulation* $(m > 1.05)$

When the modulation index is higher than 91.7% $(m > 1.05)$ of the physical modulation limitation, NRMVs will be encountered. In this scenario, a suitable modulation technique needs to be able to bypass the NRMVs by jumping to joint switching states close to the missing ones. However, the modulation technique shown in section A aims at providing evenly distributed switching levels and thus cannot handle the requirements for NRMVs. To solve this problem, the triangle waveforms are redefined as shown in Fig. 5. It can be noticed that the switching level ranges from 0 to 10, but levels 3 and 7 are avoided by stretching the triangle waveforms so that the amplitude is doubled around these levels. The rules to produce the switching states by comparison to the triangle waveforms are the same as in typical modulation described above. The resulting switching state can be seen to have large jumps around levels 3 and 7. In a practical implementation, the triangle frequency would be much higher (but is lowered here to illustrate the switching rules). Although the switching state jumps levels, the fast-average (average over one period of the triangle waveform) is

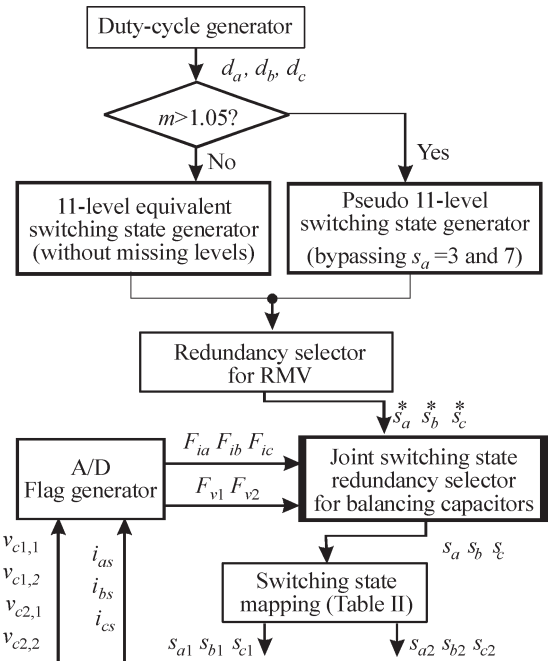

Fig. 6. Modulation control flowchart.

the same as the duty cycle. Therefore, the resulting voltage still tracks the fundamental component, but with slightly increased harmonics.

C. Modulation Algorithm

Fig. 6 shows a flow chart for the modulation process. First, the duty cycles are generated according to (15)–(17). Depending on the modulation index being used, either the 11-level or pseudo 11-level modulation process (as described in Figs. 4 and 5, respectively) is used to obtain global switching states. This is passed through a redundant state selector to avoid missing vectors for RMV (as described in section A above). The resulting commanded switching states s_a^*, s_b^*, and s_c^* are passed through another stage of RSS which has the goal of balancing the capacitor voltages and ensuring that $v_{c1,1} = v_{c1,2}$ and $v_{c2,1} = v_{c2,2}$. The details of this process are not described herein, but involves evaluating all redundant states and using the one which improves the capacitor voltage balance [11], [12]. For this operation, the values of capacitor voltages and phase currents can be used [12] or the direction of the capacitor voltage error and phase current direction (analog flags) can be use as input to a table for faster processing [11].

IV. Simulation and Experimental Validation

A computer simulation was developed for verifying the cascade-3/3 11-level inverter where $v_{dc1} = 625$ V, $v_{dc1} = 156$ V, and $f_e = 60$ Hz. The load was an R–L load with parameters $R = 15\ \Omega$ and $L = 24.2$ mH per phase. It is interesting to view the simulated inverter performance for several values of modulation index. Fig. 7 shows the utilized voltage vectors for modulation indices of $m = 0.6$, $m = 0.9$, and $m = 1.13$. For the lower modulation indices, the vectors follow the commanded value (ideal circle) with utilization of the

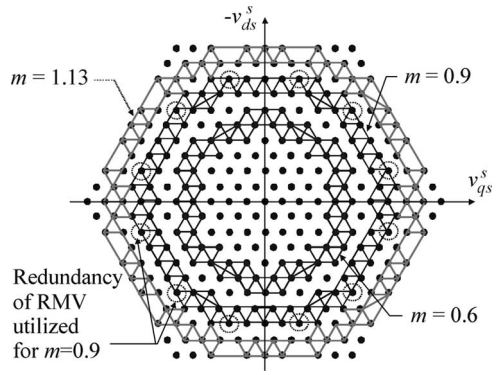

Fig. 7. Ideal space-vector patterns for the cascade-3/3 converter n overdistention operation.

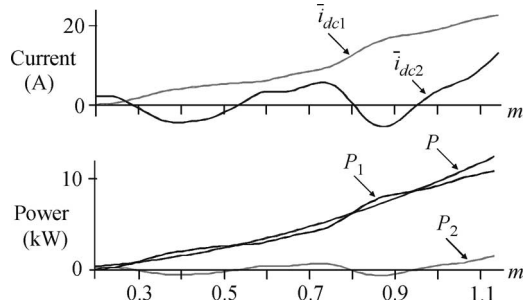

Fig. 8. Average steady-state dc current and power versus modulation index (overdistention operation).

nearest voltage vectors. This demonstrates the effectiveness of the RMV method for obtaining the available voltage vectors. For the modulation index $m = 1.13$, it can be seen that the modulator effectively moves around the missing vectors. Fig. 8 shows the dc current and inverter powers versus modulation index, where $\bar{i}_{dc1}$ and $\bar{i}_{dc2}$ denote the average steady-state current of inverter 1 and inverter 2, respectively. The powers are defined as

$$P_1 = v_{dc1}\bar{i}_{dc1} \tag{18}$$

$$P_2 = v_{dc2}\bar{i}_{dc2} \tag{19}$$

$$P = P_1 + P_2. \tag{20}$$

From Fig. 8 it can be seen that the total power is increased with the increasing modulation index for a fixed load and fixed frequency. However, inverter 2 may either provide or absorb power. This will not be a problem if the dc source allows power absorption. Since the dc voltage of inverter 2 is much lower than inverter 1, the power from inverter 2 is relatively small. Therefore, power source providing v_{dc2} can be much smaller than the main power source providing v_{dc1}.

Fig. 9 shows simulation results for modulation indices of $m = 0.55$ and $m = 1.13$. These operating points were chosen since they have positive power from inverter 2 and will be used for later comparison with laboratory measurements where inverter 2 is supplied from a rectifier source. In Fig. 9, the line-to-line voltage waveform (defined as $v_{ab} = v_{as} - v_{bs}$) and the a-phase current are shown. The corresponding utilized vectors are also shown. As with other multilevel inverters, the line-to-line voltage shows even steps between levels for the case where

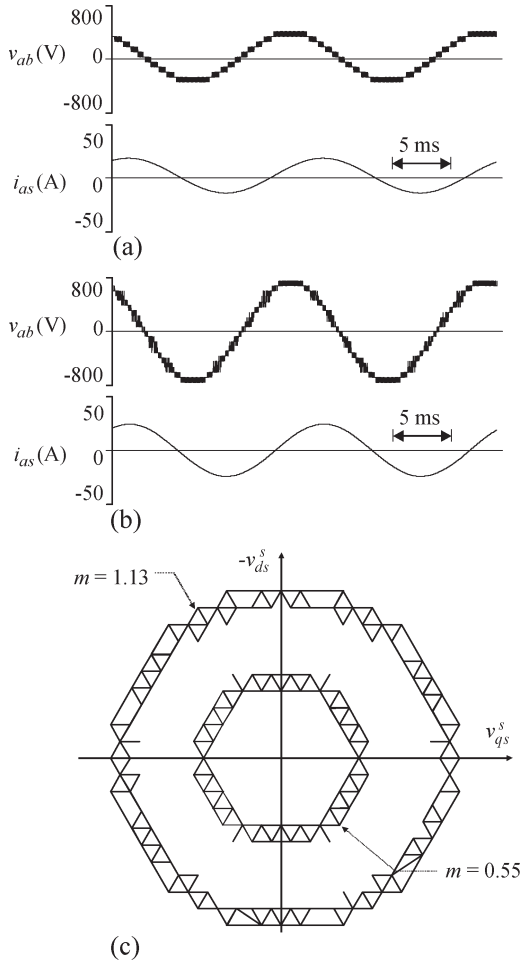

Fig. 9. Overdistented cascade-3/3 inverter simulation results. (a) Low modulation index ($m = 0.55$). (b) High modulation index ($m = 1.1.3$). (c) Utilize voltage vectors.

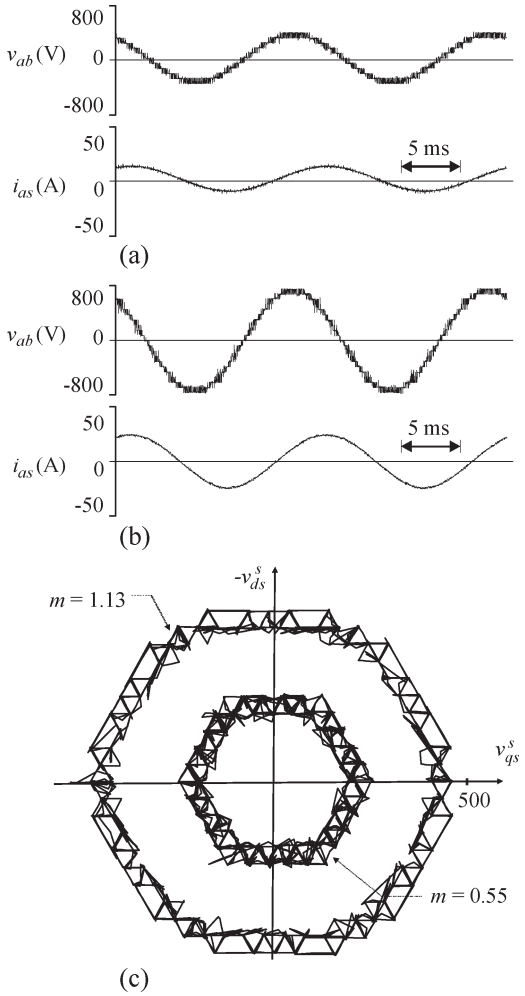

Fig. 10. Overdistented cascade-3/3 inverter laboratory measurements. (a) Low modualtion index ($m = 0.55$). (b) High modulation index ($m = 1.13$). (c) Utilize voltage vectors.

$m = 0.55$. For this case, the THD of v_{ab} is 12.53%. The reason for this (relatively) high THD is that the voltage steps are more significant compared to the fundamental component for lower modulation indices. For the case where $m = 1.13$, larger steps are seen in some portion of the waveform. This corresponds to the points where the modulation skips the missing levels and is also seen in the plot of utilized voltage vectors. The THD of v_{ab} was 8.40% for this study.

The conditions for the laboratory set-up are the same as those used for the simulations described above. Fig. 10 shows the laboratory studies with the same operating conditions as those of Fig. 9. As can be seen, the laboratory measurements are nearly the same as the simulation results. The THD numbers of v_{ab} were 12.47% for $m = 0.55$ and 7.77% for $m = 1.13$ which were close to the simulation results. The laboratory measurements confirm the operation of the modulation methods proposed herein.

V. Conclusion

This paper has studied the overdistention operation of cascaded multilevel inverters. This form of operation is desired since it effectively increases the available voltage converting levels in spite of some missing levels. An advanced modulation technique for overdistention operation was introduced based on the cascade-3/3 inverter. When the modulation index is lower than 91.7%, it can generate an equivalent space vector pattern as the conventional 11-level inverter. When the modulation index is higher than 91.7% of the upper physical limit, it can generate a slightly degraded 11-level space vector pattern, which still has exceptional power quality. Computer simulation was used to verify the proposed methods and laboratory measurements were very close to simulation predictions.

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