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Mahyar Zarghami

Mariesa Crow
Missouri University of Science and Technology, crow@mst.edu

Jagannathan Sarangapani
Missouri University of Science and Technology, sarangap@mst.edu

Yilu Liu

et. al. For a complete list of authors, see https://scholarsmine.mst.edu/ele_comeng_facwork/809

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A Novel Approach to Interarea Oscillation Damping by Unified Power Flow Controllers Utilizing Ultracapacitors

Mahyar Zarghami, *Member, IEEE*, Mariesa L. Crow, *Fellow, IEEE*, Jagannathan Sarangapani, *Senior Member, IEEE*, Yilu Liu, *Fellow, IEEE*, and Stan Atcitty

***Abstract*—This paper discusses a novel approach for damping interarea oscillations in a bulk power network using multiple unified power flow controllers (UPFCs) utilizing ultracapacitors, also known more generally as electrochemical capacitors (ECs). In this paper, a new control is introduced to mitigate interarea oscillations by directly controlling the UPFCs' sending and receiving bus voltages that better utilizes the stored energy in the ECs. The results of this controller are compared with and without ECs. The proposed control provides better interarea oscillation mitigation when applied to multiple UPFCs in the 118-bus IEEE test system.**

***Index Terms*—Electrochemical capacitors (ECs), oscillation damping, power system stability, unified power flow controller (UPFC).**

I. Introduction

In addition to steady-state power flow control, damping oscillations in a power network is one of the primary applications of a unified power flow controller (UPFC). As high-voltage power electronics become less expensive, flexible ac transmission systems (FACTS) devices will become more prevalent in the bulk transmission system to control active power flow across congested corridors and ensure voltage security. An added benefit of UPFCs deployed in the transmission system is that they can also effectively control active power oscillations that can damage generators, increase line losses, and increase wear and tear on network components. Therefore, developing suitable control strategies is a requirement before UPFCs can be confidently utilized in the power system.

Mitigating power oscillations can be accomplished by rapidly changing the power flow through the series part of the UPFC. By controlling the amplitude and angle of the series-injected voltage, the active and reactive power flow in the transmission line can be altered. Several authors have investigated utilizing the UPFC to damp interarea oscillations utilizing a variety of control approaches [1]–[10]. Some of this research is based on a linear control analysis of the UPFC and power system [1]–[5], whereas other authors consider nonlinear control systems theory and Lyapunov energy functions [6]–[10]. Regardless of which approach the control law is based upon, the UPFC controller ultimately performs the control by commanding the appropriate modulation amplitudes (k_1 and k_2) and angles (α_1 and α_2) of the series and shunt voltages.

Further mitigation control can be achieved by the inclusion of independent high-power-density energy storage. Ultracapacitors [electrochemical capacitors (ECs)] can be used as rapid-discharge energy storage for power applications. ECs have been used extensively in pulsed power applications for high-energy physics and weapons applications. Ideal power system applications for ECs are short-duration storage applications such as power stabilization, power quality ridethrough applications, and voltage flicker mitigation among other applications that require high power density and rapid recharge. The major difference between an EC compared to a conventional capacitor is that the liquid electrolyte structure and porous electrodes give the EC a high effective area that minimizes the distance between the two plates. Additionally, unlike batteries, ECs have cells that can be connected in series and parallel to obtain the desired voltage level and capacitance [11]. The dc-link capacitor of the UPFC voltage-source converter provides the ideal interface for an EC. In steady-state, the dc-link capacitor serves as a dc voltage from which the sinusoidal voltage waveform is constructed through pulsewidth modulation. The voltage of this capacitor is tightly controlled so that there is no degradation in the staircase waveform. During small transients, the dc-link capacitor will charge or discharge to compensate for converter losses in the UPFC. During large transients, however, the ability to exchange active power with the external power system is desirable to aid in damping oscillations. In this situation, the energy stored in the dc-link capacitor is inadequate to accomplish significant damping without severe dc voltage degradation. By utilizing a bidirectional dc-dc converter, the EC can be fully discharged without significantly impacting the voltage across the dc-link capacitor. For this reason, an EC is an attractive solution for providing large amounts of short-term active power.

In this paper, a new control methodology, specifically designed to take advantage of the EC, is introduced for damping

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M. Zarghami is with ABB, Inc., Raleigh, NC 27610 USA.

M. L. Crow and J. Sarangapani are with the Department of Electrical and Computer Engineering, Missouri University of Science and Technology, Rolla, MO 65409-0810 USA.

Y. Liu is with the Electrical and Computer Engineering, University of Tennessee, Knoxville, TN 37996 USA.

S. Atcitty is with Sandia National Laboratories, Albuquerque, NM 87123-3453 USA.

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interarea oscillations in which the sending and receiving end voltages are controlled instead of the active and reactive powers. This is based on a two-stage control scheme in which the controlling UPFC voltages are first determined, and then the desired sending and receiving end conditions are imposed upon the UPFC dynamics to derive the controlling modulation amplitudes and angles. This approach effectively utilizes the energy stored in the EC by discharging (or charging) the EC by the amount required to achieve the desired bus voltages and angles. The control approach is validated using a full nonlinear system simulation in the 118-bus IEEE test system. The resulting dynamics indicate that the proposed controller provides significant damping.

II. UPFC Model

The UPFC is the most versatile FACTS device. It consists of a combination of a shunt and series branches connected through a dc capacitor, as shown in Fig. 1. The series-connected inverter injects a voltage with controllable magnitude and phase angle in series with the transmission line, thus providing real and reactive power to the transmission line. The shunt-connected inverter provides the active power drawn by the series branch plus the losses, and can independently provide reactive compensation to the system. The dc-link capacitor is connected to the EC through a bidirectional dc-dc converter. The UPFC model is a combination of the static synchronous compensator (STATCOM) and static synchronous series compensator (SSSC) models [12] (see (1)–(6) at the bottom of the page, where the parameters are as shown in Fig. 1). The currents i_{d1} and i_{q1} are the dq components of the shunt current. The currents i_{d2} and i_{q2} are the dq components of the series current. The voltages $V_1\angle\theta_1$ and $V_2\angle\theta_2$ are the sending end and receiving end voltage magnitudes and angles, respectively. The UPFC parameters are the following:

$\omega, (\omega_s)$	(synchronous) angular frequency;
R_{s_1}, L_{s_1}	shunt resistance and inductance;
R_{s_2}, L_{s_2}	series resistance and inductance;
$V_{\rm dc}$	dc-link voltage;
$C_{\rm dc}, R_{\rm dc}$	dc-link capacitance and resistance;
$V_{\rm dcEC}$	EC dc voltage;
$C_{\rm EC}, R_{\rm ESR}$	EC capacitance and equivalent resistance.

The UPFC is controlled by varying the phase angles $(\alpha_1 \text{and} \alpha_2)$ and magnitudes $(k_1 \text{and} k_2)$ of the converter shunt and series output voltages $(e_1 \text{and} e_2)$, respectively. The EC is connected to the dc-link capacitor of the UPFC through a bidirectional dc-dc converter such as the SEPIC/Zeta converter [13]. The steady-state dc-link capacitor voltage and the EC voltage are related through the duty cycle ratio D [13] as

$$V_{\rm dc} = \frac{D}{1-D} V_{\rm dcEC}. \tag{7}$$

The duty cycle $0 \le D \le 1$ is the percent of a switching cycle in which the EC discharges. For example, if $D = 0.5$, then the EC is in steady state and discharges (and charges) for half of each cycle, and $V_{\rm dc} = V_{\rm dcEC}$. If $D > 0.5$, then the EC discharges for a greater portion of the switching cycle and $V_{\rm dcEC}$ drops (and *vice versa* charges for $D < 0.5$).

The power balance equations at bus 1 are given by

$$\begin{aligned} 0 =& V_1 \left((i_{d_1} - i_{d_2}) \cos\theta_1 + (i_{q_1} - i_{q_2}) \sin\theta_1 \right) \\ & - V_1 \sum_{j=1}^{n} V_j Y_{1j} \cos\left(\theta_1 - \theta_j - \phi_{1j}\right) \end{aligned} \tag{8}$$

$$\frac{1}{\omega_s}\frac{d}{dt} i_{d_1} = \frac{k_1 V_{\rm dc}}{L_{s_1}} \cos(\alpha_1 + \theta_1) + \frac{\omega}{\omega_s} i_{q_1} - \frac{R_{s_1}}{L_{s_1}} i_{d_1} - \frac{V_1}{L_{s_1}} \cos\theta_1 \tag{1}$$

$$\frac{1}{\omega_s}\frac{d}{dt} i_{q_1} = \frac{k_1 V_{\rm dc}}{L_{s_1}} \sin(\alpha_1 + \theta_1) - \frac{R_{s_1}}{L_{s_1}} i_{q_1} - \frac{\omega}{\omega_s} i_{d_1} - \frac{V_1}{L_{s_1}} \sin\theta_1 \tag{2}$$

$$\begin{aligned} \frac{1}{\omega_s}\frac{d}{dt} i_{d_2} =& -\frac{R_{s_2}}{L_{s_2}} i_{d_2} + \frac{\omega}{\omega_s} i_{q_2} + \frac{k_2}{L_{s_2}} \cos(\alpha_2 + \theta_1) V_{\rm dc} \\ & - \frac{1}{L_{s_2}} (V_2 \cos\theta_2 - V_1 \cos\theta_1) \end{aligned} \tag{3}$$

$$\begin{aligned} \frac{1}{\omega_s}\frac{d}{dt} i_{q_2} =& -\frac{R_{s_2}}{L_{s_2}} i_{q_2} - \frac{\omega}{\omega_s} i_{d_2} + \frac{k_2}{L_{s_2}} \sin(\alpha_2 + \theta_1) V_{\rm dc} \\ & - \frac{1}{L_{s_2}} (V_2 \sin\theta_2 - V_1 \sin\theta_2) \end{aligned} \tag{4}$$

$$\begin{aligned} \frac{C}{\omega_s}\frac{d}{dt} V_{dc} =& -k_1 \cos(\alpha_1 + \theta_1) i_{d_1} - k_1 \sin(\alpha_1 + \theta_1) i_{q_1} \\ & - k_2 \cos(\alpha_2 + \theta_1) i_{d_2} - k_2 \sin(\alpha_2 + \theta_1) i_{q_2} \\ & - \left(\frac{1}{R_{\rm dc}} + \frac{1}{R_{\rm ESR}} \right) V_{\rm dc} + \frac{D}{1-D} \frac{V_{\rm dcEC}}{R_{\rm ESR}} \end{aligned} \tag{5}$$

$$\frac{C_{\rm EC}}{\omega_s}\frac{d}{dt} V_{\rm dcEC} = \frac{1}{R_{\rm ESR}} \left(\frac{(1-D)}{D} V_{\rm dc} - V_{\rm dcEC} \right) \tag{6}$$

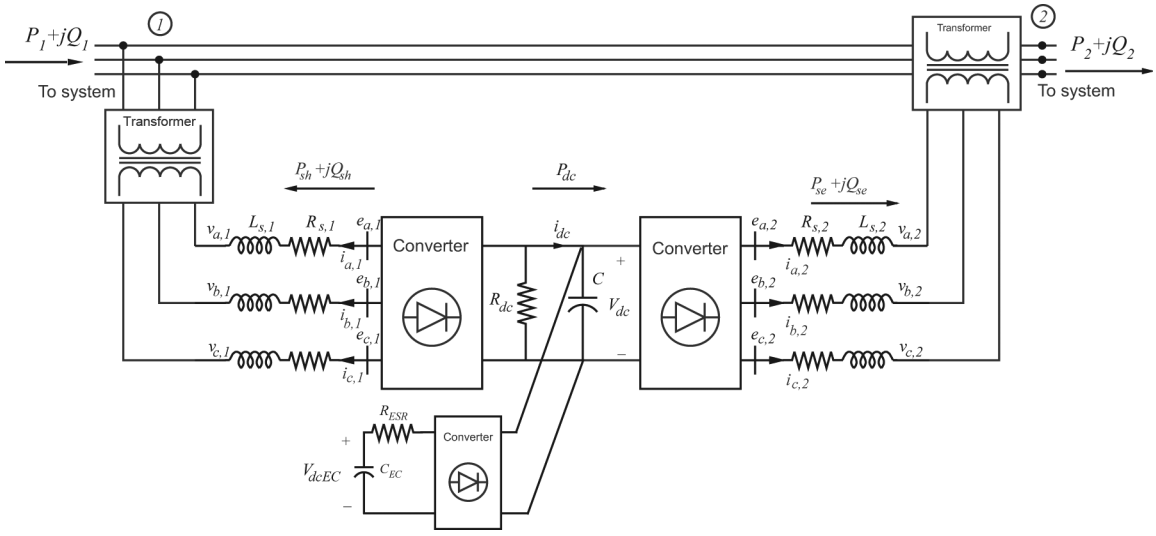

Fig. 1. UPFC with EC Diagram.

$$0 = V_1\left((i_{d_1} - i_{d_2})\sin\theta_1 - (i_{q_1} - i_{q_2})\cos\theta_1\right) - V_1\sum_{j=1}^{n} V_j Y_{1j}\sin\left(\theta_1 - \theta_j - \phi_{1j}\right) \tag{9}$$

and at bus 2

$$0 = V_2\left(i_{d_2}\cos\theta_2 + i_{q_2}\sin\theta_2\right) - V_2\sum_{j=1}^{n} V_j Y_{2j}\cos\left(\theta_2 - \theta_j - \phi_{2j}\right) \tag{10}$$

$$0 = V_2\left(i_{d_2}\sin\theta_2 - i_{q_2}\cos\theta_2\right) - V_2\sum_{j=1}^{n} V_j Y_{2j}\sin\left(\theta_2 - \theta_j - \phi_{2j}\right). \tag{11}$$

III. UPFC Controller Design

For control development purposes, it is desired to isolate the independent current injection points in the network; therefore, several assumptions are initially made. The two simplifying assumptions are that the system loads are modeled as constant impedance loads and can therefore be absorbed into the bus admittance matrix. Second, the generators are modeled as the classical "transient reactance behind constant voltage" model. Note that these assumptions are for control development only—the proposed control is validated with the full nonlinear tenth-order power system model given in the Appendix. Using the load impedance model, the only points of current injection into the network are the generator internal buses, and the UPFC sending and receiving end buses. Furthermore, Kron reduction enables the transmission network to be reduced to an admittance matrix of size $(N + 2n \times N + 2n)$, where N is the number of generator buses and n is the number of UPFCs in the system. Fig. 2 illustrates the reduced system showing the points of current injection. Each UPFC has two current injections i_1 and i_2 at the sending and receiving ends, respectively. The generator current injections are given by i_G. The classical model for the reduced network including the UPFCS is, therefore, given by (12) and (13) at the bottom of the page, where $E_j\angle\delta_j$ is the voltage at bus j, $Y_{jk}\angle\phi_{jk}$ is the (j,k)th element of the reduced admittance matrix, P_{m_j}, M_j, and ω_j are the mechanical power, inertia constant, and angular speed, respectively, of machine j, and ω_s is synchronous speed. The first summation represents the active power injected at each generator bus, the second summation represents the active power injected at each UPFC sending bus, and the third summation represents the active power injected at each UPFC receiving bus.

$$\dot{\delta}_j = \omega_j - \omega_s, \quad j = 1, \ldots, N \tag{12}$$

$$\dot{\omega}_j = \frac{1}{M_j}\left[P_{M_j} - E_j\sum_{k=1}^{N} E_k Y_{jk}\cos\left(\delta_j - \delta_k - \phi_{jk}\right) - E_j\sum_{k=N+1}^{N+n} E_k Y_{jk}\left(\cos\left(\delta_j - \phi_{jk}\right) r_{2(k-N-1)+1} + \sin\left(\delta_j - \phi_{jk}\right) r_{2(k-N-1)+2}\right) - E_j\sum_{k=N+n+1}^{N+2n} E_k Y_{jk}\left(\cos\left(\delta_j - \phi_{jk}\right) r_{2(k-N-1)+1} + \sin\left(\delta_j - \phi_{jk}\right) r_{2(k-N-1)+2}\right)\right] \tag{13}$$

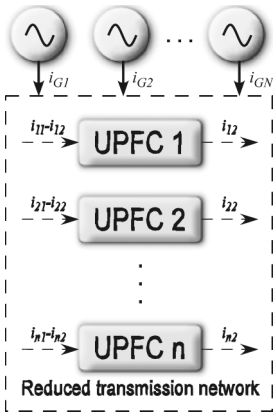

Fig. 2. Equivalent power system from the "voltage control" view.

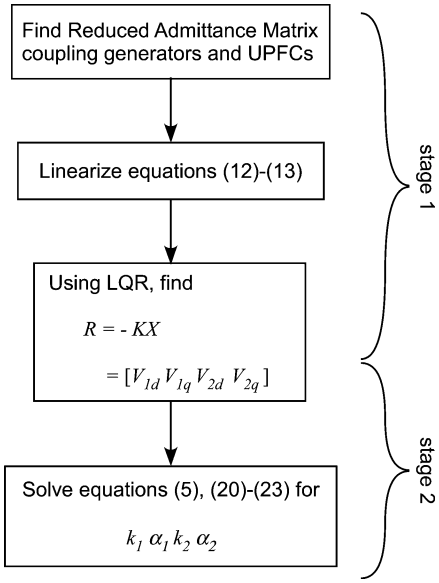

Fig. 3. Two-stage control design.

This nonlinear system has $2N$ states and $4n$ intermediate control inputs r_j defined as

$$r_{2(j-1)+1} = V_{1dj} \tag{14}$$
$$r_{2(j-1)+2} = V_{1qj} \tag{15}$$
$$r_{2(j-1)+2n+1} = V_{2dj} \tag{16}$$
$$r_{2(j-1)+2n+2} = V_{2qj}, \qquad j = 1, \ldots, n \tag{17}$$

where V_{1dj}, V_{1qj}, V_{2dj}, and V_{2qj} are the dq components of the sending (1) and receiving (2) ends for the jth UPFC, respectively. This step describes the first stage of the two stage control. Note that this stage is independent of the UPFC dynamics.

Linearizing this reduced system results in a linear system of the form

$$\dot{X} = AX + BR \tag{18}$$

where R represents the vector of the UPFC dq voltages. This linear system can be stabilized through the feedback control

$$R = -KX \tag{19}$$

where K is chosen using optimal LQR control processes to minimize speed and angle deviations in the generators. The Q and R matrices where chosen to be diagonal matrices. The R matrix was taken as the identity matrix. The diagonal elements of Q corresponding to the generator rotor angles deltas are chosen to be zero, since changes in δ are not penalized. The diagonal elements of Q corresponding to ω are proportional to the inertia constant H.

If the original system were linear, this feedback control would result in the optimal values of voltage magnitudes and angles at both the sending and receiving buses of the UPFC to damp the interarea oscillations.

The second stage of the control is to convert the control inputs R into the modulation gain, and phase angles k and α for each UPFC. The first step in this stage is to find the values of currents i_{d1}, i_{q1}, i_{d2}, and i_{q2} from the UPFC active and reactive power balance equations at the sending and receiving end buses given in (8)–(11).

If it can be assumed that the time scale difference between the UPFCs and the generator dynamics is large (i.e., $1/\omega_s \ll 1/M_i$) and letting $1/\omega_s \approx 0$, then (1)–(4) can be rewritten as their algebraic counterparts; see (20)–(23) at the bottom of the page. Solving (20)–(23) together with (5) provides the values of k_1, α_1, k_2, and α_2 which are the true control inputs to the UPFC. This procedure can be repeated for each UPFC independently since the first stage of the control provides the network coupling during the determination of the input R (the sending and receiving end voltages). Fig. 3 shows a flow chart that illustrates the two-stage control.

$$0 = \frac{k_1 V_{dc}}{L_{s_1}} \cos(\alpha_1 + \theta_1) + \frac{\omega}{\omega_s} i_{q_1} - \frac{R_{s_1}}{L_{s_1}} i_{d_1} - \frac{V_1}{L_{s_1}} \cos\theta_1 \tag{20}$$
$$0 = \frac{k_1 V_{dc}}{L_{s_1}} \sin(\alpha_1 + \theta_1) - \frac{R_{s_1}}{L_{s_1}} i_{q_1} - \frac{\omega}{\omega_s} i_{d_1} - \frac{V_1}{L_{s_1}} \sin\theta_1 \tag{21}$$
$$0 = -\frac{R_{s_2}}{L_{s_2}} i_{d_2} + \frac{\omega}{\omega_s} i_{q_2} + \frac{k_2}{L_{s_2}} \cos(\alpha_2 + \theta_1) V_{dc} - \frac{1}{L_{s_2}} (V_2 \cos\theta_2 - V_1 \cos\theta_1) \tag{22}$$
$$0 = -\frac{R_{s_2}}{L_{s_2}} i_{q_2} - \frac{\omega}{\omega_s} i_{d_2} + \frac{k_2}{L_{s_2}} \sin(\alpha_2 + \theta_1) V_{dc} - \frac{1}{L_{s_2}} (V_2 \sin\theta_2 - V_1 \sin\theta_2) \tag{23}$$

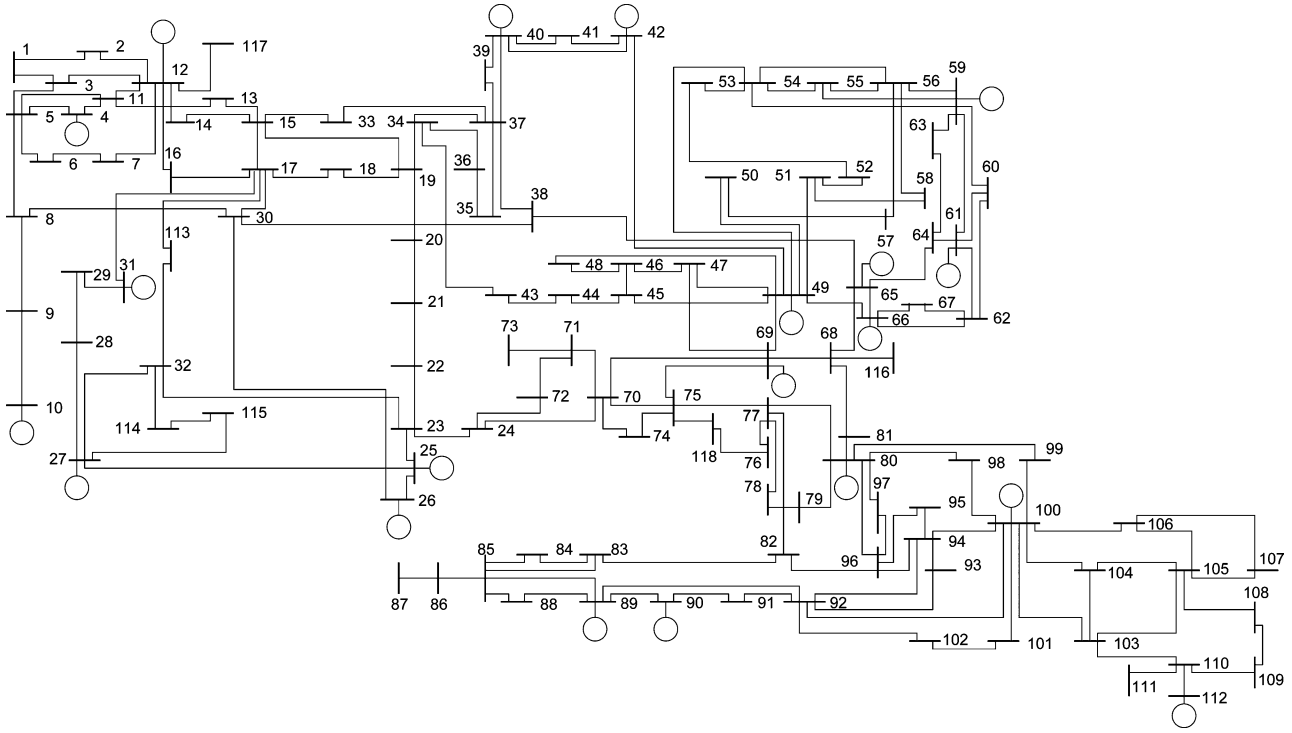

Fig. 4. IEEE 118-bus test system.

The dc-link capacitor voltage is coupled to the EC through a bidirectional dc-dc converter. Since switch level dynamics are not appropriate for a system level study, the dc-dc converter behavior is captured through the effect of a single control where the duty cycle ratio is controlled via a proportional-integral (PI) control as

$$D = \frac{1}{2} - \left(K_p \left(V_{\rm dc} - V_{\rm dc}^{\star} \right) + K_i \int \left(V_{\rm dc} - V_{\rm dc}^{\star} \right) \right) + \left(K_{p2} \left(V_{\rm dcEC} - V_{\rm dc}^{\star} \right) + K_{i2} \int \left(V_{\rm dcEC} - V_{\rm dc}^{\star} \right) \right) \quad (24)$$

where $K_p \gg K_{p2}$ and $K_i \gg K_{i2}$ are the PI control gains. Note that both $V_{\rm dc}$ and $V_{\rm dcEC}$ return to the same reference voltage $V_{\rm dc}^{\star}$, since at steady-state, there is no energy exchange with the EC, and the EC current is zero.

IV. Test System

The IEEE 118-bus test system has been used to compare the two different controllers. The diagram of the network is shown in Fig. 4. This system has 20 generators, each modeled with the set of equations given in the Appendix. This system exhibits two dominant low-frequency modes; therefore, two UPFCs are deployed in the system. Preliminary studies showed that one UPFC was not sufficient to damp the interarea oscillations. The two UPFCs were installed in the system in lines 30–38 and 65–68 with the shunt (sending) parts on buses 38 and 68, respectively. The placements of the UPFCs were chosen according to the approach outlined in [15]. Several researchers have addressed the optimal placement of FACTS controllers. Larsen *et al.* [16] used modal sensitivity to determine placement of TCSCs. Eigenvalue shift is used as a placement strategy for SVCs in [17]. Martins and Lima [18] focused on the determination of the best bus placement for SVCs to damp interarea oscillations. Another recent work addresses the use of modal controllability indexes, specifically for FACTS placement for oscillation damping [19].

TABLE I
UPFC Parameters (in pu)

	R_1	L_1	R_2	L_2	R_{dc}	C_{dc}	R_{ESR}	C_{EC}
1	0.01	0.15	0.001	0.015	50.0	1.0	0.1	20
2	0.01	0.10	0.001	0.010	50.0	1.0	0.1	20

The parameters of the UPFCs are given in Table I. The per unit approach is the same as in [20] on a 100-MW, 100-kV system.

V. Controller Results and Comparisons

In the highlighted example, a solid symmetrical fault has been applied on bus 20 at 0.01 s and has been cleared in 0.11 s. The location and duration of the fault were chosen to provide a significant disturbance to the interior of the power system. The initial conditions of the system are such that the UPFCs are initially quiescent.

A. With DC-DC Converter and EC

The frequencies of a selected set of generators is shown in Fig. 5. Not all of the frequencies are shown due to space constraints, but the results are similar. The generator frequencies with the proposed control (thick line) show significant damping of both the low- and high-frequency content over the uncontrolled case (thin line). This figure shows a qualitative improvement of the proposed control over the noncontrolled case. Since

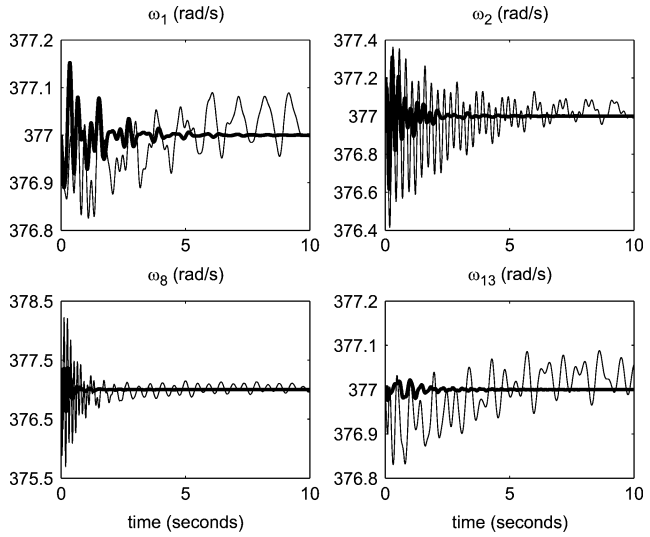

Fig. 5. Generator frequency (no control—thin line, proposed control—thick line).

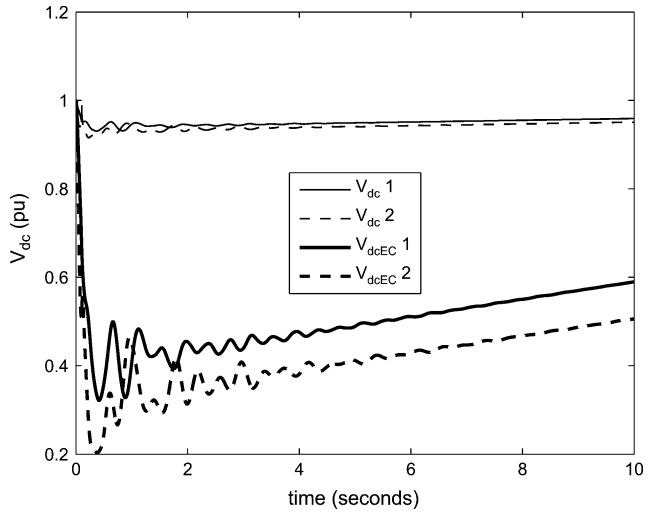

Fig. 6. UPFC dc voltages (in per unit)—thin lines, EC voltages (in per unit)—thick lines.

the dynamic waveforms are highly nonlinear, the damping factors cannot be easily extracted, and a quantitative metric is not readily available.

The dc-link voltages and the voltage of the ECs are shown in Fig. 6. The proposed control is designed to hold the voltage magnitudes at both UPFC terminals nearly constant. This requires significant active power to be drawn from the EC while maintaining a constant voltage across the dc-link capacitor to preserve controllability. The active power is alternately injected and absorbed by the UPFC in antipathy with the active power oscillations in the system. The ECs are able to discharge very quickly due to their high power density. They are then recharged at a much slower rate so that the dc-link voltages can be maintained. The ECs are fully recharged within a minute after the fault. Because the dc-link voltages maintain near-constant voltage throughout the fault and afterward, the UPFC retains its full range of operation and controllability.

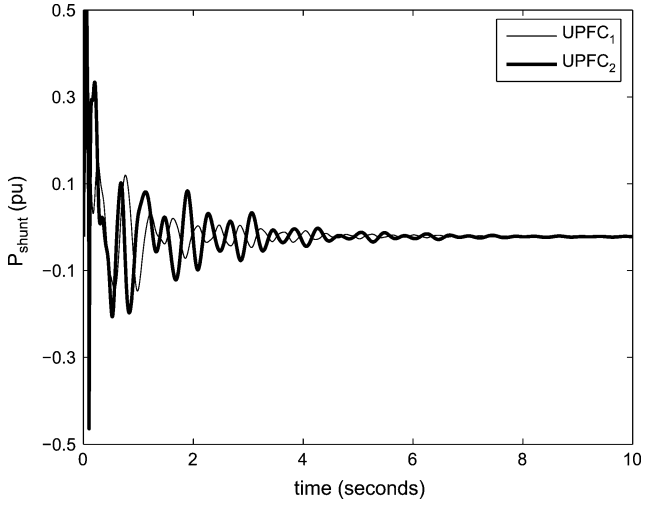

Fig. 7. UPFC injected shunt power (in per unit); UPFC 1—thin line, UPFC 2—thick line.

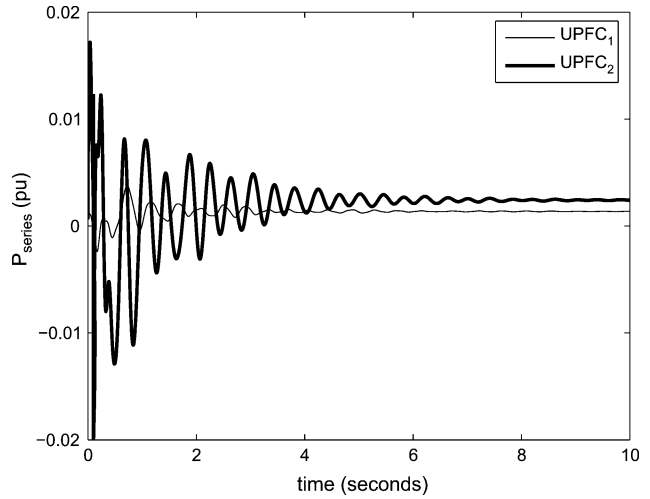

Fig. 8. UPFC injected series power (in per unit); UPFC 1—thin line, UPFC 2—thick line.

The active power injected by the shunt converter of each UPFC is shown in Fig. 7. Note that the proposed control is designed such that this active power is discharged from the EC to stabilize the system. The active power injected by the series converter of each UPFC is shown in Fig. 8. As expected, the amount of active power is quite small, since the majority of the EC active power is discharged through the shunt bus.

B. With EC, No DC-DC Converter

To better understand the full effectiveness of the proposed control with the EC, the same fault is applied to the system without the dc-dc converter linking the EC. The EC is attached directly across the dc-link (electrolytic) capacitor. The system is unable to regain stability after the fault is removed. A selection of voltages for the case with no dc-dc converter is shown in Fig. 9. Several of the bus numbers are identified on the figure. Note that the voltages on bus 65 and 68 are obviously diverging. These are on opposite ends of UPFC 2. Without sufficient additional active power injection, the UPFC itself constrains the power flow through the system causing a surplus of active power

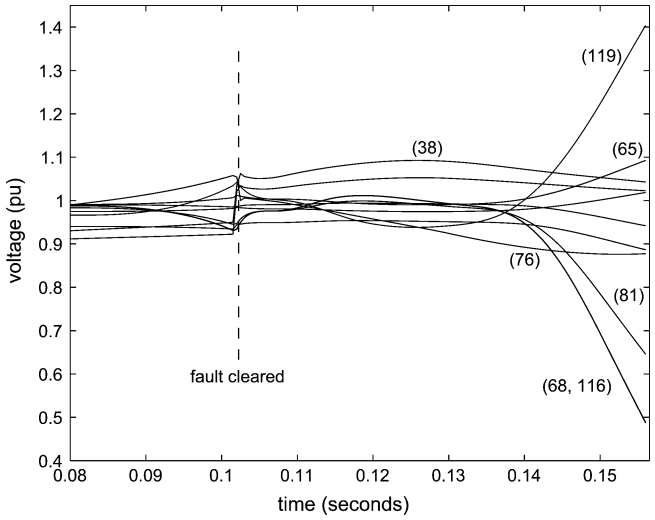

Fig. 9. System voltages after fault without EC.

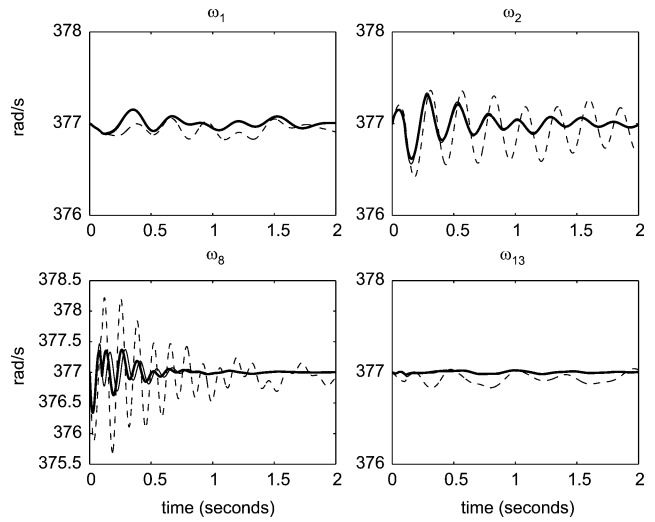

Fig. 10. Generator frequencies: no control—dotted line, proposed control with 20 pu EC and dc-dc converter—thick line, large 225 pu capacitor—thin line.

in one area and a dearth in the other, causing loss of synchronism. The power flow is constrained through current limiters to protect the hardware of the series portion of the UPFC. This portion could potentially be bypassed, but then all corrective control would be lost.

C. With Large Capacitance

The last comparison is a study to determine how large the dc-link capacitance must be to be used without a dc-dc converter. This is the same topology as reported previously, but the capacitance is increased to a size that gives comparable results to the EC with dc-dc converter. To achieve the same results, the EC must be increased to 225 pu. This increase in size is necessary to provide the required active power discharge while maintaining the dc-link voltage. For comparison purposes, the generator frequencies with and without the dc-dc converter are shown in Fig. 10. Note that the control results are nearly indistinguishable between the large capacitance and the EC with dc-dc converter.

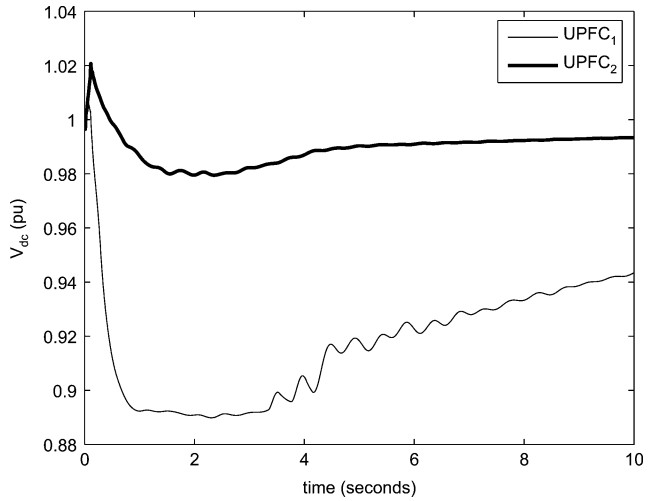

Fig. 11. Dc-link voltage for the large EC/no dc-dc converter topology; UPFC 1—thin line, UPFC 2—thick line.

The dc-link voltage for the large capacitance topology is shown in Fig. 11. Note that the dc-link voltages do not drop significantly below 90%. This is the lowest allowable voltage that can still produce a controllable output.

VI. Conclusion

This paper introduced a novel approach for damping interarea oscillations in a bulk power network using UPFCs with ECs. In this paper, a new multistage control had been proposed that specifies the bus voltages (phase and magnitude) at the sending and receiving ends of the UPFCs to damp the oscillations. These desired voltages are then converted into the required switching commands that directly control the UPFCs. Furthermore, the proposed control is shown to be especially effective for UPFCs that are interfaced with ECs through a dc-dc converter.

The results of this controller are compared with and without ECs. The proposed control provides better interarea oscillation mitigation when applied to multiple UPFCs in the 118-bus IEEE test system.

Appendix

Two-Axis Generator Model

$$\begin{aligned}
\dot{\delta}_i &= \omega_i - \omega_s \\
M_i\dot{\omega}_i &= T_{M_i} + \frac{V_i}{x'_{d_i}} \\
&\quad \times \left(E'_{d_i}\cos(\theta_i - \delta_i) + E'_{q_i}\sin(\theta_i - \delta_i)\right) \\
T'_{d0_i}\dot{E}'_{q_i} &= -\frac{x_{d_i}}{x'_{d_i}}E'_{q_i} + \frac{\left(x_{d_i} - x'_{d_i}\right)}{x'_{d_i}}V_i\cos(\theta_i - \delta_i) \\
&\quad + E_{fd_i} \\
T'_{q0_i}\dot{E}'_{d_i} &= -\frac{x_{q_i}}{x'_{d_i}}E'_{d_i} - \frac{\left(x_{q_i} - x'_{d_i}\right)}{x'_{d_i}}V_i\sin(\theta_i - \delta_i).
\end{aligned}$$

Assumption: $x'_{q_i} = x'_{d_i}$ and $R_s = 0$.

$$
\begin{aligned}
T_{E_i}\dot{E}_{fd_i} &= -K_{E_i}E_{fd_i} - S_{E_i}\left(E_{fd_i}\right)E_{fd_i} + V_{R_i} \\
T_{A_i}\dot{V}_{R_i} &= -V_{R_i} + K_{A_i}R_{F_i} - \frac{K_{A_i}K_{F_i}}{T_{F_i}}E_{fd_i} + K_{A_i}\left(V_{\mathrm{ref}_i} - V_i\right), \qquad V_{R_i}^{\min} \le V_{R_i} \le V_{R_i}^{\max} \\
T_{F_i}\dot{R}_{F_i} &= -R_{F_i} + \frac{K_{F_i}}{T_{F_i}}E_{fd_i}
\end{aligned}
$$

IEEE Type I Exciter/AVR Model. See equation at the top of the page.

Turbine Model

$$
\begin{aligned}
T_{\mathrm{RH}_i}\dot{T}_{M_i} &= -T_{M_i} + \left(1 - \frac{K_{\mathrm{HP}_i}T_{\mathrm{RH}_i}}{T_{\mathrm{CH}_i}}\right)P_{\mathrm{CH}_i} \\
&\quad + \frac{K_{\mathrm{HP}_i}T_{\mathrm{RH}_i}}{T_{\mathrm{CH}_i}}P_{\mathrm{SV}_i} \\
T_{\mathrm{CH}_i}\dot{P}_{\mathrm{CH}_i} &= -P_{\mathrm{CH}_i} + P_{\mathrm{SV}_i}.
\end{aligned}
$$

Speed Governor Model

$$
\begin{aligned}
T_{\mathrm{SV}_i}\dot{P}_{\mathrm{SV}_i} &= -P_{\mathrm{SV}_i} + P_{C_i} - \frac{1}{R_i}\frac{\omega_i}{\omega_s} \\
0 \le P_{\mathrm{SV}_i} &\le P_{\mathrm{SV}_i}^{\max}.
\end{aligned}
$$

Power Balance Equations

Generator Buses

$$
\begin{aligned}
0 &= \frac{V_i}{x'_{d_i}}\left(E'_{q_i}\sin\left(\delta_i - \theta_i\right) - E'_{d_i}\cos\left(\delta_i - \theta_i\right)\right) \\
&\quad - V_i\sum_{j=1}^{n} V_j Y_{ij}\cos(\theta_i - \theta_j - \phi_{ij}) \\
0 &= \frac{V_i}{x'_{d_i}}\left(E'_{q_i}\cos\left(\delta_i - \theta_i\right) + E'_{d_i}\sin\left(\delta_i - \theta_i\right) - V_i\right) \\
&\quad - V_i\sum_{j=1}^{n} V_j Y_{ij}\sin(\theta_i - \theta_j - \phi_{ij}).
\end{aligned}
$$

Load Buses

$$
\begin{aligned}
0 &= P_{L_i} - V_i\sum_{j=1}^{n} V_j Y_{ij}\cos(\theta_i - \theta_j - \phi_{ij}) \\
0 &= Q_{L_i} - V_i\sum_{j=1}^{n} V_j Y_{ij}\sin(\theta_i - \theta_j - \phi_{ij}).
\end{aligned}
$$

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Mahyar Zarghami (S'05–M'09) received the B.Sc. degree in electrical engineering from K. N. Toosi University of Technology, Tehran, Iran, in 1993, the M.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2001, and the Ph.D. degree in electrical engineering from Missouri University of Science and Technology, Rolla.

He is currently with ABB, Inc., Raleigh, NC. His research interests include power system dynamics and FACTS devices.

Mariesa L. Crow (S'83–M'90–SM'94–F'10) received the B.S.E. degree from the University of Michigan, Ann Arbor, and the Ph.D. degree from the University of Illinois, Urbana-Champaign.

She is currently the Director of the Energy Research and Development Center and the F. Finley Distinguished Professor of Electrical Engineering, Missouri University of Science and Technology (formerly University of Missouri-Rolla), Rolla. Her research interests include developing computational methods for dynamic security assessment and the application of power electronics in bulk power systems.

Jagannathan Sarangapani (SM'99) received the Ph.D. degree from the University of Texas, Austin, in 1994.

He is currently a Site Director of the NSF I/UCRC on Intelligent Maintenance Systems with the Missouri University of Science and Technology, Rolla, where he is also the Rutledge-Emerson Distinguished Professor of Electrical Engineering. His research interests include developing nonlinear and adaptive controllers for complex dynamic systems, diagnostics and prognostics, and their applications to complex networks such as power systems.

Yilu Liu (F'04) received the B.S. degree from Xian Jiaotong University, Xian, China, and the M.S. and Ph.D. degrees from The Ohio State University, Columbus.

She is currently a Governor's Chair Professor of Electrical Engineering and Computer Science in the University of Tennessee and Oak Ridge National Laboratory, Knoxville. She has been with the Bradley Department of Electrical Engineering, Virginia Tech, Blacksburg. Her current research interests include wide-area monitoring and measurements, power system analysis, power quality, and transient analysis, power system equipment modeling and diagnoses. She is engaged in the development of a North America Power System Frequency Disturbance Monitoring Network.

Stan Atcitty received the B.S. and M.S. degrees in electrical engineering from New Mexico State University, Las Cruces, and the Ph.D. degree from Virginia Tech University, Blacksburg.

He is currently a Power Electronics Consultant with the Energy Storage System Program, Sandia National Laboratories, Albuquerque, NM. His research interests include high-power electronics and applications to power systems.