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Series-Parallel Approaches and Clamp Methods for Extreme Dynamic Response with Advanced Digital Loads

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Abstract **– The series-input parallel-output dc-dc converter combination provides inherent sharing among the converters. With conventional controls, however, this sharing is unstable. Recent literature work proposes complicated feedback loops to correct the problem, at the cost of dynamic performance. This paper shows that a simple sensorless current mode control stabilizes sharing with fast dynamics suitable for advanced digital loads. With this control in place, a "super-matched" current sharing control emerges. Sharing occurs through transients, limited only by the energy limits of the converters. The control approach has considerable promise for high-performance voltage regulator modules. For even faster response, clamping techniques are proposed.**

I. INTRODUCTION

The series-input parallel-output (SIPO) configuration [1,2] was proposed for high-voltage input applications. In this paper, it is shown to offers advantages over conventional parallel switching voltage regulator modules (VRMs) for current sharing. It also provides single-stage 48 V dc bus conversion. However, control must be performed properly to ensure dc stability and current sharing during transients. Sensorless current-mode (SCM) control [3,4] provides a suitable approach. When SCM is applied to the SIPO topology, current matching becomes nearly ideal – high matching gain produces a "super-match" characteristic that holds even during transient conditions, limited only by the physical energy exchange limits inherent to any switching converter. For even faster response requirements, high-speed clamp circuits can be applied.

A typical power circuit for the SIPO method is given in Fig. 1. The figure shows four flyback converters, but in fact can be implemented with a range of possible converters. In general, any number of converters $n > 1$ can be used. Push-pull, half-bridge, or full-bridge forward converters, for instance, can be used in place of the flyback circuits. There are also diode-connected non-isolated converters similar to high-side gate-drive level shifters that support the arrangement. The flyback provides a basis for discussion here.

On the input side, the series connection means that the average currents in each of the four converters must be identical. Since the switches must be able to function independently, four input capacitors decouple the inputs. (It is advantageous to interleave the converter switching, for the same reasons as in conventional VRMs.) Since the input currents match, the output currents also match if the coupled inductor turns ratios are the same.

The currents match, but is this arrangement stable? With conventional controls, the answer is "no" [1,2]. Indeed, the emphasis of the previous work is to add control complexity in an attempt to establish stable operation. Under any conventional method, if one converter is perturbed to see a slightly lower input voltage, its input current will increase as it attempts to keep supplying the load. This will remove energy from its input capacitance and further reduce the input voltage. The end result is that the converters will not share the load.

The stability problem can be avoided by applying sensorless current mode (SCM) control to each converter. As detailed in [3], SCM is an observer-based method that reconstructs an inductor current by integrating the input voltage, except the converter output voltage is replaced by a desired reference value V_{ref} when it appears in the inductor voltage expression. The method then controls the converter by comparing this integrated signal to a carrier ramp waveform. In the nth flyback converter, SCM uses the integral law $\int\left(q_n V_{in}' - \bar{q}_n V_{ref}\right)dt$, where V_{in}' is the individual converter's input voltage and V_{ref} is the desired output reflected to the primary side of the coupled inductor. The signals q_n and $\bar{q}_n$ represent the transistor and synchronous

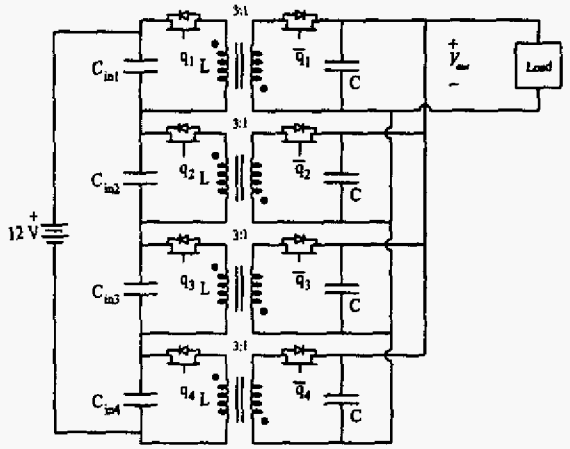

Fig. 1. Flyback series-input parallel-output converter: typical example for 12 V to 1 V VRM.

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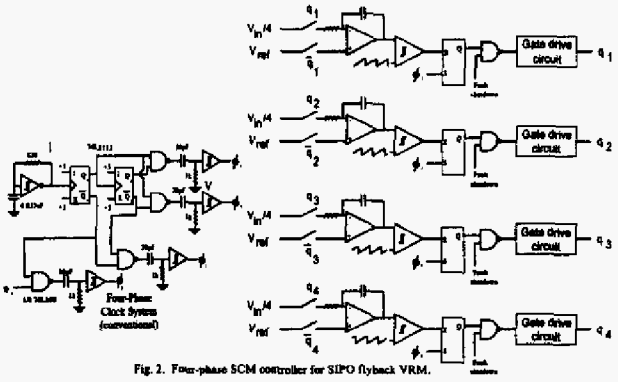

Fig. 2. Four-phase SCM controller for SIPO flyback VRM.

rectifier switching functions.

In SCM, it is recognized that the output voltage V_{out} is not intended to be a dynamic state, and instead is to be driven to an external reference signal. In the VRM application of a SIPO topology, we consider the additional point that the individual converter voltage V_{in}' is intended to be V_{in}/n, where n is the number of converters, then use this in place of the actual input. With these substitutions, the control law becomes $\int\left(q_n V_{in}/n - \bar{q}_n V_{ref}\right)dt$. Typically, V_{ref} is modified to include a voltage output feedback term to correct for errors, as in [4].

II. Implementation

A control circuit that implements the proposed method is shown in Fig. 2. There are four operational amplifiers that perform the SCM integration for the respective converters. A separate n-phase clock sets latches, and a comparator resets them based on the integrator output compared to a stabilizing ramp.

The SCM structure in Fig. 2 enforces input voltage matching while the SIPO topology enforces current matching. In this case, if one converter has its voltage perturbed low, the control signals are unaffected. This means the converter's output voltage will drop, reverse biasing its output diode and shutting off current. With reduced or zero load current, the input capacitor recovers and matching is restored. The "matching gain" is extremely high: just a few millivolts of voltage disturbance can swing the output current by a large amount, since SCM inherently generates low output impedance. This means there is a built-in high-gain process to restore current matching – hence the term "super matched" current in this arrangement. The gain from input voltage mismatch to output current mismatch in effect is the output admittance.

The unique aspects of the combination of Figs. 1 and 2 are as follows:

- Fig. 2 provides a direct and simple way to keep operation of the SIPO connection stable.
- The SIPO circuit in Fig. 1 inherently shares current, while the SCM control makes it share voltage as well.
- The turns ratio in the coupled inductor can be used to support extreme voltage ratios. A 48 V input to 1 V output conversion, for example, is readily supported by Fig. 1.

A particularly compelling aspect of the SIPO connection operated under SCM is that current sharing is enforced by energy storage properties of the input-side capacitors. This means there is no particular limit to current sharing bandwidth at least up to the dynamic limits of the converter controls. A simulation test, as in Fig. 3, shows that dynamic sharing is actually limited only by the switch action itself. The figure demonstrates dynamic current sharing with a SPICE simulation of the circuits of Figs. 1 and 2. The figure overlays all four converter output currents. Here the VRM is serving a 1 V load at approximately 12 A. At time t ≈ 300μs, a step change is made to the input voltage. SCM is robust to input voltage changes. Only a tiny perturbation appears in the output currents. At time t = 400 μs, the load resistance drops in half. The currents rise rapidly to accommodate the new load. Notice how the current peaks rise consistently with the overall trend – limited only by the open-loop energy dynamics of the converters. In practice, closed-loop SCM design would be used. It inherently provides much faster dynamics, and greatly decreases the response time of the converter set.

The SIPO connection offers advantages in terms of robustness. Small differences in internal resistances or differences in inductor values do not alter the current sharing. More extreme errors, such as a turns-ratio mismatch, will result in current differences only as big as the mismatch. Experimental sharing is discussed in the following section. The isolated converter requirement might appear as a limitation. After all, a flyback converter exhibits a right-half-plane zero that limits its dynamic performance. Notice that in

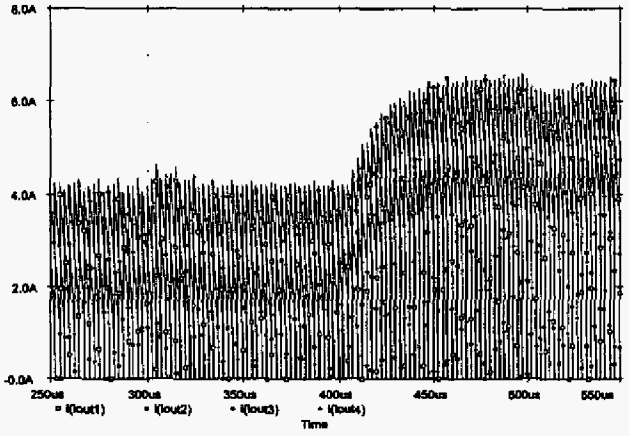

Figure 3: Output Currents, Four Stages of Fig. 1

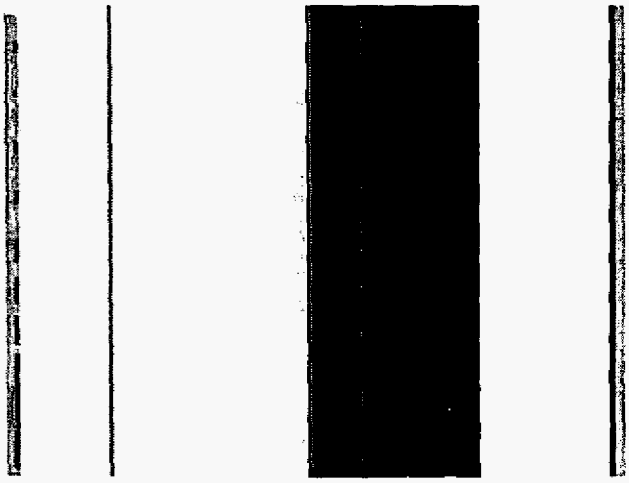

Figure 4: Two Push-Pull SIPO Converter, 12 V to 1 V

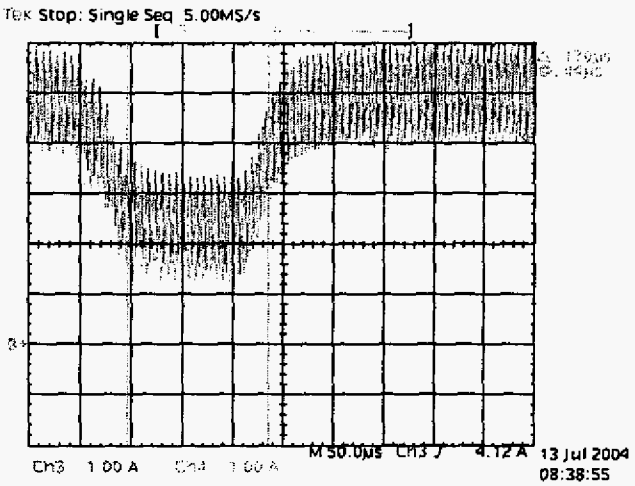

Figure 5: Inductor Current Waveforms Through Load Transient

Fig. 3 this delay behavior does not seem to appear. Initial analysis suggests that the right-half-plane zero is raised in frequency by a factor of *n* for *n* multi-phase converters.

III. Experimental Results

The SIPO topology will work effectively with many underlying converter types. A 12 V input, 1 V output at 20 A converter was built with two push-pull converters in series/parallel. Synchronous rectification was used on the output to increase efficiency, as is typical for such a low output voltage. Control was implemented with SG3526 PWM ICs, a DG211 analog switch IC, and some operational amplifiers (op amps) and logic. A photograph is shown in Fig. 4.

The resulting inductor current waveforms are shown in Fig. 5. Through a load drop, the two converters share current nearly exactly. Voltage sharing is shown in Table 1. Across the load range, the two converters split the input voltage nearly equally, always within 5%, usually within 2%.

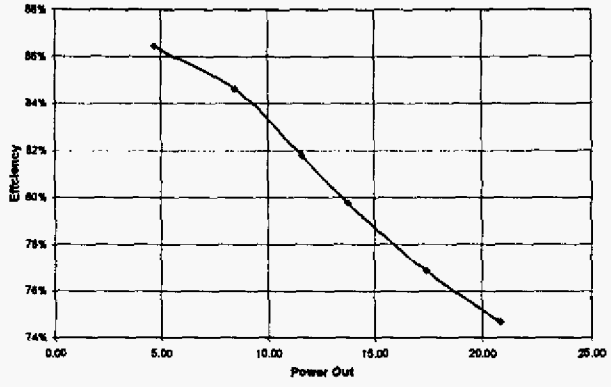

Figure 6: SIPO Efficiency

High efficiency is possible with this architecture, with appropriate attention to magnetic design and parasitic losses. The transformers of the converter shown in Fig. 4 are wound on P36/22 cores with a 4:1 ratio, with special attention to minimizing leakage inductance. The efficiency achieved is shown in Fig. 6.

IV. Active Clamp

When load changes outpace the physical capability of a converter, the ESR of the load interface capacitance determines the short-term dynamic response. This is often considered a fundamental limit. But consider that a typical digital load presents extreme transients relatively infrequently. In this case, a clamp circuit can be used to limit transient overshoots and undershoots with minimal power loss.

An active clamp circuit is shown in Fig. 7. Output voltage is sensed and compared to two references, allowing for ripple and small transients. When the output voltage exceeds the limits, a fast, high-gain amplifier drives a MOSFET to source current into or out of the output. The

Table 1: Voltage Sharing

Input Voltage	Output Power	Upper Half Voltage	Lower Half Voltage	Mismatch
12.956	4.70	6.522	6.434	1.36%
12.912	8.50	6.513	6.399	1.77%
12.873	11.60	6.485	6.388	1.51%
12.843	13.78	6.472	6.371	1.57%
12.793	17.41	6.472	6.321	2.36%
12.741	20.85	6.521	6.22	4.72%

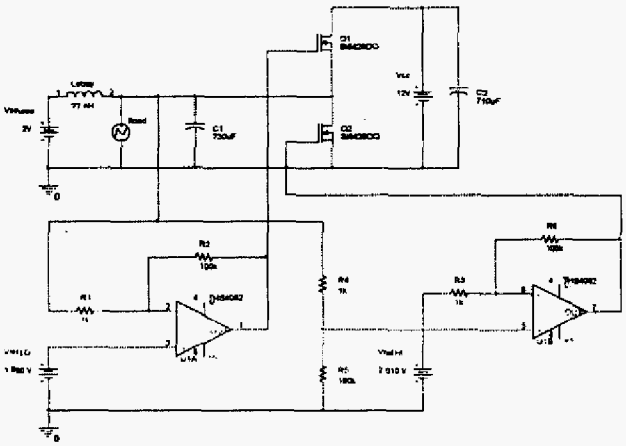

Figure 7: Simplified Active Clamp Circuit

devices chosen were THS4062 high-speed op amps and Si6426DQ MOSFETs. The THS4062 has a gain-bandwidth of 180 MHz and an output resistance of 12 Ω. The capacitor on V_{out} was composed of five 10 µF ceramic surface mount capacitors plus one 680 µF polymer electrolytic capacitor.

Waveforms are shown in Fig. 8. A load step of 25 A with a di/dt of 97 A/µs is applied to the output. In Fig. 8(a), the clamp is disabled, and the output dips substantially (90.8 mV). In Fig. 8(b), the clamp is enabled, mitigating the output droop (57.2 mV—a 37% improvement).

V. Conclusions

The series-input parallel-output topology introduced in [1,2] can be made stable and robust through the application of sensorless current mode control. A VRM based on this technique achieves super-matched current sharing with an inherent high-gain matching action. It also achieves full-rate dynamic current matching limited only by the converter physics. The approach has significant promise for VRM applications as currents and voltage ratios increase. Experimental results demonstrate dynamic current sharing, static voltage sharing, and high efficiency. An active clamp has been demonstrated that mitigates voltage droop during a load step with di/dt nearly 100 A/µs.

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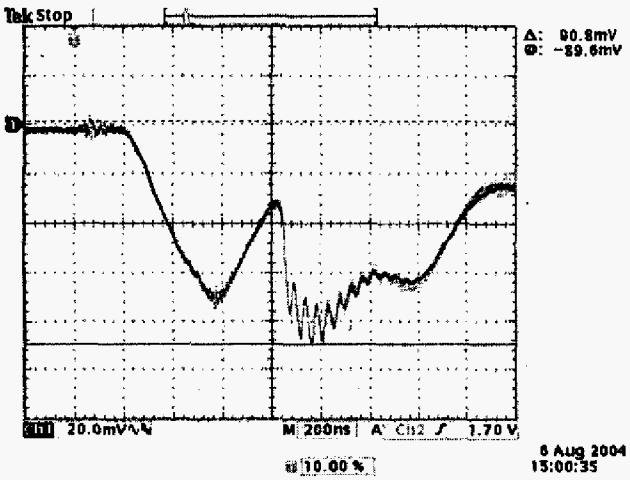

Figure 8(a): Output Voltage Transient, No Clamp

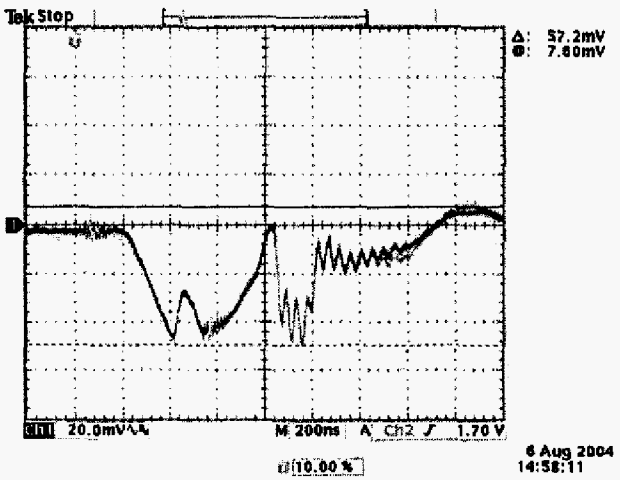

Figure 8(b): Output Voltage Transient, With Clamp