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Probabilistic Balancing of Fault Coverage and Test Cost in Combined Built-In Self-Test/Automated Test Equipment Testing Environment

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Abstract

As design and test complexities of SoCs ever intensify, the balanced utilization of combined Built-In Self-Test (BIST) and Automated Test Equipment (ATE) testing becomes desirable to meet the required minimum fault-coverage while maintaining acceptable cost overhead. The cost associated with combined BIST/ATE testing of such systems mainly consists of 1) the cost induced by the BIST area overhead and 2) the cost induced by the overall testing time. In general, BIST is significantly faster than ATE, while it can provide only limited fault-coverage and driving higher fault-coverage from BIST means additional area cost overhead. On the other hand, higher fault-coverage can be easily achieved from ATE, but excessive use of ATE results in additional test time. Combined fault-coverage from BIST and ATE plays a significant role, since it can affect the area overhead in BIST and test time in BIST/ATE. This paper is to propose a novel probabilistic method to balance the fault-coverage and the test overhead costs in combined BIST/ATE test environment. The proposed technique is then applied to two BIST/ATE test scenarios to find the optimal fault-coverage/cost combinations.

1: Introduction

In the last decade, System-on-Chip (SoC) technology has been developed rapidly which results in highly integrated and complex chips. So, the testing is becoming more and more difficult with the comparatively old test machines. Usually Automatic Test Equipment (ATE) is used to drive the test patterns to the device-under-test (DUT) and then strobe the output from it to see the test result is a pass or fail. The testers used in industry usually have up to 1024 channels [12]. Each channel can drive or strobe signal from the 1 or more DUT pins and can measure the electrical parameters of the DUT. Compared with the current GHz chips, the most testers are working at 100MHz level [12]. The full speed test machine is too expensive for production so that some other testing techniques are used to complement ATE testing [13]. BIST is widely used for this purpose nowadays [6, 11]. The main advantage of BIST is the fast testing speed which is almost at the full speed of DUT [6] regardless the speed of the test machine, its speed is kind of tester independent. So for the high speed BIST testing takes the place of ATE for speed up. The disadvantage is although there are lots of sophisticated way to generate test patterns for BIST, still many random-resilient faults can not be

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detected while those faults can be detected by deterministic fault-oriented patterns in ATE testing [6, 11]. Considering test time is one of the most contributor to test cost, it is obvious that using BIST test to achieve a relatively acceptable fault coverage which can result in a test time reduction because of the higher testing speed, then using the deterministic patterns to achieve the required final fault coverage by slower ATE testing. On the other hand, the higher BIST fault coverage will result in a larger BIST area overhead which may significantly increase the cost of designing and silicon fabricating. So these two portions of the test cost must be taken into consideration for the overall cost, and this paper will discuss this issue later.

Parallel testing is another factor which should be taken into consideration for the purpose of the overall test cost reduction. The typical tester in manufacturing industry has 256 to 512 channels so that it is possible to put multiple DUTs onto the test head to do the testing in parallel, meaning that a set of DUTs tested at the same time. This kind of method is widely used for memory chips like SDRAM, Flash because those kind of chips usually have less pins so that testers have enough channels to support like 32 or 64 DUTs parallel testing [12]. For some very complex devices like CPUs or chipsets, which have hundreds of signal pins, a single test head can not support parallel testing due to the limitation of channels. Some advanced testers can support more than one test head so that parallel testing can be applied as well. So the parallel testing can be used in more complex chip testing as a way to increase the test yield and efficiency.

As discussed in [1], during parallel test, most of the resources of the ATE such as memory, test channels, power supply, are shared among DUTs. Therefore, when determined as faulty, a DUT can not be replaced until the test process for all the DUTs completed [12]. So in this process, the channels assigned to those DUTs, which have already been diagnosed as faulty, are idling until the test finish. The idle time is a function of the yield and faulty coverage [1] and contributes to the total cost of the overall test process which will be analyzed in this paper.

2: Preliminaries

This paper deals with the cost-driven optimization of combined BIST/ATE testing. The total test cost is comprised of several factors, such as yield, fault coverage for different test stage, test sequence, test process modeling and so on. A novel method to optimize the factors in order to minimize the total cost is to be proposed in this paper. As a few works have been done to analyze the parallel testing in [1], similar approaches are used throughout the paper, yet more practical factors are considered to model the test process with respect to the overall test cost.

1. *BIST/ATE in separate stages:* the DUTs go through the BIST test first. DUTs which have been found faulty by BIST are screened out (i.e., will not go to the next ATE test stage) by delayed replacement. The DUTs which can pass BIST test go to ATE test in another stage.
2. *BIST/ATE in same stage:* the DUTs go through the BIST test first, too. No matter what is the test result of BIST, all the DUTs will go to ATE test without being purged off from test head.

Compared with ATE stage, the tester used in BIST stage is not required to be so advanced, and usually has slower working frequency, small memory, etc. So the price of the tester is cheaper as well as the test time cost. In this case, we can combine the BIST with some comparatively simple DC testing such as open/short test, IDDQ/leakage test in the low end tester and in the later discussion in this paper, a cost saving can be reached by using this scheme in some situation. After this test stage, pass those good DUTs to the following ATE stage. In this stage, usually a high-end tester with higher speed and memory is needed to drive test patterns to DUTs and observe the

results. So, the cost per unit-time is different in these two stages from the machine utilization point of view. An additional touchdown between these two stages should be taken into consideration as well.

For the second approach, BIST and ATE are utilized in the same test stage. So the tester used for this approach is usually a high-end tester, which is more costly than the tester for the first approach. The advantage of this scheme is, because the DUTs which failed in BIST test do not need be removed from the test head, no additional touchdown is required so that it can help saving test time cost. Also please remember that, because the BIST and ATE test are combined in the same test round, no matter the DUTs pass or fail the first BIST test, they will be automatically tested by the second ATE test. In this case, the failed DUTs will still stay on the test board which is a resource waste which can induce additional cost.

As already shown in [1], the test time is a function of fault coverage. For BIST testing, additional circuitry should be added to the chip to get a certain desired level of fault coverage. Compared with ATE, which uses Automatic Test Pattern Generation (ATPG) tools to generate patterns to achieve a desired level of fault coverage, the fault coverage achieved by BIST is much more expensive. Because of the very fast application time in BIST test, the test time in BIST stage is much lower than in ATE which can contribute to the cost reduction. In order to address the BIST/ATE balancing issue, a novel cost-driven optimization technique for combined BIST/ATE testing is proposed, and then validated through parametric simulations in this paper.

A few numerical models for test time of parallel testing has been reported in [1] and the proposed cost-driven optimization technique is based on the models. The following notation will be used throughout this paper.

1. t_p: expected time required for a DUT to pass the entire test process
2. t_f: expected time required to diagnose a faulty DUT
3. y: yield
4. V: number of total test vectors
5. n_0: expected number of faults per faulty chip
6. f_M: required fault coverage for the whole testing process
7. f_E: fault coverage achieved by ATE testing
8. N_s: number of patterns in the minimal test set applied by ATE
9. T_{avg}: average test time for parallel testing

In order to characterize the test time in parallel testing, several terms have been defined in the paper. y is the yield (i.e. the number of good DUTs at the end of test divided by the total input DUTs in percentage), t_p is the test-time-good which is the expected time required for a good DUT passing the whole test process, and t_f is test-time-bad which is the expected time required to diagnose a faulty device. So the expected test time of a DUT, which is designated by t, can be calculated by $t = t_p \times y + t_f \times (1 - y)$.

As per the discussion in [2], n_0 is the possible average number of faults per faulty chip, so the probability of a faulty DUT to be detected by test vector v (among the total of V test vectors) can be given by

$$p_f = \frac{(V - v + 1)^{n_0}}{V^{n_0}} - \frac{(V - v)^{n_0}}{V^{n_0}} \tag{1}$$

From [1] and [2], the expression can be explained as follows; there are total of V^{n_0} combinations in which the V available vectors can detect the n_0 faults. The number of combinations in which only a vector v detects the fault and none of the previous vectors (1 to v-1) detects any of the n_0 faults is $(V-v+1)^{n_0}-(V-v)^{n_0}$. Thus the expected test-time-bad for a faulty device with n_0 faults is given by

$$t_f \propto \sum_{v=1}^{v=V} \frac{(V-v+1)^{n_0}-(V-v)^{n_0}}{V^{n_0}} \times v \approx \frac{V}{n_0+1} \tag{2}$$

Also we define C as the number of DUTs can be put onto test head simultaneously for parallel testing, D as the number of total input DUTs. As shown in [1], the average test time of a parallel testing is

$$T_{avg} = (1-y)^C \times t_f + (1-(1-y)^C) \times t_p \tag{3}$$

In [4], an almost linear relationship between test set size and fault coverage has been found in semi-logarithmic scale. In other words,

$$f_E = \frac{f_M}{\log_{10} N_s} \times \log_{10} V \tag{4}$$

where f_E is the fault coverage achieved by ATE testing, f_M is the required fault coverage for the whole testing process (combined BIST/ATE), V is the test vector size in ATE and N_s is the number of patterns in the minimal test set which are applied by the ATE [1, 4].

3: Test Time Overhead Cost Analysis

In the manufacturing factory, test time can significantly affect most of the costs such as machine utilization, direct people resource, relevant material storage (auxiliary machines), etc. Thus, if test time can be reduced, the total testing cost can be cut significantly. Considering the fast testing speed of BIST, as the BIST test coverage increases, to reduce the ATE test coverage to speed up the overall test process, the total test time can be significantly reduced. The following notation will be used throughout the paper, in addition to the notation defined in the previous section:

1. λ : a constant to model the random-resilience of faults
2. f_B: fault-coverage achieved by BIST testing
3. t_{pB}/t_{fB}: expected test time for a DUT passing/failing in BIST test
4. t_{pE}/t_{fE}: expected test time for a DUT passing/failing in ATE test
5. T_{avgE}: expected test time for ATE testing

By the Williams' model shown in [3], the BIST coverage after applying Nth vector can be expressed as $f_B = f_M \times (1-e^{-\lambda \times log_{10} N})$, where λ denotes a constant that is used to model the random-resilience of faults. The larger λ is, the easier the fault can be detected by random test patterns. Since the test time is proportional to the number of test vectors, we can solve N from the equation and then get the test time as follows

$$t_{pB} \propto N = 10^{\frac{-1}{\lambda} \times ln(1-\frac{f_B}{f_M})} \tag{5}$$

Because the passing/failing status can be known for a DUT only after all the test vectors are executed, the test-time-good and test-time-bad are the same in BIST. So we have t_{pB}=t_{fB}. From

equation (3), the average test time T_{avgB} in BIST stage for total D DUTs can be calculated as $T_{avgB} = D/C \times t_{pB}$. Using the same method, we can solve V from equation (4), and $f_E = f_M - f_B$. Also, the expected test time for a DUT passing in ATE is proportional to the test vector size, and can be expressed as follows

$$t_{pE} \propto V = 10^{\frac{f_M - f_B}{f_M} \times log_{10} N_s} \tag{6}$$

From equation (2) and (6), it can be observed that the t_{fE} proportional to the function of f_B. Now, let us scale the test time and let α denote the relative speed of BIST over ATE [4, 5], so that we have

$$t_{pB} = 10^{\frac{-1}{\lambda} \times ln(1 - \frac{f_B}{f_M})} \tag{7}$$

$$t_{pE} = \alpha \times 10^{\frac{f_M - f_B}{f_M} \times log_{10} N_s} \tag{8}$$

$$t_{fE} = \frac{\alpha}{n_0 + 1} \times 10^{\frac{f_M - f_B}{f_M} \times log_{10} N_s} \tag{9}$$

In the first approach, the detected faulty DUTs by BIST should be removed from the total D DUTs. In order to get the parallel test time in ATE stage, we need calculate the remaining T DUTs after BIST.

In [6], Williams and Brown showed that $D_L = 1 - y^{1-f}$, where y is the yield of a test stage,D_L is the defect level and f is the fault coverage of the current test stage. Because the combined BIST and ATE fault coverage is f_M, and the ATE coverage is $f_M - f_B$, we can calculate the yield of BIST y_B and yield of ATE y_E, as well as the final yield y. Here we assume the D_L of each test stage is known from the empirical data.

$$y_B = e^{\frac{log_e(1 - D_{Lb})}{1 - f_B}} \tag{10}$$

The D_{Lb} here is the tolerable defect level for BIST test station.

$$y_E = e^{\frac{log_e(1 - D_{Le})}{1 - (f_M - f_B)}} \tag{11}$$

The D_{Le} here is the tolerable defect level for ATE test station.

$$y = e^{\frac{log_e(1 - D_{Le})}{1 - f_M}} \tag{12}$$

Since BIST and ATE are two successive stages. Thus the number of good DUTs after BIST, which is designated by M, is

$$M = D \times y_B = D \times e^{\frac{log_e(1 - D_{Lb})}{1 - f_B}} \tag{13}$$

In order to calculate the test time in ATE by equation (3),we can put the y_E into the equation. Now, we can get the test time in ATE, which is T_{avgE}

$$T_{avgE} = M/C \times [(1 - y_E)^C \times t_f E + (1 - (1 - y_E)^C) \times t_p E] \tag{14}$$

Since we use different testers in these two serial test stages, and ATE cost is much higher than BIST cost because the ATE testing requires more test channels to drive and strobe signals from the DUT so that the machine is more advanced. Thus, it is assumed that the cost in ATE is β times

higher than in BIST stage. Let us further assume that cost in BIST is expected as dollar per unit test time and the touchdown time cost is ϕ which is based on the manufacturing process. We can scale ϕ as a percentage of cost in ATE. So, the cost for the test process is

$$Cost_{test} = 1 \times T_{avgB} + \beta \times (1 + \phi) \times T_{avgE} \tag{15}$$

The ϕ can reflect numerous factors of cost in the manufacturing line. It highly depends on the process, like how to get the DUTs out from the first tester and how to merge several subsets of DUTs into a new set and then go to the next stage. So once the manufacturing process of the factory is defined, the ϕ can be obtained from the empirical data. ϕ has a significant impact on the total cost in test.

The defect level D_L can also affect the cost accordingly - the defect level is lower then the cost is higher. Because when we try to minimize the D_L, which means to reduce the possibility of an indeed faulty DUT to pass the whole test and be recognized as a "good" DUT, we need put more efforts like introducing more patterns to the test stage and the total test cost will increase as a result. Now, we simulate the result from the sets of Defect Per Million (DPM) values in Table (1), keeping and all the other parameters as the same. Normalized costs for the DPM values are also shown. As expected, normalized cost increases as DPM goes down.

Table 1. DPM values and Normalized Costs

	Defect level (DPM)	*Normalized Cost*
1	$D_{Lb} = 700$ $D_{Le} = 500$	9164
2	$D_{Lb} = 500$ $D_{Le} = 300$	9174
3	$D_{Lb} = 200$ $D_{Le} = 100$	9186
4	$D_{Lb} = 100$ $D_{Le} = 50$	9191

In the second approach, BIST and ATE testing are executed in one test stage (i.e. one tester), although those two different testing phases are still in two successive steps. Since no DUT will be removed from the test head even if it fails in BIST testing, the test time for the whole testing session is t_{pBE} and is given by the sum of BIST and ATE pass times

$$t_{pBE} = t_{pB} + t_{pE} \tag{16}$$

Assuming that all faults are equally likely, f_B is the probability that a DUT fails at BIST stage and f_M-f_B is the probability that a DUT fails at ATE stage. So, the fail time is

$$t_{fBE} = t_{fB} \times f_B + t_{fE} \times (f_M - f_B) \tag{17}$$

Now, t_{pBE} and t_{fBE} can be plugged into equation (3), and the total parallel test time can be obtained from

$$\begin{aligned} T_{avgBE} &= D/C \times [(1-y)^C \times (t_{fB} \times f_B \\ &+ t_{fE} \times (f_M - f_B)) \\ &+ (1 - (1-y)^C) \times (t_{pB} + t_{pE})] \end{aligned} \tag{18}$$

It is notable that the tester for this testing scheme is an advanced tester and there is no additional touchdown time cost ϕ. Now, we can have the cost in this scheme

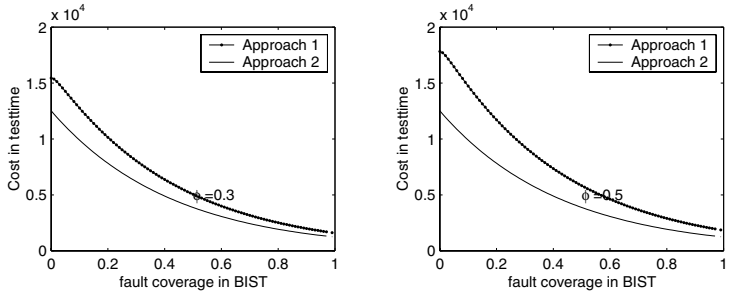

Figure 1. Costs of two approaches versus BIST coverage with different ϕ values

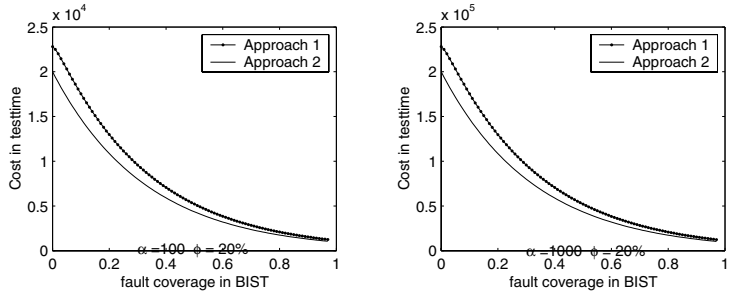

Figure 2. Cost of two approaches versus BIST coverage with different α values

$$Cost_{testBE} = \beta \times T_{avgBE} \tag{19}$$

Now, let us compare the two different test scenarios. Parametric simulation results are shown in figure (1), where α=100, β=2,ϕ has different values 0.3 and 0.5 and D_{Lb}=700 DPM(Defect per million),D_{Le}=500 DPM which are commonly used coefficients in industry. We can see the ϕ plays a significant part on the difference between these two approaches, when the ϕ increases, the first approach shows a worse performance from the cost point of view compared with the second approach. More parametric simulation results are shown in figure (2), where ϕ=20%, β=2, and α has different values 100 and 1000.

The BIST/ATE speed ratio is denoted by α. In certain manufacturing processes, the parameters such as β, $yield$, ϕ are known in priori. So, if α is small, and pretty high f_B, the first approach has some advantages over the second one. As the f_B approaches to 100%, these two approaches yield similar results. Also, there are many other factors which can affect the cost results of those two approaches. For a certain manufacturing process, those relevant parameters can be plugged into the equations (15) and (19) and then choose the less costly one of these two different schemes. Those parameters can be either obtained from factory processing or empirical data. So, we can use the same analysis method above to decide which approach is more suitable for a certain case.

4: BIST Area Overhead Cost Analysis

To implement BIST, we need to design and include additional circuitry on the chip to realize the desired testing function; meanwhile an additional cost is induced. Compared with the test time cost

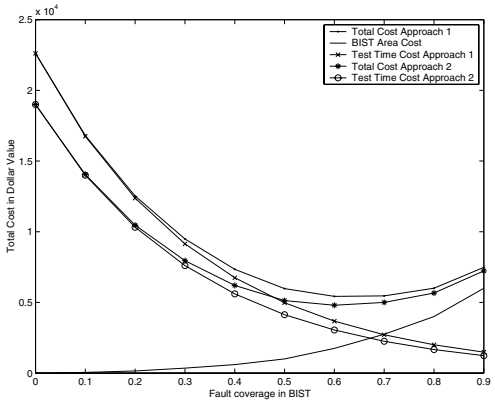

Figure 3. Total cost versus BIST coverage

in the manufacturing process, the physical chip fabrication cost is much higher. Also, the higher fault-coverage from BIST testing means even higher cost due to increased design complexity and area requirement. Although, as shown in figure (1), the cost in test time decreases when fault coverage in BIST increases, we cannot let the fault coverage to be unrealistically high because the additional cost due to BIST area overhead. So, fault-coverage and area overhead should be well-balanced.

The area overhead of BIST depends on numerous factors [7, 8, 9, 11, 10]. So, it is hard to derive a unique mathematical model to characterize the relation between the area overhead and the fault coverage. Instead, it is possible to gather empirical data to describe the relation between the fault coverage and the area overhead.

Let us scale the cost in BIST overhead by unit-test-time cost in BIST. Assuming the unit overhead cost is γ times higher than unit-test-time cost in BIST, the area overhead cost of D DUTs is

$$Cost_{area} = \gamma \times D \times Area \tag{20}$$

The $Area$ is BIST circuit in cm^2 divided by the total chip circuit in cm^2 in percentage.

5: Combining Test Time Cost and Area Overhead Cost

From the above analysis, the overall cost can be obtained by adding those two separate costs together

$$Cost_{all} = Cost_{test} + Cost_{area} \tag{21}$$

Drawing a plot of $Cost_{all}$ in normalized cost value in Y axis and versus BIST fault coverage f_b in percentage value in X axis, we can see that there is a minimum point in the curve which is the minimum cost point we need achieve.

In order to obtain figure (3), several parameters are predefined. The required fault coverage f_M is set to 98%, the overall yield is set to 95% which we can obtain from industry empirical data; α is assumed as 100 which means BIST test speed is 100 times faster than ATE; β is set to 2 which means the tester in ATE stage is 2 times more expensive than the one in BIST stage; ϕ is defined as 20%, and those three parameters α β ϕ are based on which kind of manufacturing process is employed. The defect levels of each stage are D_{Lb}=700 DPM (Defect per million),D_{Le}=500 DPM which are from industrial requirement. N_s is 10 as well as λ which are from empirical data.

There are five curves in the graph; BIST area overhead cost curve, test time cost curves for the two approaches and total cost curves for the two approaches respectively. Both of the total cost curves have the minimum point at f_B=60%, which means we can achieve minimum cost if we design the BIST circuit to get 60% fault coverage in the conditions we described in above paragraph. But, obviously, in this case, the second approach costs less than the first one. Thus, in this kind of manufacturing process, we can feedback to design engineers to develop BIST with 60% fault coverage and generate ATE test patterns to achieve the rest f_M-f_B=38% fault coverage; and use the second approach which means put BIST and ATE in one test stage (i.e. same tester) then can achieve the minimum cost. The proposed optimization model is flexible enough to accommodate different sets of parameters to find the optimal cost and BIST fault coverage combinations.

6: Conclusion

In this paper, a probabilistic optimization technique for BIST/ATE environment to achieve the balanced fault-coverage and test cost are proposed and validated. Significant testing parameters such as $yield$, touchdown time ϕ, BIST/ATE speed ratio α, Defect level D_L and the correlation table of area overhead versus BIST fault coverage f_B are also defined to determine suitable ATE/BIST test settings to use and how high BIST fault coverage f_B should be maintained in order to achieve a minimal cost. Two different BIST/ATE test scenarios are analyzed in different parameter values and the way to make better selection between those two approaches is proposed. Parametric simulation results assure that the proposed cost-driven optimization technique is simple and effective to balance BIST/ATE test environment.

References

[1] H. Hashempour,F.J. Meyer and F. Lombardi, "Using Built-In Self-Test and Automatic Test Equipment for Parallel Testing at Manufacturing," *Internal technical report, Dept of Electrical & Computer Engineering, Northeastern University, MA, USA*, 2003

[2] V.D. Agrawal, S.C. Seth, and P. Agrawal, "Fualt Coverage Requirements in Production Testing of LSI Circuits," *IEEE Journal of Solid State Circuits*, Vol. SC-17,No.1, pp. 57-61, May. 2001

[3] T.W. Williams, "Test Length in a Self-Testing Environment," *IEEE design and Test*, pp. 59-63, Apr. 1985

[4] H. Hashempour, F.J. Meyer and F. Lombardi, "Test Time Reduction in a Manufacturing Environment by Combining BIST and ATE," *Proc. IEEE Int. Symposium on DFT in VLSI Systems*, Vancouver, 2002

[5] M. Sugihara, H. Date and H. Yasuura, "Analysis and Minimization of Test Time in a Combined BIST and External Test Approach," *Proc. Intl. Test Conf.*, pp.134-140, 2000

[6] T. Williams and C. Brown, "Defect Level as a Function of Fault Coverage," *IEEE Trans. on Computers*, Vol. C-30, No.12, pp. 987-988, Dec 1981

[7] N. Nicolici and B.M. Al-Hashimi, "TAckling Test Trade-Offs for BIST RTL Data Paths: BIST Area Overhead, Test Application Time And Power Dissipation," *IEEE ITC International Test Conference*, pp. 72-81, 2001

[8] C.E. Stroud and R.F. Shaw, "An ASIC Level BIST Implementation for System Level Testing," *IEEE International ASIC Conference*, pp. p6-4/1-4, Sep 1991

[9] S.K. Chiu and C.A. Papachristou, "A Built-In Self-Testing Approach for Minimizing Hardware Overhead," *IEEE International Conference on VLSI in Computers and Processors*, pp. 282-285, Oct 1991

[10] M. Nakao, S. Kobayashi, K. Hatayam, K. Iijima, "Low Overhead Test Point Insertion For SCAN-Based BIST," *IEEE ITC International Test Conference*, pp.348-357, 1999

[11] A. Jas, C.V. Krishna and N A. Touba, "Hybrid BIST Based on Weighted Pseudo-Random Testing: A New Test Resource Partitioning Scheme," *IEEE ITC International Test Conference*, pp. 2-8, May 2001

[12] Adventest - USA, "Adventest-USA official website", http://www.advantest.com.

[13] F.C. Wang "Digital Circuit Testing" *Academic Press*, Aug 1991