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Abstract

With molecular-scale materials, devices and fabrication techniques recently begin developed, high-density computing systems in nanometer domain emerge. An array-based nanoarchitecture has been recently proposed based on nanowires such as carbon nanotubes (CNTs) and silicon nanowires (SiNWs). High-density nanoarray-based systems consisting of nanometer-scale elements are likely to have many imperfections; thus, defect-tolerance is considered as one of the most significant challenges. In this paper, we propose a probabilistic yield model for the array-based nanoarchitecture. The proposed yield model can be used 1) to accurately estimate the raw and net array densities, and 2) to design and optimize more defect and fault-tolerant systems based on the array-based nanoarchitecture. As a case study, the proposed yield model is applied to the defect-tolerant addressing scheme called h-hot addressing and simulation results are discussed.

1: Introduction

The end of photolithography as the driver for Moore's Law is predicted within seven to twelve years [1]. Although this might be seen as an ominous development, nanotechnologies are emerging that are expected to continue the technological revolution [2]. One of the most promising nanotechnologies is the crossbar-based architecture, a two-dimensional array (nanoarray) formed by the intersection of two orthogonal sets of parallel and uniformly-spaced nanometer-sized wires [3, 8], such as carbon nanotubes (CNTs) and silicon nanowires (SNWs). Experiments have shown that such wires can be aligned to construct an array with nanometer-scale spacing using a form of directed self-assembly.

Nanoarrays offer both an opportunity and a challenge. The opportunity is to achieve ultra-high density which has never been achieved by photolithography (a density of 10^{11} crosspoints per cm^2 has been achieved [6]). The challenge is to make them *defect & fault-tolerant*, since high-density systems consisting of nanometer-scale elements are likely to have many imperfections (raw fabrication defect densities over 50% are expected [2]), and a computing or storage system designed on conventional defect basis would not work [14]. Ultrahigh-density fabrication could potentially be very inexpensive if researchers can actualize a chemical self-assembly, but such a circuit would require laborious testing and repair processes, implying a significant overhead cost. Usually, defect & fault-tolerant systems have an upper limit to the number and types of defects and faults they can handle. Conventional defect & fault-tolerance techniques for photolithographic fabrication technology has been designed to handle 25% or less raw defect densities [2] and have relatively complex

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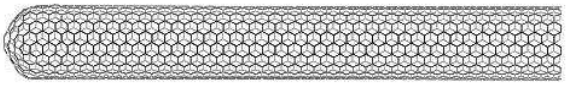

Figure 1. Carbon nano tube (CNT) molecular structure (nanometers in diameter and microns long)

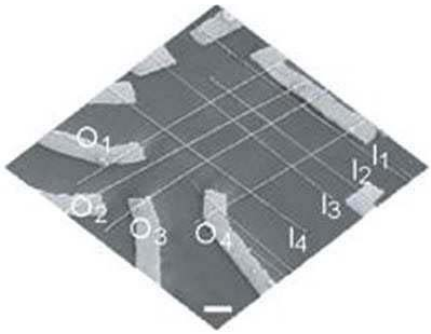

Figure 2. 2:4 binary decoder based on SiNWs (thin wires) [7]

structures in case they are integrated on chip. Also, types of defects and faults in such nanodevice-based computing systems are fully different from the conventional IC's; meaning that they cannot be directly used for nanosystems fabricated by directed self-assembly with the raw defect densities over 50% and the fully different anatomies of defects and faults.

In order to be a viable nanotechnology, nanoarrays should be 1) defect & fault-tolerant enough to overcome the extreme defect densities, 2) structurally simple enough to be fabricated by directed self-assembly technique, and 3) able to support at-speed testing, repair and reconfiguration for enhanced cost realism and computing efficiency.

The main objectives of this paper are to 1) identify possible defects and their effects on array-based nanoarchitecture and 2) establish a probabilistic yield model. The proposed yield model then will be used to accurately evaluate the performance of a defect-tolerant addressing scheme called h-hot addressing.

2 Preliminaries

One of the most promising nanotechnologies is the crossbar-based architecture, a two-dimensional array (nanoarray) formed by the intersection of two orthogonal sets of parallel and uniformly-spaced nanometer-sized wires, such as carbon nanotubes (CNTs) and silicon nanowires (SiNWs) (e.g., CNT molecular structure is shown in Figure 1 and a 2:4 binary decoder based on SiNWs is shown in Figure 2). Experiments have shown that such nanoscale wires can be aligned to construct an array with nanometer-scale spacing using a form of directed self-assembly [6, 7].

One or more crosspoints can be grouped together to form a memory or logic device. Lieber et al have shown electro-mechanical switching devices using suspended nanotubes (see Figure 3) [8]. The NT-NT junction is bistable with an energy barrier between the two states. In one state, the tubes are far apart and mechanical forces keep the top wire from descending to the lower wire. At this distance, the tunneling current between the crossed conductors is small, resulting in a very high resistance (GΩs). In the second state, the tubes come into contact and are held together via molecular forces. In this state, a little resistance (100 KΩ) exists between the wires. SiNWs can be substituted for the lower wire, and these junctions can rectifying such that the connected state exhibits p-n-diode rectification behavior.

Doped SiNWs exhibit FET (Field Effect Transistor) behavior [9]. That is, oxide can be grown over the SiNW to prevent direct electrical contact of a crossed conductor (see Figure 4). The electrical field of one wire can then be used to gate the other wire by locally evacuating a region of

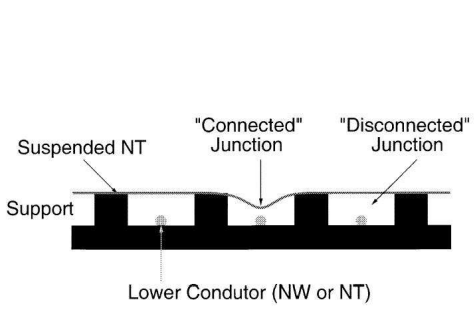

Figure 3. Suspended NT switching device

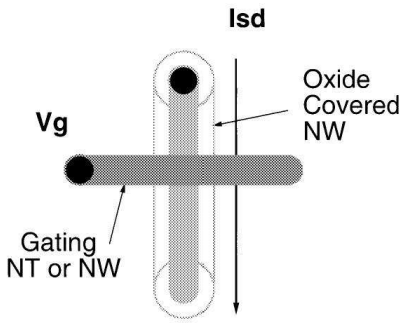

Figure 4. CNT-SiNW nanoscale FET device

the doped SiNW of carriers to prevent conduction. CNTs also demonstrate FET behavior [10, 11].

Using the suspended switching, we can assemble configurable OR planes, with connected wires acting as low-resistance p-n-junctions and distant wires isolated by high resistance (see Figure 5) [3]. In Figure 5, two logic functions are implemented by configuring nanoscale switches at crosspoints: *out1 = in1 OR in3* and *out2 = in1 OR in2*. Similarly, configurable NOR planes can be assembled. Since {OR, NOR} is a complete logic set, any digital logic circuits can be implemented if sufficiently interconnected OR and NOR planes are given.

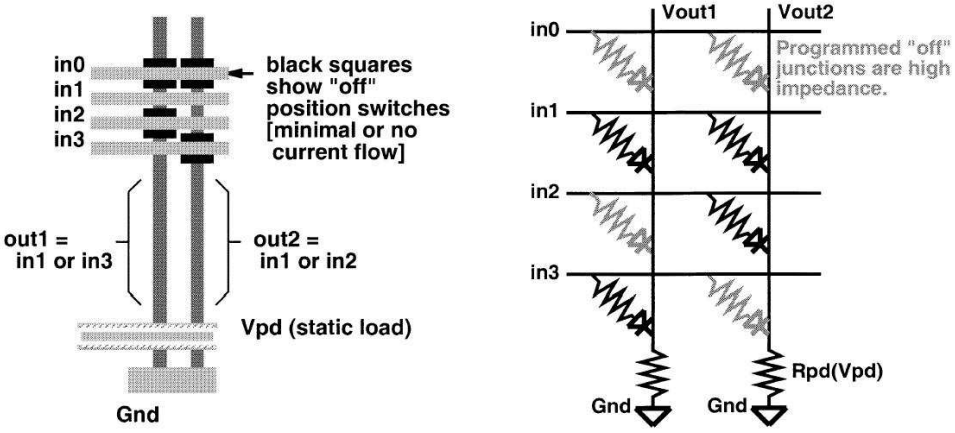

Figure 5. Programmable diode OR array [3]

DeHon has shown how to organize the CNTs, SiNWs and molecular-scale devices that now being developed into an operational computing system [3]. The molecular-scale wires can be arranged into interconnected, crossed arrays with non-volatile switching devices at their crosspoints. The crossed arrays can act as memory cores, PLA planes and crossbar - memory, compute and interconnect - all the key elements we need to implement computations. The assembled array-based nanoscale computing system has three main components: 1) nanoscale array cores, 2) address decoders, and 3) microscale global interconnects (see Figure 6).

Nanoarrays offer both an opportunity and a challenge. The opportunity is to achieve ultra-high density which has never been achieved by photolithography (a density of 10^{11} crosspoints per cm^2

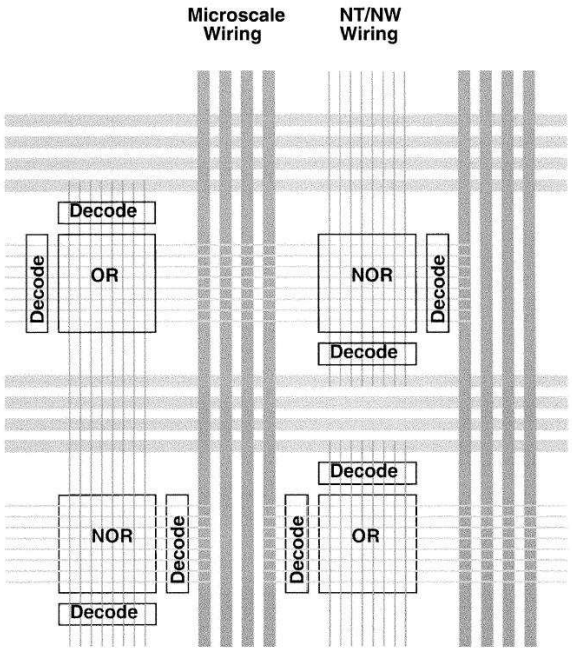

Figure 6. Assembled nanoarrays [3]

has been achieved [6]). The challenge is to make them *defect-tolerant*, since high-density systems consisting of nanometer-scale elements are likely to have many imperfections in diameter, pitch, length, etc, (raw fabrication defect densities over 50% are expected [2]), and a computing or storage system designed on conventional defect basis would not work [14]. High-density fabrication could potentially be very inexpensive if researchers can actualize a chemical self-assembly, but such a circuit would require a laborious testing and repair processes, implying a significant overhead cost. Also, defect-tolerant systems have an upper limit to the number of defects they can handle in general. Conventional defect-tolerance techniques for photolithographic fabrication technology has been designed to cope with 25% or less raw defect densities [2] and have relatively complex structures in case they are integrated on chip; meaning that they cannot be directly used for nanoarrays fabricated by directed self-assembly with raw defect densities over 50%.

Although we can directly apply a voltage to the CNTs/SiNWs in the array so that we can change the state or logic of the crosspoint, this will result in poor addressing efficiency and lower array density. On the other hand, the conventional binary address decoding scheme is not so suitable either, since it is less defect-tolerant (one defective addressing wire results in half of the address space inaccessible. So, "h-hot" address decoder with imprinted pattern during fabrication has been proposed to address these issues [3, 4]. Unlike the conventional binary address decoding scheme, in which N_a address wires address 2^{N_a} address locations, only h "hot" (i.e., activated) address wires are required to access an address location; in other words, $\binom{N_a}{2}$ address locations can be accessed by N_a address lines, if $h = 2$.

N_a could be as small as $O(logN)$ wires (N is the number of addressable nanowires), if we use the binary address decoding scheme; however, if we use such a dense encoding, a single fault in the address wires could render half of the array inaccessible. Instead, 2-hot addressing needs

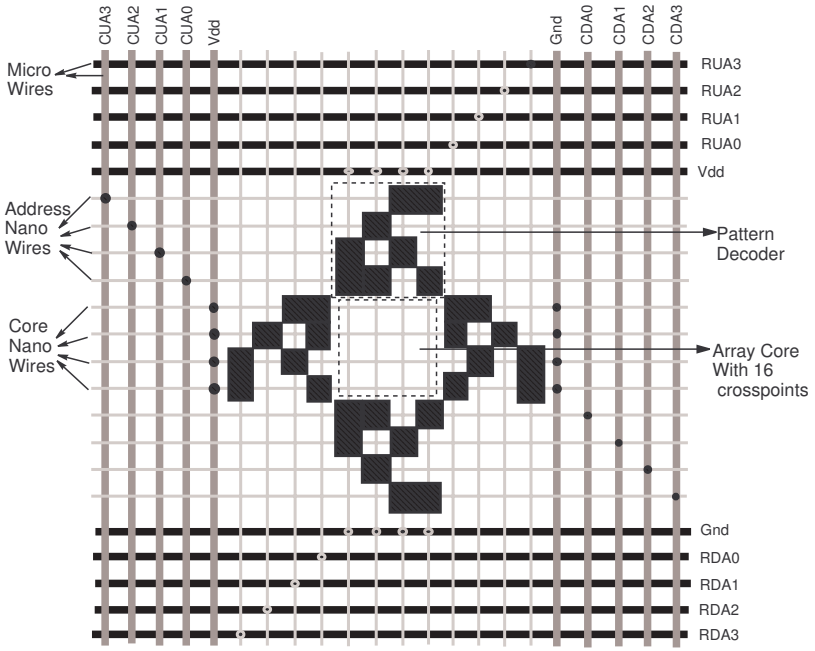

Figure 7. A 4×4 nano-array with imprinted pattern decoder

$N_a = O(\sqrt{N})$ and guarantees that we only lose $O(\sqrt{N})$ wires on any address fault.

In the decoder pattern, where the pattern leaves blank, the two orthogonal CNTs are contacted to produce a strongly coupled FET; where the pattern leaves black, the two crossed wires are kept far enough to prevent coupling each other. By using this kind of address decoder, we can access each intersection in the nanoarray.

In [3], DeHon also proposed a simple yield model for the proposed array-based nanoarchitecture. In this paper, we will further improve and extend the DeHon's basic model by: 1) introducing more defect factors to make the model more practical, 2) using a more general $h - hotaddressing$ technique to make the model more flexible, and 3) modifying the model to be more accurate so that the number of core nanowires N can be any continuous value instead of some limited discrete value.

By using the proposed extended yield model, we can accurately estimate both raw and net array densities. Also, different defect tolerance techniques for the proposed architecture can be compared so that quantitative design and optimization can be done based on that.

3: Defect Characterization and Yield Modeling

Let us consider a single array core with N nano wires and N_a micro address lines and using the *h-hot addressing scheme*. In order to get the yield for the single element array, we need to identify how many different factors many impact the yield, first. The following factors are considered in this paper:

1. *Nanowire crosspoint fails:* In the array, the crosspoint of two nanowire/nanotube can work

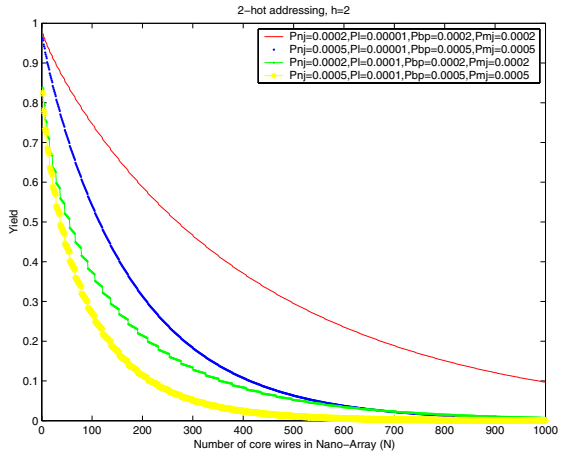

Figure 8. Yield of single nanoarray versus array size with 2-hot addressing

as a FET [3] and the connection has a probability P_{nj} that the junction is fabricated as sufficiently poor as to be defective.

2. *Contact between nanowire and microwire fails:* The microwires are used to address the crosspoint in the nanoarray and provide power supply. So, the contact also has a probability P_{mj} to be defective.
3. *Decoder pattern fails:* In the nanoarray, a decoder pattern that is customized during directed self-assembly is used to program the array (see Figure 7). The black blocks are used to keep two crossing nanowires far away enough to interfere each other. For those black blocks, P_{bp} is the probability to be defective.
4. *Length/Break fails:* With probability of P_l, there is an open or short in a nanowire.

First, we need to calculate the yield of a single addressable nanowire. In a single decoder row or column, there are total $h \cdot N$ blank blocks(FETs). So for each addressable nanowire there are $Q_1 = (h \cdot N)/N_a$ FETs in the decoder sections. As well as there are $N_a \cdot N - h \cdot N$ black blocks in the decoder and for each address wire, there are $Q_2 = (N_a \cdot N - h \cdot N)/N_a$ black blocks.

Also we need to take into account the length of each address nanowire. The width taken by each nanowire is W_{nano} and the width taken by each microwire is W_{micro}, including pitch. Considering we also have power supply provided by microwires, so the length of each nanowire/nanotube is:

$$L = 4 \cdot N_a \cdot W_{micro} + (2 \cdot N_a + N) \cdot W_{nano} \tag{1}$$

Considering the current manufacturing process, we assume that the $W_{micro} = 20 \cdot W_{nano}$. In the following discussion, we use nanowire width as unit length of 1 and scale down the W_{micro} by the nanowire width.

From the architecture, we can see there is only one junction to microwire in each address line. So for a single address nanowire to yield:

$$\begin{aligned} P_{half-add} &= (1 - P_{mj}) \cdot (1 - P_l)^L \\ &\quad \cdot (1 - P_{nj})^{Q_1} \cdot (1 - P_{bp})^{Q_2} \end{aligned} \tag{2}$$

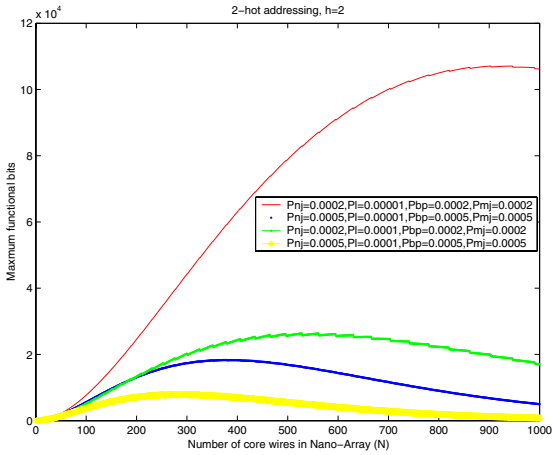

Figure 9. Maximum functional bits can be achieved with 2-hot addressing

If we further look at the array architecture, we need to account the upper and lower decoders to address a nanowire in the array core. This means we must have a pair of functional address nanowires to correctly address one core nanowire. So the yield should be modified to: $P_{add} = P_{half-add}^2$.

Second, we need to calculate the yield for a single nanowire in the array core. For each core nanowire, there are $2h + N$ blank blocks (FETs) in the core array and decoder. Also there are $2 \cdot (N_a - h)$ black blocks in the decoder area and 2 junctions with microwires. So, the yield for a single core nanowire is:

$$\begin{aligned} P_{core-wire} &= (1 - P_{mj})^2 \cdot (1 - P_l)^L \\ &\cdot (1 - P_{nj})^{(2h+N)} \\ &\cdot (1 - P_{bp})^{2\cdot(N_a - h)} \end{aligned} \tag{3}$$

If using a $h - hot$ addressing technique, the number of lines can be addressed by N_a address lines is:

$$N_{la}(N_a) = \frac{N_a!}{h! \cdot (N_a - h)!} \tag{4}$$

Then, let us calculate the expectation of how many core nanowires in the rows are addressable by N_a address lines:

$$\begin{aligned} E(N) &= \frac{N}{N_{la}(N_a)} \cdot \sum_{m=0}^{m=N_a} N_{la}(N_a - m) \cdot C(N_a, m) \\ &\cdot P_{add}^{N_a - m} \cdot (1 - P_{add})^m \end{aligned} \tag{5}$$

where the $C(N, M)$ is the number of combinations of taking M things from N at a time. And then we can calculate the net row yield $Yield_{row}$:

$$Yield_{row} = \frac{E(N)}{N} \cdot P_{core-wire} \tag{6}$$

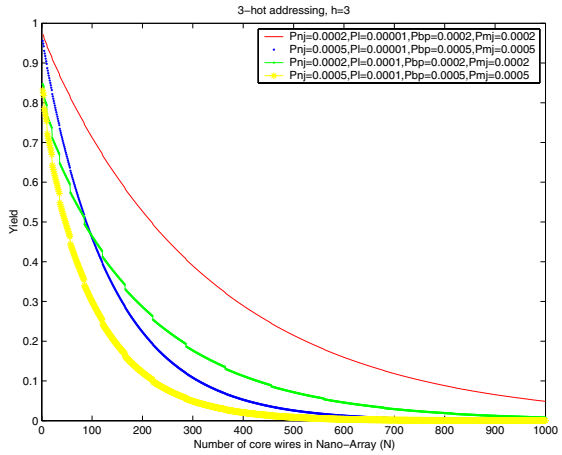

Figure 10. Yield of single nanoarray versus array size with 3-hot addressing

This is about the row yield, by symmetry, we can get the column yield all the same way. Thus the final yield of the array core is:

$$Yield_{core} \quad = \quad Yield_{row} \cdot Yield_{column} \tag{7}$$

Based on recent reports [9, 13] on the reliable growth of SiNWs and yield of junctions, we assume the P_{nj} from 0.0002 to 0.0005 as well as the P_{bp} and P_{mj} and assume P_l from 0.00001 to 0.0001. We can also calculate the maximum number of functional bits in the array and find out the optimal point by the equation:

$$Q_{function-bits} = Yield_{core} \cdot N^2 \tag{8}$$

In order to validate the proposed yield model, parametric simulations are conducted for $h = 2$ and 3 cases (i.e., 2 and 3-hot addressing schemes) using numerous sets of parameters. In Figure 8), the yield of single nanoarray vs. array size with 2-hot addressing scheme is shown. Then, the maximum functional bits can be achieved for these cases are shown in Figure (9). The maximum functional bits per array can be achieved at approximately N =900, 500, 400 and 300, respectively. The simulation results for 3-hot addressing case is shown in Figures (10) and (11), too. In both cases, the proposed yield model estimates both the yield and the density of the given nanoarray. Likewise, the proposed yield model can be also used to evaluate and optimize different defect-tolerance techniques for nanoarrays.

4: Conclusion

In this paper, We have introduced various defects associated with the nanoarray architecture, such as the crosspoint failure rate, nano-wire to micro-wire connection failure rate, decoder failure rate, etc. Based on those characterized defects, a comprehensive probabilistic yield model for the array-based nanoarchitecture has been proposed and verified. Then, we have used a series of numerical simulations to obtain simulation results such as the nano array yields and subarray densities using a wide variety of parameter sets. Also, we introduce a way to find the optimal subarray density, in

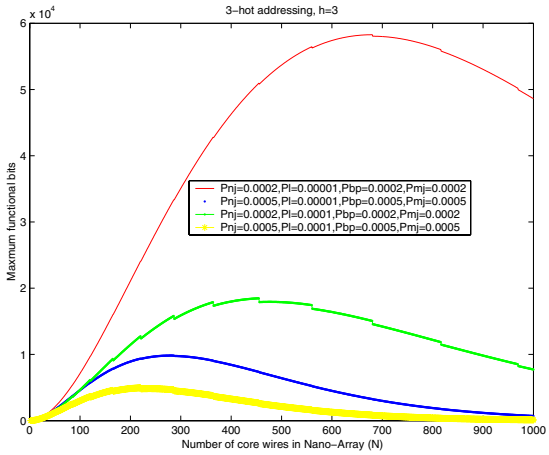

Figure 11. Maximum functional bits can be achieved with 3-hot addressing

which we can achieve the largest number of functional bits in the subarray. Finally, we compare the results from different $h - hotaddressing$ schemes. Using the proposed probabilistic yield model and some experimental/industry data, we can accurately estimate the yield and subarray density. Also, we can compare the efficiency of different fault tolerance techniques.

References

[1] International Technology Roadmap for Semiconductors, "International Technology Roadmap for Semiconductors (ITRS) 2003," *http://public.itrs.net*, 2003.

[2] G. Bourianoff, "The future of nanocomputing", IEEE Computer, Vol. 38, No. 8, pp. 44-53, Aug 2003.

[3] Andre Dehon, "Array-Based Architecture for FET-Based, Nanoscale Electronics," *IEEE transactions on Nanotechnology, Vol.2 No.1*, March 2003

[4] Benjamin Gojman, Eric Rachlin, and John E. Savage, "Decoding of Stochastically Assembled Nanoarrays", International Symposium on VLSI, pp. 11-18, Feb 2004.

[5] C. Dekker "Carbon nanotubes as molecular quantum wires," *Phys. Today, pp.22-28*, May 1999

[6] N. Melosh, A. Boukai, F. Diana, B. Gerardot, A. Badolato, P. Petroff and J. Heath, "Ultrahigh-density nanowire lattices and circuits", Science, Vol. 300, pp. 112-115, Apr 2003.

[7] Y.Huang, X.Duan, Q.Wei and C.M.Lieber "Directed assemble of one-dimensional nanostructures into functional networks," *Science, vol. 291, pp.630-633,*, Jan 2001

[8] T.Rueckes, K.Kim, E.Joselevich, G.Y.Tseng, C.L.Cheung, and C.M.Lieber "Carbon nanotube based nonvolatile random access memory for molecular computing," *Science, vol.289, pp. 94-97,*, 2000

[9] Y.Huang, X.Duan, Y.Cui, L.Lauhon, K.Kim, and C.M.Lieber "Logic gates and computation from assembled nanowire building blocks," *Science, vol.294, pp. 1313-1317,*, 2001

[10] S.J.Trans, A.R.M.Verschueren, and C.Dekker "Room-temperature transistor based on a single carbon nanotube," *Nature, vol.393, pp. 49-51,*, May 7, 1998

[11] V.Derycke, R.Martel, J.Appenzeller, and Ph.Avouris "Carbon nanotube inter- and intramolecular logic gates," *Nano Lett, vol.1, no.9, pp. 453-456,*, 2001

[12] S.J.Wind, J.Appenzeller, R.Martel, V.Deycke, and Ph.Avouris "Vertical scaling a of carbon nanotube field-effect transistors using top gate electrodes," *Appl. Phys.Lett., vol.80, no.20, pp. 3817-3819,*, 2002

[13] M.S.Gudiksen, J.Wang, and C.M.Lieber "Synthetic control of the diameter and length of semiconductor nanowires," *J.Phys. Chem. B, vol.105, pp. 4062-4064,*, 2001

[14] J. R. Heath, P. J. Kuekes, G. S. Snider, and R. S. Williams, "A defect- tolerant computer architecture: Opportunities for nanotechnology", Science, Vol. 280, pp. 1716-1721, 1998.