01 May 2006

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Recommended Citation

M. Lai et al., "Modeling of the IC's Switching Currents on the Power Bus of a High Speed Digital Board," *Proceedings of the 10th IEEE Workshop on Signal Propagation on Interconnects (2006, Berlin, Germany)*, pp. 51-54, Institute of Electrical and Electronics Engineers (IEEE), May 2006.
The definitive version is available at https://doi.org/10.1109/SPI.2006.289186

Modeling of the IC's switching currents on the power bus of a high speed digital board

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Abstract

When the performances of the electronic technology increase (higher frequencies, more power, lover power supply, faster transistors, reduced chip dimensions), designing electronic equipment becomes more challenging for the electronic engineers. Signal and power integrity on board become of paramount importance. One of the main causes of board malfunctions and electromagnetic radiation is the simultaneous switching noise (SSN) due to the integrated circuits soldered on the board. The paper proposes two simple procedures to model the SSN, so to evaluate its effects in any point of the board.

Introduction

The trend in the electronic market makes available each year integrated circuits (ICs) with always higher clock rates, full of different electronic functions. The used downward scaled technology yields faster transistors with very short channel lengths which, due to the increasing of the ICs power consumption and to the reducing of their supply voltage levels, draw high currents with an high di/dt ramping rate. Consequently the on board power integrity, i.e., the capability of delivering the needed amount of power at the requested noise free voltage level, becomes of paramount importance in the design of the high speed digital boards and has to be studied at the early stage of the project. The simultaneous switching noise (SSN), due to the fast switching of the ICs on board, can excite the resonant modes of the power/ground (PWR/GND) plane pairs, altering the correct functioning of the chips on the same power bus and generating electromagnetic interference (EMI) problems. It is obvious at this point that, to quantify the effects of the SSN, the availability of the power distribution network (PDN) model and of the IC's model, such as the profile of the current drawn from the PDN, is critical. A lot of job has been made to characterize the layer-cake structures obtained stitching together several pairs of power/ground layers separated by thin dielectric material [1-6]. Instead, the modeling of the chips as noise current sources on the power bus has to be developed in more details. Two different approaches can be used: simulations and measurements. Simulating the current drawn by an IC from the power bus can not be simple for a power integrity engineer, because it needs the knowing of a lot of parameters not usually available, such as the on-chip grid metallization, the netlist of the on-chip interconnects, drivers, receivers and semiconductor substrate [7].

An alternative could be developing the IC's current stimulus by examining its silicon function status [8] or using sophisticated measurement techniques such as, e. g., near-field scan data [9].

This paper deals with a simple technique to obtain, starting from S-parameter and power spectrum measurements, equivalent noise current sources representing the activity of an IC on the connected power bus, without knowing its internal circuitry and characteristics. The procedure presented in [10] by the authors has been developed in more details for an FPGA (Field Programmable Gate Array) where two different voltage levels supply its logic core and I/O buffers. The netlist loaded on the FPGA, named CINP (Chip for studying I Noise on Power bus), allows to control the number of logic gates and I/O buffers active. Two different equivalent noise current sources are modeled, acting simultaneously: the first one between the power and ground planes supplying the FPGA's core, the second one on the power bus supplying the FPGA's I/Os. Two different measurement procedures are proposed, named direct and indirect. The direct procedure measure the power spectrums on two ports underneath the FPGA, the indirect procedure, instead, the power spectrums on two ports faraway from the chip.

Theory

By letting d be the diagonal of the FPGA package and λ the wavelength in the dielectric, for frequencies such as $d/\lambda < 0.2$ the SSN effects due to the currents through multiple chip's PWR/GND pins can be evaluated with sufficient accuracy by considering a lumped-noise current source placed in the geometric center of the FPGA [11]. There is one lumped-noise current source for each supply voltage level. Let's consider CINP supplied by two different voltages: V_{dd} for the internal core and V_{cc} for the peripheral I/Os. Consequently two different lumped-noise current sources have to be considered in the middle of the FPGA footprint: the first one connected between the V_{dd}/GND plane pair, the second one between the V_{cc}/GND (Fig. 1).

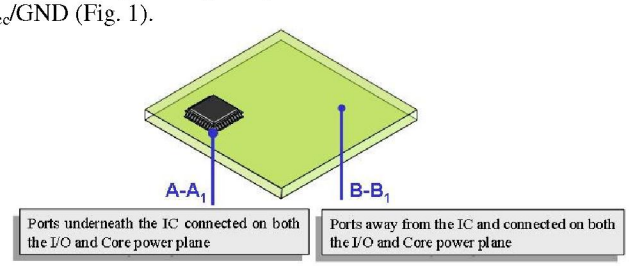

Fig. 1 – Sketch of the FPGA on board with the ports used for measurements

These sources act simultaneously, so to account for the reciprocal influence of the noise on the two different power planes. Two different procedures are proposed to evaluate the current profiles of the two equivalent noise sources. The direct

procedure start from power spectrum measurements on two ports A, A_1 connected underneath the IC at its center respectively on the I/O power bus and core. The indirect procedure, instead, uses power spectrum measurements on the ports B, B_1 faraway from the IC on the I/O and core power buses.

a) Direct Procedure

Let's consider two ports A, A_1 connected underneath the IC at its center, respectively on the I/O power bus and core.

The procedure proposes an equivalent circuit representation for the noise current sources injected into the board, from a PDN point of view, as in Fig. 2.

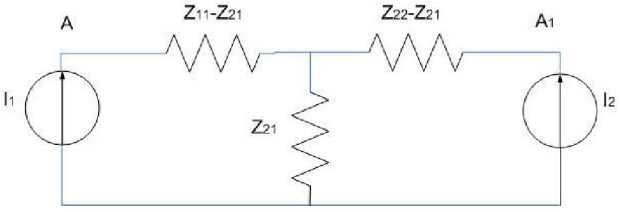

Fig. 2 – Equivalent circuit representation for the noise current sources injected into the board between ports A, A_1

From Fig. 2, Zij are the impedances of the board, obtained from S-parameter measurements or simulated, between the ports A and A_1. The magnitudes of I_1 and I_2, i. e. the equivalent noise currents injected in the I/O and core power buses, can be evaluated from the measured power spectra at A and A_1. Let's refer to the circuit in Fig. 3 for the power spectra measurements at ports A, A_1: L_1, L_2 are the inductances of the surface mounted adapters (SMAs) used for connecting the spectrum analyzer, 50Ω is the input impedance of the instrument and the board is schematized using its impedances as in Fig.2.

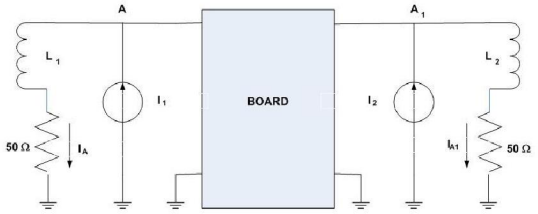

Fig. 3 – Equivalent circuit for measuring the power spectra on ports A, A_1

Considering that, when measuring the power at port A, the current $I_{A1} = 0$ and, when measuring the power at port A_1, the current $I_A = 0$, the magnitudes of the currents I_1 and I_2 can be obtained solving the system of equations (1):

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} (Z_{11} + 50 + j\omega L_1) I_A \\ (Z_{22} + 50 + j\omega L_2) I_{A1} \end{bmatrix}, \quad (1)$$

where:

$$\begin{cases} P_A = \left(\frac{|I_A|}{\sqrt{2}} \right)^2 * 50 \\ P_{A_1} = \left(\frac{|I_{A_1}|}{\sqrt{2}} \right)^2 * 50 \end{cases} \quad (2)$$

b) Indirect Procedure

Let's consider the four ports A, A_1, B, B_1 as in Fig. 1, connected on the used power buses. The system is equivalent to the circuit in Fig. 4 during the power spectra measurements at ports B, B_1. The board is schematized with its four-port Z-parameters, while the SMAs used for connecting the spectrum analyzer to the board are represented by their inductances L_1, L_2. During the measurement on port B it is $I_{B1} = 0$, while it is $I_B = 0$ when the measurement is on port B_1.

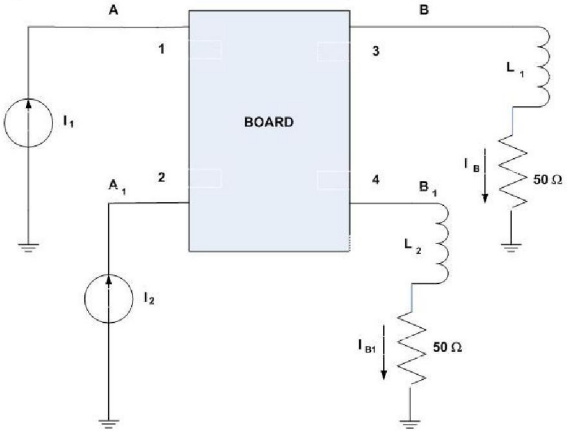

Fig. 4 – Equivalent circuit for measuring the power spectra on ports B, B_1

It follows that the magnitudes of the currents I_1 and I_2 can be obtained solving the system of equations (3):

$$\begin{bmatrix} Z_{31} & Z_{32} \\ Z_{41} & Z_{42} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} (Z_{33} + 50 + j\omega L_1) I_B \\ (Z_{44} + 50 + j\omega L_2) I_{B1} \end{bmatrix}, \quad (3)$$

where:

$$\begin{cases} P_B = \left(\frac{|I_B|}{\sqrt{2}} \right)^2 * 50 \\ P_{B_1} = \left(\frac{|I_{B_1}|}{\sqrt{2}} \right)^2 * 50 \end{cases} \quad (4)$$

As it is evident, the equation systems (1), (3) have the same structure. Consequently it is possible to provide two equivalent circuits, one for each equation in the two systems, which allow to evaluate the currents I_1, I_2, when the powers at the various

ports are measured in the direct and indirect procedures (Fig. 5). In Fig. 5a the powers are measured at port A (direct procedure) or B (indirect procedure), while in Fig. 5b at port A_1 (direct procedure) or B_1 (indirect procedure). The used parameters are as follows:

- *Direct procedure*: $Z_1 = 50$; $Z_2 = Z_{11}-Z_{21}$; $Z_3 = Z_{21}$; $I_{L1} = I_A$; $Z_4 = 50$; $Z_5 = Z_{22}-Z_{21}$; $Z_6 = Z_{21}$; $I_{L2} = I_{A1}$
- *Indirect procedure*: $Z_1 = 50+Z_{33}-Z_{31}$; $Z_2 = Z_{31}-Z_{32}$; $Z_3 = Z_{32}$; $I_{L1} = I_B$; $Z_4 = 50+Z_{44}-Z_{42}$; $Z_5 = Z_{42}-Z_{41}$; $Z_6 = Z_{41}$; $I_{L2} = I_{B1}$.

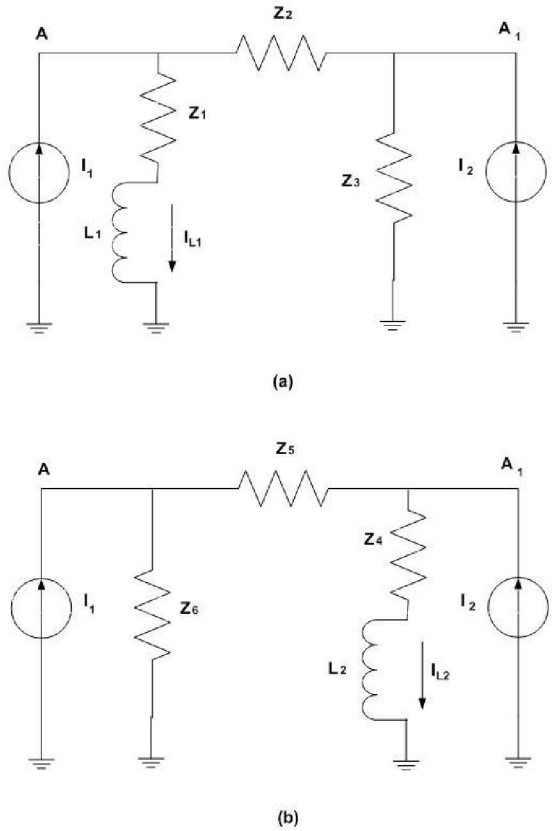

Fig. 5 – Equivalent circuits for power measurements at: a) ports A, B; b) ports A_1, B_1

Test board

Fig 6 shows the test board where the CINP is soldered. CINP is an FPGA of the XILINX Spartan IIE family. It has a PQ208 package with a size of 28mm x 28mm. There are 12 core power (V_{ccint} = 1.8V) pins, 16 I/Os power (V_{cco} = 2.5V) pins and 24 ground (GND) pins. These power pins are soldered on two different contiguous power planes (V_{ccint}, V_{cco}) sandwiched between two GND planes.

The power supply decoupling is obtained by means of 36 x 100nF + 1 x 33µF decaps connected on the V_{cco} plane and 18 x 100nF + 1 x 33µF decaps connected on the V_{ccint} plane beneath the FPGA. The CINP is clocked with an external clock at 155.52MHz. The activity of the I/O is determined by the netlist downloaded in the FPGA and it is strongly dependent on the number of I/Os and switching frequency. The activity of the core is mainly determined by the way how the FPGA is programmed and does not strongly depend on the number of the I/Os the logic is driving. The netlist is loaded in the FPGA by means of its JTAG pins. Four SMA connectors are used to connect the ports A, A_1, B, B_1 on board to the measurement instruments.

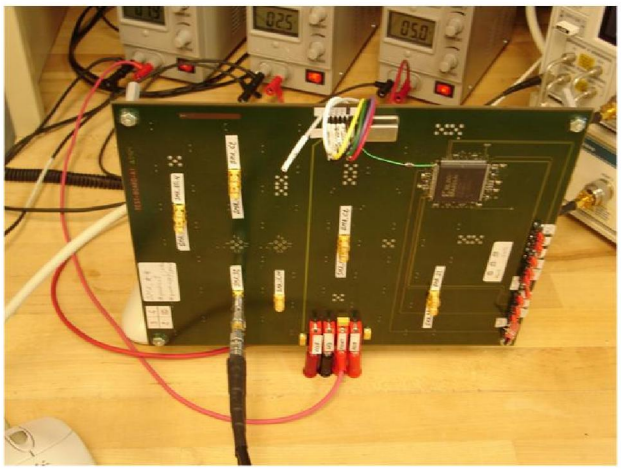

Fig. 6 – Test board

Results

Two ports (A, A_1) and four ports (A, A_1, B, B_1) S-parameters are measured using an Anritsu 37247C vector network analyzer (VNA) with multi-port test set. The S-parameter matrices are transformed into the impedance matrices using the equation:

$$[Z] = Z_0 \frac{[I]+[S]}{[I]-[S]}, \qquad (5)$$

where [I] is the identity matrix and Z_0 = 50Ω is the characteristic impedance of the VNA.

The netlist downloaded in the FPGA activate 12 LVCMOS2 drivers and receivers connected in loop, 8 differential LVDS drivers back looped with the corresponding receivers at the end of matched traces. The buffers are driven with 155.52Mbps pseudo random sequences.

Considering the diagonal of the FPGA d = 40cm, the condition $d/\lambda < 0.2$ [11] sets the frequency range of validity of the proposed noise current model. In our case the frequency range of interest is almost up to 1GHz.

Applying the direct and indirect procedures as in the previous paragraph, the magnitudes of the I_1 and I_2 currents are obtained as in Figs. 7, 8.

As it is evident, the 2 and 4-port approach allows estimating the noise current sources with a pretty good accuracy. Only a little shift in the frequency components can be appreciate. This means that ideally in any position of the board it is possible to estimate the same noise currents which can be estimated by means of probes located just underneath the chip under test. When the equivalent noise current sources are known, it is possible to evaluate the effects of the SSN due to the FPGA in any points of the board, estimating, e. g, the S-parameters between the FPGA and the chosen points with some multilayer cavity model that will also include eventual decaps located on the board.

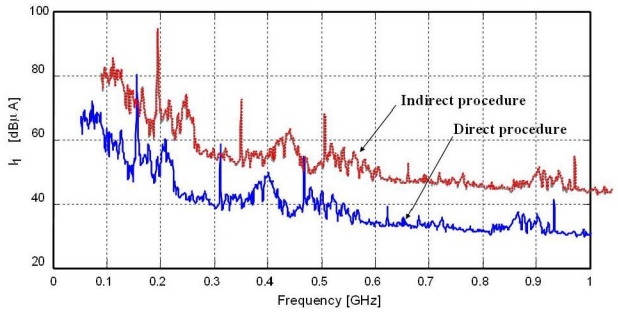

Fig. 7 – Equivalent noise current source between the I/O power plane and GND

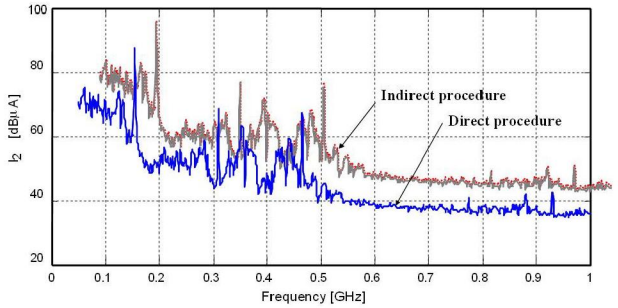

Fig. 8 – Equivalent noise current source between the core power plane and GND

Conclusions

Two different procedures for the evaluation of the equivalent noise current sources, accounting for the effects of SSN due to an FPGA, are presented in this paper. At each IC's power supply has been associated an equivalent noise current source and all the sources act simultaneously, so to take into account the cross-simultaneous switching noise (X-SSN) among different power planes in proximity. In the proposed case study, because of the X-SSN, on the core supply power plane are seen contributions in the power spectrum coming from the I/Os and, dually, contributions from the core supply are shown in the power spectrum on the I/O power bus. Using the proposed FPGA noise model together with some multilayer cavity model of the power planes, the power integrity on board can be carefully evaluated. Because the activity of the FPGA changes the spectrum of the noise current sources, in the future works a statistical study of the power spectra in the power planes for different FPGA working conditions will be carried out, so to obtain a more realistic model for the noise current associated with the FPGA itself.

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