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Cascaded Multilevel Converters with Non-Integer or Dynamically Changing DC Voltage Ratios

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Abstract- **Multilevel converters made of cascaded cells (MCCC) offer a high number of voltage levels with a given switch count. Many variants of the MCCC topology have been introduced over years. Mostly, only integer dc voltage ratios between the cascaded converter cells have been applied to its PWM modulation. This is mainly due to the non-uniform distribution of voltage vectors with the non-integer dc ratios. It poses difficulty to the conventional SVM modulators relying on locating the equilateral "triangle" made of three nearest vectors enclosing the reference vector. In this paper, an original modulation method is introduced to operate with any dc voltage ratio between cascaded converter cells, integer or non-integer; and even with a dynamically varying ratio; while the normal PWM output fast-average is not disrupted. The space vector analysis and the detailed simulations verify the modulation method.**

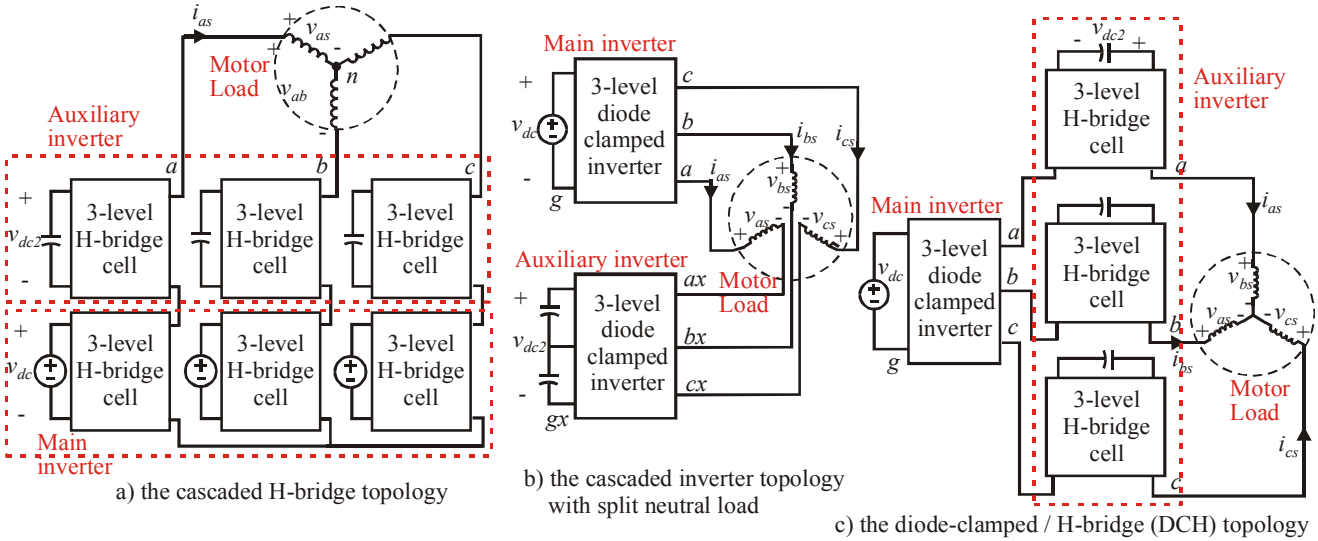
The new concept of MCCC PWM with non-integer dc voltage ratio offers great flexibility in its practical operation, particularly in MCCC with single dc source where the auxiliary inverter cell dc-link capacitor voltage can be regulated at arbitrary value online. Its wide range of practical applications is briefly discussed in this paper.

I. Introduction

In summary, there are three major types of topologies for multilevel converter with cascaded converter cells (MCCC). Figs. 1 (a), (b) and (c) show the cascaded H-bridges, cascaded multilevel converters through split neutral load and the multilevel converter in series with H-bridge cells, respectively. Given the same dc voltage ratio between the cascaded cells, all three topologies can provide the equivalent voltage levels with same IGBT switch count.

Recent developments in MCCC control methods witnessed two major trends. First is the hybrid operation between converter cells [1, 4, 5 and 8], where the main and auxiliary inverter cells operate at fundamental and PWM frequencies respectively. The other progress is in single dc source operation [4, 5 and 8], with only capacitor sources in auxiliary inverter. This greatly simplifies the converter dc front end complexity. Therefore, the topologies (b) and (c) are particularly preferable since only one isolated dc source is needed in the main converter cell (suppose diode clamped topology is used), while the topology (a) requires three of them.

The MCCC output performance (directly related to the number of voltage levels or layers of the voltage vectors in the hexagon patterns) depends on the dc-link voltage ratio between the main and auxiliary converter cells. The Fig. 2 shows the examples when two three-level converters are cascaded. As the voltage ratio increases, fewer voltage vectors overlap and there're more voltage vector positions available for the modulator, until the 4:1 ratio results in discontinuous vector pattern on the edge of the plot. So the voltage ratio 3:1 is called "maximal distension" [6, 7], and its total voltage levels (layers of hexagon rings in plot) are the product of the level numbers of all cascaded converter cells. In this example, the maximal distension offers 9-level performance.



a) the cascaded H-bridge topology

b) the cascaded inverter topology with split neutral load

c) the diode-clamped / H-bridge (DCH) topology

Figure 1. The three major MCCC topologies.

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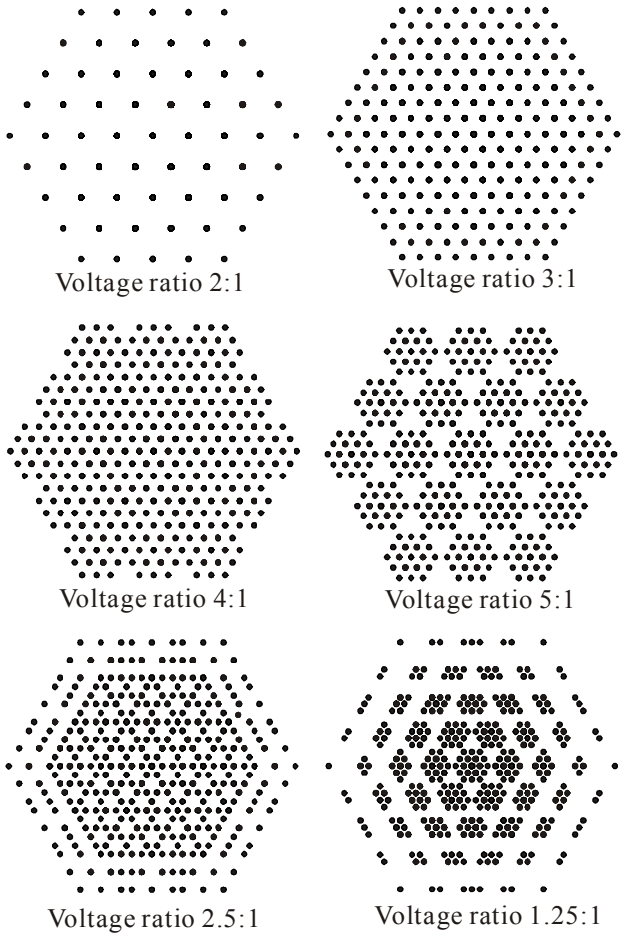


Figure 2. Vector plot with different dc voltage ratio

All integer dc ratios at or below maximal distension result in evenly distributed voltage vectors constituting the meshes of equilateral triangles. The 4:1 ratio is called "over-distension" [7], and for the m-index lower than the discontinuous region, it offers higher output resolution than "maximal distension". At the voltage ratio beyond "over-distension", like 5:1, the vector pattern becomes isolated "islands", hence an invalid option for modulator.

The non-integer voltage ratios between the MCCC cells can be used in the fundamental frequency switching (block switching) with Selective Harmonics Elimination (SHE) to achieve extra orders of harmonics elimination [9 and 10]. However, the non-integer ratio creates non-uniformly distributed vectors as in Fig. 2. The PWM modulator locating the enclosing equilateral triangle for the reference vector seems to be impossible. That is most likely the reason why there's no previous report on the PWM with non-integer voltage ratio in MCCC.

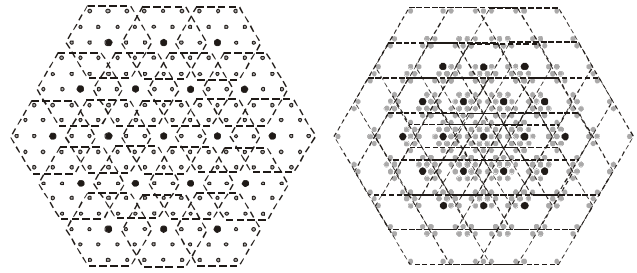
The "hierarchical modulation" introduced in the next section solves the problem. It can always locate the equilateral triangles out of the unordered vector patterns. Moreover, this method works even with the online changing of the voltage ratio, i.e. dynamic changing vector patterns. The normal MCCC output will not be disrupted during the transient.

II. Proposed Modulation Method

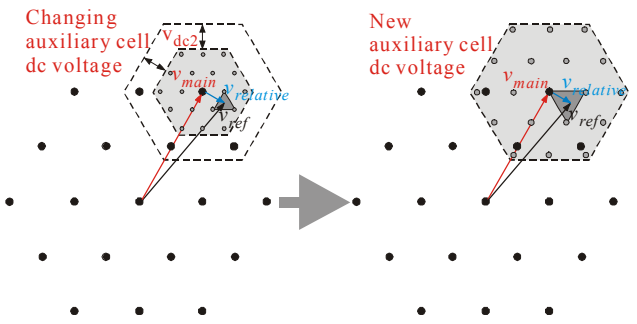
Various multilevel converter modulation schemes have been introduced over years. The book [13] provides a comprehensive review for recent developments in modulation techniques. Particularly in [11, 12], the new coordinate system for SVM is introduced and then the equivalence between the SVM and the carrier based modulation (natural sampling) is proven. The conventional carrier based multilevel modulation uses multi-layer carrier comparison with the reference signal in each phase. The resulting switching states are then decomposed into the switching states for each converter cell using lookup table. In SVM perspective, this method automatically locates the enclosing triangle and the vectors on its vertex; it can also generate the optimal switching sequence and duty ratios when the proper common mode reference signal is applied [12]. As stated previously, this conventional practice will not handle the non-uniform vector patterns when non-integer dc voltage ratio is applied to MCCC.

The "hierarchical modulation" method is proposed to address this problem. The voltage vector plot of MCCC can be readily represented by the hierarchical organization of the switching states of the main and auxiliary inverter cells. Fig. 3(a) shows such an example with two cascaded 3-level converters at 3:1 dc voltage ratio. The heavy vector dots form a 3-level vector pattern representing all switching states of the main converter. Each vector is then cascaded with complete enumeration of the auxiliary converter switching states, which forms a sub-hexagon designated by dotted line. The sub-hexagon dimension is 1/3 of the main hexagon. As voltage ratio changes (integer or non-integer value), the size of the sub-hexagon and the vectors distribution changes accordingly. As illustrated in Fig. 3(b) and (c), beneath the seemingly convoluted vector patterns at non-integer ratio, there're still cascaded sub-hexagons made of meshes of equilateral triangles.

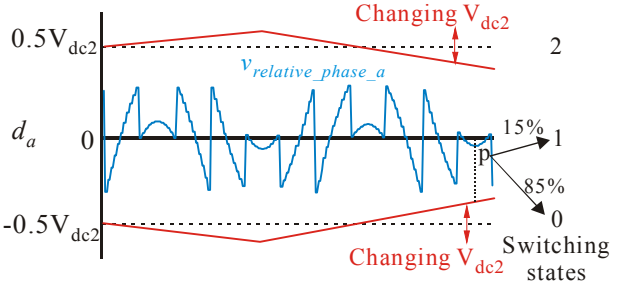
As in Fig. 3(c), any reference voltage vector v_{ref} can be decomposed into the combination of the nearby main cell vector v_{main} and the "relative reference vector" $v_{relative}$ with the origin at v_{main}. The problem is then hierarchically reduced to synthesizing $v_{relative}$ within the 3-level sub-hexagon. Still in Fig. 3(c), suppose the v_{ref} and V_{dc} remains fixed; as the voltage ratio (or V_{dc2}) changes, it could fall into a different triangle with its size changed as well. To trace its enclosing triangle with changing size, all the vector computations must use their actual values (instead of m-index) and the resulting $v_{relative}$ is then transformed into the *a-b-c* coordinate to obtain the reference signal $v_{relative\text{-}phase\_x}$ per-phase. The instantaneous auxiliary inverter dc voltage V_{dc2} measurement is updated every PWM cycle to compute the duty ratios for each phase leg according to the illustration in Fig. 3(d). Herein, the point 'p' is the a-phase reference value in certain PWM cycle. It is synthesized by 15% of state 1 and 85% of the state 0 in the auxiliary inverter a-phase (three level inverter with switching state 0, 1 and 2 in each phase).



(a) voltage ratio 3:1 (b) voltage ratio 1.25:1



(c)changing dc voltage ratio with the fixed voltage reference



(d) auxiliary converter duty ratio computation

Figure 3. Hierarchical modulation illustration

In the space vector view, the above modulation process automatically locates the enclosing equilateral triangle with its size changing at the same ratio as the V_{dc2}. Then the duty ratio of each vector on its vertex is computed.

The above description of generating the reference signal per-phase is a simplistic version of the real process. The 3-phase reference signal will be further adjusted with common mode reference to balance the voltages between the capacitors in the auxiliary cell as analyzed in [8]. In topologies in Fig. 1(a), (c), the balance is between the three phase capacitors, and in Fig. 1(b), the balance is between the upper/lower capacitors.

The complete process of the hierarchical modulation also needs to determine which main inverter cell vector is to be applied at given reference vector position along its locus. This process determines the main inverter vector traversal pattern, i.e. all the main inverter vectors to be used in a fundamental cycle and their time duration. This traversal pattern directly affects the power flow distribution between the main and auxiliary inverter cells as in [5]. For example, when MCCC operates at single dc source mode, the net power into the auxiliary cell is to be maintained at zero by properly adjusting the main inverter vector traversal pattern, so as to maintain its overall capacitor charges and V_{dc2}.

III. The Non-integer Volatge Ratio Operation Space Vector Analysis

Fig. 4 provides an insightful look at the non-integer voltage ratio PWM output using the proposed modulation method. The ratio 1.25:1 is used in the example. Its complete vector plot is in Fig. 3(b). The Fig. 4(a), (b) and (c) are the zoom-in illustrations of the modulation when the main inverter uses switching states 200, 210 and 220, respectively. The red circle represents the locus of the reference vector. The larger grey dots represent all switching states of the main inverter. Only the sub-hexagons affiliated with 200, 210 and 220 are shown here for clarity.

The line to line output voltage v_{ab} is usually shown as the indicator of the multilevel output performance. The resulting v_{ab} with the non-integer ratio has interesting pattern as shown in Fig. 4(d). In space vector view, v_{ab} is the ab-axis projections of all the voltage vectors used along the modulation path. The labels ('a' through 'g') along the ab-axis as shown in Fig. 4 (a), (b) and (c) represent such projections and also correspond to the labels in Fig. 4(d). The highlighted triangles are the ones used to synthesize the reference vector. From Fig. 4(a) to (c), there're totally 11 such triangles used. When triangle 1 (belonging to the sub-hexagon 200) is used, the v_{ab} switches between level 'a' and 'b'; then it switches between 'b' and 'c', when triangle 2, 3, 4 are used. At certain point when the reference is going across the triangle 4, the main inverter switches to 210 and the triangle 5 in the new sub-hexagon will be used to synthesize the reference vector. The projections of triangle 5 and subsequent triangle 6 onto the axis-ab are between 'd' and 'e', then the triangle 7 is between 'e' and 'f'. These are corresponding to the ['d', 'e'], ['e', f'] segments in v_{ab} time domain waveform.

At certain point when the reference is in triangle 7, the main vector jumps to 220, and the triangle 8 is then used. Hence the v_{ab} will switch from segment ['e', 'f'] to ['g', 'h'] during this transition. The triangle 9, 10 and 11 are then used subsequently. The same space vector analysis is applicable for the whole fundamental circle of the reference vector.

The multilevel PWM output of MCCC with non-integer ratio does not have clear cut number of levels in its line to line voltage as in the case when the integer voltage ratio is used. v_{ab} waveform of non-integer ratio appears to have more levels. However, the THD is not lowered by more observable levels. The dominant PWM frequency harmonics magnitudes are approximately proportional to the size of the equilateral triangle.

IV. Operations with Different M-index or Dynamically Changing Voltage Ratio

The shape of the v_{ab} evolves with the main inverter vectors traversal pattern. In MCCC single DC source operation, the m-index directly affects the traversal pattern [5] and hence the v_{ab} output shape. A simulation

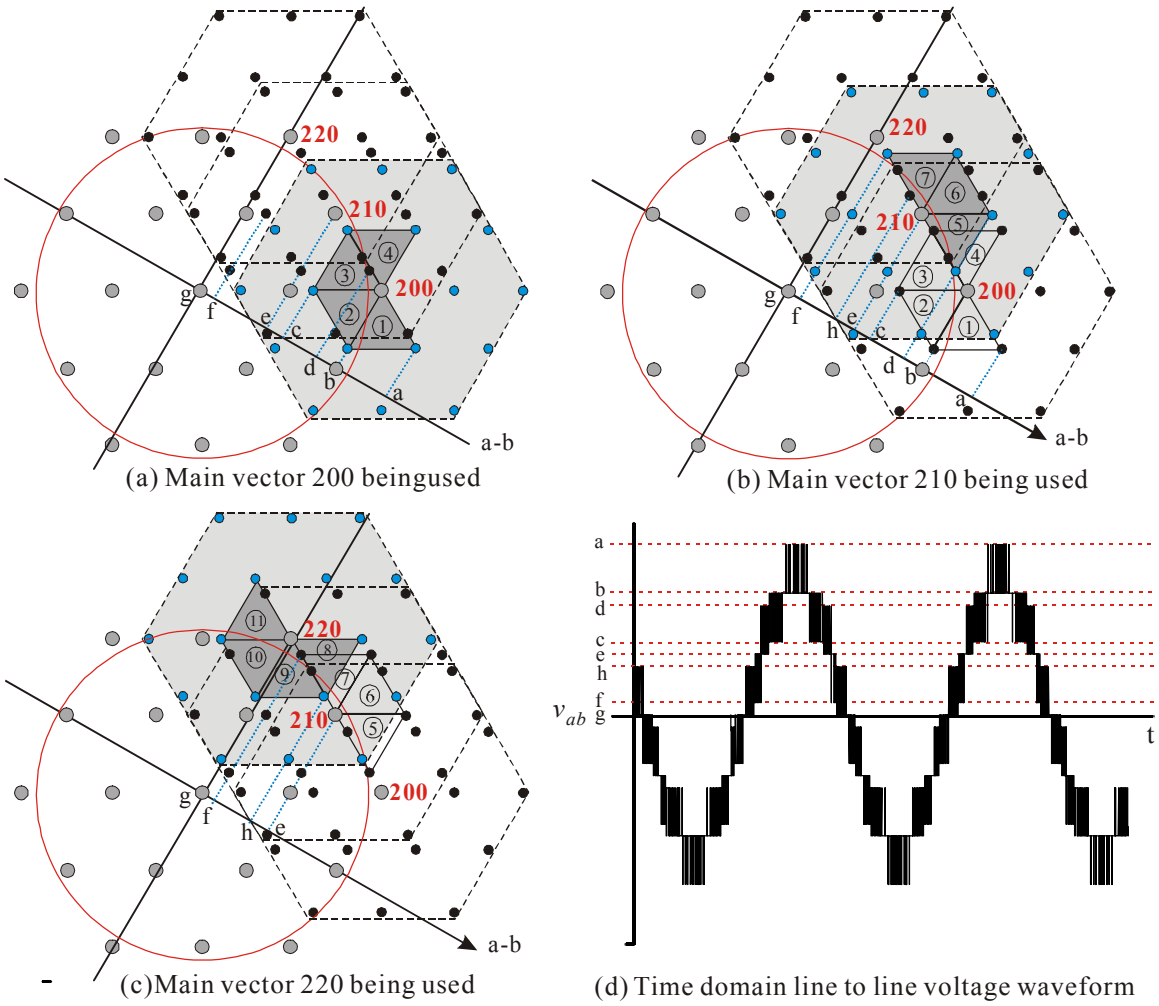


Figure 4. Space vector analysis of non-integer ratio

is given in Fig. 5 where the m-index is lower than the previous case and the main inverter vectors follow the star-shaped pattern as in Fig. 5(a). The resulting voltage waveforms as shown in Fig. 5(b) are different than the previous case. As the main inverter vector jumps from 201 to 110, the triangles labeled 1(in red) and 2(in blue), which belongs to the sub-hexagons originating from the vector 201 and 110, are used. Their projections onto the ab-axis are highlighted in v_{ab}. Despite the evolving shape of the MCCC output voltage envelope, its fast average is always correctly synthesized with the proposed modulation method, as verified by the sinusoidal phase voltage v_{ffas} after the PWM filter.

The Fig. 6 shows the effectiveness of the proposed modulation method during the voltage ratio dynamic change. Herein, the voltage ratio is dynamically changed from 2:1 to 3:1 by commanding net power out of the auxiliary inverter which has only capacitor source. The

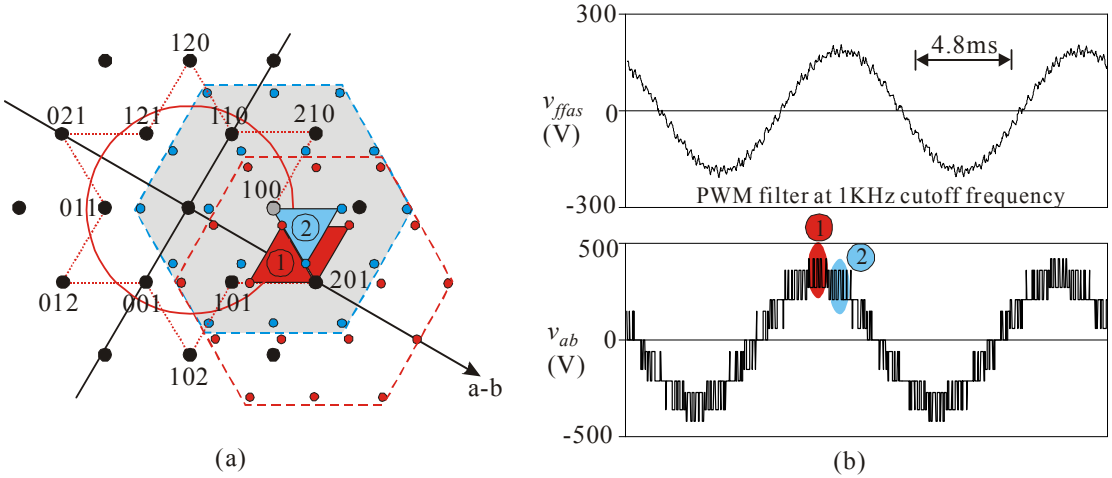


Figure 5. Space vector analysis with dc ratio at 1.25:1 (m-index is smaller)

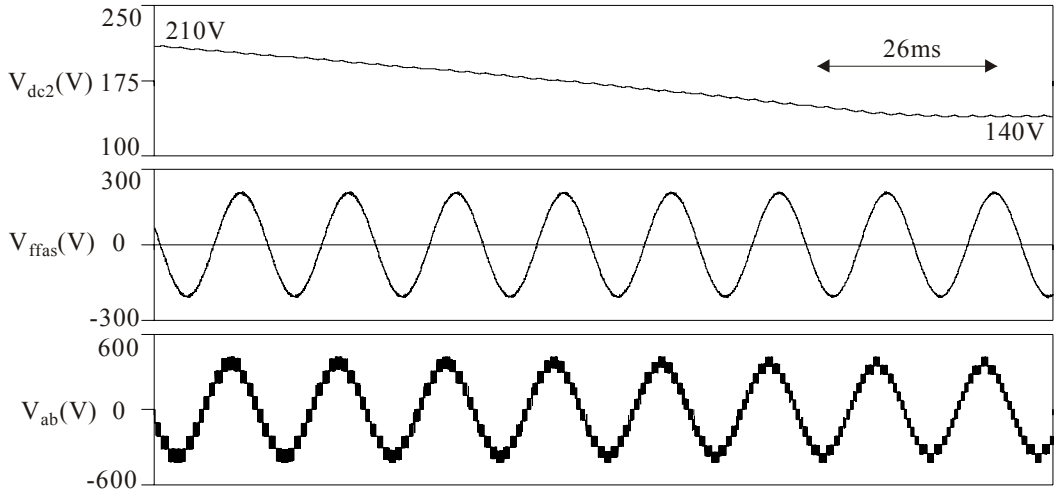


Figure 6. The dynamic voltage ratio change from 2:1 to 3:1 (V_{dc2} from 210V to 140V)

m-index (sinusoidal reference magnitude) is kept constant during the process. Initially, v_{ab} has 5-levels with the ratio 2:1. As V_{dc2} decreases to 1/3 of the main inverter V_{dc}, the levels in v_{ab} increases to seven. It is instructive to observe the gradual transition of the v_{ab} waveform. The first trace in Fig. 6 shows the V_{dc2}, which is decreased from 210V to 140V (V_{dc} is 420V). The phase voltage fast average (trace 2 in Fig. 6) after PWM filter remains sinusoidal and not disrupted during dynamic voltage ratio transition.

V. Conclusion

In this paper, a new concept of the non-integer dc voltage ratio operation in MCCC PWM operation was introduced. The modulation method proposed offers the unique feature which enables the online change of the auxiliary inverter capacitor (dc-link) voltage without disrupting the MCCC output voltage. Obviously, this offers the wide range of practical application possibilities.

First, the new concept can be applied to the large hybrid electric vehicle or electric vehicle propulsion [14], where MCCC is used in the electric power train; the ultra-capacitor banks are directly installed across the auxiliary converter cell dc-link, and its state of charge can be regulated online at any value. This offers a unique way to manage the vehicle regenerative braking energy without using a dc-dc converter to interface the ultra-capacitor. Many technical details to implement and integrate this general concept with the vehicle motor drive are addressed in the literature [14].

Similarly, the concept can be easily adapted to other large motor drive systems with frequent braking and accelerations. Hereby, the regenerative braking energy can be stored for subsequent motor acceleration, which avoids a complicated inverter regenerative front-end design or braking resistor energy loss.

Furthermore, for any type of application using one of the topologies of the multilevel converter with cascaded cells, the proposed new concept will provide an efficient and simplified energy storage methodology to directly place the energy storage devices across the dc-link since the wide dc-link voltage variation will be transparent to the voltage output.

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