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RF Isolation Using Power Islands in DC Power Bus Design

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Abstract: Power island structures are often employed for minimizing the propagation of high-frequency noise on DC power buses. The rationale is based on introducing a series impedance in the power plane to provide isolation of a noise source from the rest of the PCB design. The power island concept is investigated herein experimentally, to determine its noise mitigation attributes and limitations. A modeling approach that is suitable for arbitrary PCB island geometries including lumped SMT decoupling capacitors is also presented. The modeling and measurements indicate that island structures can achieve some degree of isolation under certain conditions.

equation formulation, denoted CEMPIE, is applied herein to model various power island structures. Since this formulation is based on Maxwell's equations, it incorporates the distributed nature of the power bus, and is suitable into the several giga-hertz range. The agreement between the modeling and measurements demonstrate that it is a powerful modeling tool for analyzing high frequency behavior of power island structures. The modeling approach is conceptually similar to the partial element equivalent circuit (PEEC) method [4]. However, critical differences in the Green's functions yield significantly different lumped element models, though both have been well demonstrated experimentally.

I. INTRODUCTION

The high-frequency noise on a DC power-bus caused by simultaneous switching noise is a primary source of many EMI and SI problems in high-speed digital circuit design [1], [2], [3]. A power plane with segmentation, i.e., complete isolation or islanding, is often employed for mitigating noise propagation on the DC power bus. From a signal integrity perspective, the segmentation provides a series impedance in the power plane reducing the conducted noise currents beyond the island, thus providing isolation of a noise source from the rest of the PCB layout.

The RF performance of segmentation is not clearly known. It is typically supposed that a power island structure can be modeled as a π -network with two capacitors representing the parallel plane capacitance of each power area, and a series inductance for the narrow neck connecting the two areas. Similarly, isolated power planes might be thought of as a π -network comprised of two shunt capacitances and one series capacitance for the coplanar capacitance of the gap. Although this modeling provides some underlying conceptual base motivating a power-island or dual-isolated power plane structure for mitigating noise coupling, it is not an accurate high-frequency model incorporating the distributed behavior of the planes. In practice, power-plane segmentation can not be treated in a lumped manner, even at frequencies as low as a few hundred megahertz for typical 6"-8" size PCBs. A circuit extraction approach based on a mixed potential integral

To understand the relevant physics, and further establish guidelines for designing segmented power buses, both $|S_{21}|$ measurements on unpowered boards, and noise spectrum measurements on powered boards were conducted to compare and contrast the RF isolation behaviors among a dual-isolated power plane, a continuous power plane, a segmented plane with a thin conducting neck that provides a path for DC power, and a segmented plane using a ferrite bead to provide DC continuity.

A comparison between CEMPIE modeling and measurements are presented to demonstrate the modeling. Further, a simple example is given to illustrate the usage of CEMPIE modeling for understanding the effects of various segmentation factors, such as gap width, gap location, neck width, neck position, etc.

II. EXPERIMENTAL RESULTS

A simple power bus structure was studied. As illustrated in Figure 1, a two-layer board with 43-mil layer spacing was adopted with the top and bottom layer representing the power and ground layers, respectively. The dimensions were $a = 150$ mm, $b = 100$ mm, $c = 74$ mm, $d = 49$ mm, $t = 2$ mm, and $e = 2$ mm. The four cases investigated experimentally were a continuous power plane without segmentation, which was used as a reference, a completely gapped power plane, and two cases with a neck providing DC continuity either through

a conducting strip or an SMT ferrite. In many cases, it is desirable to implement a structure achieving RF isolation, as well as providing DC continuity.

The $|S_{21}|$ is used herein to characterize the behavior of the power bus. It is straightforward to measure, and it is indicative of the transfer characteristics between the two measurement ports. The relationship between S_{21} and Z_{21} is [5]

$$|Z_{21}| \approx 0.5Z_0 |S_{21}| \quad (1)$$

provided that $|S_{21}|, |S_{12}| \ll 1$ and $|S_{11}|, |S_{22}| \approx 1$, which is approximately the case for a DC power bus. Assuming that there is a current source or sink at Port 1, $|Z_{21}|$ indicates the magnitude of the noise voltage at Port 2 induced by this current change, for $I_2=0$. Therefore, $|S_{21}|$ is also a means of evaluating the noise coupling between two locations on the power bus.

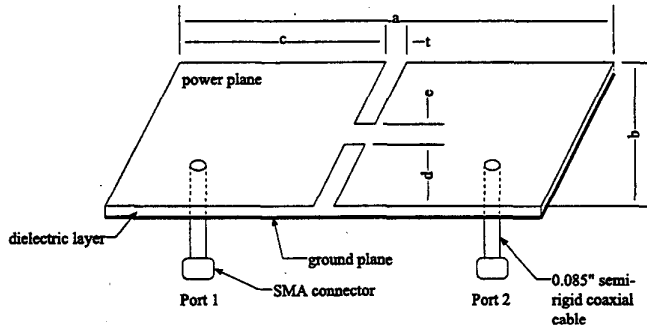


Figure 1: Geometry for the power segmentation investigation.

An HP8753D network analyzer was used to measure the $|S_{21}|$. The reference planes were at the 3.5 mm test cable connectors. A simple 12-term error correction model using an open, short, and load was used in the calibration. Port extension was used to move the measurement plane to the coaxial cable feed terminals looking into the power bus.

Figure 2 shows the measured $|S_{21}|$ results for all four cases studied experimentally. Compared with the continuous power plane, the completely gapped or dual-isolated plane has better isolation over nearly the entire frequency range, except at the board resonances. All four board configurations have a resonance at approximately 0.7 GHz, which is the half-wavelength resonance frequency of the board. The resonance is the same even for the planes with gaps because the gap was introduced in the middle of the board. Consequently for modes of the parallel plate structure that had a current null along the gap line, the segmentation did not disturb this mode. Below the 0.7 GHz resonance frequency, the segmented power plane with a conducting neck yields no obvious benefit over the continuous power plane, though its first resonance is shifted to a slightly lower value. Above the 0.7 GHz resonance frequency, a segmented power plane with or without a conducting neck has comparable degrees of isolation due to the decrease of the conductive coupling through the neck because of the increasing neck impedance.

Though a conducting neck can provide DC continuity between two gapped portions, it compromises the isolation achieved by the gap in the low frequency band. An alternative is to use a ferrite to provide RF impedance but DC continuity. Figure 2 shows that an SMT ferrite connection has almost the same degree of isolation as the completely gapped plane in the entire test band, except that the ferrite also provides DC continuity. Finally, the Q_s of the resonances shown in Figure 2 are much higher than is the case for a fully populated board.

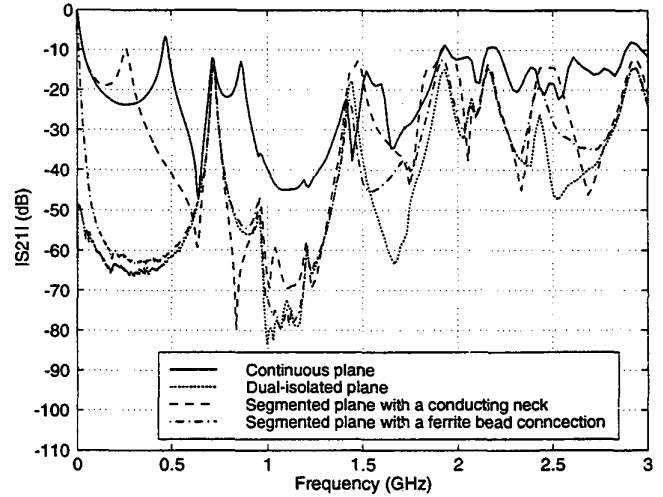


Figure 2: $|S_{21}|$ measurements for the continuous and segmented power bus configurations.

Although $|S_{21}|$ is a good indicator for power bus evaluation, the noise voltage spectrum for an active circuit is a more direct indication of the noise coupling. Power bus noise measurements were performed for the same four power bus structures with the source port replaced by a fast CMOS buffer, IDT74FCT, as illustrated in Figure 3. The buffer was powered at 5V DC with a lab power supply, and a 40 MHz square-wave signal was input at Pin 1. The noise voltage at the victim port was measured with a Tektronix 2712 spectrum analyzer from 9 kHz - 1.8 GHz.

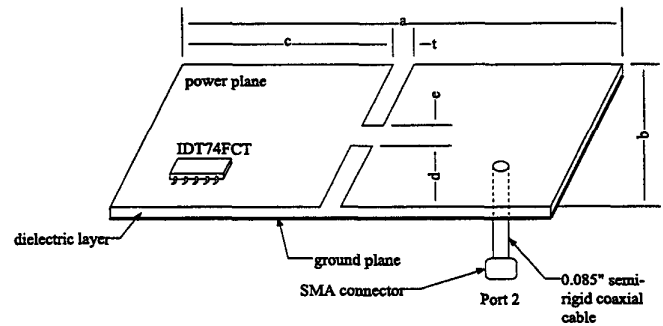


Figure 3: Power bus noise measurement setup.

The measured results for the active test circuit are shown for the four board configurations in Figures 4-7. The input signal to the buffer was a 40 MHz clock signal (square wave). The even harmonics are somewhat stronger than the odd harmonics possibly due to the switching current shoot through at both the rising and falling edges, which has a fundamental frequency of 80 MHz. The parallel plane resonances are apparent in the noise spectrum at approximately 0.45, 0.7, and 1.4 GHz. The completely gapped plane does achieve RF isolation over this frequency range as compared with the continuous power plane. The distributed resonances associated with the segmented plane seen in Figure 2 are also quite clear in Figure 5 at 0.7 and 1.4 GHz. Similar to the IS211 measurements, the power plane with a conducting neck has noise coupling comparable with the continuous plane as seen in Figure 6. However, for the segmented plane with a ferrite bead connection, the noise spectral components are almost at the same level as those of the completely isolated power plane.

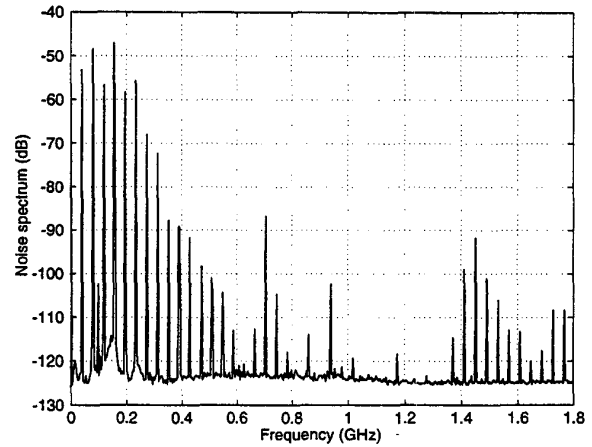


Figure 6: Power bus noise spectrum for a segmented plane with a conducting neck.

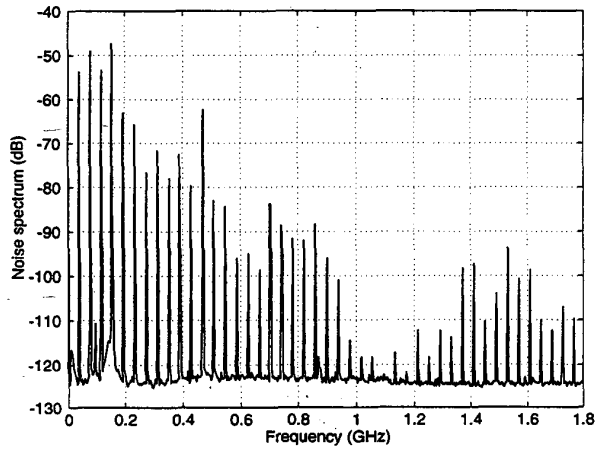


Figure 4: Power bus noise spectrum for a continuous plane.

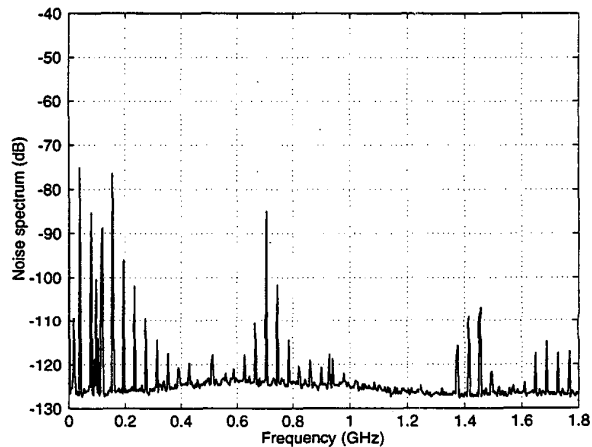


Figure 7: Power bus noise spectrum for a segmented plane with a connection through an SMT ferrite.

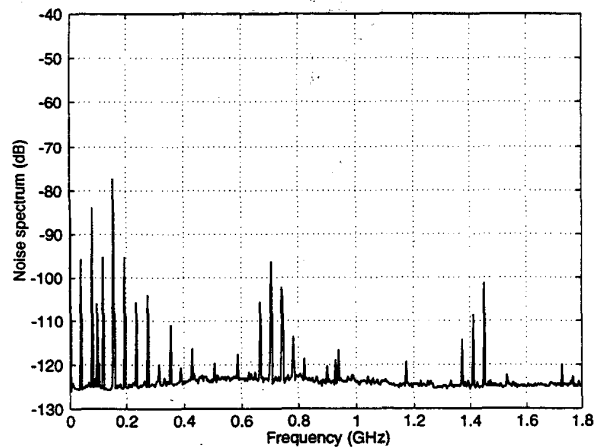


Figure 5: Power bus noise spectrum for a dual-isolated power bus.

III. MODELING RESULTS

Though many power bus design concerns can be investigated with hardware for a specific design, general design guidelines and modeling tools are desirable. A full-wave integral equation formulation with circuit extraction is used herein for modeling. There are a number of advantages in having a suitable equivalent circuit model. For example, the circuit quantities, *i.e.*, current and voltage, are directly useful for investigating SI and EMI problems, the extracted circuit model can be reused for both time- and frequency-domain simulations, and many well-developed SPICE and IBIS models for sources, loads, and transmission lines can be easily

incorporated into the power bus model. A modeling tool denoted herein as CEMPIE (a Circuit Extraction approach based on a Mixed-Potential Integral Equation formulation) has been developed for this purpose [6]. A schematic representation of the tool is shown in Figure 8.

A current density $\vec{J}(\vec{r})$ and charge density $\sigma(\vec{r})$ is induced on the metal plane (arbitrary power layer metallization) as a result of an incident electric field \vec{E}^{inc} . An integral equation results when enforcing boundary conditions on the conducting plane [7], [8]

$$\vec{E}^{inc}(\vec{r}) = j\omega \iint_S \vec{G}^A(\vec{r}, \vec{r}') \cdot \vec{J}(\vec{r}') ds' + \nabla \iint_S G^S(\vec{r}, \vec{r}') \sigma(\vec{r}') ds', \quad (2)$$

where $\vec{G}^A(\vec{r}, \vec{r}')$ is the dyadic Green's function for the vector potential, and $G^S(\vec{r}, \vec{r}')$ is the Green's function for the scalar potential. In this case the Green's functions are for grounded dielectric slabs [9], and the ground plane is considered to be of infinite extent. The integral equation is then discretized using the Method of Moments with a triangular mesh and vector basis functions [10], [11]. Further, a mixed-potential integral equation results when assuming the scalar potential is constant within each triangular cell [12]. This transformation from an EFIE to an MPIE simplifies the circuit extraction. The circuit model is extracted from the moment matrix without solving the matrix equation [11].

There are four distinct steps for modeling a power bus structure in this approach. First, a triangular mesh is generated for the metallization plane of concern, *i.e.*, the power plane, which can be arbitrarily shaped. A ground plane is assumed infinite and its contribution is incorporated into the Green's functions. The second step is to calculate the Green's functions for an arbitrary layer stack-up. The moment method problem is then formulated and implemented, and a circuit model is extracted. Once the circuit model is obtained, simulations for various "what if" scenarios can be performed using a SPICE simulator.

A simple power island structure as shown in Figure 1, with sizes of $a = 100$ mm, $b = 55$ mm, $c = 49$ mm, $d = 25$ mm, $e = 5$ mm, and $t = 2$ mm, was used as an example to demonstrate the effectiveness of the CEMPIE modeling. The $|S_{21}|$ between two test ports was both measured and modeled, and their comparison is shown in Figure 9. The modeled result agrees with the measurement very well up to 3 GHz, though there are significant discrepancies in the magnitudes at resonance frequencies, since losses are not considered in the CEMPIE model.

CEMPIE modeling provides a convenient means for examining the isolation as a function of geometry factors such as gap and neck sizes, location, gap type, *etc.* The example addressed herein uses the same power island structure shown in Figure 1, and it was modeled with one geometry factor varying at a time.

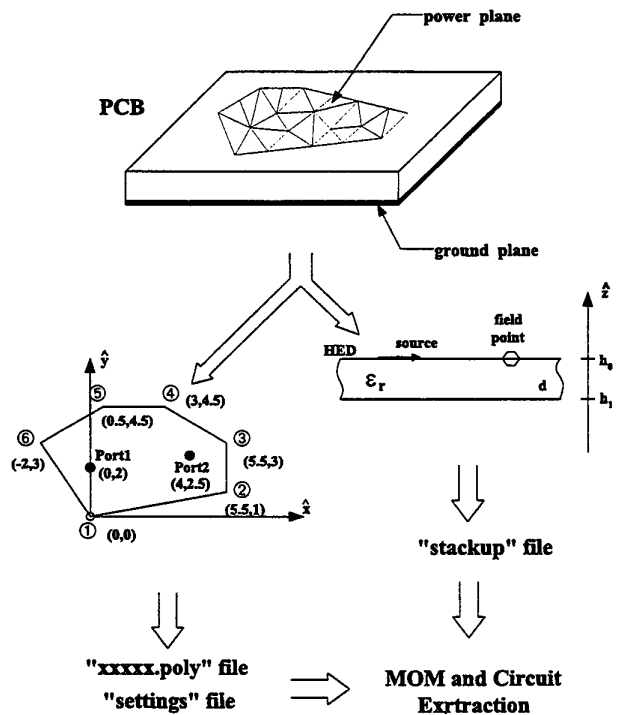


Figure 8: Overview of the CEMPIE modeling.

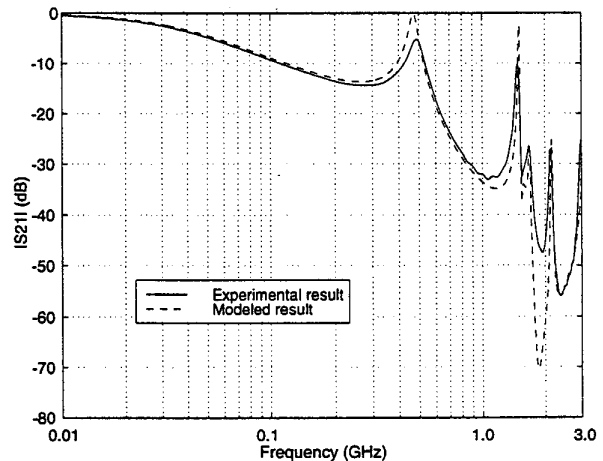


Figure 9: Comparison of CEMPIE modeled and measured results.

Figure 10 illustrates the effect on isolation when changing the neck width. The neck is located in the center of the board. The relevant dimensions are $a = 100$ mm, $b = 55$ mm, $c = 49$ mm, $t = 2$ mm, and the neck width is 2, 5 and 10 mm, respectively. The change of neck width affects the series impedance between the two segmented portions in the low frequency band so that a dramatic shift of the first resonance

results. In the high frequency band, conductive coupling through the neck-is no longer dominant and there is little difference between the three cases when the frequency is higher than 1 GHz.

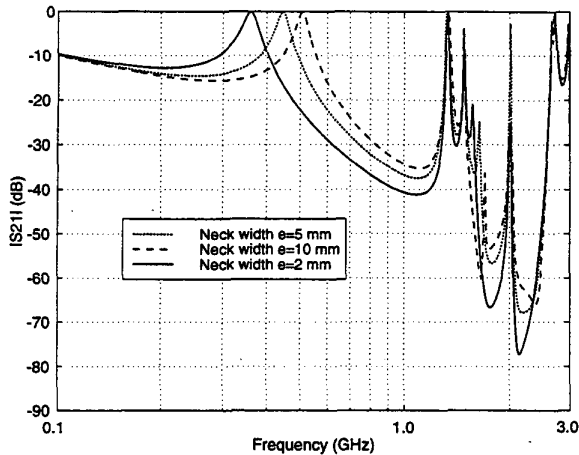


Figure 10: RF noise isolation versus neck width.

A change in gap width also results in little difference in the $|S_{21}|$ results, as shown in Figure 11 where $a = 100$ mm, $b = 55$ mm, $d = 25$ mm, $e = 5$ mm and $t = 1$ mm, 2 mm, and 100 mils. The gap is located at the center of the board. Figure 12 shows the cases when changing the neck location. The gap is at the center and $t = 2$ mm. The neck width was kept unchanged ($e = 5$ mm) while $d = 15, 20,$ and 25 mm.

Another three cases are shown in Figure 13 where $d = 25$ mm, $e = 5$ mm, $t = 2$ mm and $a = 29, 39,$ and 49 mm. The change of gap location results in a change of the sizes of two segmented portions, thus moving in frequency the resonances associated with these dimensions. The behaviors are quite different over a broad frequency range, though the coupling between the two portions was negligibly impacted.

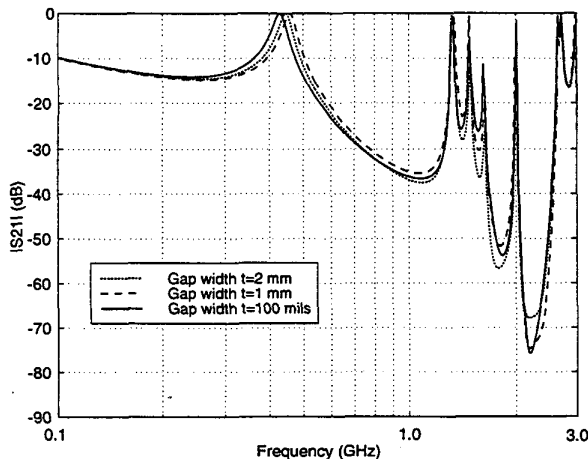


Figure 11: RF noise isolation versus gap width.

Overall, the few cases studied for a conducting neck indicate that there are possibly few if any configurations of conducting necks that will provide RF isolation for a power island with power areas contained in the same planes. The results demonstrate the utility of the modeling approach for easily pursuing various “what-if” scenarios that would be time-consuming experimentally.

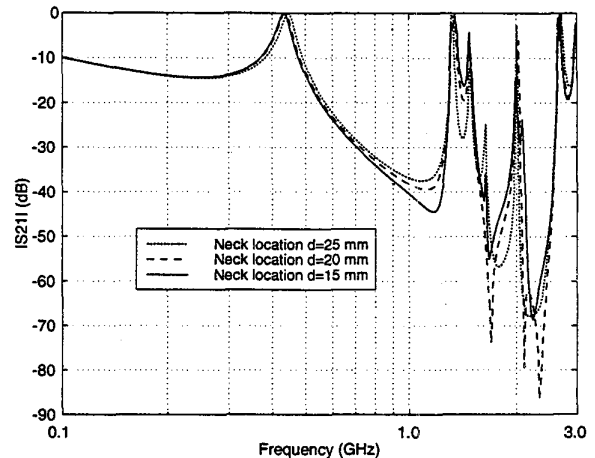


Figure 12: RF noise isolation versus neck location.

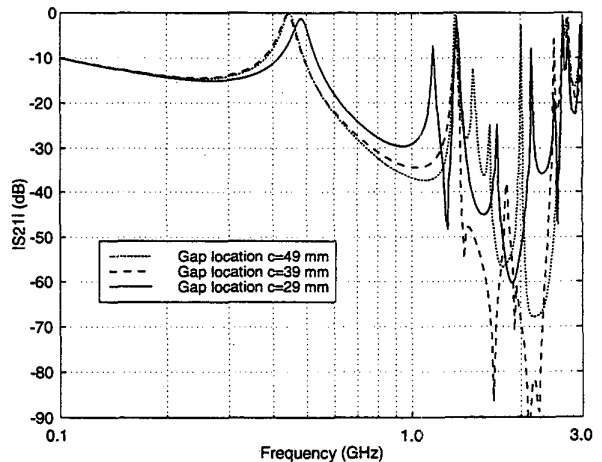


Figure 13: RF noise isolation versus gap location.

A recent development allows vertical discontinuities such as vias, interconnects, ports, etc., to be included rigorously in the CEMPIE modeling. Thus it is more suitable for modeling arbitrary PCB power bus structures including lumped SMT decoupling capacitors close to devices where mutual coupling may be important [13]. The integral equations are formulated both on power planes and the surfaces of vertical discontinuities [14].

A simple two-layer power bus geometry with a shorting pin, as shown in Figure 14, was modeled using CEMPIE. Figure 15 demonstrates the agreement of modeling and measurements up to approximately 5 GHz.

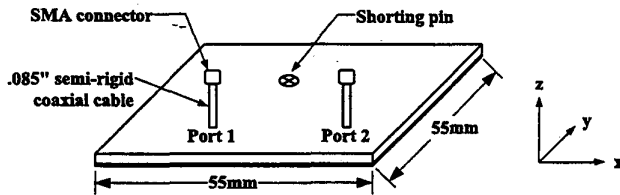


Figure 14: Geometry for the investigation of vertical discontinuities.

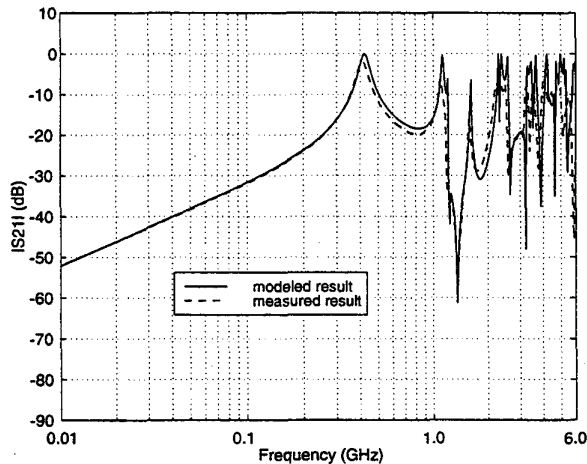


Figure 15: Comparison of CEMPIE modeled and measured results for the geometry shown in Figure 14.

CONCLUSION

Measured and modeled results show that complete segmentation of a power plane will achieve some degree of noise isolation except possibly at board resonances. If DC continuity is needed, a ferrite bead connection is much better than a conducting bridge. A conducting connection will greatly degrade the isolation achieved from the segmentation.

The CEMPIE modeling approach provides a useful and powerful tool in designing power island structures with a minimum of measurements.

REFERENCES

- [1] C. R. Paul, *Introduction to Electromagnetic Compatibility*, John Wiley, New York, 1992.
- [2] H. W. Johnson, and M. Graham, *High-Speed Digital Design, a Handbook of Black Magic*, Prentice Hall PTR, New Jersey, 1993.
- [3] R. Senthinathan, and J. L. Prince, *Simultaneous Switching Noise of CMOS Devices and Systems*, Kluwer Academic Publishing, Boston, 1994.
- [4] B. Archambeault, and A. Ruehli, "Electrical Package Modeling Including Voltage and Ground Reference Planes Using the Partial Element Equivalent Circuit (PEEC) Method," *13th International Zurich Symposium and Technical Exhibition on Electromagnetic Compatibility*, February 1999.
- [5] D. M. Pozar, *Microwave Engineering*, Addison Wesley, 1990.
- [6] H. Shi, J. Fan, J. L. Drewniak, T. H. Hubing, and T. P. Van Doren, "Modeling multilayered PCB power-bus designs using an MPIE based circuit extraction technique", *Proceedings of IEEE International Symposium on Electromagnetic Compatibility*, vol. 2, pp. 647-651, August 1998.
- [7] C. A. Balanis, *Advanced Engineering Electromagnetics*, John Wiley & Sons, New York, 1989.
- [8] K. Umashankar, and A. Taflove, *Computational Electromagnetics*, Artech House, 1993.
- [9] G. Dural, and M. I. Aksun, "Closed-form Green's functions for general sources and stratified media", *IEEE Trans. Microwave Theory and Techniques*, vol. 43, no. 7, July 1995.
- [10] S. M. Rao, D. R. Wilton, and A. W. Glisson, "Electromagnetic scattering by surfaces of arbitrary shape," *IEEE Trans. Antennas propagat.*, Vol. 30, No. 3, pp. 409-418, May 1982.
- [11] H. Shi, "Study of printed circuit board power bus design with a circuit extraction technique based on a quasi-static MPIE/MOM formulation," Ph.D. Thesis, Department of Electrical and Computer Engineering, University of Missouri-Rolla, 1997.
- [12] F. Y. Yuan, T. K. Postel, and L. M. Rubin, "Analysis and modeling of power distribution networks and plane structures in multichip modules and PCB's," *Proceedings of IEEE International Symposium on Electromagnetic Compatibility*, pp. 447- 452, August 1995.
- [13] T. Hubing, T. Van Doren, F. Sha, J. Drewniak, and M. Wilhelm, "An experimental investigation of 4-layer printed circuit board decoupling," *Proceedings of IEEE International Symposium on Electromagnetic Compatibility*, August 1995.
- [14] J. Fan, H. Shi, A. Orlandi, and J. L. Drewniak, "Modeling Power Bus Structures with Vertical Discontinuities - Mixed Potential Integral Equation Formulation with Circuit Extraction," internal EMI modeling progress summary, Electromagnetic Compatibility Laboratory, University of Missouri-Rolla, <http://www.emclab.UMR.edu>, January 1999.